Matterhorn, a high flux detector for 4th generation synchrotrons

A. Mozzanica*, R. Barten, F. Baruffaldi, A. Bergamaschi, M. Brückner, M. Carulla, R. Dinapoli, S. Ebner, E. Fröjdh, D. Greiffenberg, S. Hasanaj, J. Heymes, V. Hinger, T. King, P. Kozlowski, C. Lopez Cuenca, D. Mezza, K. Moustakas, A. Mozzanica, K. Paton, C. Ruder, B. Schmitt, D. Thattil, X. Xie J. Zhang

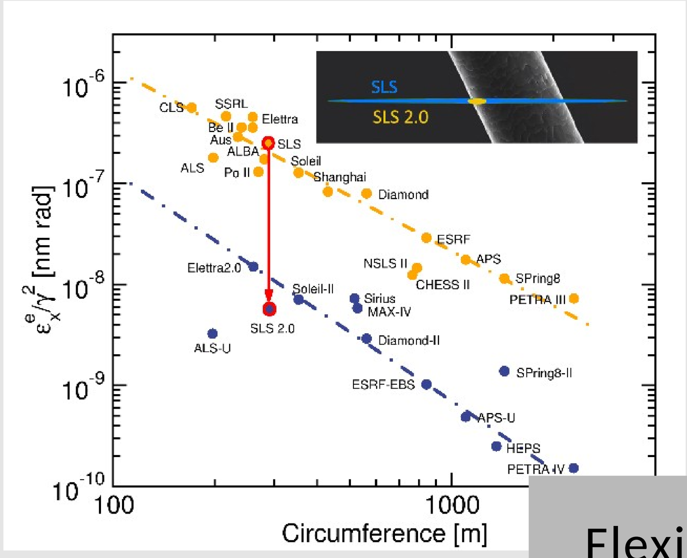
Paul Scherrer Institut (PSI), Photon Science Division Detector Group, CH-5232 Villigen PSI, Switzerland

*PM24, Elba, May 2024, *aldo.mozzanica@psi.ch*

Introduction to Matterhorn

Why a high flux photon counter:

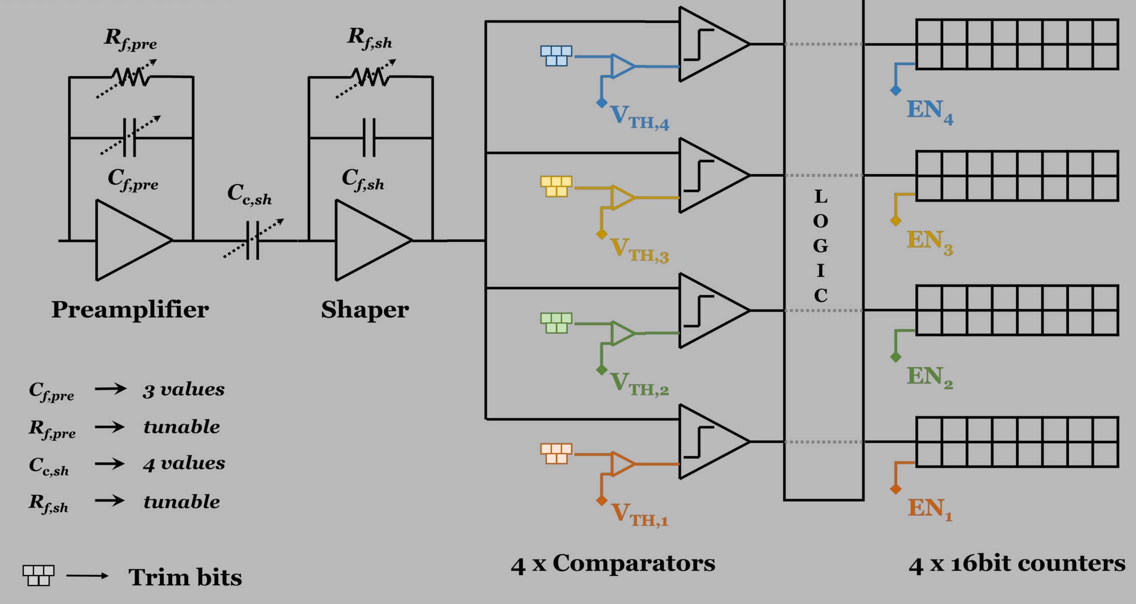
- 4th generation sources are delivering low emittances and increased brilliances [1]
- charge integrating detector (e.g. Jungfrau, CITIUS) can cope with very high fluxes, but deployment and operation can be challenging
- a high rate single photon counting (SPC) detector could be the workhorse for many beamlines



What is Matterhorn:

- a 75x75µm² pixel pitch SPC detector
- with a low threshold, flexible gating schemes and
- a high count rate capability

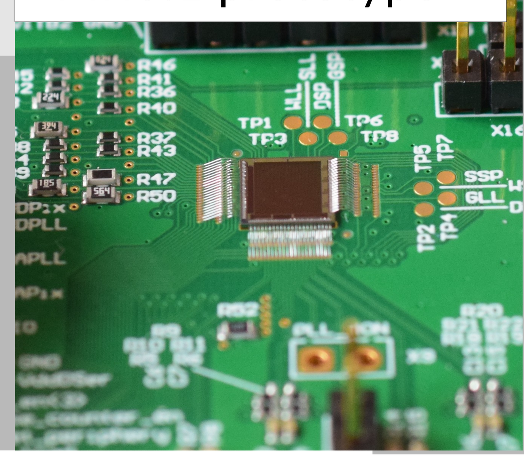
Flexible pixel architecture:



Final system performances:

- 10KHz readout at 16b/pixel
- 250eV to 80keV energy range with special sensors (4keV-20keV with Silicon)
- 20ns gating, multiple gating.

MH0.1 prototype

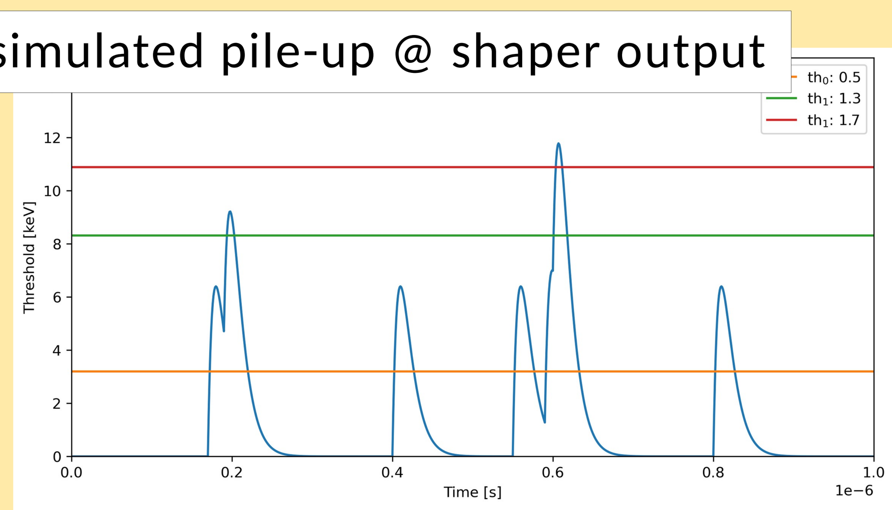


Extending the count rate with multiple threshold

Basic Idea[2]:

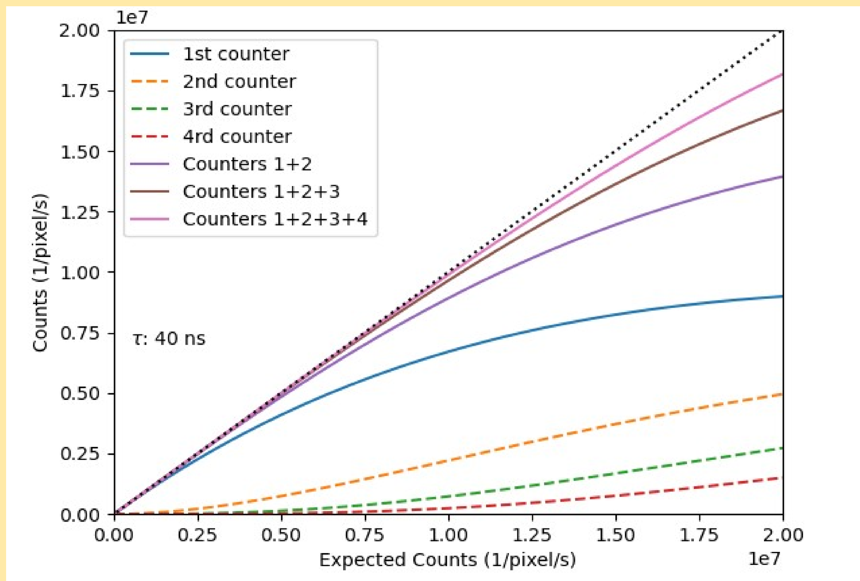
- up to 4 counters per pixel, read them out then sum them.
- with threshold adjustment, works well with poissonian distributed arrival time

simulated pile-up @ shaper output



What can be achieved:

- 90% efficiency at 20Mcps with 4 counters,
- starting from 2Mcps with a single thresold

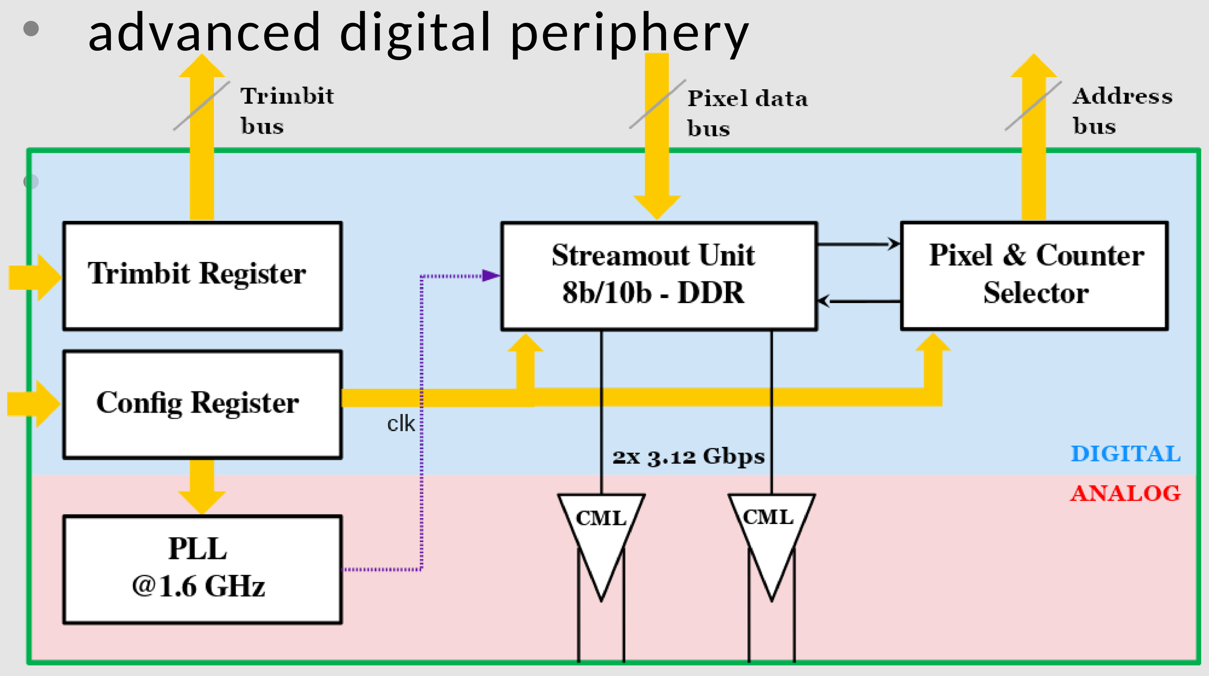


simulated rate response with time constant from single counter measurement

The MH0.2 prototype

Small scale ASIC:

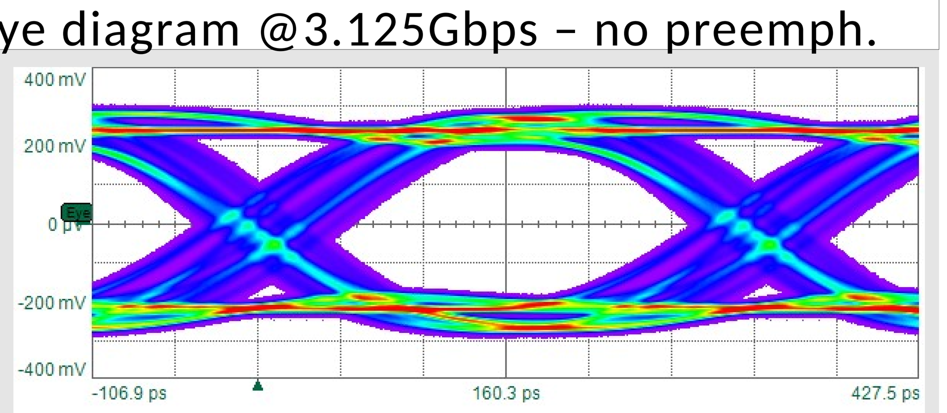
- quasi-final pixel design
- advanced digital periphery



Digital periphery:

- synthesized from VHDL (analog on top)
- controlling DACs, trimbits, PLL and pixel counter configurations
- receiving pixel matrix data
- converting to 8b/10b encoding
- 3.125Gbps DDR serializer feeding the offchip CML drivers.

eye diagram @3.125Gbps – no preemph.

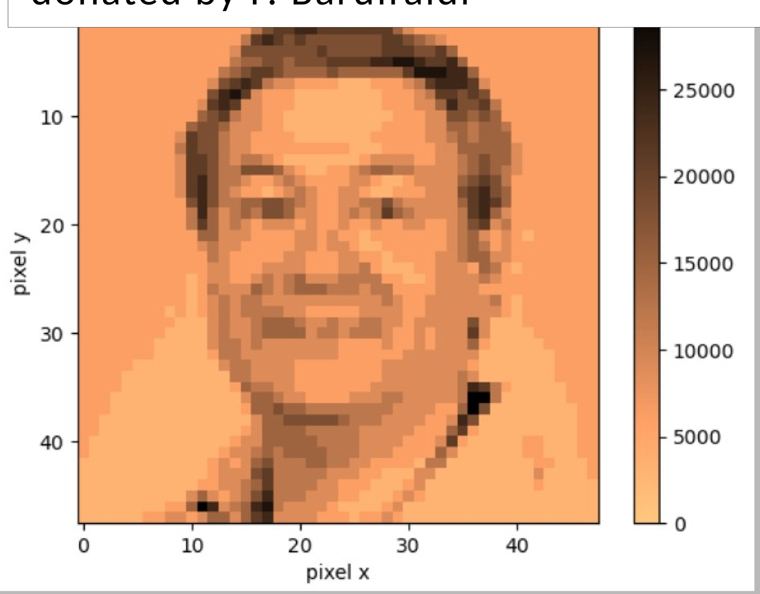


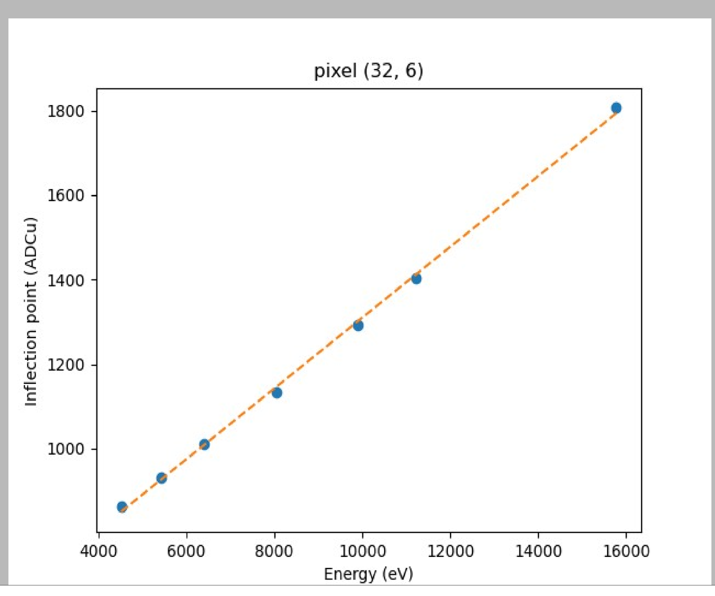
- links work reliably (BER<10^{-15})
- 64b/66b version for the full scale ASIC under design

Prototype results

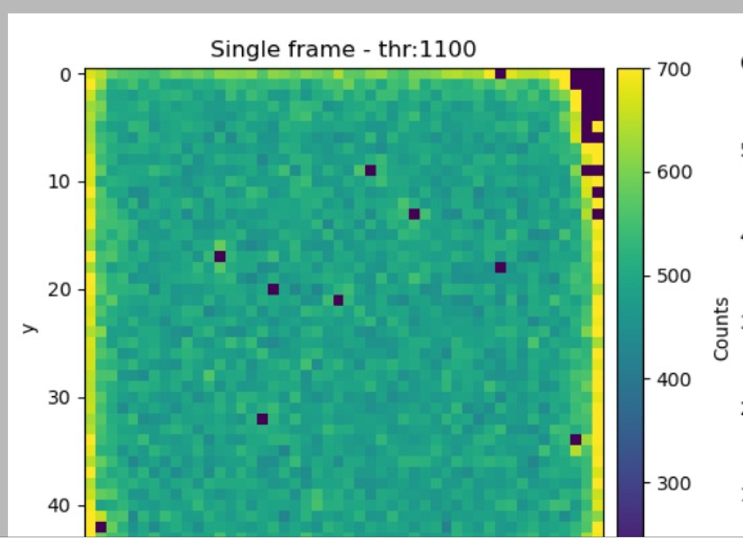
- noise ENC <80e⁻ in standard settings
- threshold dispersion 35e⁻ (with preliminary trimming)

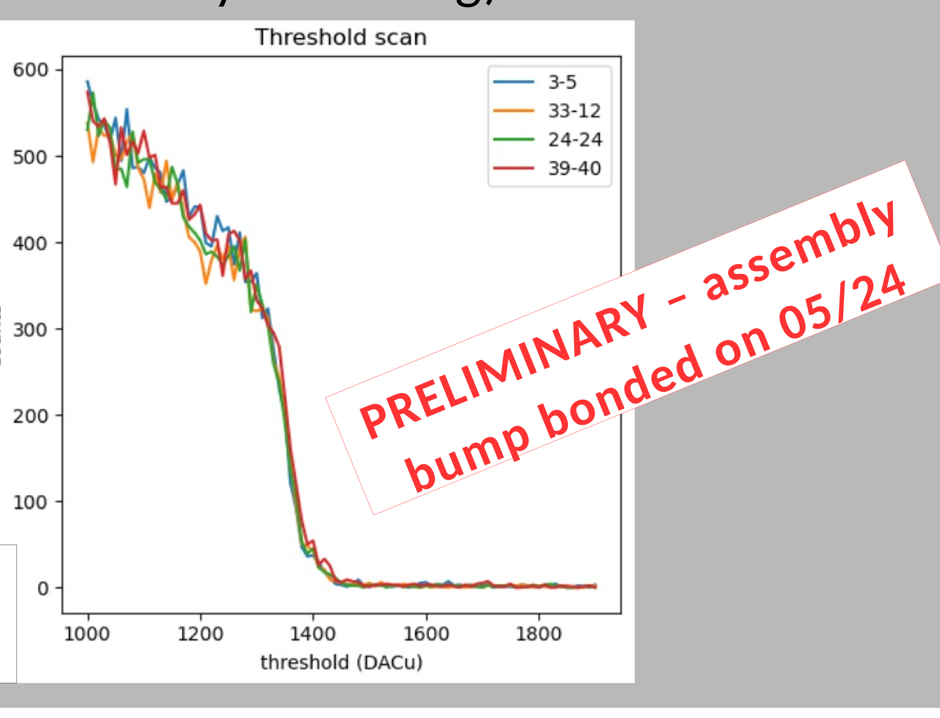
R. Dinapoli (b. 1971)
Self portrait of an ASIC designer, 2024
Trimbits and pulsing on Silicon
48 x 48x pixels
donated by F. Baruffaldi





MH0.1 energy calibration plot





MH0.2 FlatField and sample S-curve after trimming – Cu XRF - 8keV

[1] A. Streun et al, *Journal of Synchrotron Radiation*, 25(3) (2018)
[2] Andrä, M. et al., *Journal of Instrumentation*, 14(11), C11028 (2019)