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ATLAS Level-0 Muon Barrel Trigger System Status and Integration Tests for Phase-II

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The ATLAS Level-0 muon trigger system aims to quickly and efficiently identify events containing muons, facilitating the selection of interesting physics events and reducing the data rate for further processing.
In the barrel region of the detector, three concentric layers of Resistive Plate Chambers (RPC) are currently used for selecting muon candidates with predetermined transverse momentum, using a coincidence-based algorithm on the three RPC stations.
In preparation for the High-Luminosity Large Hadron Collider (HL-LHC), imperative upgrades are in progress to fortify the ATLAS Level-0 Barrel muon trigger system. These enhancements involve the incorporation of a novel inner layer of RPC detectors. A replacement of the trigger and readout electronics is vital to retain the RPCs excellent trigger and tracking performance even with the extremely high particle rates.
The existing on-detector electronics (Pad and Splitter box) will be replaced by the innovative Data Collector and Transmitter (DCT) boards. The DCTs will be responsible for gathering RPC hit data, applying zero suppression, and transmitting it to the off-detector electronics, the Barrel Sector Logic (SL) boards, situated in the counting room.
For the HL-LHC configuration, a new SL board has been developed to collect the digitized detector data coming through optical fibers from up to 50 DCTs. It will execute the Level-0 trigger algorithm on the four RPC stations, perform detector readout logic, and convey muon candidate coordinates along with trigger threshold measurements to the Monitored Drift Tubes (MDT) Trigger Processor (MDTTP) board. The MDTTP, with its more accurate measurement of the candidate's transverse momentum, will efficiently reduce the RPC data rate.
This report outlines the outcomes of the hardware and firmware validation for the DCT final prototypes, leveraging Xilinx Series 7 FPGAs, and the second and final SL prototype, built upon Xilinx Ultrascale+ FPGAs and SoC architecture.

Collaboration

ATLAS TDAQ

Role of Submitter

The presenter will be selected later by the Collaboration

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