ATLAS Level-0 Muon Barrel Trigger System Status and Integration Tests for Phase-II

Pisa Meeting 2024, 26 May - 1 June 2024, La Biodola - Isola d'Elba, Italy

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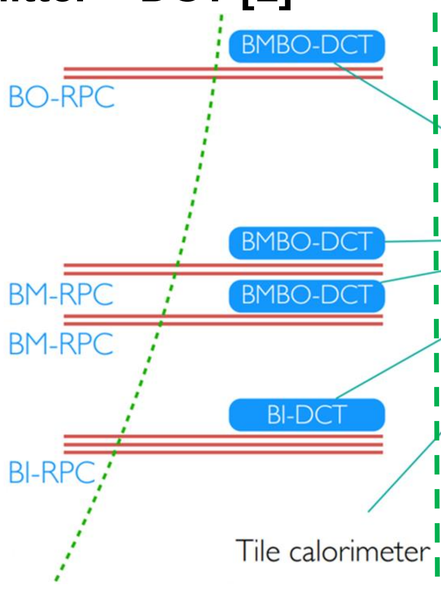
Phase-II Muon Barrel L0 Trigger

Detector: 4 RPC stations in Barrel region: 3 legacy **BM-BO RPC** doublets + 1 **novel BI RPC** triplet [1]

ON-Detector Electronics:
Digital Collector and Transmitter – DCT [1]

- 1208 **BM-BO DCT** boards replace actual PADs and splitters. They digitise the RPC-FE signals with 800 ps time binning (FPGA-TDC) and perform zero suppression.
- 338 **BI-DCT** decode the Manchester signal coming from the FE boards and implement zero suppression.



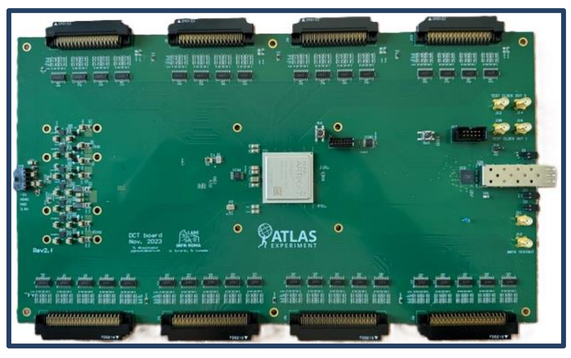
- DCTs send zero suppressed data to barrel Sector Logic (**SL**) in counting room (USA15).

OFF-Detector Electronics: Sector Logic – SL [2]

- 32 barrel SL boards receive all the RPC data and control from the DCTs.
- Each SL board is connected with up to 50 DCTs through optical fibres.
- SL boards produce trigger candidates based on RPC and Tile Calorimeter data and interface with the Monitored Drift Tubes (**MDT)** Trigger Processor (for further refinements).
- Final muon L0 trigger candidates sent to ATLAS central trigger through Muon Central Trigger Processor Interface (**MUCTPI**) board.
- SL boards store readout data into local memories during Level-0 trigger latency.
- Muon hit data is transmitted to High Level Trigger and readout system via FELIX modules when an L0-Accept signal is received.

BMBO-DCT and SL Hardware & Firmware Status

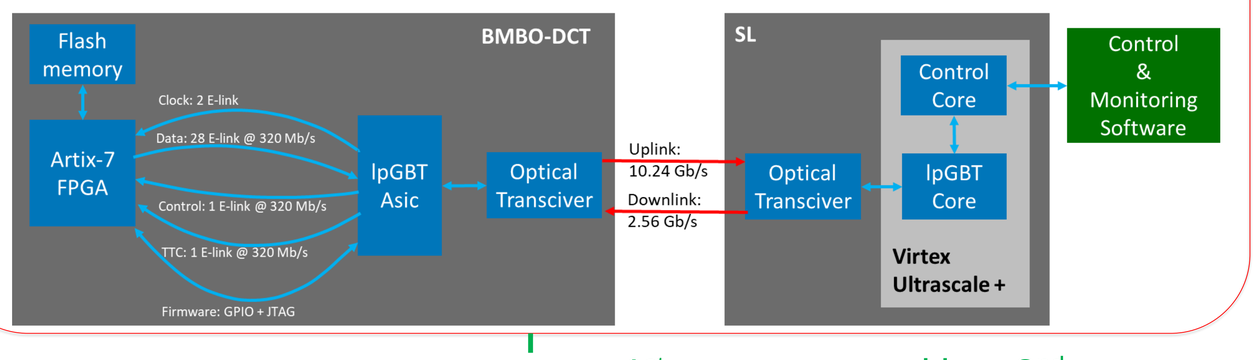
- **BMBO-DCT FPGA-based on Artix-7 (XC7A200)**
- **lpGBT ASIC** used to handle the serial data transmission between DCT and SL.
- Optical transmission with **SFP+** optical module.

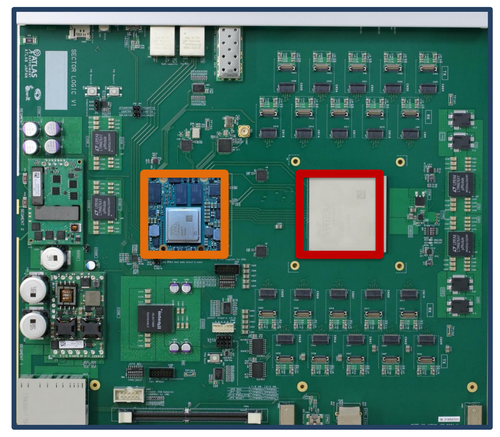


- 1st prototype working.
- 2nd prototype recently produced, currently being tested.
- Firmware ready and tested in lab and on RPC detector.
- Rad-hard tests to be completed on **2024**.

DCT-SL Interface

DCT to SL: 256bit @ 40MHz (10.24 Gb/s bandwidth, 8.96 Gb/s user data)
SL to DCT: **32bit @ 80MHz** (2.56 Gb/s bandwidth, 1.28 Gb/s user data)





- **SL FPGA-based on Virtex Ultrascale +** (XCVU13P)
- **lpGBT interface** implemented on FPGA to handle the serial data transmission between DCT and SL.
- Optical transmission using **Firefly** optical modules.

- 1st prototype working, 2nd prototype to be delivered soon.
- Firmware ready, hardware tests ongoing.
- Different trigger algorithm approaches under investigation: spatial coincidences (roads), pattern matching, NN.

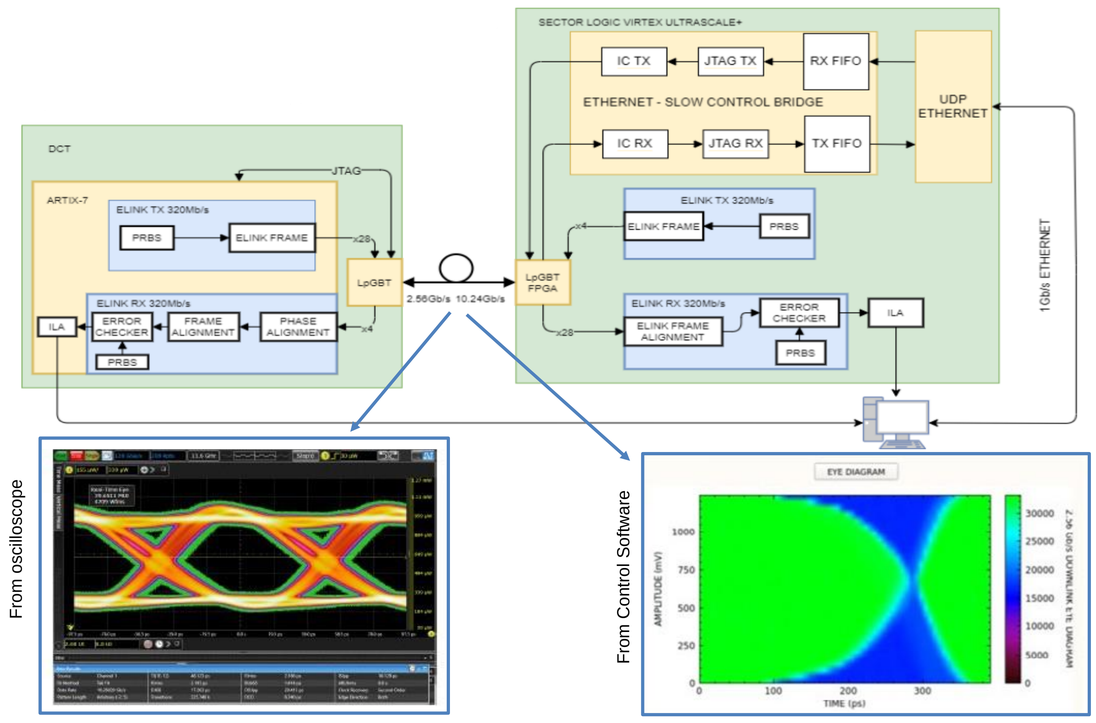
Test communication between BMBO-DCT and SL in the L0 Muon test stand

Configuration & monitoring

- **Control software** used for DCT/SL configuration, monitoring through ethernet connection.
- DCT FPGA, flash, and lpGBT **configured** via SL.
- DCT **monitoring**: reading voltages and temperatures from decoded lpGBT data.

Data communication test

- **IBERT test** @ **10.24 Gb/s**.
- **BER test**: send packets with PRBS7 data using a delimiter (automatic phase and packet alignment). A logic block deserialises the frame and aligns them using a custom header.
- **All Elinks** tested both in **uplink** and **downlink** @ **320 Mb/s**.
- **ILA** used to monitor transmission errors.
- **No transmission errors found for a 24h test**.



References:
1 ATLAS Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*. CERN-LHCC-2017-017.
2 ATLAS Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*. CERN-LHCC-2017-020.

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