ATLAS upgrade for HL-HLC

FEDERICO LASAGNI MANGHI ON BEHALF OF THE ATLAS COLLABORATION

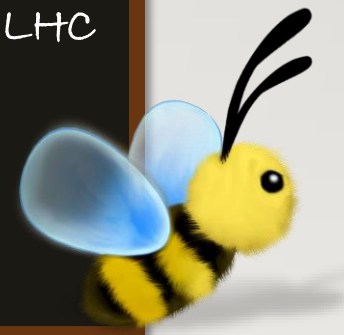
PISA MEETING ON ADVANCED DETECTORS

Why HL-LHC?

- Rare process searches and precision physics require a larger dataset
- HL-LHC will achieve a factor 10 higher integrated luminosity

Why upgrade ATLAS?

- Face factor 4 higher instantaneous luminosity:
  - From $2x10^{34}$ $cm^{-2}s^{-1}$ up to $7.5x10^{34}$ $cm^{-2}s^{-1}$
  - L1 trigger rates from 100 kHz to 1 MHz
  - pile-up conditions – from $<\mu>=20$ (now 60) of LHC design up to $<\mu>=200$ for HL-LHC
- Many systems are suffering from wear and irradiation
  - 15 more years of operation and 20x increase in irradiation expected
- New detectors can achieve improved precision DESPITE the luminosity increase

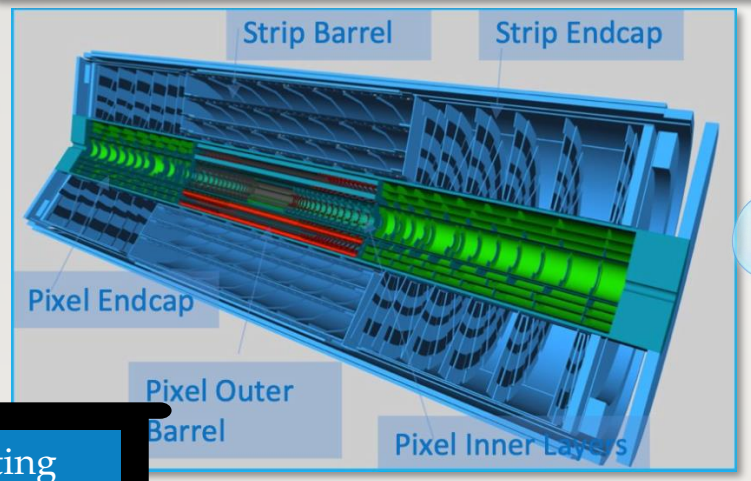


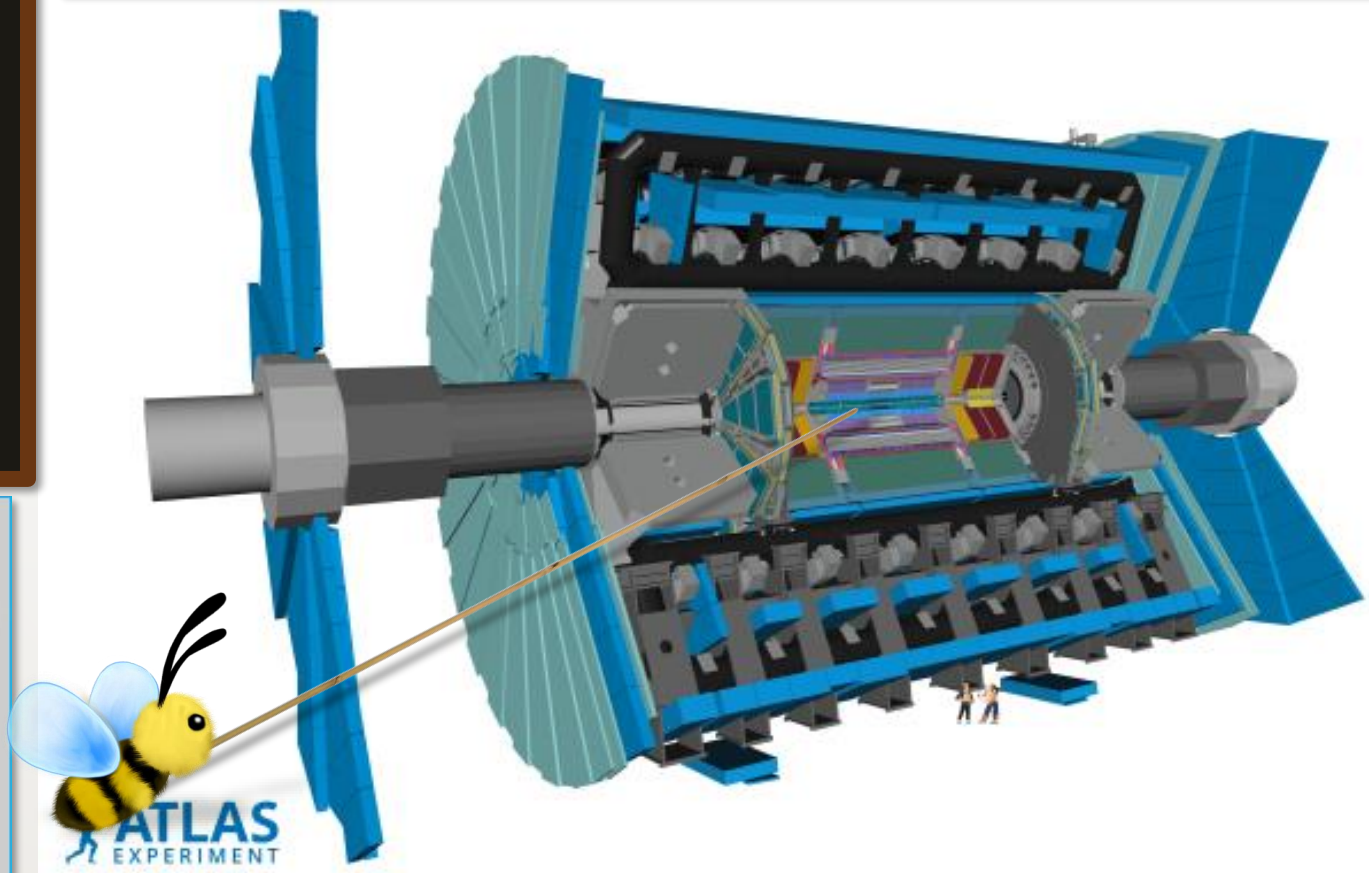
Upgrade summary

3

New Inner Tracker (ITk)

- All silicon with 9 layers up to $|\eta|=4$
- Less material finer segmentation
- Improve vertexing, tracking, b-tagging





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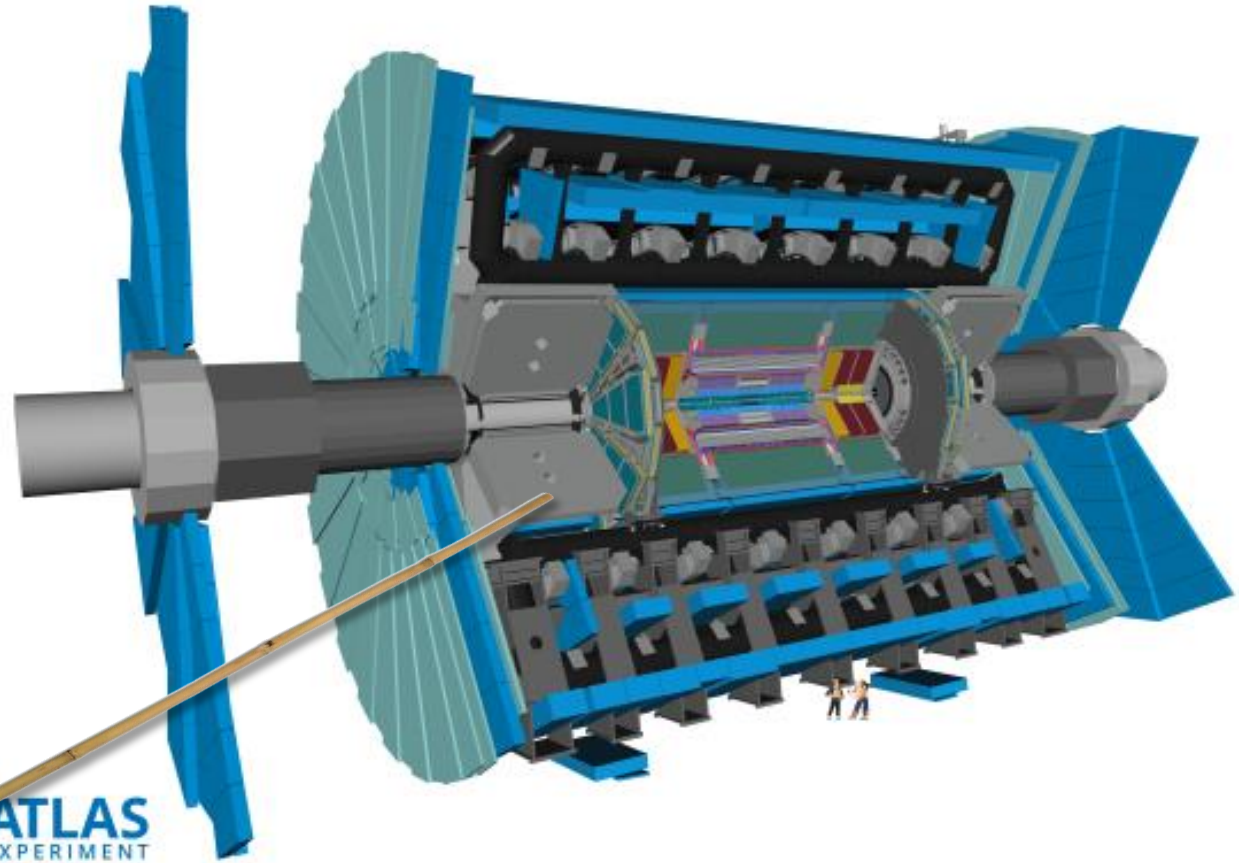
Upgrade summary

4

Calorimeter Electronics

- On-detector electronics upgrades of LAr and Tile Calorimeters
- Provide 40 MHz readout for triggering



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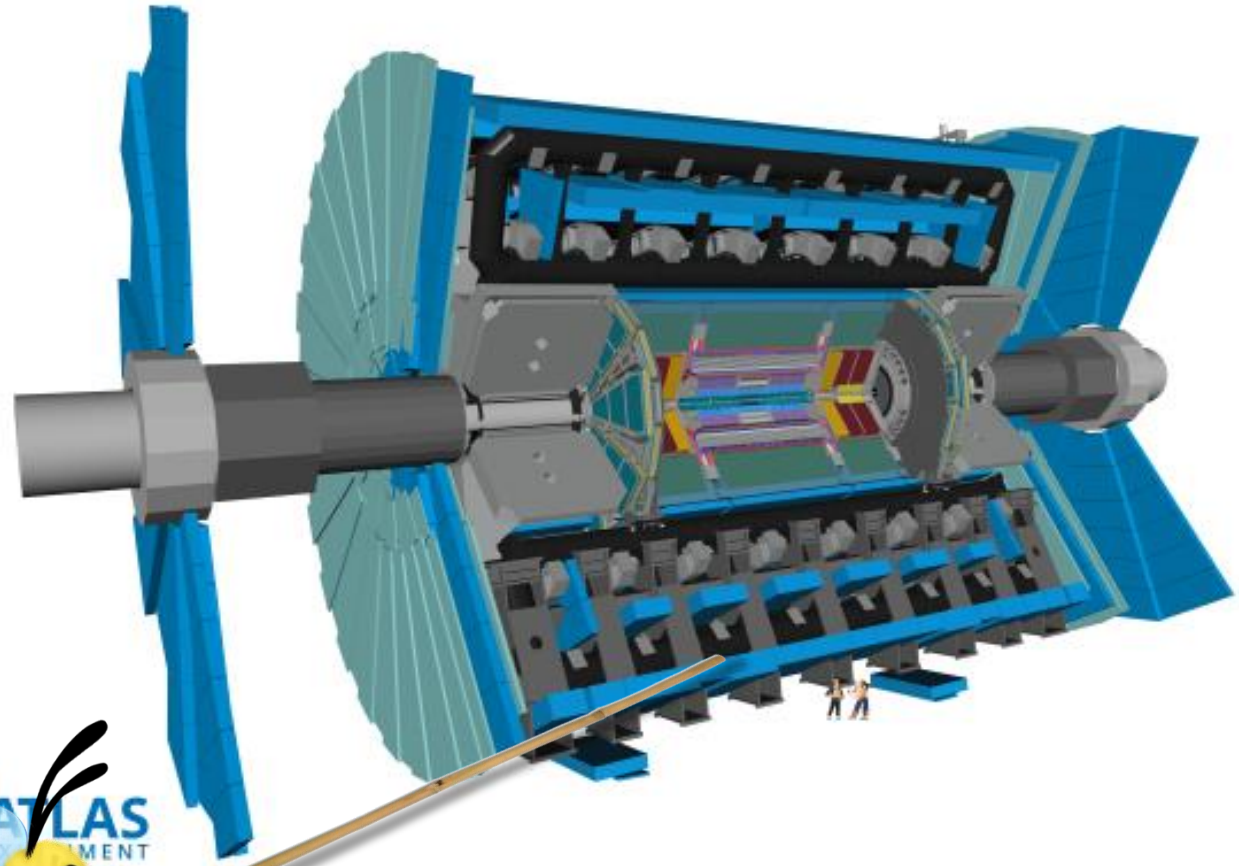
Upgrade summary

Muon Detector

- Upgrade of the detector electronics for new TDAQ system
- Upgrade of inner barrel chambers with new RPC and sMDT
- Improve trigger efficiency and momentum resolution, and reduced fakes



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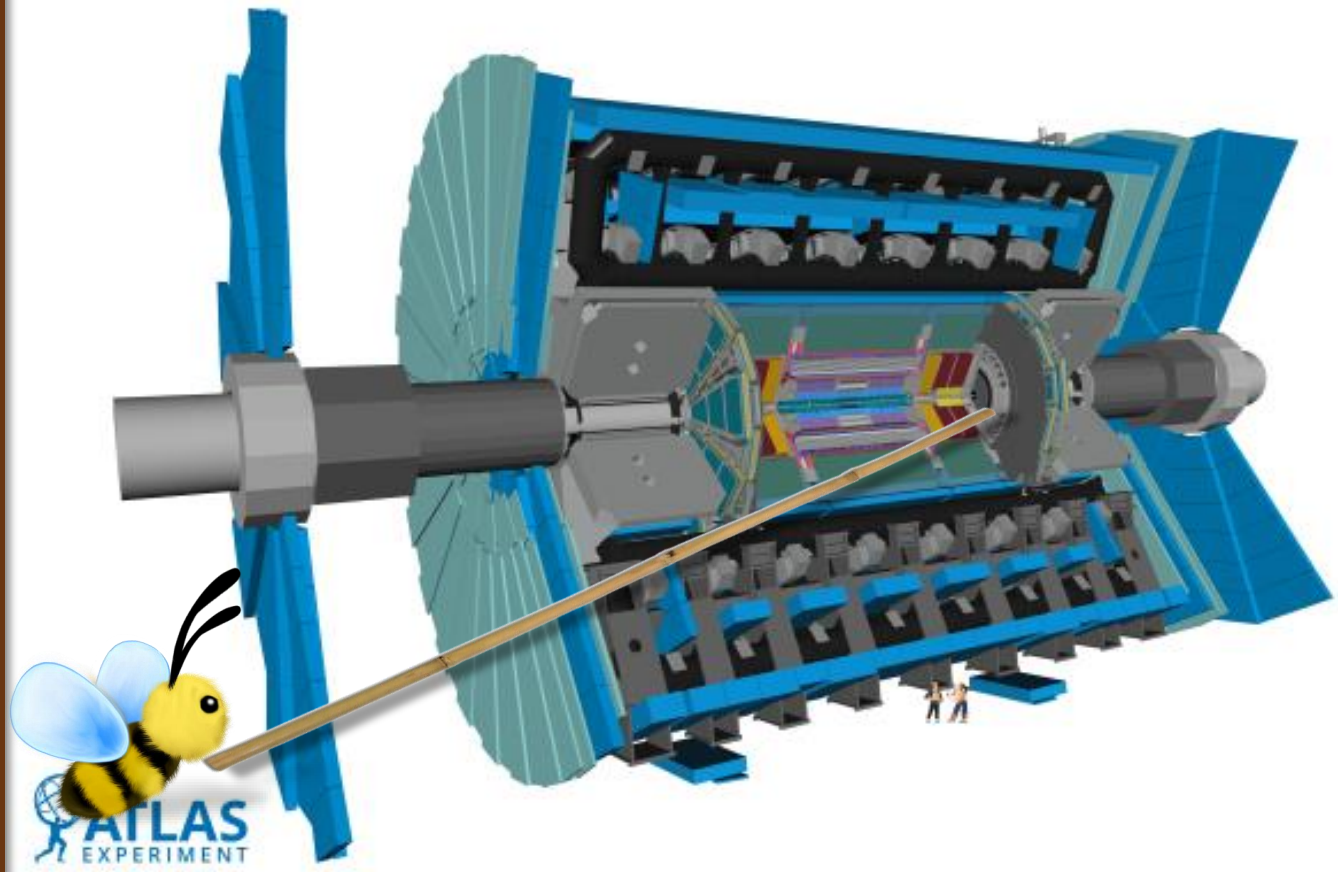
Upgrade summary

New High Granularity Timing Detector

- Precision track timing (30 ps) with LGAD in the forward region.
- Improve pile-up rejection in the forward region



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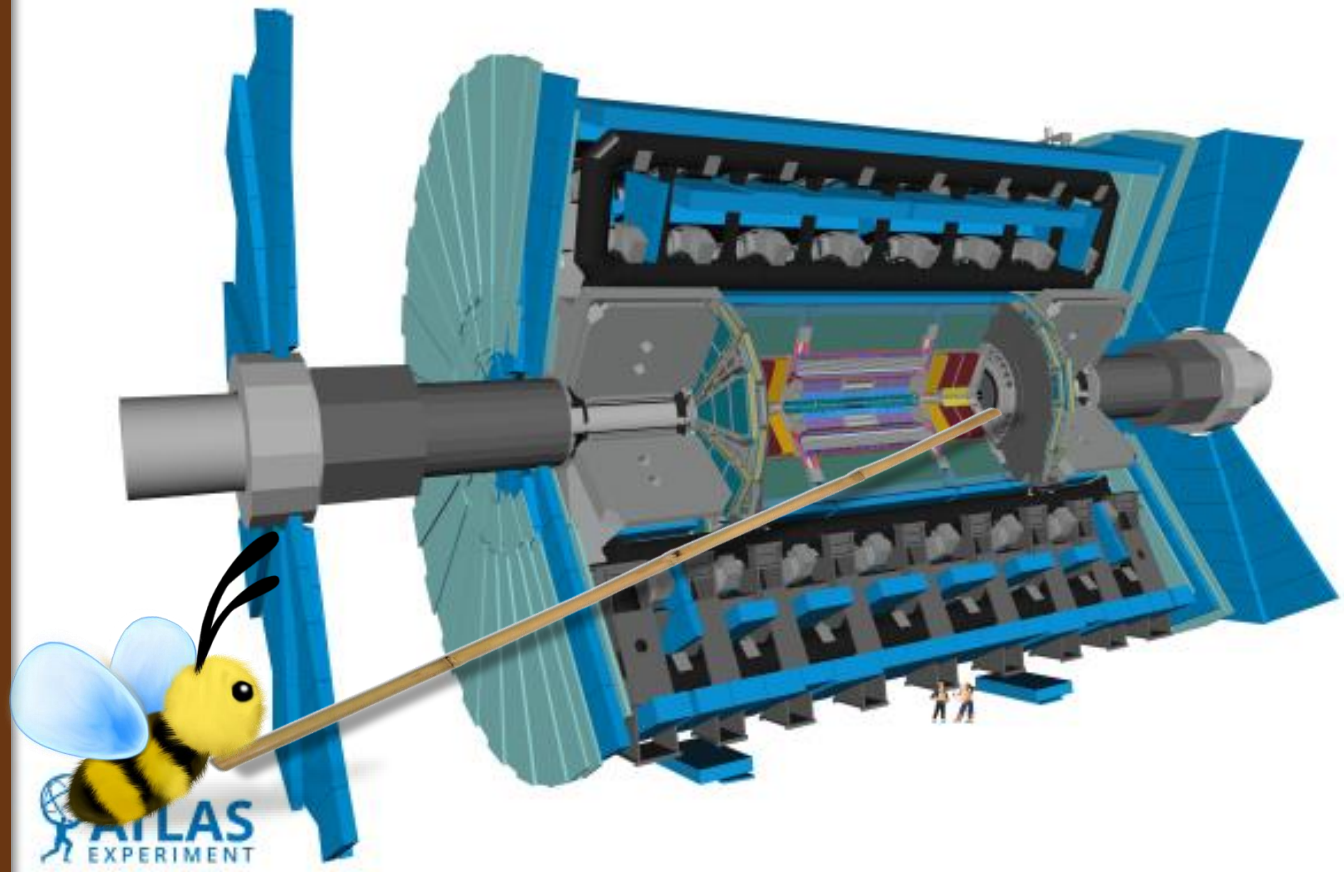
Upgrade summary

Luminosity & FWD detectors

- Objective: luminosity to < 1% resolution
- LUCID-3 complete TDAQ and detector upgrade
  - + BMA
- ITk-BCM', HGTD
- New ZDC



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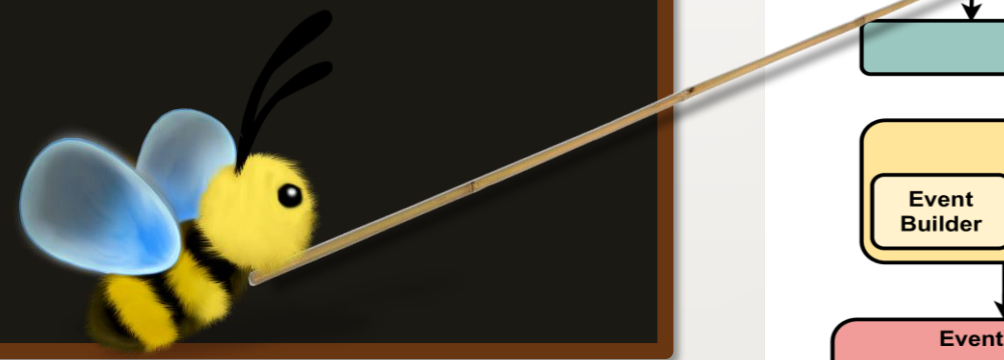
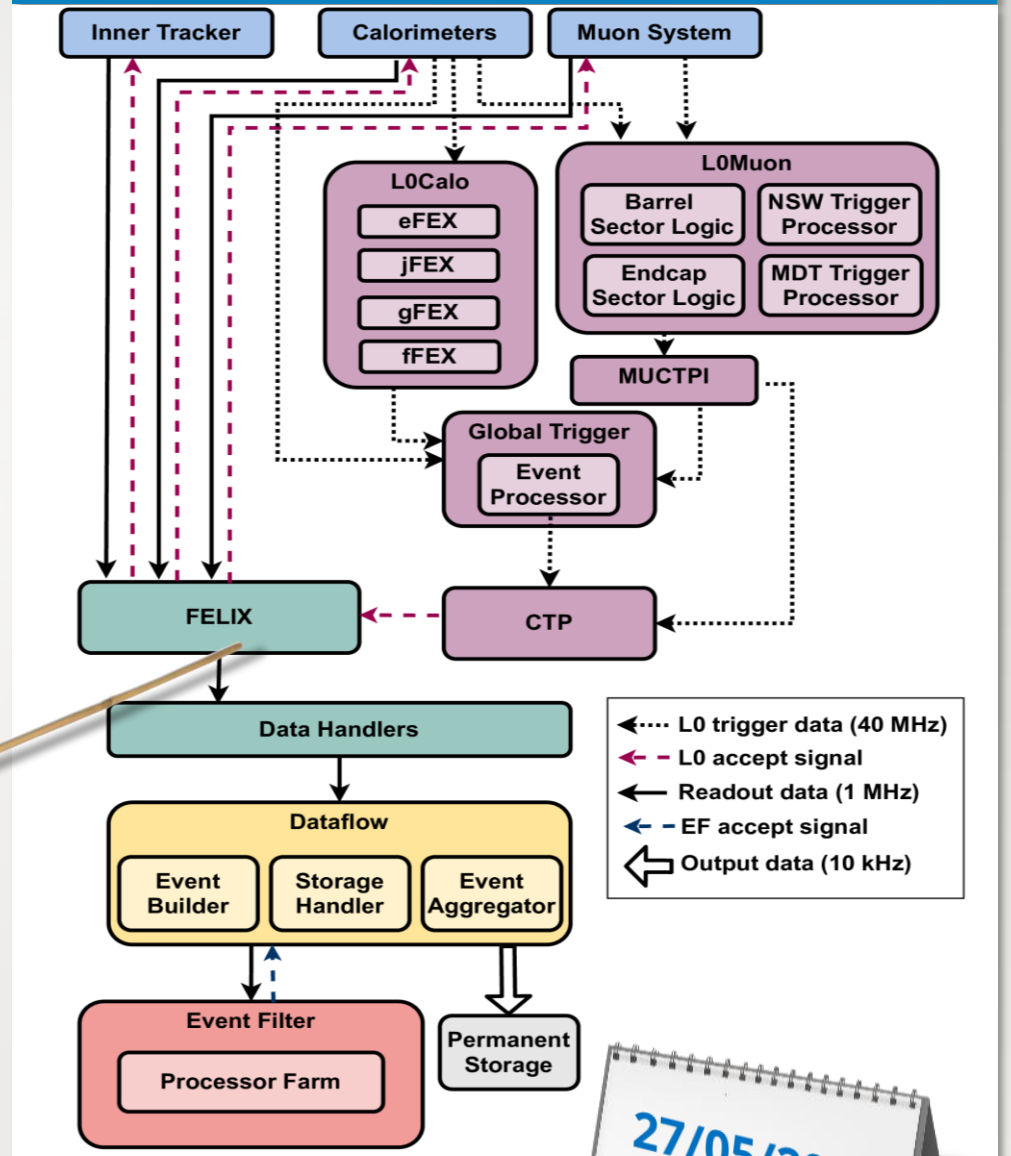
Upgrade summary

8

Trigger and DAQ Upgrade

- Single level Trigger with 1 MHz output (x 10 current)
- Improved DAQ system with faster FPGAs
- Upgrade to multiple systems





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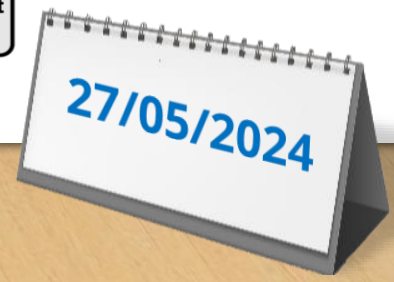

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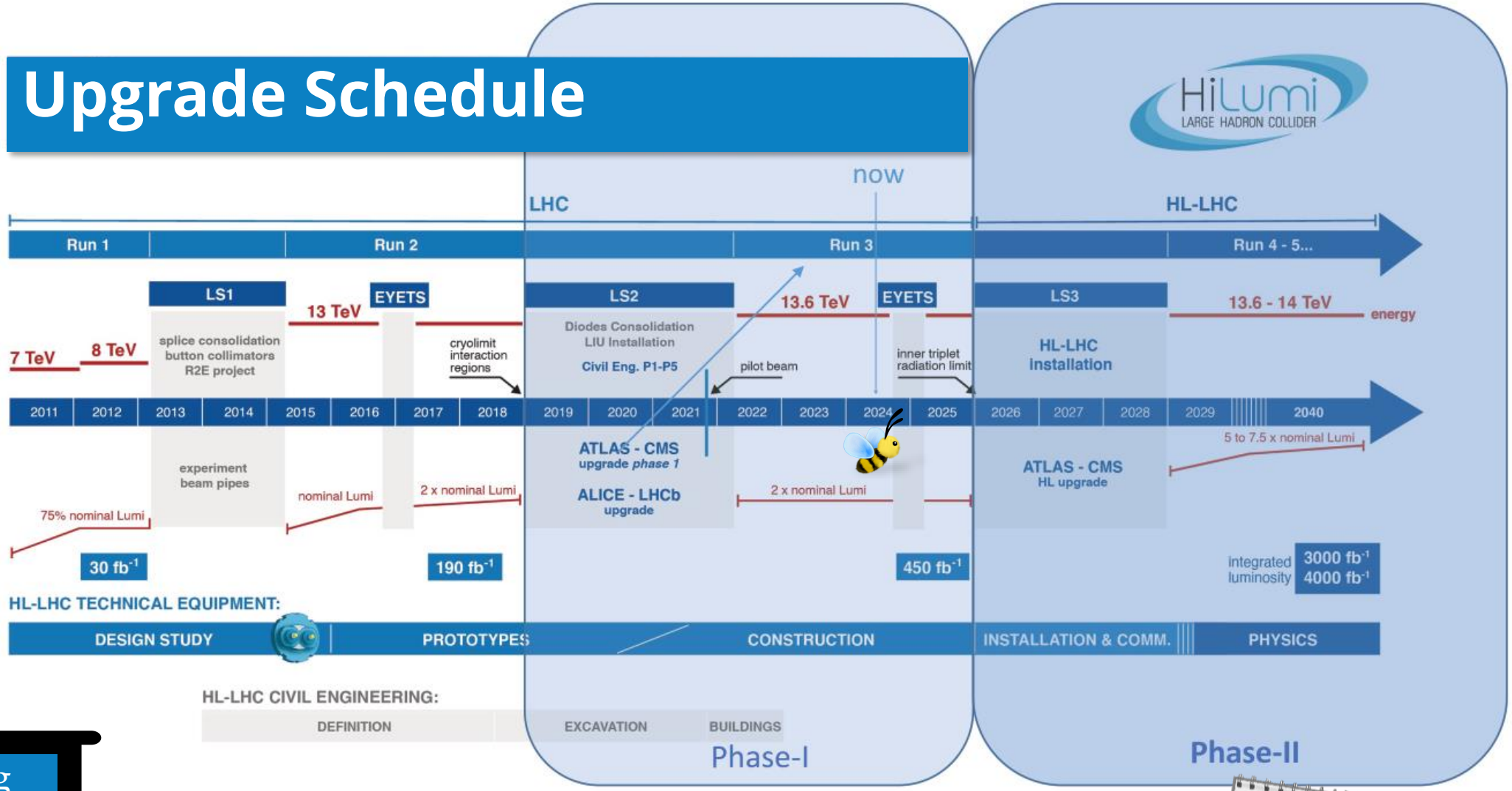
Upgrade Schedule



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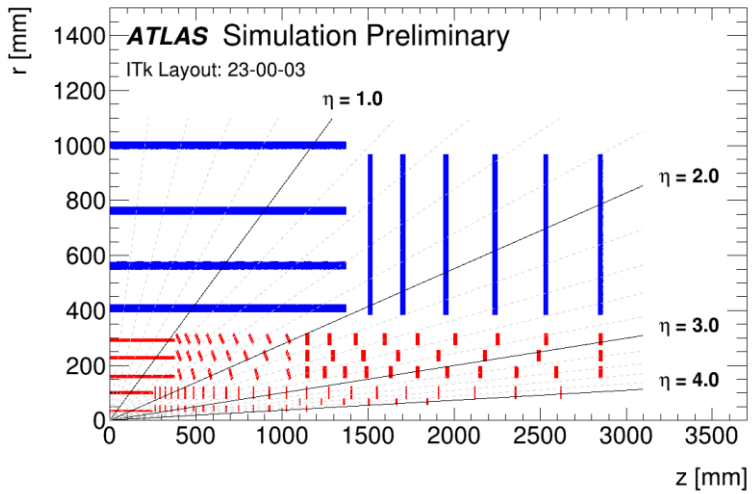
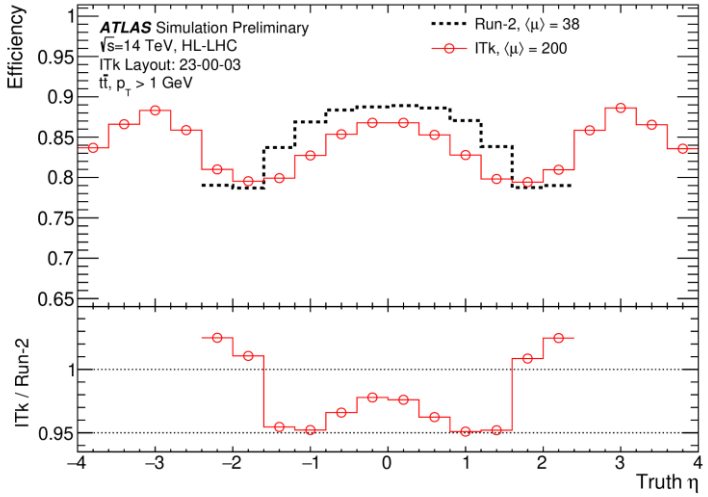
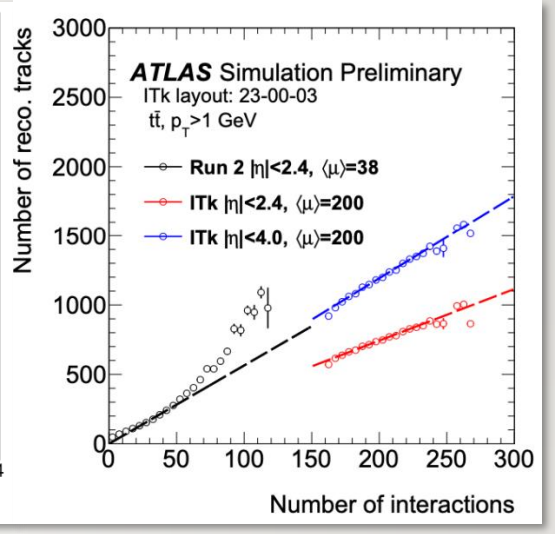
Inner Tracker







- All-silicon inner tracker, acceptance $|\eta|<2.5$ (ID) to $|\eta|<4$ (Itk)
  - 165 m2 of silicon strip and 13 m2 of silicon pixels
- Tracking performance comparable or better than before at much higher pile-up conditions
- Inner part made from 5 barrel layers and end-cap rings of pixel detectors
- Outer part made from 4 barrel layers and 6 end-cap disks of strip detectors

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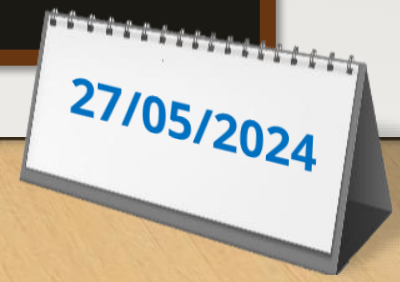
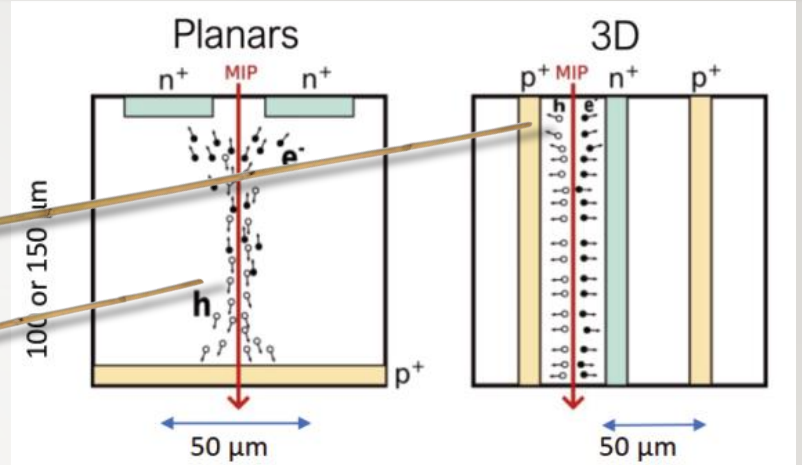
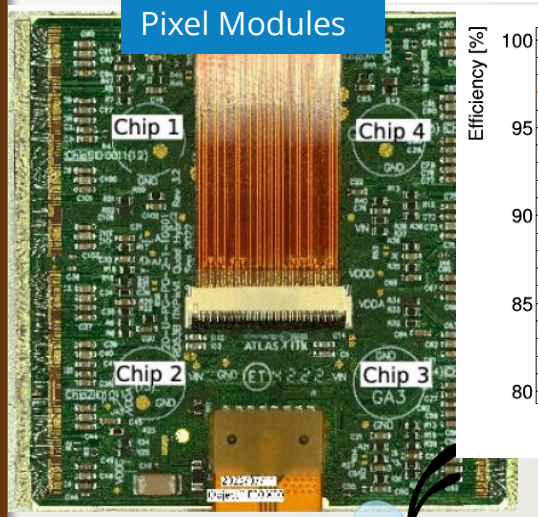


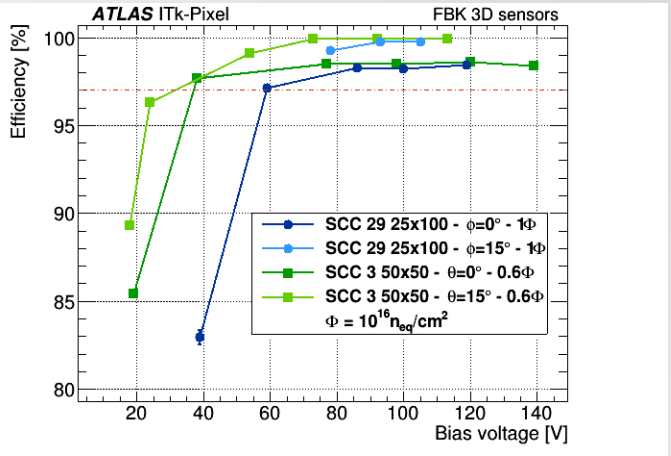
Itk Pixel

- Silicon sensors with 50x50 and 25x100 μm pixel size, 100-150 μm thickness
  - Radiation hard 3D sensors for the inner layers
  - Planar sensors for larger area layers
- Sensor production is in progress
- ASIC production started
- Module production starts this year (2024)
- Tests with pre-production items are ongoing



Pixel Modules





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Check out Craig's talk and Sonia's poster

https://agenda.infn.it/event/37033/timetable/?view=standard#62-atlas-itk-pixel-detector-ov

https://agenda.infn.it/event/37033/timetable/?view=standard#311-atlas-itk-pixel-outer-endc

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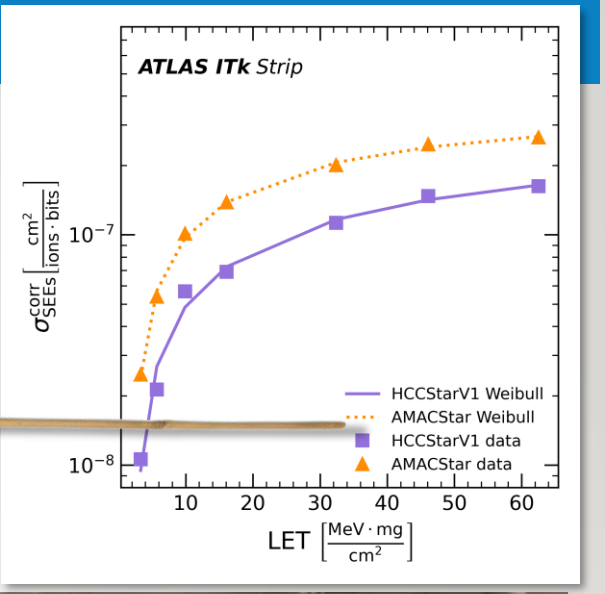
Itk Strip

- Silicon strip sensors with 70-80 μm pitch
- Sensor and ASIC production is well underway
- Mechanical sub-structures in pre-production
- System tests are ongoing



Check out Carles' talk and Sergio's poster
https://agenda.infn.it/event/37033/timetable/?view=standard#502-the-atlas-itk-strip-detect
https://agenda.infn.it/event/37033/timetable/?view=standard#256-overview-of-the-atlas-itk

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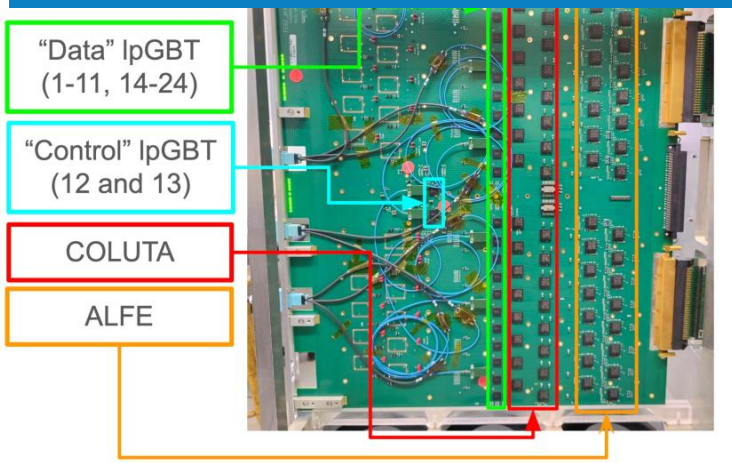
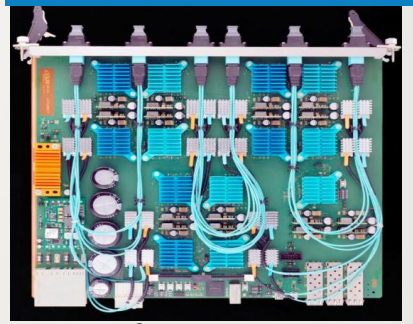
Liquid Argon (LAr) EM calorimeter

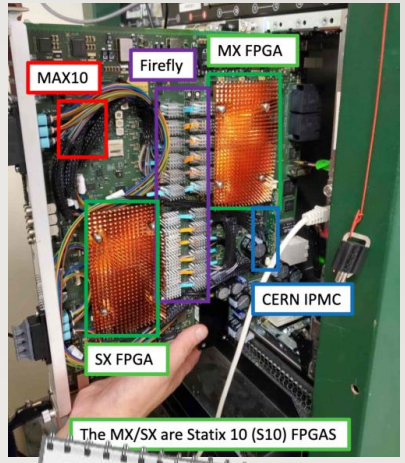
- Complete replacement of the on- and off-detector electronics to meet new radiation, trigger and readout performance criteria (40 MHz continuous readout)
- New calibration board
- Major progress on all LAr HL-LHC upgrade
  - Custom LAr-specific ASICs in production.
- Prototype boards becoming available.

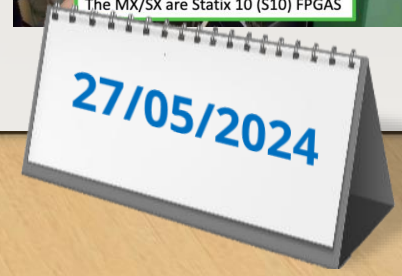
On-detector: 128 channel FEB2v2



Off-detector: Timing System & Signal Processor







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More information in Ki's and Sully's posters

https://agenda.infn.it/event/37033/timetable/?view=standard#81-development-of-the-atlas-li

https://agenda.infn.it/event/37033/timetable/?view=standard#80-technical-challenges-and-pe

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Tile Hadronic calorimeter

Replacement of all electronics:

- Compliance with the new TDAQ architecture
  - Digital trigger with improved precision and full radial granularity
  - Higher data bandwidth with 40MHz readout
- Improved radiation hardness
- Redundancy in up-links from on-detector to off-detector electronics

Upgraded mechanical structure for front-end electronics

- Increased robustness to failures due to higher modularity

Voltage system upgrade: off-detector regulation of the PMTs

Replacement of the PMTs on the most exposed cells

Calibration system upgrades

R11187

FENICS2

Tile Mainboard

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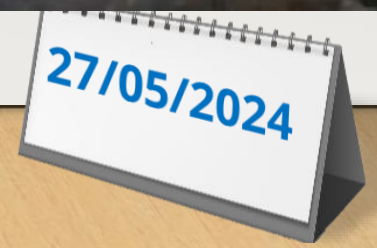
Details in David's and Viola's posters

https://agenda.infn.it/event/37033/timetable/?view=standard#408-upgrade-of-atlas-hadronic

https://agenda.infn.it/event/37033/timetable/?view=standard#407-calibration-system-of-the



The muon systems

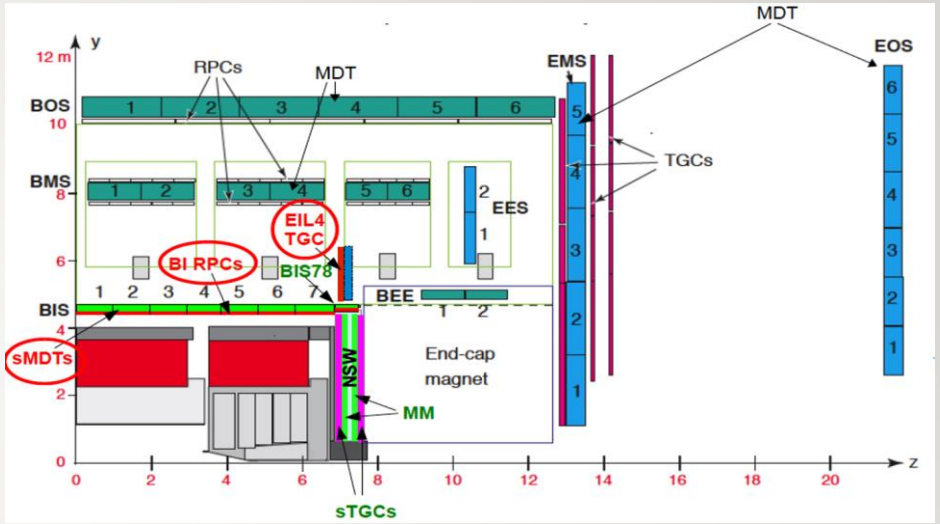
Replacement of electronics:

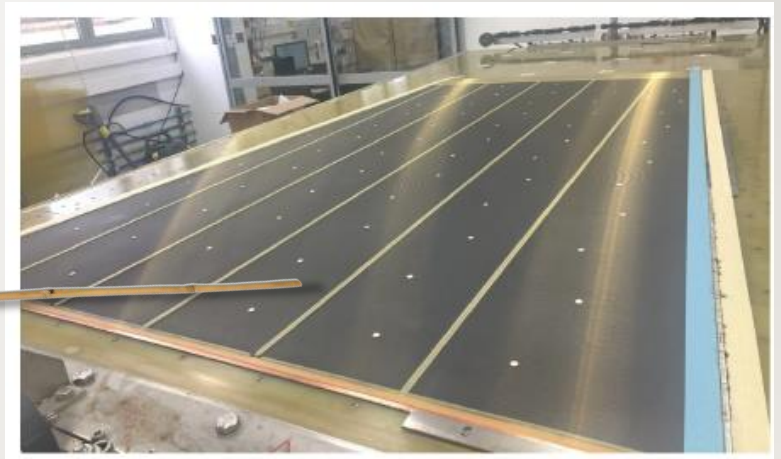
- On-detector electronics of MDT, RPC, TGC will be replaced to cope with Phase-II requirements.
- MDT FE mezzanines including ASD and TDC replaced.
  - All data to USA15, no readout buffers on detector
  - Use all hits to perform trigger logic on FPGAs

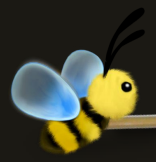
New layer of triplet RPCs installed in the inner barrel layer. MDTs in small sectors replaced with sMDT

EIL4 TGC chambers will be upgraded from doublet to triplet

Replacement of the existing power system







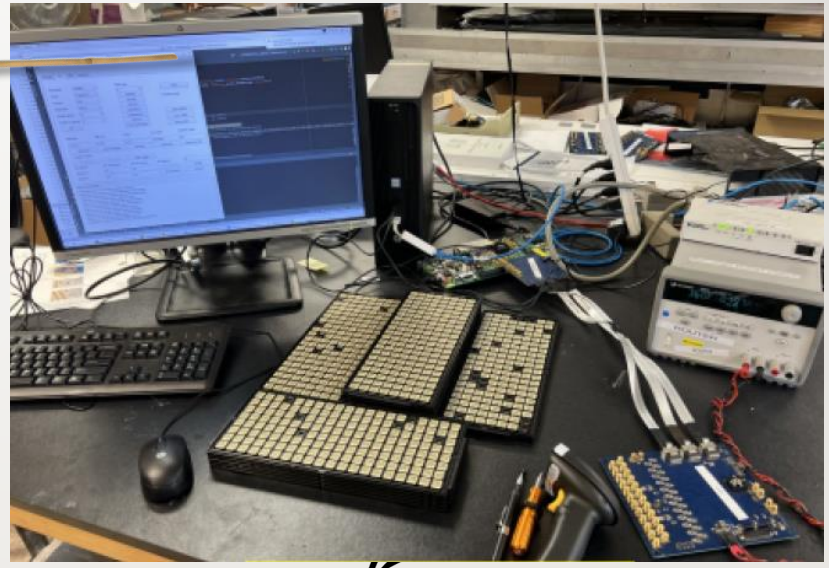
MDTs and sMDTs

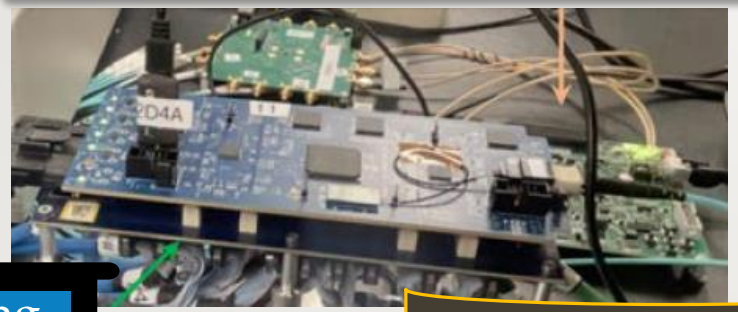
sMDT

- Production complete
- High precision and performance measured

Electronics:

- MDTs: All component passed FDR
  - ASICs are fully produced
- sMDT mezzanine delay due to cross-talk and mezzanine cable procurement





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Check out Hubert's poster

https://agenda.infn.it/event/37033/timetable/?view=standard#271-performance-of-small-diame

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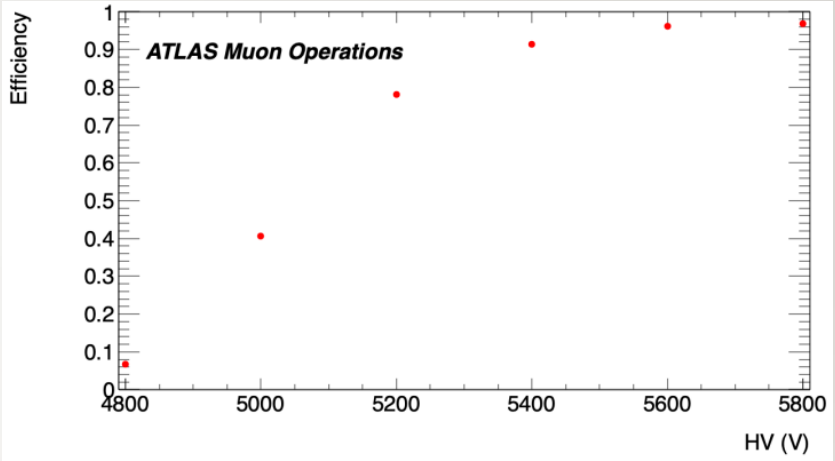
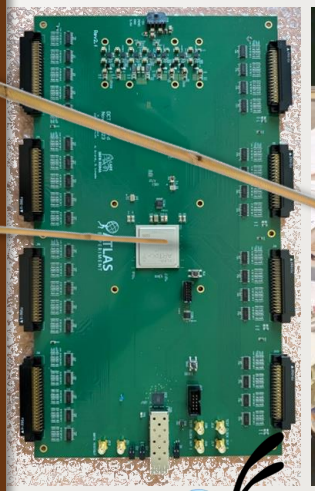
RPCs

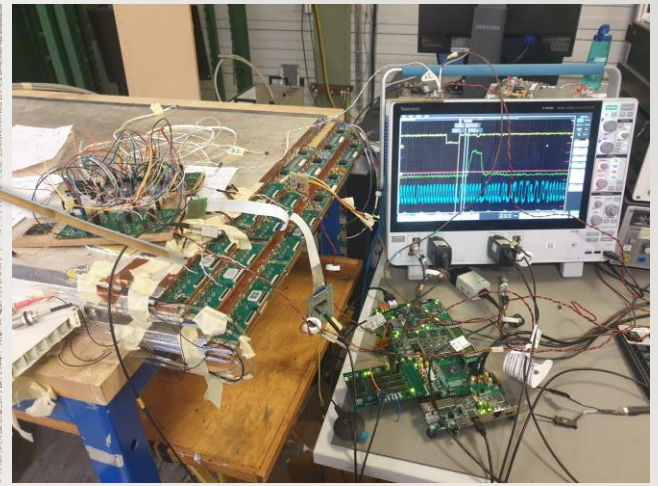
- Mechanics design validated
- Chamber production is about to start
  - Performance studied in the BIS78 project
- 1st FE-ASIC production delivered
- FE Boards final prototype
- Full validation of readout chain (RPC, FW ASIC, FE board, cable, DCT) ongoing

Trigger:

- Tests of 1st prototype BM/BO DCT with BIS78 chambers
  - Final prototype of BM-BO DCT being checked
- BI DCT full validation ongoing
- Positive tests of the DCT Manchester decoding via FPGA demo board







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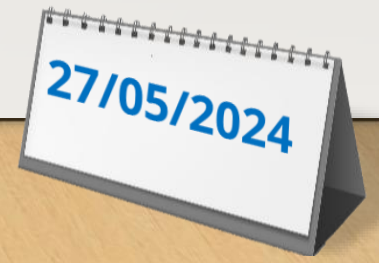
Check out Giorgia's and Sabrina's posters
https://agenda.infn.it/event/37033/timetable/?view=standard#170-study-of-environment-frien
https://agenda.infn.it/event/37033/timetable/?view=standard#51-atlas-level-0-muon-barrel-t



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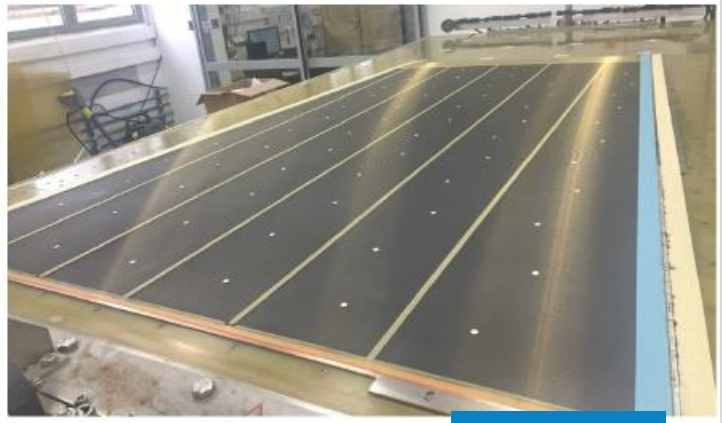
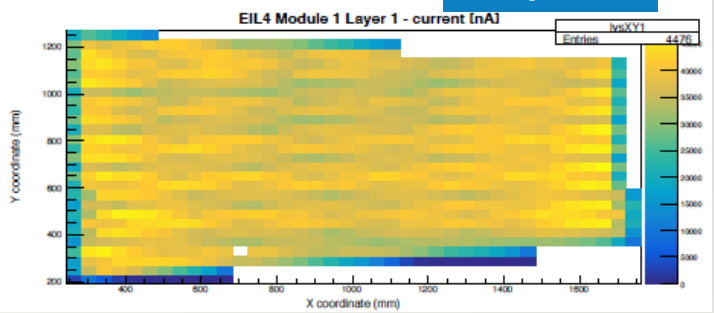
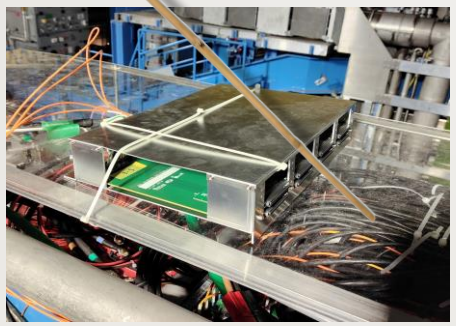
TGCs

- Chambers: Production is progressing well
  - The project will need to produce 50 units: 15xB, 15xF, 10xBs, 10xFs
  - Agreement with Muon and TC to have one EIL4 sector installed in YETS 24-25
- Electronics:
  - Phase-2 PS board demonstrator installed in UX15 and USA15
  - Initial "construction" of Phase-2 system in UX15 launched



X ray scan





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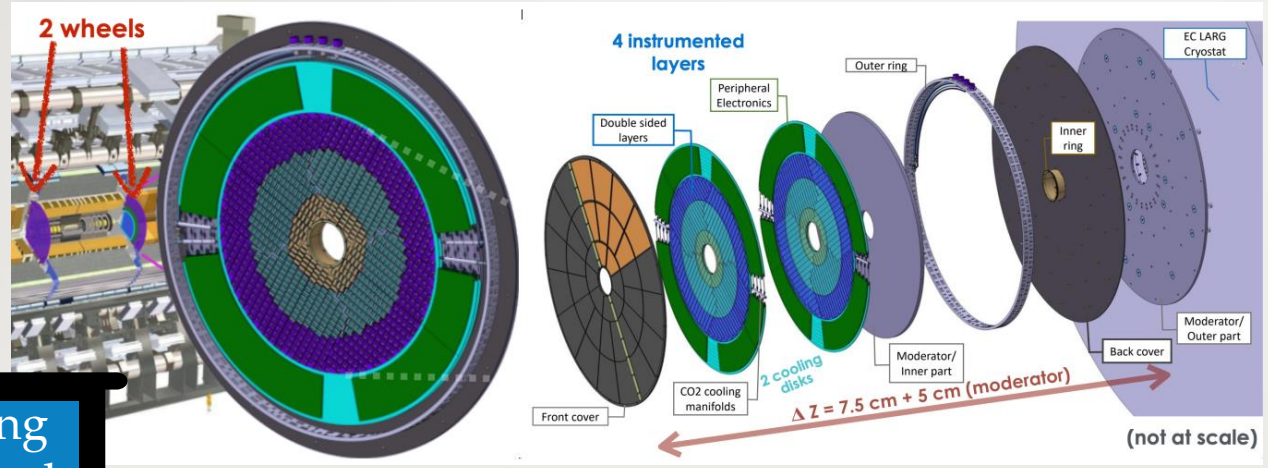
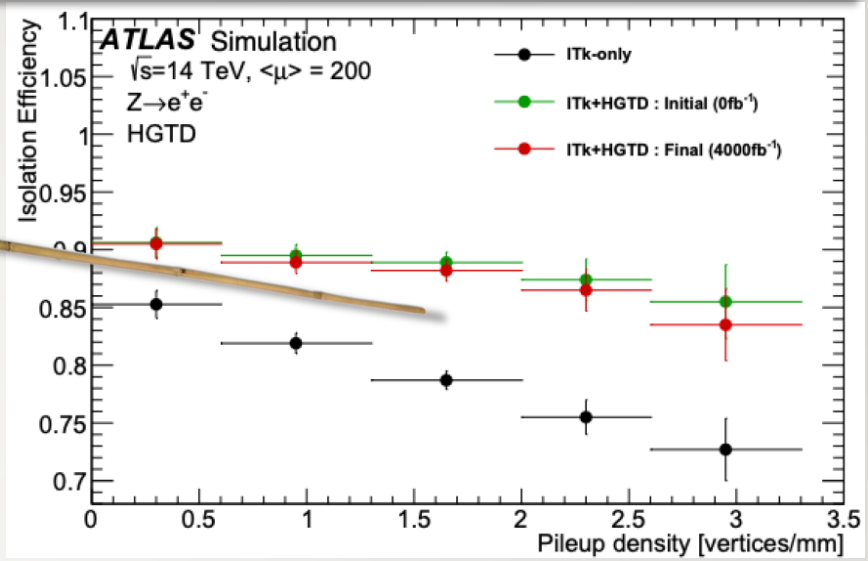
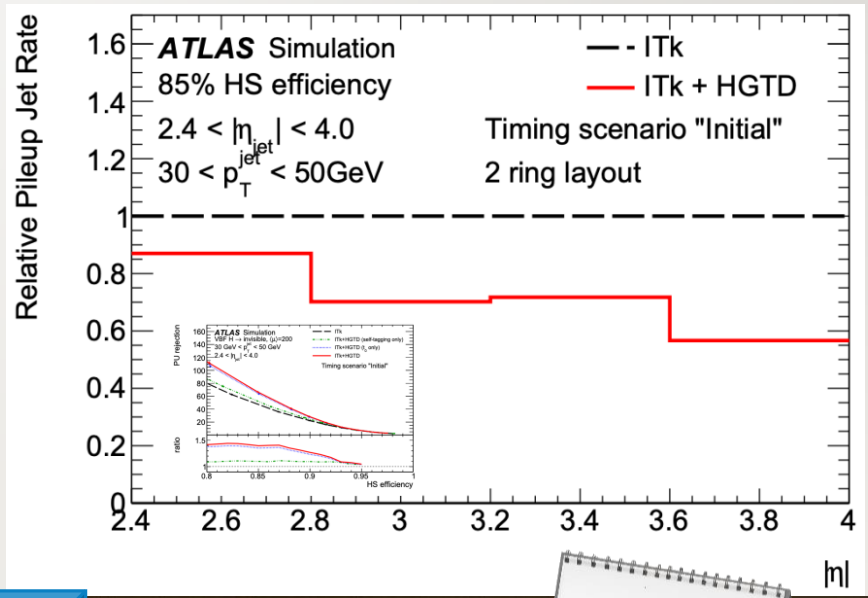
HGDT

- Fine timing (30-50ps/track) to disentangle events in large pile-up conditions
- Precision luminosity measurement bunch-by-bunch
- Four layers of silicon detector modules, covering $2.4 < |\eta| < 4.0$, 3.6 Mpix







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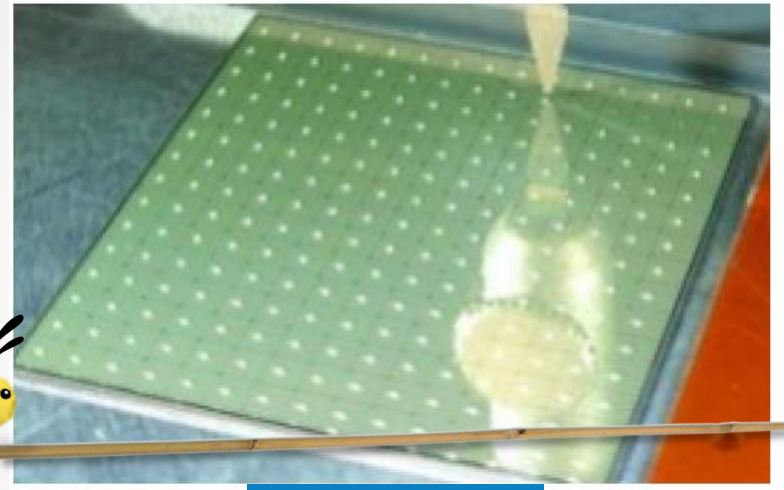
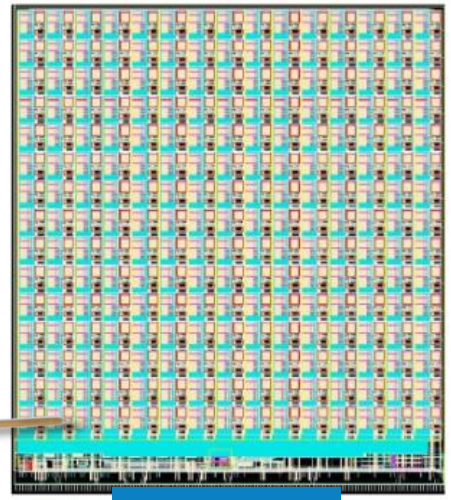
HGDT – detector and electronics

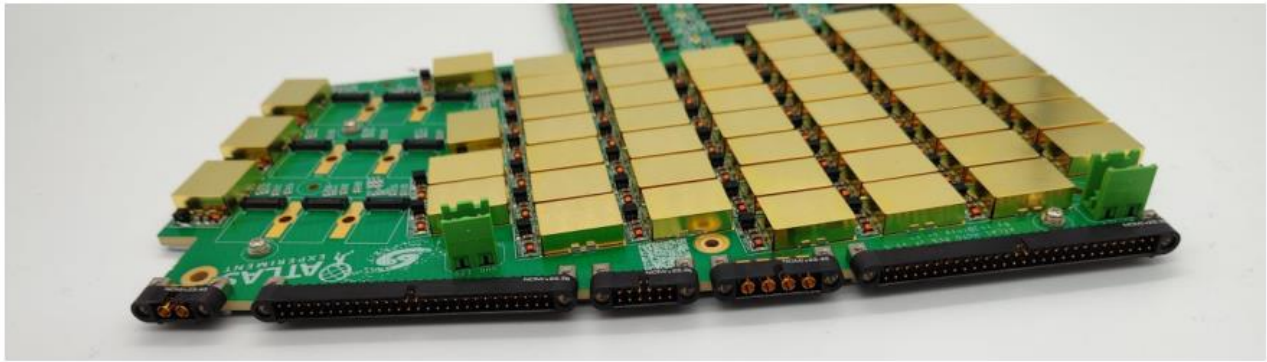
- Low gain avalanche detector (LGAD) technology sensors, bump-bonded to read-out ASIC.
- Pre-production complete, performance matches design requirements.
  - Read-out ASIC (ALTIROC3) shows good performance, pre-production version (ALTIROC-A) to be submitted soon
- Mechanics and cooling design in progress



LGAD sensor



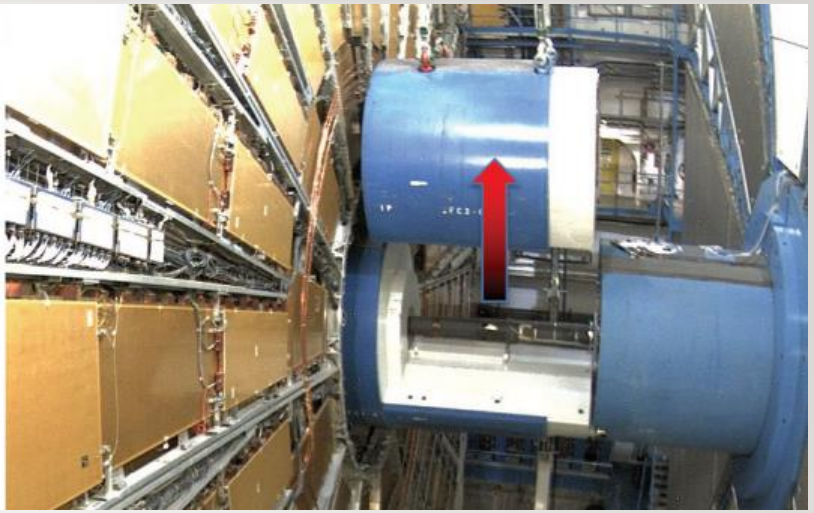
Altiroc-A

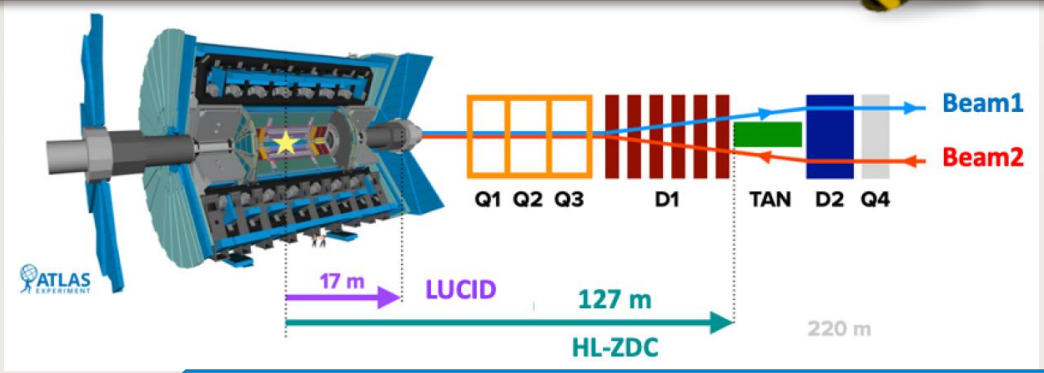


Peripheral Electronics Board (PEB) prototype

Forward Detectors

- LUCID - measure luminosity to better than 1% accuracy
  - 24/7/every day that LHC runs
- ZDC - measure high-rapidity neutrons in heavy ion collisions
  - Experimental measure of collision geometry
  - Trigger and offline selection of ultra-peripheral collisions
  - Measure azimuthal deflection angle with Reaction Plane Detectors (RPD)
- Technology: PMTs reading Cherenkov light
- Common electronics: LUCROD 2 board under development





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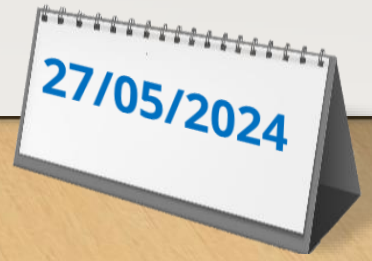

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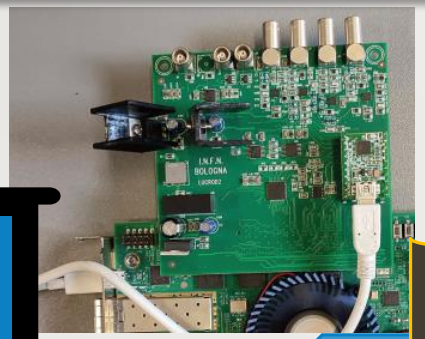
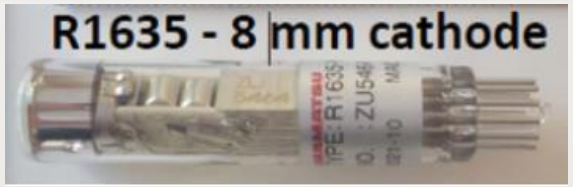
LUCID 3

- Primary goal for LUCID-3: to reduce acceptance
  - Mount the detectors on the inner surface of the JF shielding
  - 30% reduction in geometric acceptance (increased radius)
  - Also easier to access/replace during YETS
  - Use smaller PMT➡30% reduction in acceptance
- Maximize redundancy and complementarity
  - Fiber charge detector linear with <μ>, low failure risk
  - JN detector low mu-dependence
  - New LGAD – based detector: BMA
- First Electronic prototype with 12 bit ADC @ 640 MHz FADC under testing (HMCAD1520)





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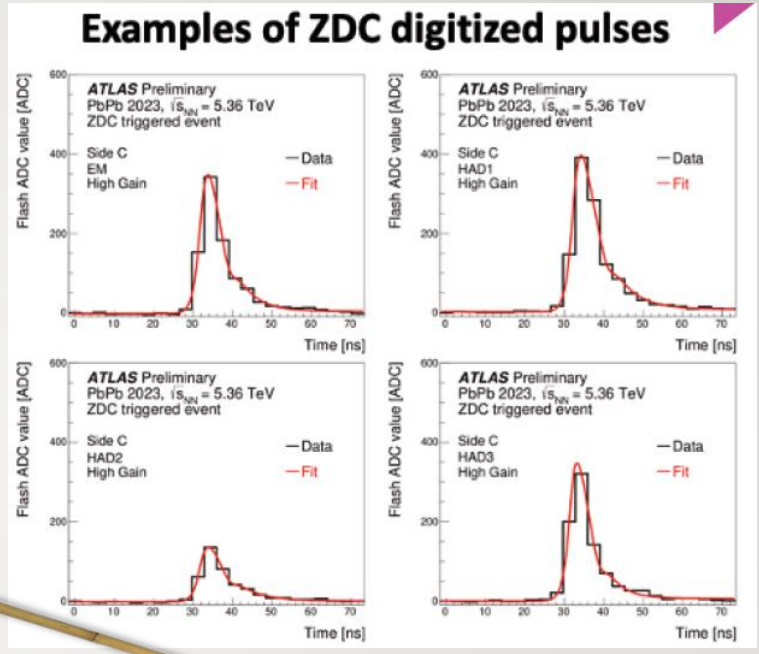
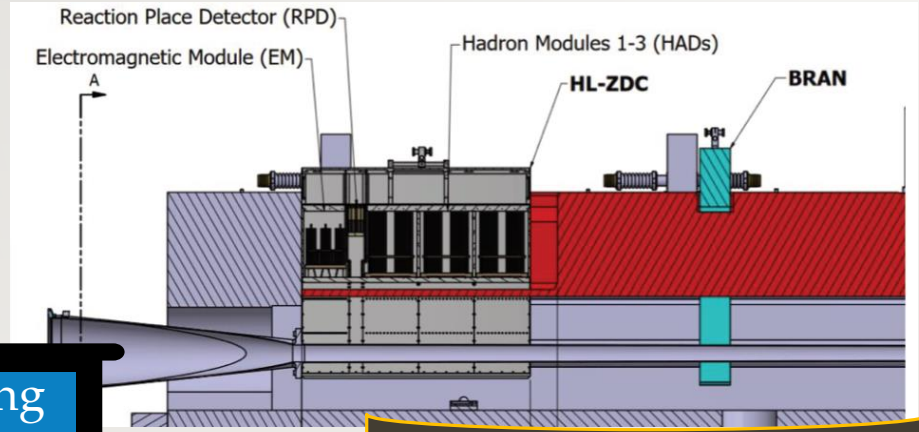
Check out Davide's poster
https://agenda.infn.it/event/37033/timetable/?view=standard#478-lucid-3-the-upgrade-of-the

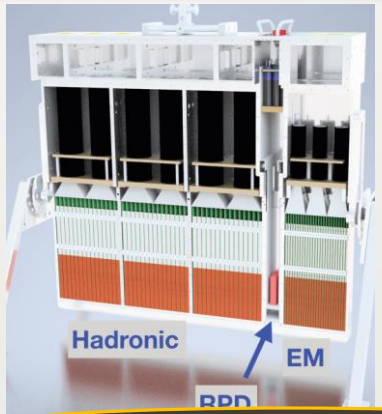
27/05/2024

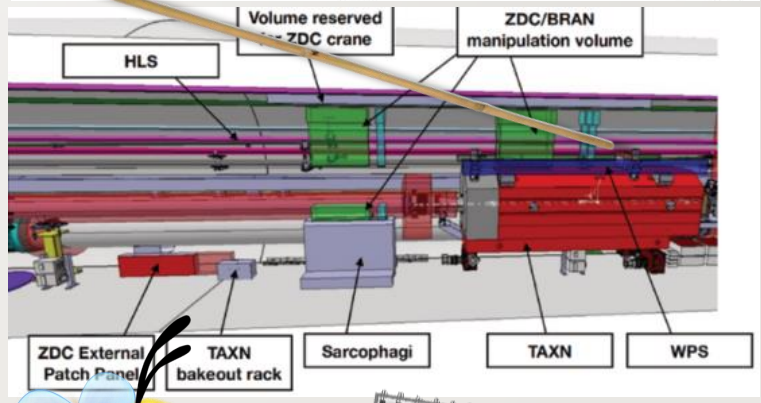
ZDC – Heavy ion runs

- We now have complete baseline detector design
  - Pre-production version to be built in 2024-2025
  - Test in SPS test beams (proton and Pb) before LS3
- Studies of different kinds of fused silica (BRAN, reactors) ➞ Rad-hard fibers in Run 3 ZDC
- Reduced acceptance enforced by HL-LHC TAXN ➞ (More than) compensated by increased longitudinal thickness (+1λInt)









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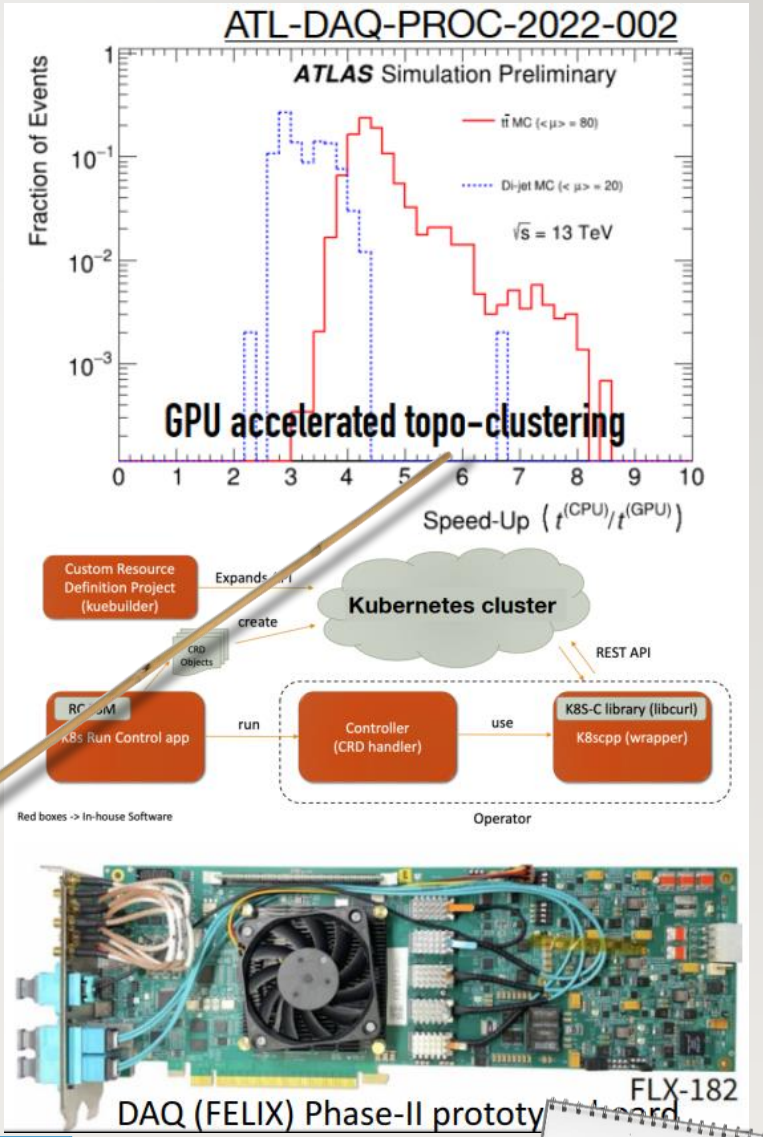
Check out Yftach's poster

https://agenda.infn.it/event/37033/timetable/?view=standard#479-atlas-zdc-for-run-3-and-ru

TDAQ

- Moved to single-level HW trigger at 1 MHz
- Detector read-out with 10us latency at 5 TB/s based on FELIX
  - 2.5-25 Gb/s optical link speeds
- Using ATCA standard
- Bi-directional TTC
- Increased usage of SoC
- Container-based farm
- Kubernetes (k8s) for farm orchestration
- Accelerators (GPU), Machine Learning (ML) and Neural Networks (NN) for online reconstruction



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Status and Conclusions

- The HL-LHC programs challenges the detector and detector electronics in many aspects, including high radiation doses and high pile-up
- ATLAS is going through a vast upgrade effort involving all systems to different degrees to ensure high efficiency and data quality
- Most detectors will have hardware upgrades or complete replacements and redesigns
- The electronics of every detector will be updated to improve performance and comply with the new TDAQ standards
- Most detectors are on schedule and have prototype systems already installed or under testing
- Some systems suffered from setbacks due to external and internal causes. We are working towards recovering the dealys

Thank you for your attention!

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Federico Lasagni Manghi

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BACKUP

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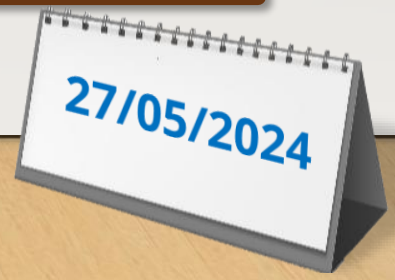

Liquid Argon (LAr) EM calorimeter

On Detector: 128 channel FEB2V2 prototypes fabricated and assembled

- Analog processing of signals, Digitization of PA/S outputs
- ALFE2 and HPS (130 nm CMOS) COLUTA (65 nm CMOS) custom ASICS

Off-Detector: LAr Timing System (LATOURNETT board):

- Trigger, Timing and Control (TTC) distribution & configuration based on lpGBT

Off Detector: LAr Signal Processor (LASP)

- digital filtering to waveforms from FEB2, energy & time, transmits to trigger and DAQ