Characterization of hybrid photodetector prototype based on MCPs and the Timepix4 ASIC

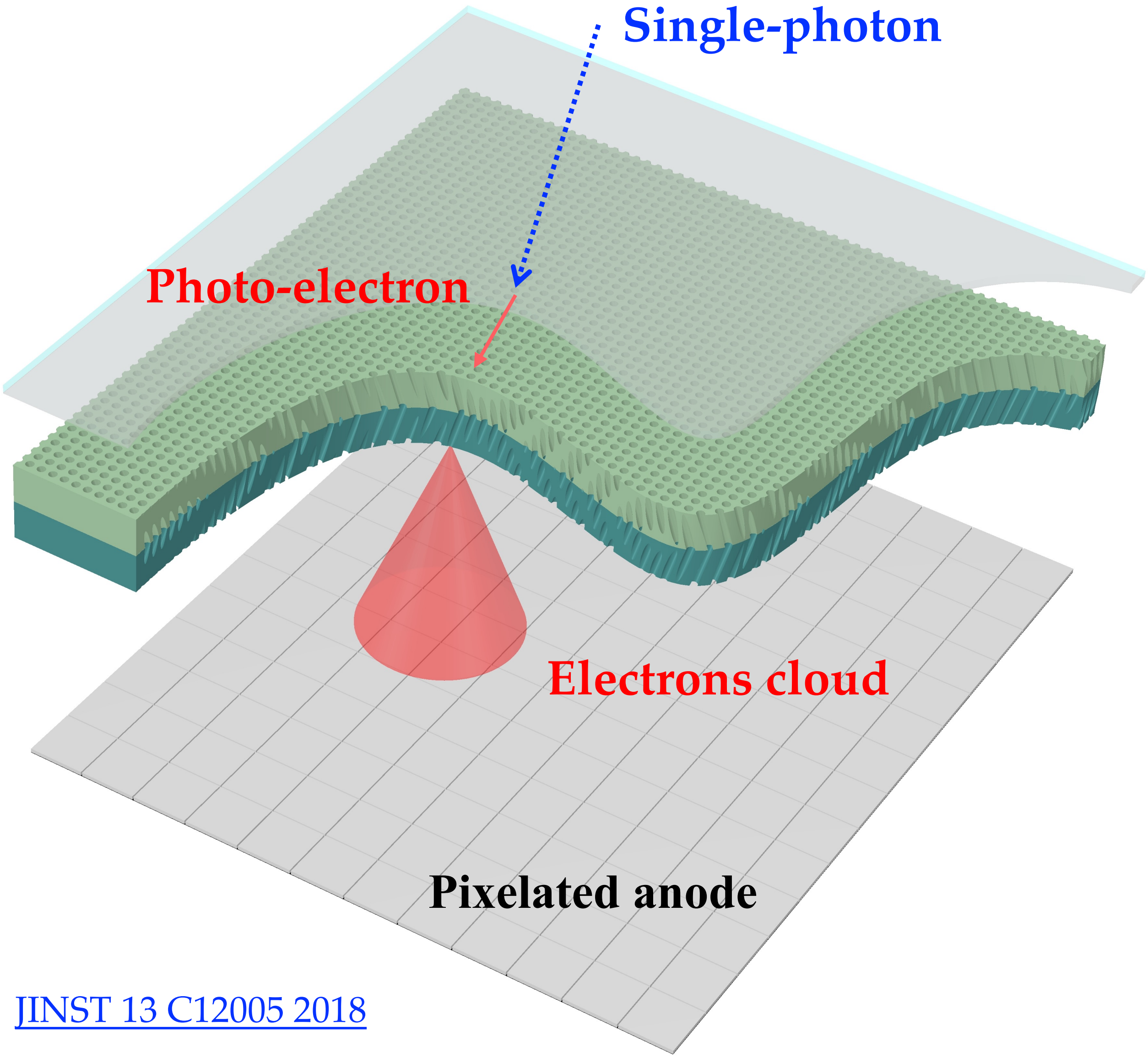
J.A. Alozy[a], R. Ballabriga[a], N.V. Biesuz[b], R. Bolzonella[b,c], M. Campbell[a], V. Cavallini[b,c], A. Cotta Ramusino[b], **M. Fiorini[b,c]**, E. Franzoso[b], M. Guarise[b,c], X. Llopart[a] , G. Romolini[b,c], A. Saputi[b]

[a] CERN [b] INFN Ferrara [c] University of Ferrara

16th Pisa Meeting on Advanced Detectors

La Biodola, May 27th 2024

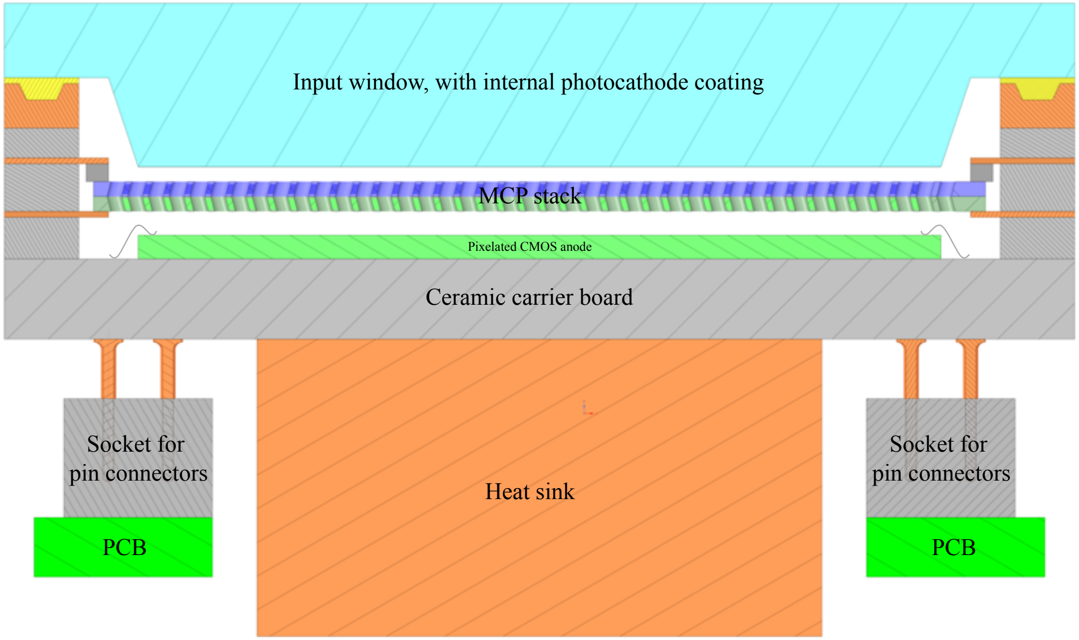
Hybrid MCP-PMT concept



JINST 13 C12005 2018

- Entrance window + photocathode
- Microchannel plate stack
- Timepix4 ASIC as pixelated anode
  - Electron cloud (pixels cluster)
  - **55µm × 55µm** pitch
  - **0.23 M pixels** measuring arrival time and duration of input signals
  - **7 cm^2** active area
  - Up to **2.5 Ghits/s**
  - Local signal processing

Detector geometry



- Shortest photocathode-to-MCP distance
  - Preserve impact position information
- Optimized MCP-to-anode distance for optimal cluster dimension
  - Improvement in both position and timing resolutions (centroiding)
- Ceramic carrier transmits electrical signals to and from the Timepix4 through a series of of vias and pins
  - Heat sink for Timepix4 (~5 W thermal power)

Pixelated anode: Timepix4 ASIC

- Timepix4 ASIC in 65 nm CMOS (TSMC) **silicon pixel technology**
  - Developed and produced by the Medipix4 Collaboration for hybrid pixel detectors
- Charge sensitive amplifier, single threshold discriminator and TDC based on Voltage Controlled Oscillator
  - 4-side buttable (TSV)
  - Data-driven and frame-based read-out

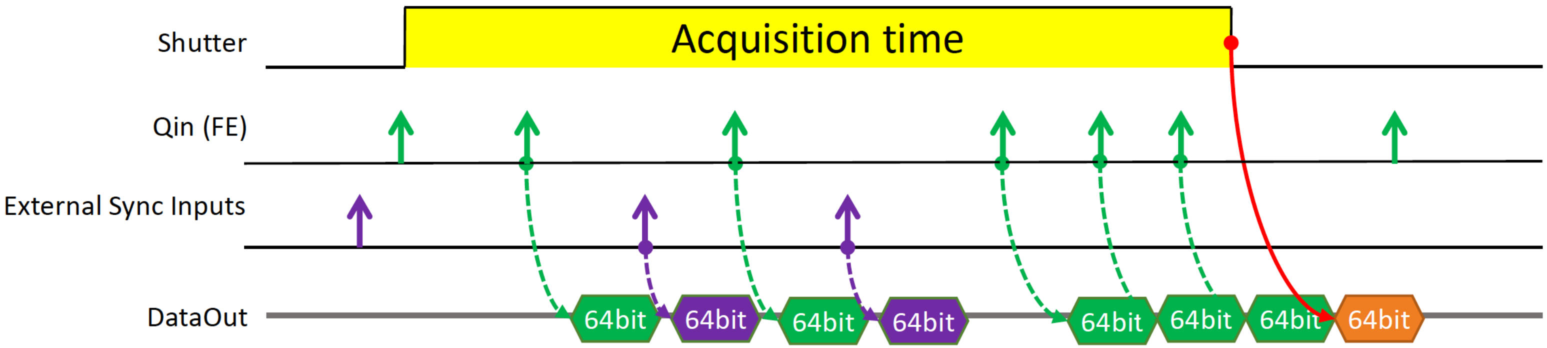
JINST 17 C01044 2022

Technology			**CMOS 65 nm**
Pixel Size			55 μm × 55 μm
Pixel arrangement			4-side buttable 512×448 (0.23 Mpixels)
Sensitive area			6.94 cm^2 (2.82 cm × 2.46 cm)
Read-out Modes	Data driven	Mode	TOT and TOA
		Event Packet	64-bit
		Max rate	358 Mhits/cm^2/s
TDC bin size			**195 ps**
Readout bandwidth			≤163.84 Gbps (16× @10.24 Gbps)
Equivalent noise charge			50-70 e^-
Target global minimum threshold			<500 e^-

X. Llopart (CERN)

Timepix4 data-driven read-out

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
- 4 external inputs to synchronize/align external signals with data



SPEC: Packet specifications ToA/ToT

Name	Width	MSB	LSB	Bits
Top	1	63	63	[63:63]
EoC	8	62	55	[62:55]
SP	6	54	49	[54:49]
Pixel	3	48	46	[48:46]
ToA	16	45	30	[45:30]
ufToA_start	4	29	26	[29:26]
ufToA_stop	4	25	22	[25:22]
fToA_rise	5	21	17	[21:17]
fToA_fall	5	16	12	[16:12]
ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

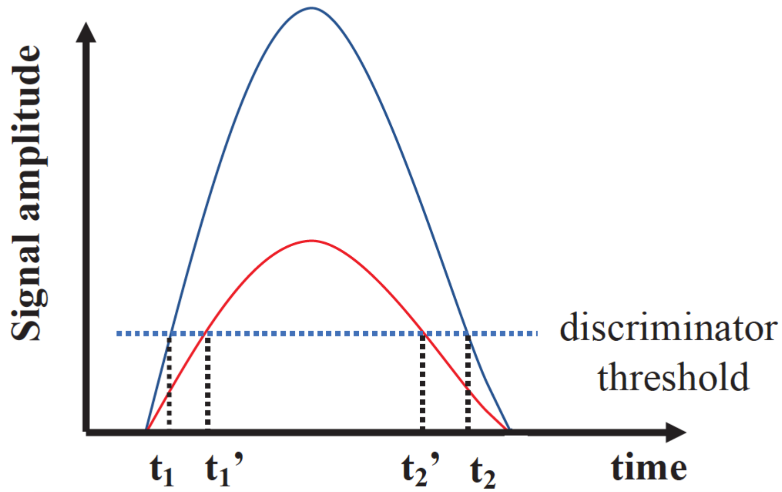
Address: 18 bits

Time: 29 bits

Energy: 21 bits

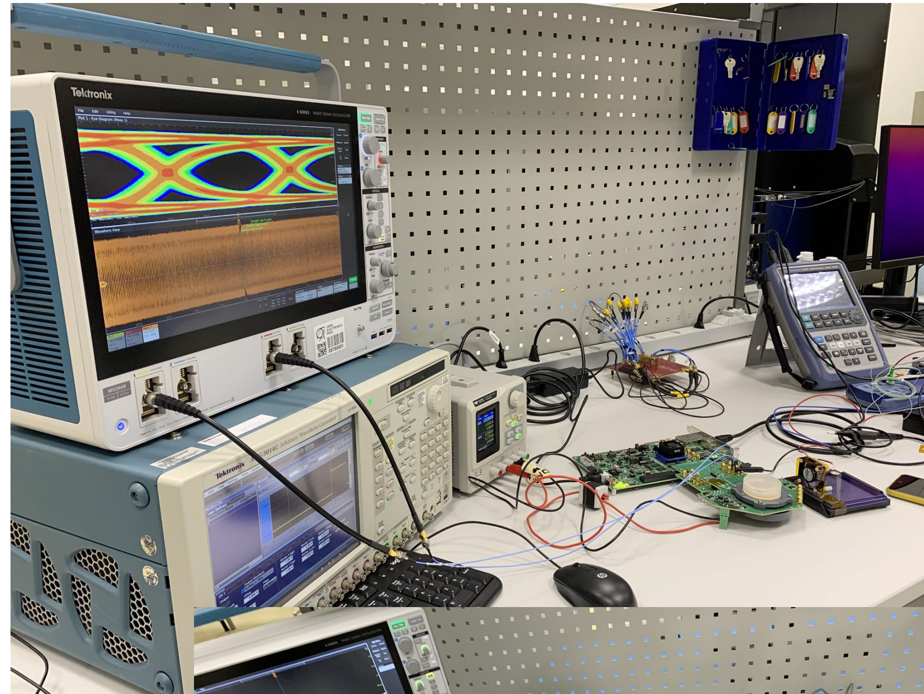
Timepix4 hit data

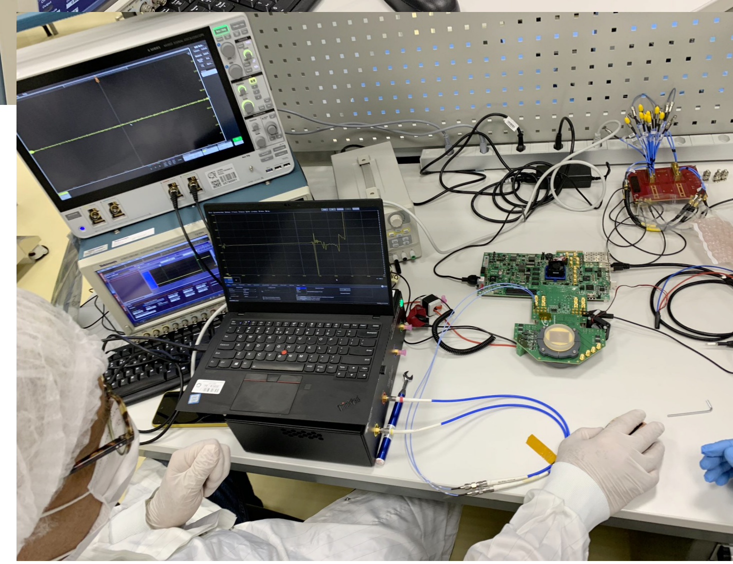
- Measure Time-of-Arrival (ToA=t_1) and Time-over-Threshold (ToT=t_2-t_1)
  - **TDC** bin size: 195 ps (**56 ps r.m.s. resolution** per pixel)
- Electron cloud spread over a number of pixels → cluster
- Use ToT information (proportional to the charge in a pixel) to:
  - Correct for time-walk effect in every pixel
  - Improve **position resolution** by centroid algorithm
    - Go from $55\mu m/\sqrt{12} \sim 16\mu m$ down to **5-10 μm r.m.s.** (MCP channels pitch)
  - Improve **timing resolution** by multiple sampling
    - Many timing measurements for the same photon → **few 10s ps r.m.s.**

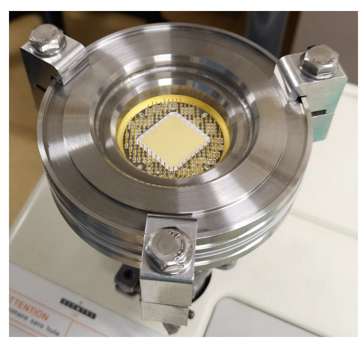


Ceramic carrier

- Electrical design critical due to 10 Gbps lines
- Signal integrity simulations
  - PGA not limiting factor per se
  - Requires careful pin placement
- Main contributions to signal degradation
  - Parasitic capacitance
  - Aluminium oxide multilayer PCB
  - Pads (wire-bond and pin pads)
- Produced by Kyocera
  - Extensive tests performed
  - Metrology, vacuum leak, thermal
  - Electrical characterization including integration with Timepix4

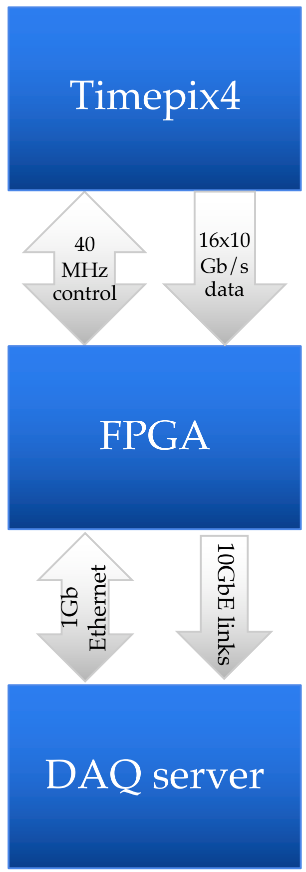


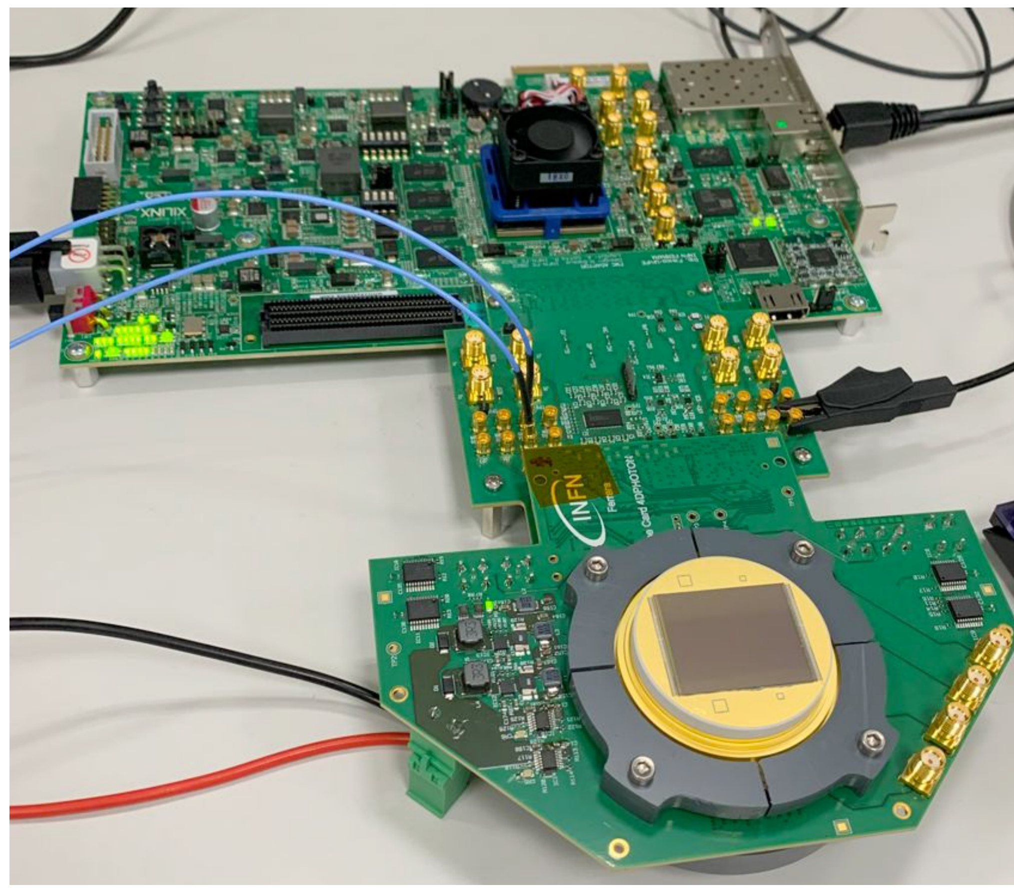




Electronics and DAQ

- On-detector electronics
  - Timepix4 ASIC in the tube; regulators; Electro-optical transceivers link the ASIC to an FPGA-based board for the exchange of configuration (slow control) and the collection of event data; etc.
- Off-detector electronics
  - FPGA far from detector
- The FPGA performs serial decoding and sends the data to a PC for data analysis and storage using fast serial data links



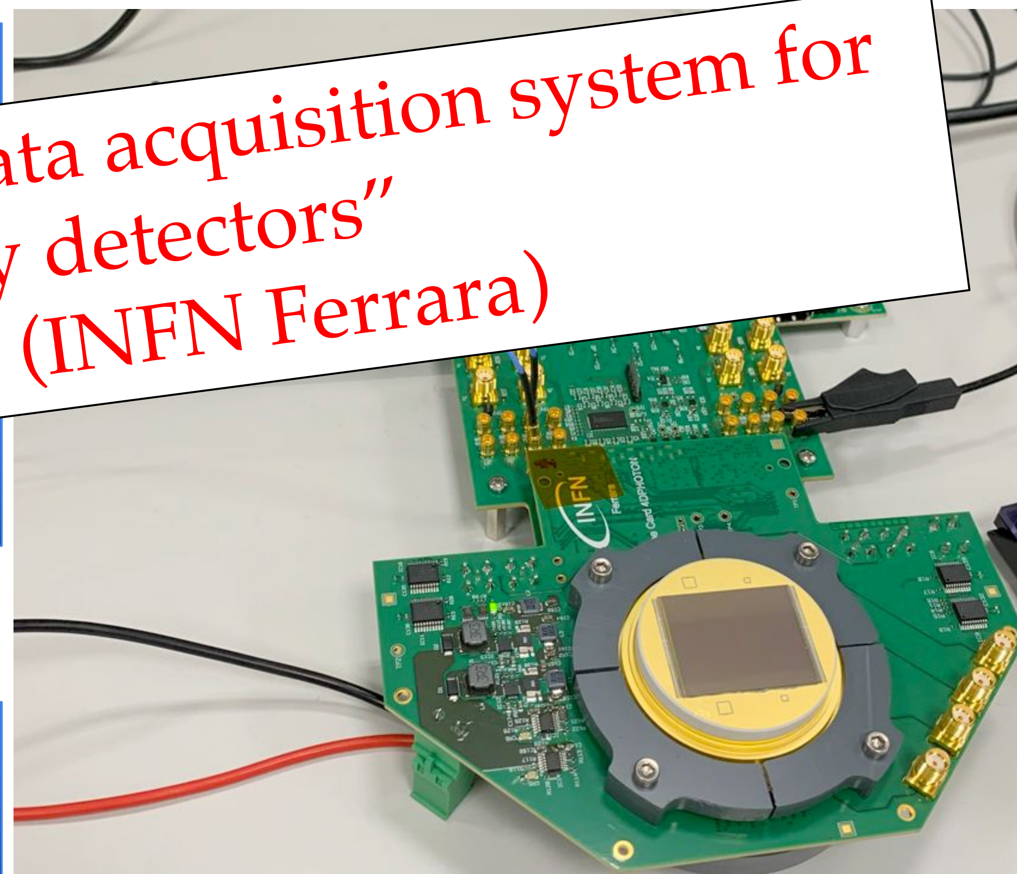


Electronics and DAQ

- On-detector electronics
  - Timepix4 ASIC in the tube; regulators; Electro-optical transceivers link the ASIC to an FPGA-based board for the exchange of configuration (slow control) and the collection of event data; etc.
- Off-detector electronics
  - FPGA far fro…

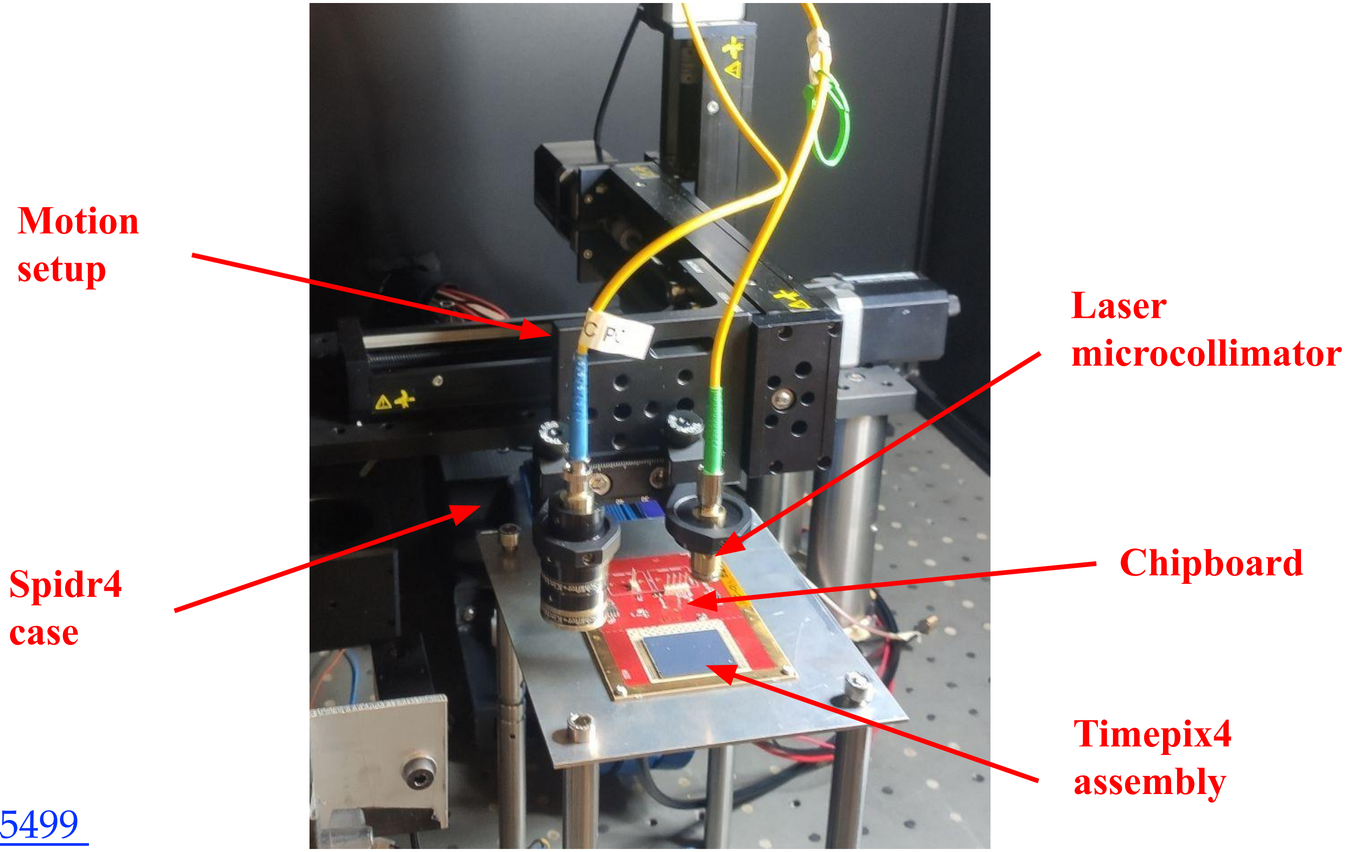
Poster "A flexible data acquisition system for the MEDIPIX family detectors" by Nicolò V. Biesuz (INFN Ferrara)

s… the data to a PC for data analysis and storage using fast serial data links



Timing resolution measurements (1)

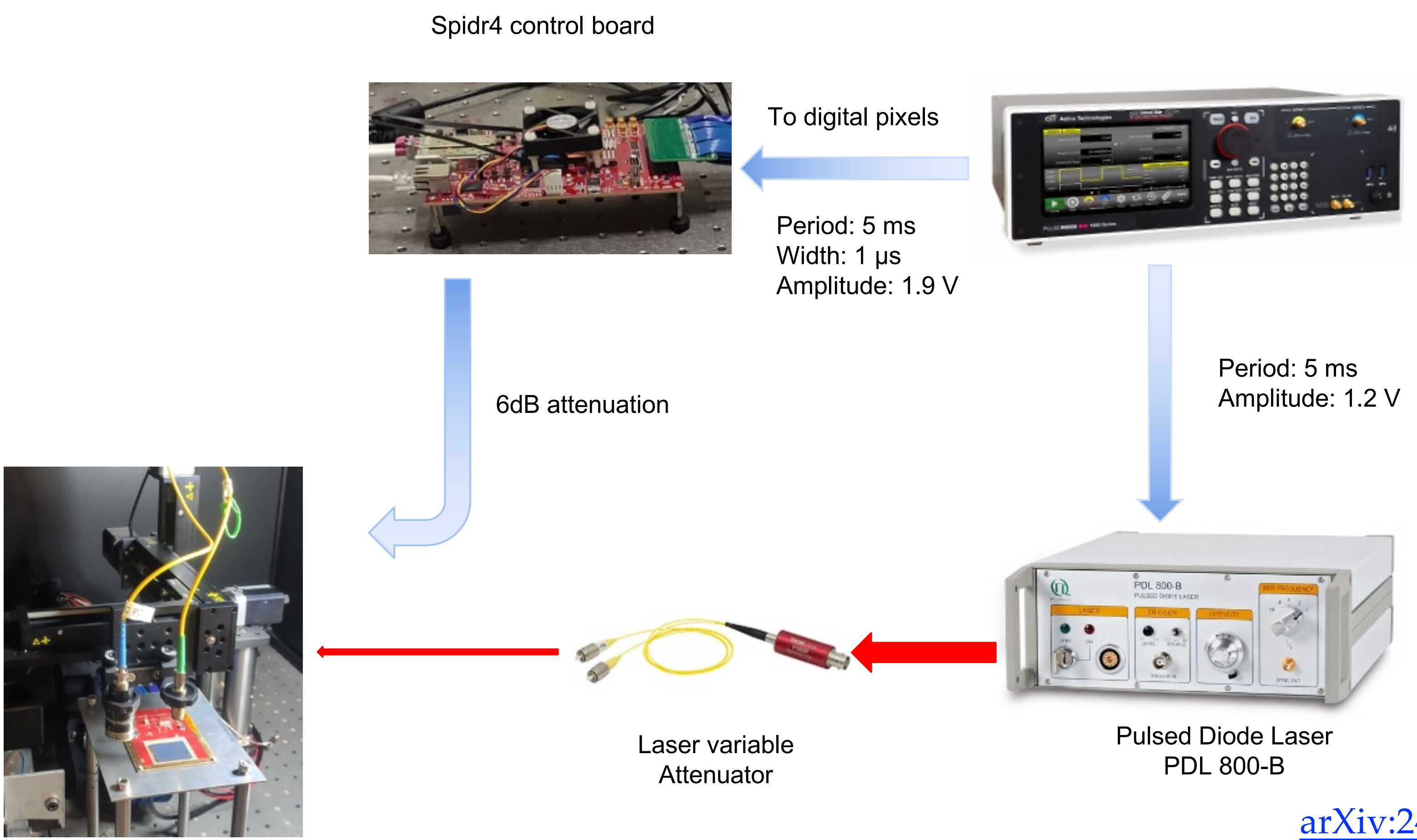
- Using SPIDR4 control board (Nikhef)
- Timepix4_v2 bonded to a 100 μm n-on-p Si detector
  - Metallization with holes pattern
  - Thanks to V. Coco (CERN), M. Van Beuzekom (Nikhef) et al. (LHCb Velo)



arXiv:2404.15499

Timing resolution measurements (2)

- Waveform generator: input signal to digital pixels + laser trigger
- Picosecond diode laser: 1060 nm + variable attenuator
- Linear translation stages: 3D position regulation with μm precision

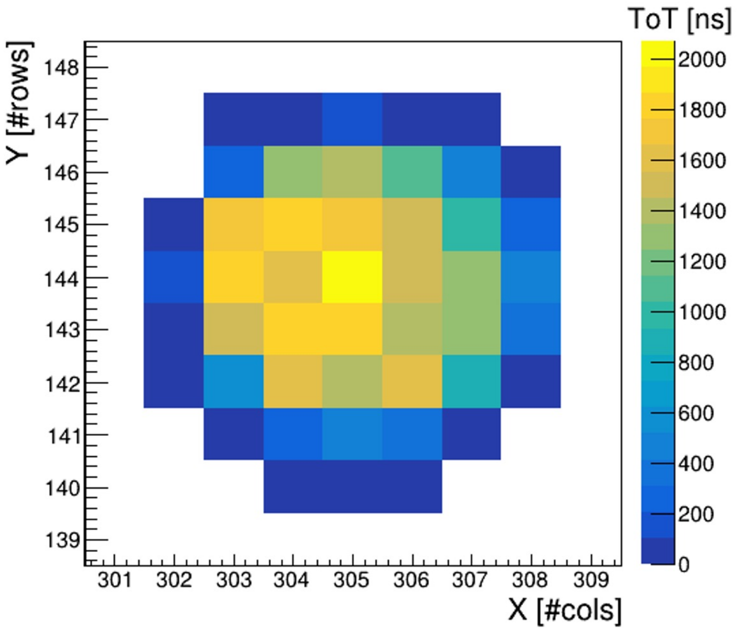


arXiv:2404.15499

Timing resolution measurements (3)

- Laser focused using micro-collimator:
  - σ = 1.4 pixel = 77 μm

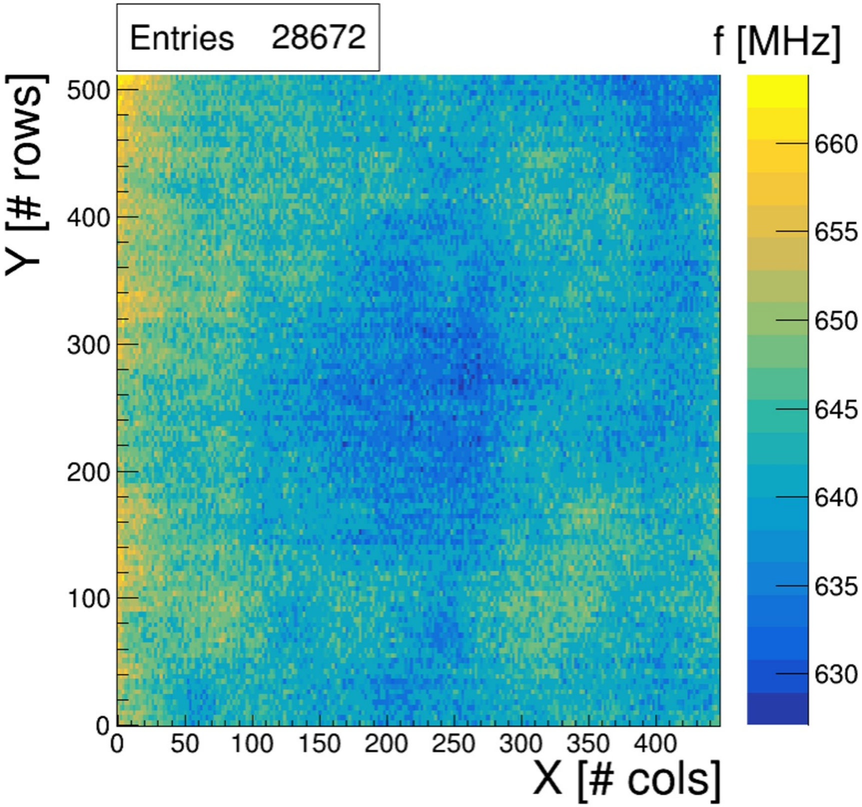
- Laser spot in fixed position for all presented measurements



[arXiv:2404.15499](https://arxiv.org/abs/2404.15499)

Timing resolution measurements (4)

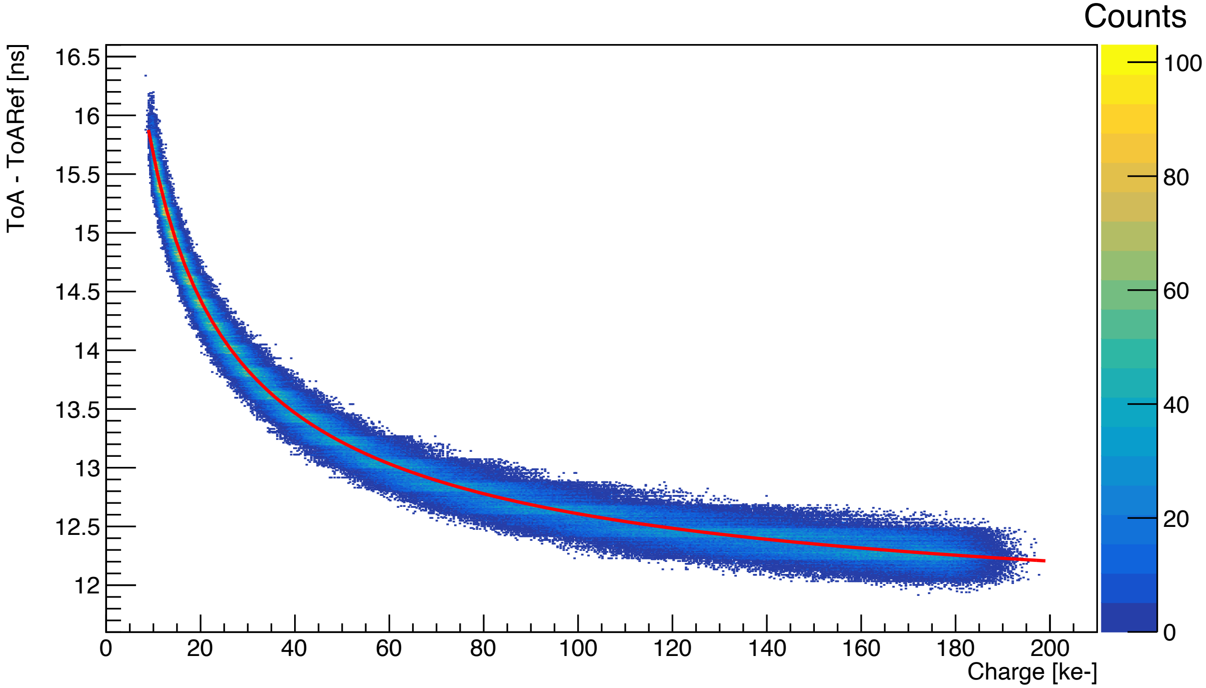
- VCO of different pixels oscillate with different frequencies
- Finer ToA bins generated with different width
- ToA and ToT measurements heavily affected by this effect
- Internal test pulse tool exploited to calibrate VCO frequencies for the whole matrix (~28.7k VCO)



[arXiv:2404.15499](https://arxiv.org/abs/2404.15499)

Single pixel resolution (1)

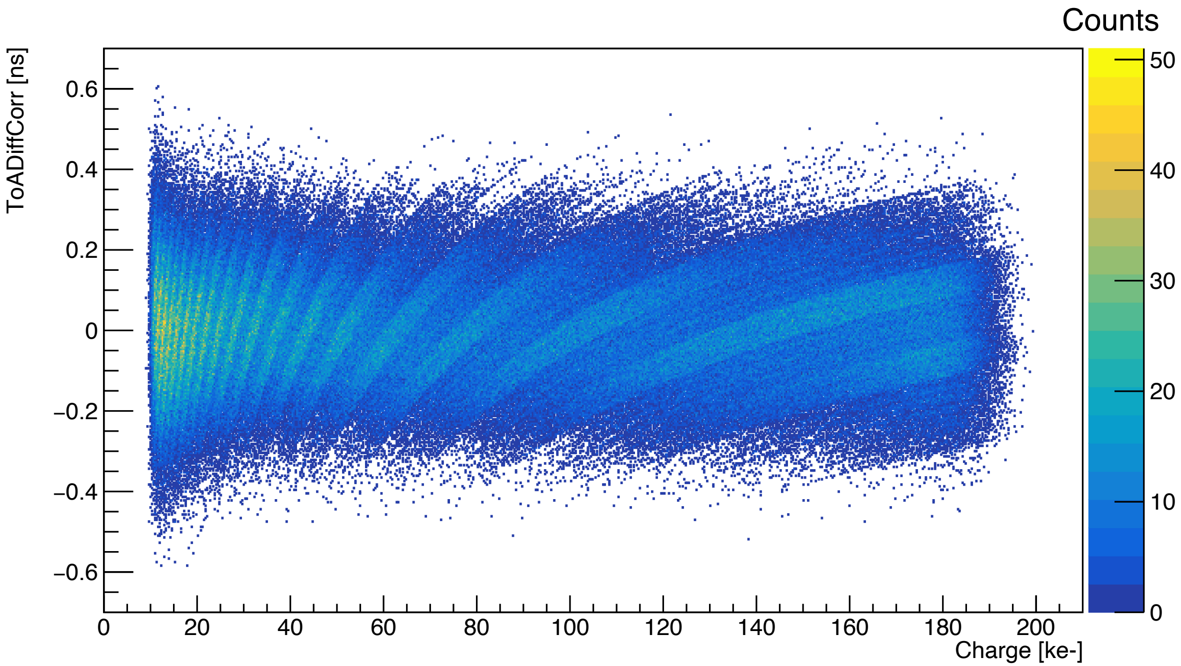
- Single pixel timing resolution
- Measurements using variable laser attenuation, populating a wide ToT range on each pixel
- Different time walk trends on different pixels
- Time walk corrected separately on each pixel



arXiv:2404.15499

Single pixel resolution (2)

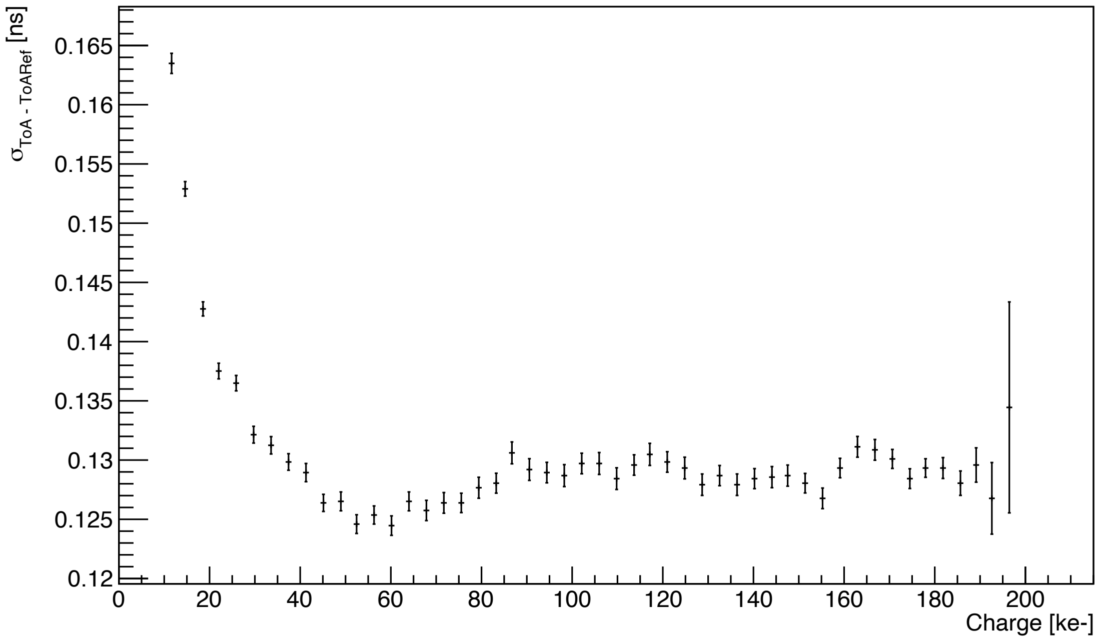
- Single pixel timing resolution
- Measurements using variable laser attenuation, populating a wide ToT range on each pixel
- Different time walk trends on different pixels
- Time walk corrected separately on each pixel



arXiv:2404.15499

Single pixel resolution (3)

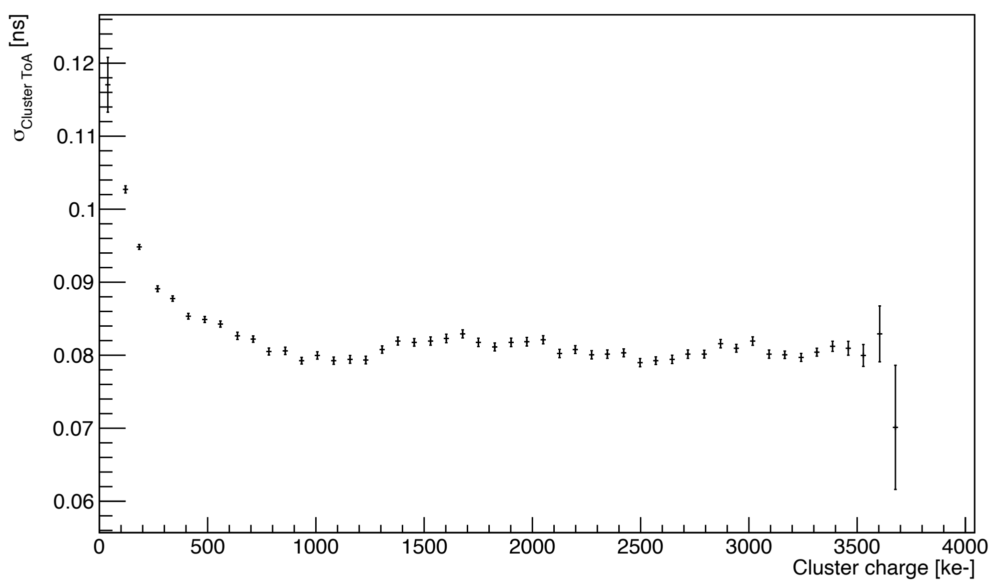
- Single pixel timing resolution
- Distribution of timing resolution as a function of injected charge
- For the pixel [305,144], where the laser is focused, the standard deviation saturates at 128±1 ps r.m.s.
- Subtracting the contribution of the reference TDC (72 ps r.m.s.), a resolution of **106±1 ps r.m.s.** is obtained for charge >40 ke$^-$



arXiv:2404.15499

Cluster resolution (1)

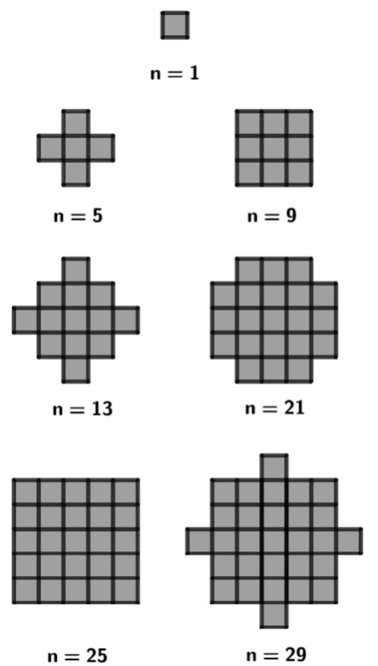
- For each cluster we compute:
  - Weighted average of ToA using charge as weights
  - Total cluster charge computed
- Timing resolution dependence on cluster charge:
  - best result: $\sigma_{ToADiffAvg}$=79 ± 1 ps r.m.s.
- Timing resolution after subtracting reference TDC contribution:
  - σ_{ToAAvg}= **33 ± 3 ps r.m.s.**

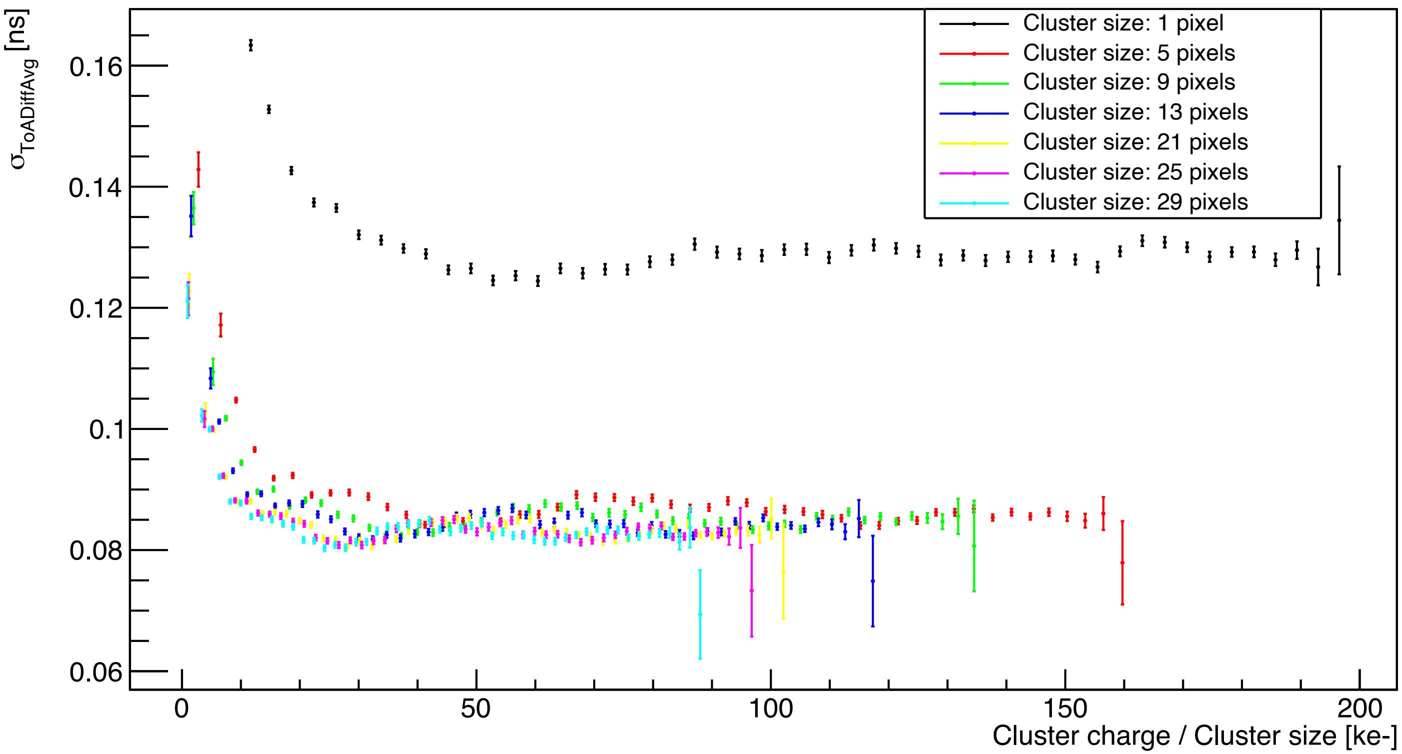


arXiv:2404.15499

Cluster resolution (2)

- Offline "variation of cluster size": consider shells of pixels within the same physical cluster
  - Large improvement in the resolution from 1-pixel clusters to 5-pixels clusters
  - Small or negligible improvement increasing further the cluster size
- This result allows the definition of optimal cluster size for MCP

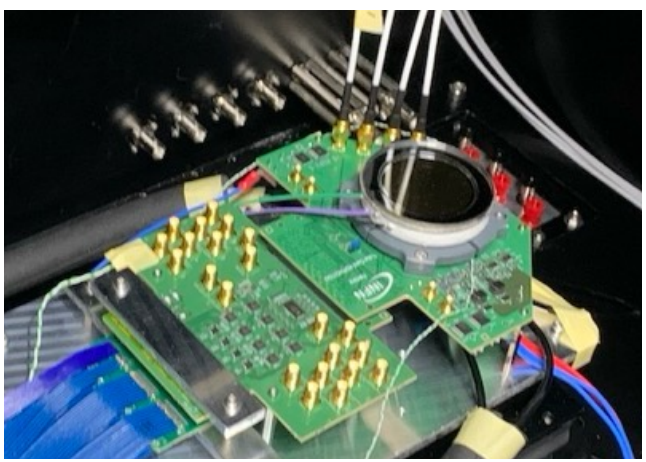


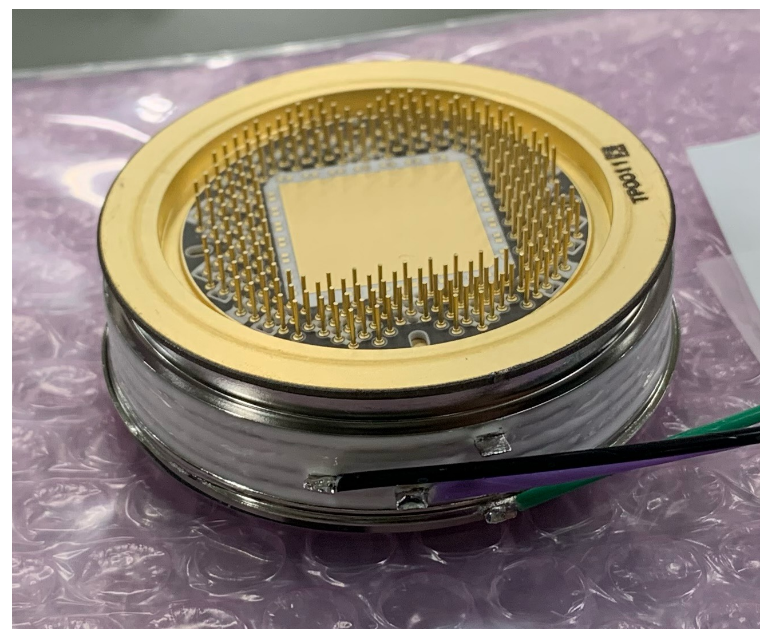


arXiv:2404.15499

Prototype vacuum tube

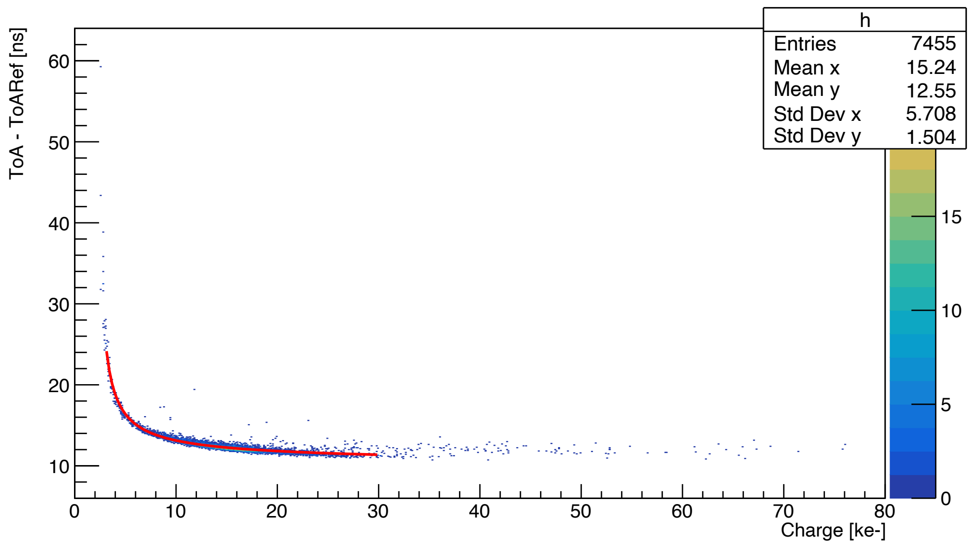
- Prototype vacuum tubes produced by Hamamatsu Photonics
  - First one delivered a couple of weeks ago
- Main characteristics:
  - Multi-alkali S20 photocathode
    - Peak QE >30% at 380 nm for the first produced sample
  - 6 μm MCP channel diameter (7.5 μm pitch)
- Different variants being produced for complete device characterization
  - 2-MCP stack and 3-MCP stack
  - 1d/2d/3d end-spoiling

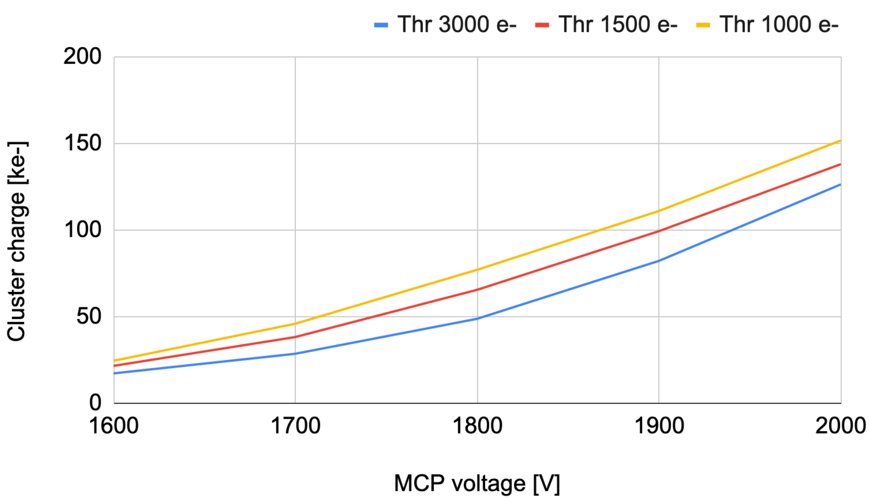




Vacuum tube: first measurements

- Preliminary results on first produced detector (2-MCP stack with 2d end-spoiling)
- Data-driven acquisitions in dark conditions (gain, DCR)
- Detector calibrations + Acquisitions of oscilloscope signals from "analogue" pads on the ceramic carrier
- Timing measurements with picosecond laser
  - Time-walk correction
  - Single-pixel timing resolution (explored low-charge range)





Outlook

- A "hybrid" MCP-PMT is being produced
  - Funded by European Research Council (G.A. No. 819627)
  - Demonstrator based on existing full-scale ASIC (Timepix4 developed by Medipix4 Collaboration for hybrid pixel detectors)
  - Complete integration of sensor and electronics
    - On-detector signal processing, digitization and data transmission with large number of active channels (~230 k pixels), with limited number of external interconnections (~200)
  - Goal: full exploitation of both timing and position resolution of MCP
- Future improvements for use in HEP harsh environments
  - Radiation hardness
    - Use rad-hard-by-design ASIC (plus rad-hard serializers)
  - High-rate capability and detector lifetime
    - Improve current MCP technology
  - Timing resolution
    - Use ASIC with smaller TDC bin size and lower front-end jitter

The DRD4 Collaboration: R&D on photon detectors and PID techniques

Massimiliano Fiorini
(INFN and University of Ferrara)

on behalf of the DRD4 Collaboration

16th Pisa Meeting on Advanced Detectors
La Biodola, May 27th 2024

DRD4 organization

- DRD4: international Collaboration with CERN as host laboratory
  - Approved by the CERN Research Board in December 2023
- Main goal: bundle and boost R&D activities in **photodetector technology** and **Particle Identification (PID) techniques** for future HEP experiments and facilities
- To be more specific, DRD4 covers the following topics:
  - Single-photon sensitive photodetectors (vacuum, solid state, hybrid)
  - PID techniques (Cherenkov based, Time of Flight)
  - Scintillating Fiber (SciFi) tracking
  - Transition Radiation (TR) using solid state X-ray detectors
- DRD4 structure initially defined in the Proposal document
  - 6 Working Groups (WGs) reflecting the main areas of R&D
    - Scientific forums for discussion: no agreed tasks, no committed resources
    - Facilitate exchange of information, know-how, samples, infrastructure, etc.
  - 5 Work Packages (WPs) reflecting the main ECFA roadmap themes and goals
    - Run like projects: divided in tasks, with agreed goals, milestones, deliverables, and are jointly funded by the resources of the participants

DRD4 activities

- 74 institutes joined DRD4 at the time of Proposal
  - 2 institutes recently admitted (more in the pipeline)
  - 20 nationalities
  - Many small groups, many with no prior experience in large R&D collaborations
  - Large effort to constitute a collaborative effort amongst a research community that has not traditionally worked together in the recent past
- DRD4 activities are ramping up: many scientific and technological discussions ongoing
  - See Indico pages for more details
  - These meetings allow building our community, enabling discussion of activities and the spread of information
- Next DRD4 Collaboration Meeting at CERN on 17-20 June 2024

DRD4 collaboration

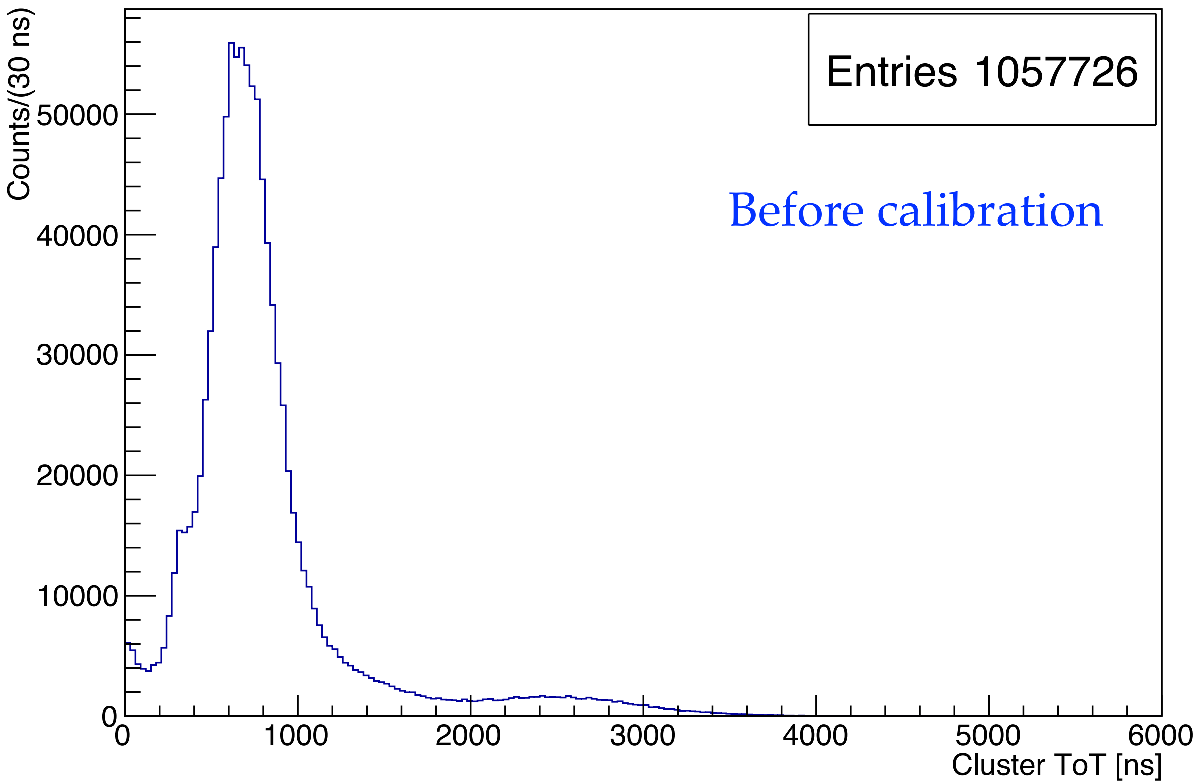
- New groups are welcome to join DRD4
  - For more information: https://drd4.web.cern.ch
  - If interested, please contact us (or simply subscribe to the "drd4-interested" list to be informed about ongoing activities)

Group photo at the DRD4 Constitutional meeting (CERN, January 2024)


THANK YOU
FOR YOUR ATTENTION
500
400
300
200
100
0
0
50
100
150
200
250
300
350
400

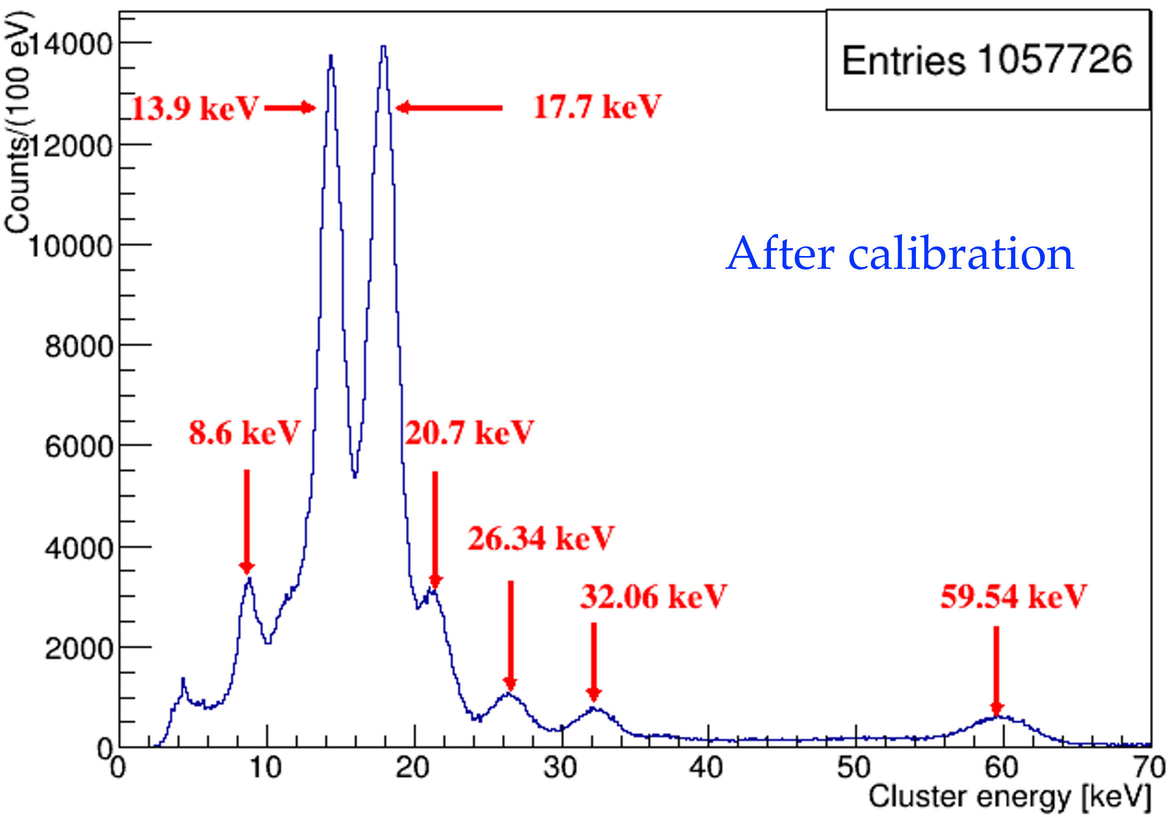
ToT Vs Q calibration

- Validation with radioactive sources (^{137}Cs and ^{241}Am superimposed spectra)



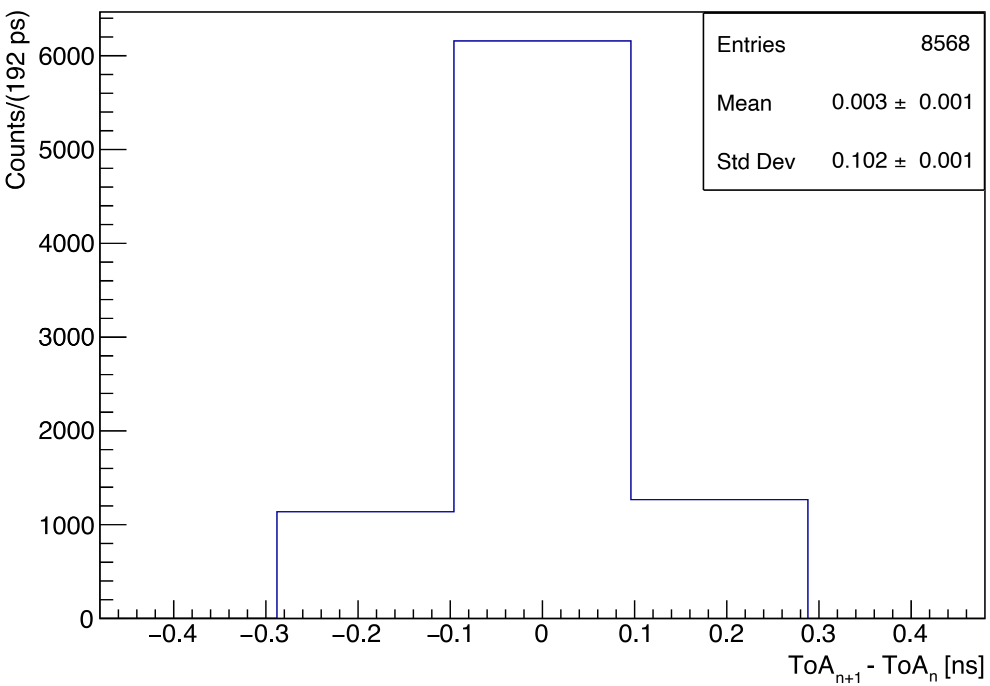
ToT Vs Q calibration

- Validation with radioactive sources (^{137}Cs and ^{241}Am superimposed spectra)



Reference signal resolution

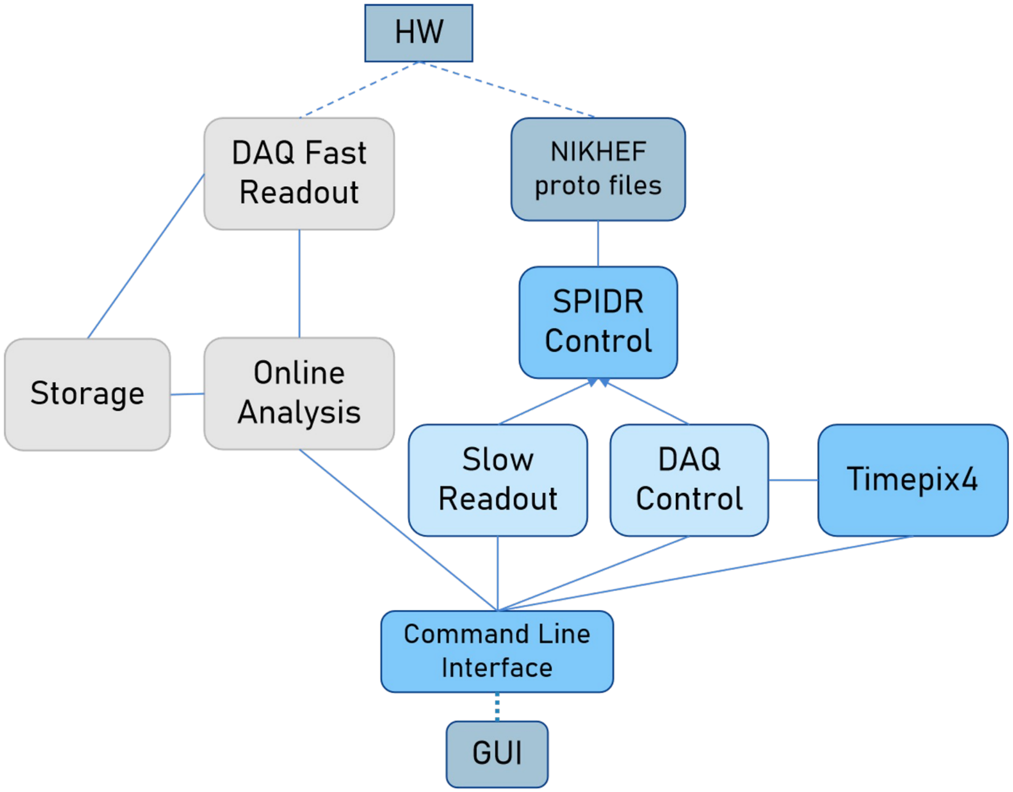
- Periodic pulse (externally generated, not synchronous to the 40 MHz Timepix4 reference clock) sent to the pixel through the digital pixels
  - Difference between the ToA of each pulse with the previous
- Result of 72 ps r.m.s. larger than 56 ps r.m.s. (contribution given by the generation of the external test pulses and their distribution to Timepix4)



arXiv:2404.15499

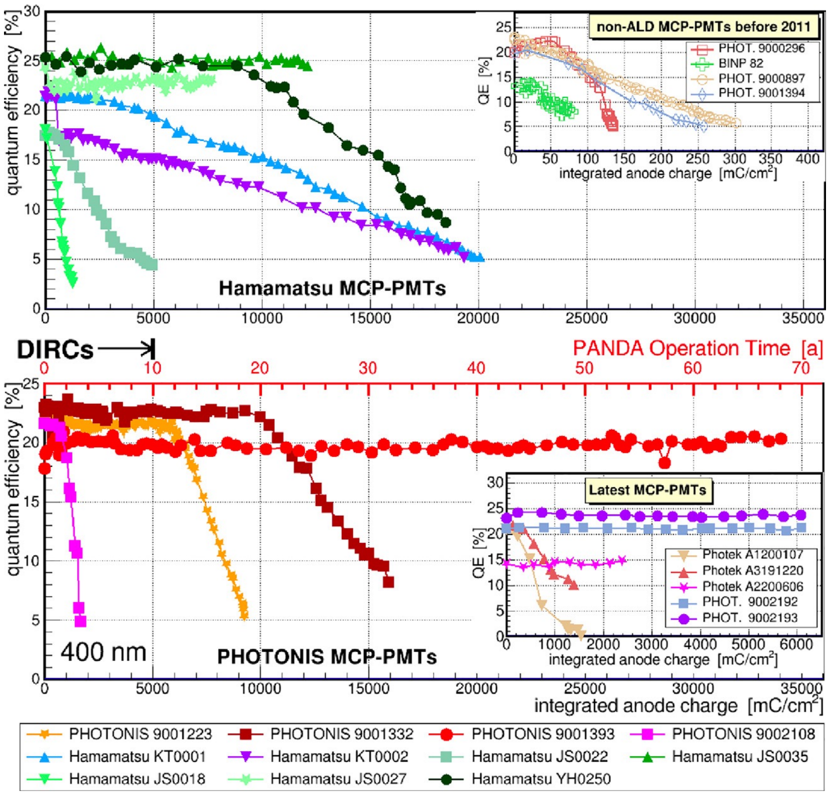
Software

- Dedicated software developed
- C++ based
  - Low-level
  - Object-oriented
- Readout and Control in unique CLI
- Read and Write register functions
- Application Programming Interfaces for Timepix4
- Packets decoder
- Open source



MCP-PMT limitations

- MCP-PMT lifetime limited by the integrated anode charge, which leads to a strong QE reduction
  - From 0.2 C/cm^2 to >30 C/cm^2 in recent years thanks to ALD
- With the expected photon hit rate (~10 MHz/mm^2), assuming a 10^4 gain (very conservative), and an operation of 10 years with 25% duty cycle we have:
  - Total IAC ~120 C/cm^2
  - Anode current density ~2 μA/cm^2
- ALD coating is based on the deposition of resistive and/or secondary emissive layers (could tune MCP properties)
  - Reported adverse effects on saturation current on some model with ALD
- Strong R&D to find the best "recipe" is needed



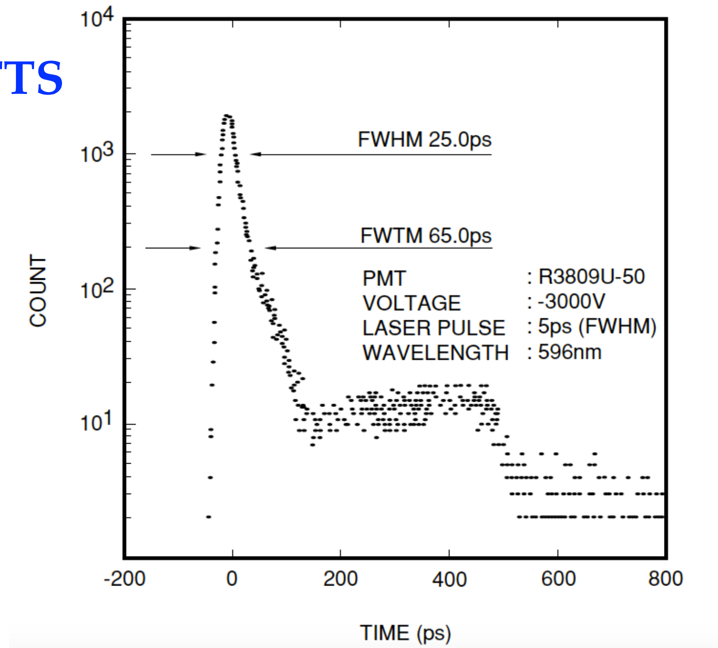
D. Miehling et al., NIM A 1049 (2023) 168047

Time resolution contributions

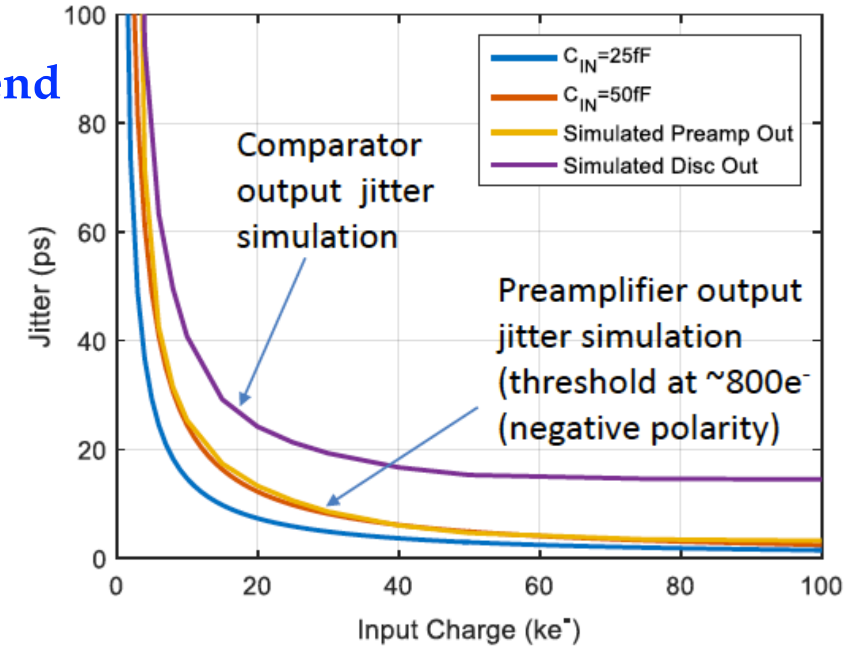
$$\sigma_{time} = TTS \oplus \sigma_{front-end} \oplus \sigma_{TDC}$$

- Contributions:
  - TTS (Transit Time Spread) of electrons: 25 ps FWHM
  - Front-end: <30 ps for input charge >10^4 e^-
  - TDC contribution: 56 ps (195 ps bin size/√12)
- Time resolution for **1 pixel**: **70 ps**

TTS



Front-end



PicoPix project

- PicoPix is intended to be a "realistic" demonstrator chip for a future upgrade of the LHCb Velo project (Velopix2)
  - Main requirement is time resolution < 30 ps rms
  - Other very challenging requirements (pixel size, radiation hardness, power, bandwidth, etc.)
- There is a limit on time resolution that are achievable for small pixels with limited power
- High-speed links in 28 nm (CERN EP R&D WP6)
  - lpGBT (10 Gbps) → DART28 (>26 Gbps)

X. Llopart (CERN)

Velopix2

- Initial requirements on Velopix2 from LHCb

	Requirement	scenario S_A	scenario S_B
	Pixel pitch [μm]	$\leq$55	$\leq$42
	Matrix size	256×256	335×335
Priority	Time resolution RMS [ps]	$\leq$ 30	$\leq$ 30
	Loss of hits [%]	$\leq$ 1	$\leq$ 1
	TID lifetime [MGy]	> 24	> 3
	ToT resolution/range [bits]	6	8
	Max latency, BXID range [bits]	9	9
	Power budget [W/cm²]	1.5	1.5
	Power per pixel [μW]	23	14
	Threshold level [e^-]	$\leq$ 500	$\leq$ 500
	Pixel rate hottest pixel [kHz]	> 350	> 40
	Max discharge time [ns]	< 29	< 250
	Bandwidth per ASIC of 2 cm² [Gb/s]	> 250	> 94

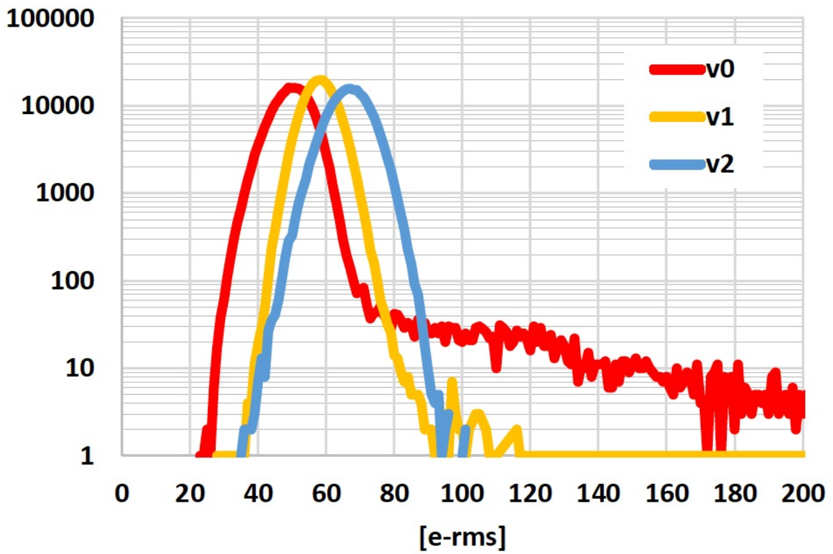
X. Llopart (CERN)

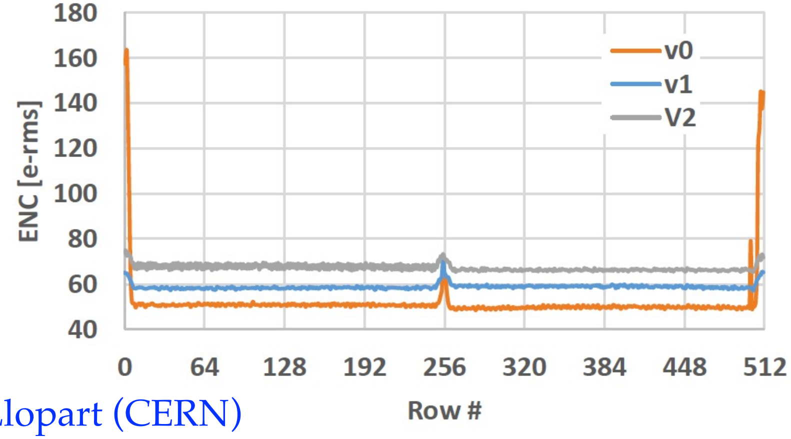
Challenging!

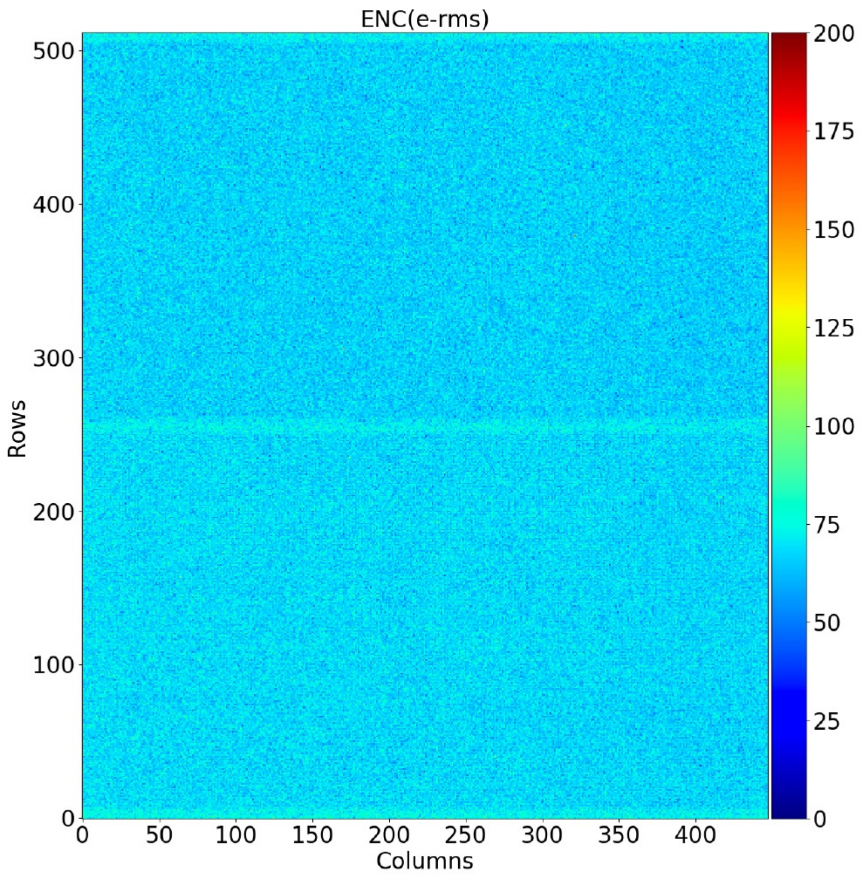
doable

Timepix4 noise

- Equivalent Noise Charge (ENC) for v0, v1 and v2





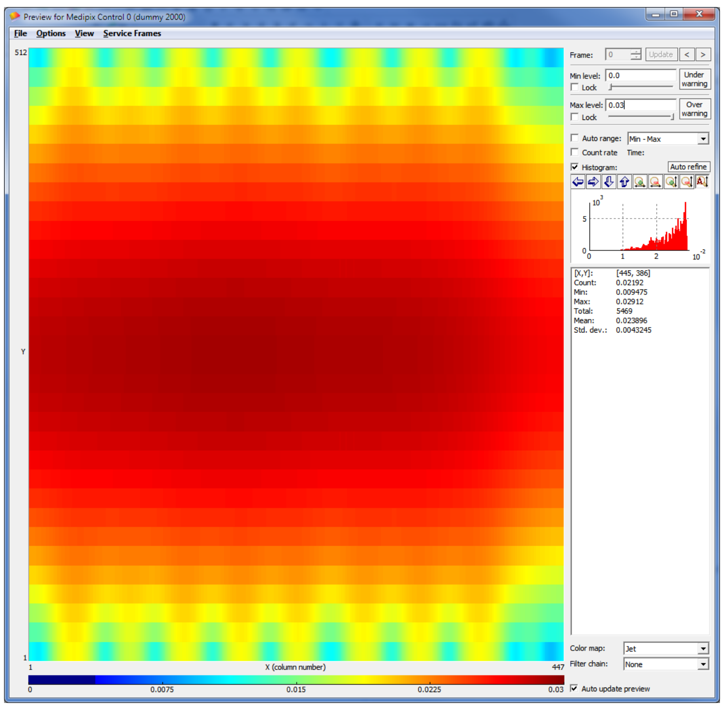


With a Si sensor the noise slightly increase ~3e⁻ / pixel

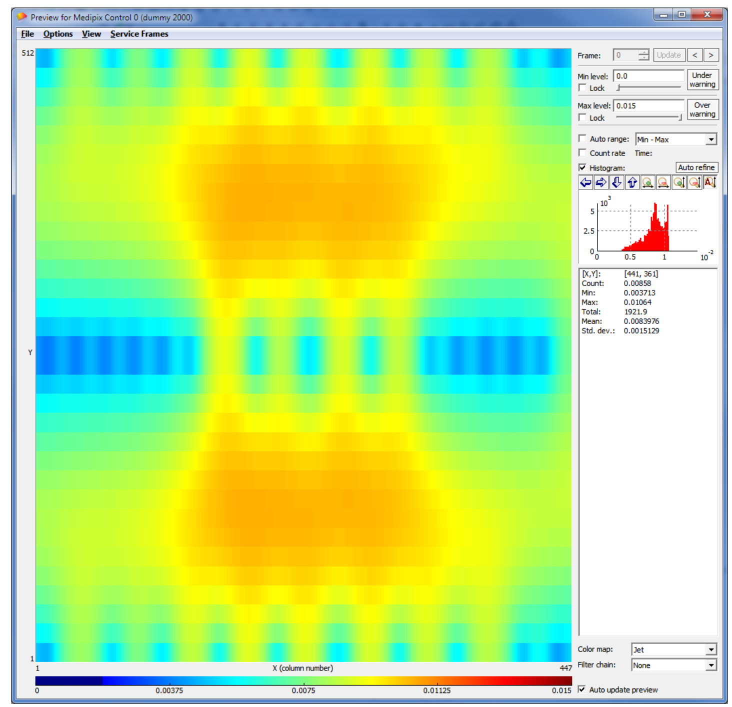
X. Llopart (CERN)

Analog (static) power supply distrib.

	Total I (chip)		2 WB	3 TSV
Nominal Analog Power [10 µA/pixel]	**~2300 mA**	V_{drop} [VDDA-GNDA]	**19.6 mV**	**6.9 mV**
		Imax pad	**60 mA**	**57 mA**
Low Analog Power [1 µA/pixel]	**~230 mA**	V_{drop} [VDDA-GNDA]	**1.96mV**	**0.69mV**
		Imax pad	**6 mA**	**5.7 mA**



2 WireBonds

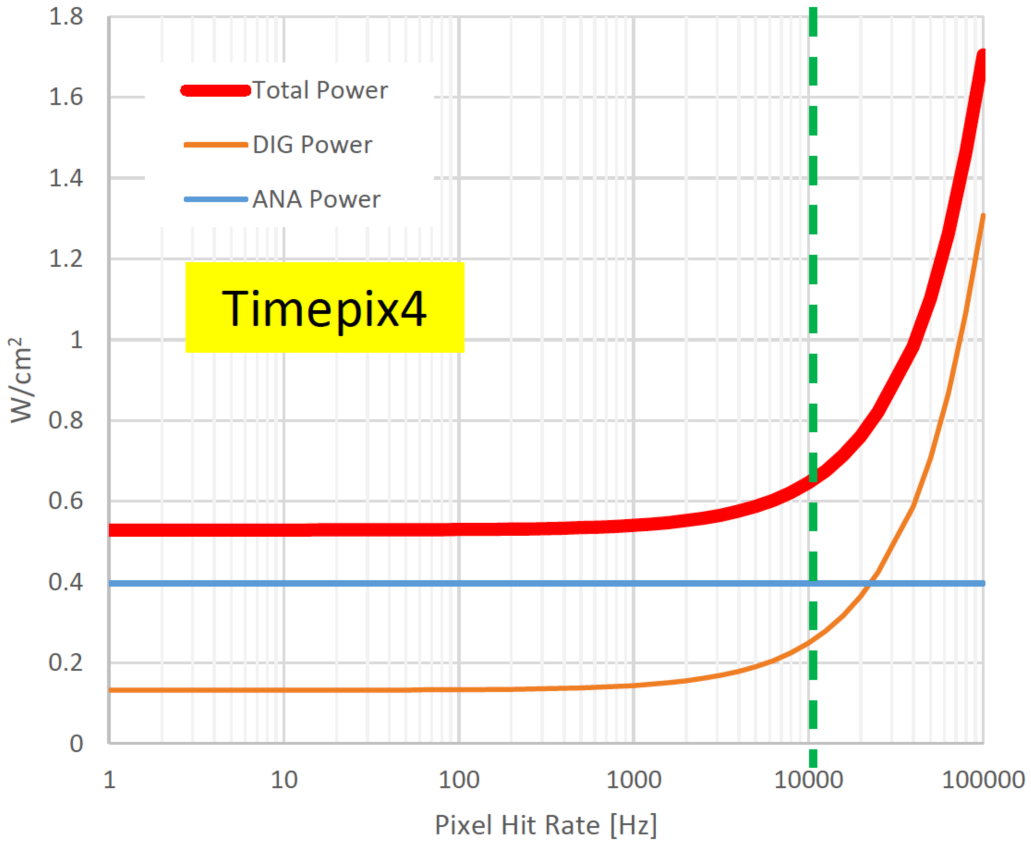


3 TSV

X. Llopart (CERN)

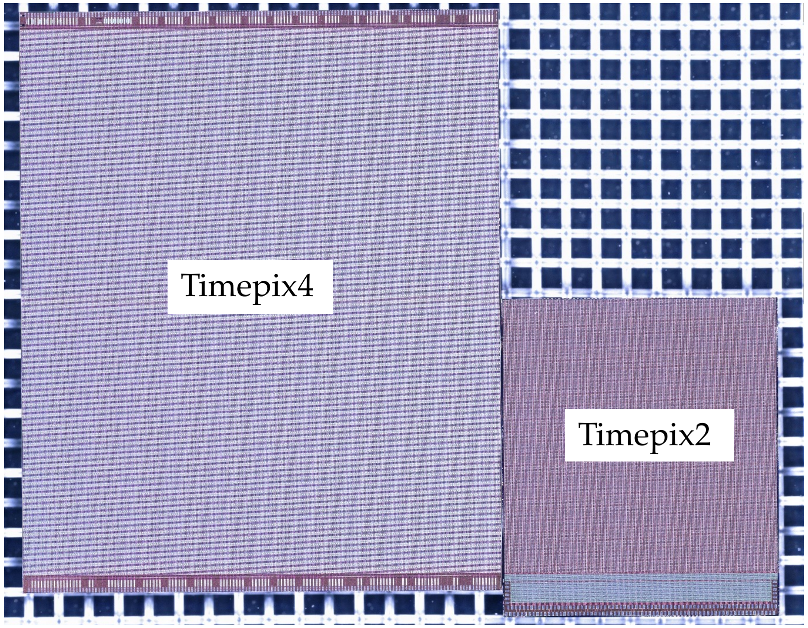
Digital (dinamic) power consuption

- Timepix4 power consumption (~5 W)
- Goal: stable operation with 20 °C inside the vacuum tube
  - Cold "finger" in thermal contact to ceramic carrier

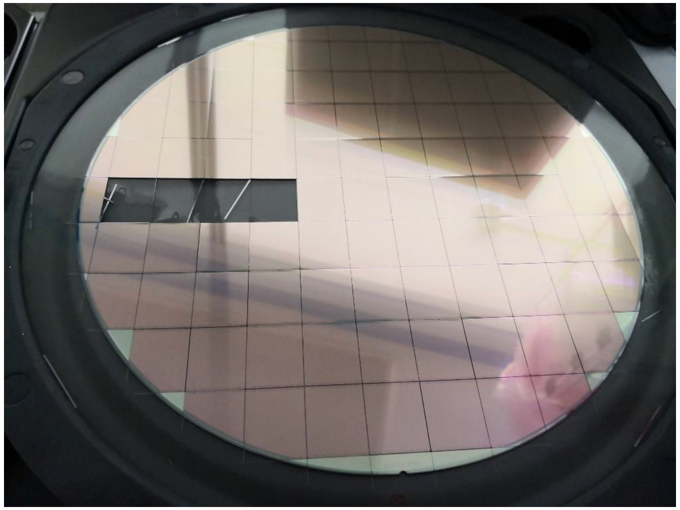


X. Llopart (CERN)

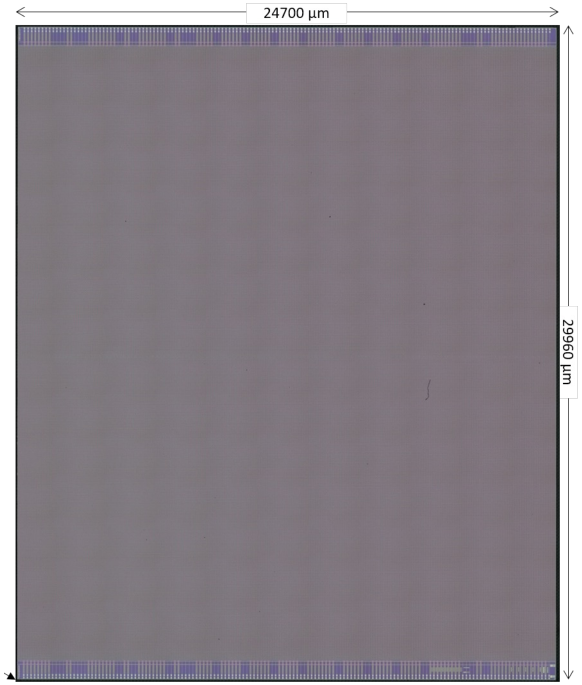
Timepix4 ASIC versions



- 65 nm CMOS (TSMC)
- ASIC productions:
  - Timepix4_v0 (Q1 2020)
  - Timepix4_v1 (Q4 2020)
  - Timepix4_v2 (Q4 2021)
  - Timepix4_v3 (Q1 2023)



Courtesy: J. Alozy, X. Llopart (CERN)



Timepix4 submissions

Q4 2019

Timepix4v0

Full mask engineering run

6 wafers received

Chip is operational

1) Excess noise coupling from peripheries to FE
2) 640 MHz clock in edge peripheries
3) VCO not oscillating at nominal frequency

Q3 2020

Timepix4v1

4 BEOL masks changed

Small test VCO chip

6 wafers received

1) Improved RDL shielding in peripheries
2) 640MHz in peripheries recovered

1) VCO not oscillating at nominal frequency

Q2 2021

Timepix4v2

4 FEOL + 4 BEOL masks changed

19 wafers received

1) TDC and High speed links working as expected
2) Further improvement in RDL shielding in peripheries

Chip at its final version

Q3 2022

Timepix4v3

2 BEOL masks changed

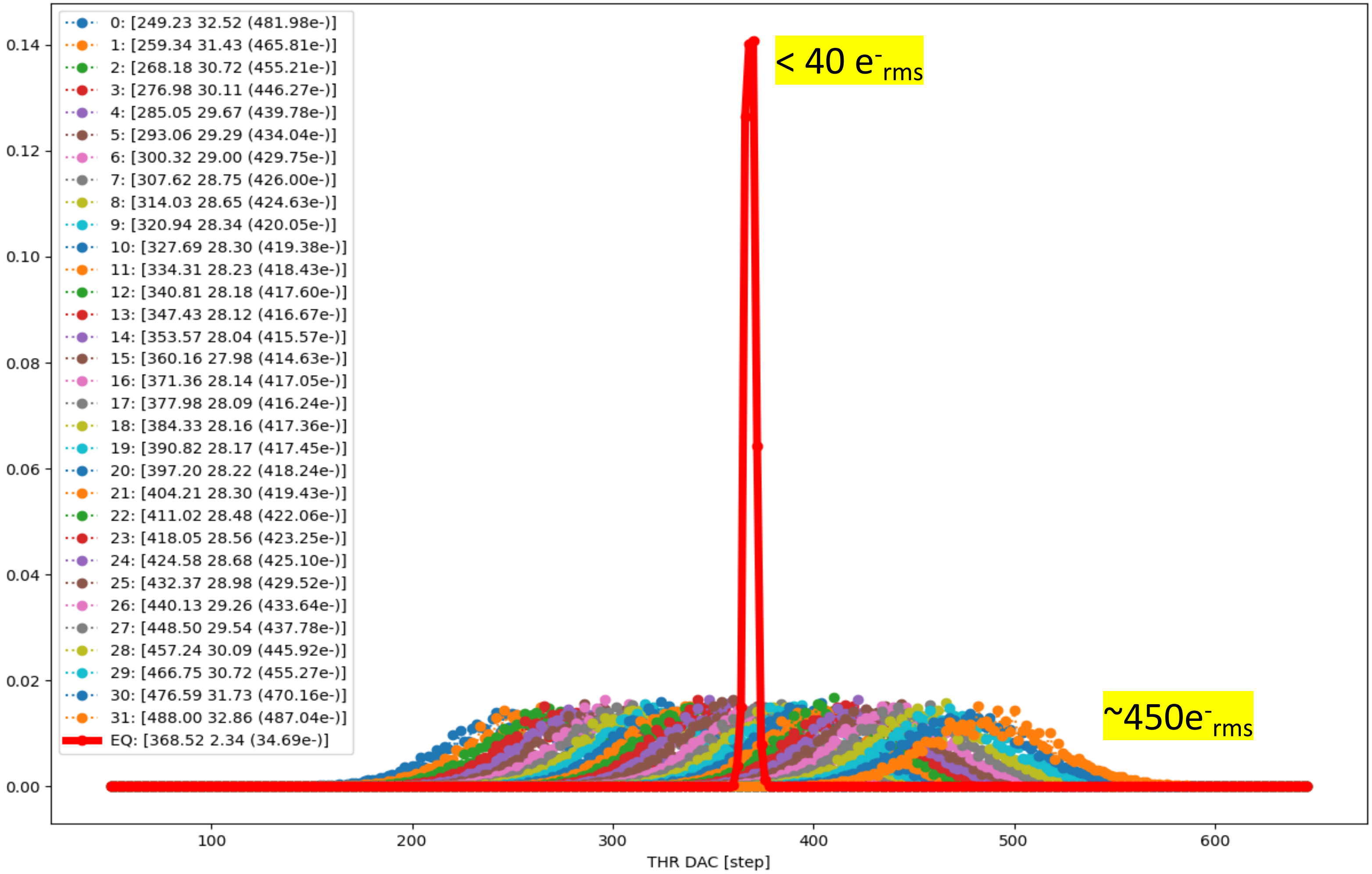
25 wafers received

1) Larger IO Pads

Chip at its final version

X. Llopart (CERN)

Timepix4 equalization

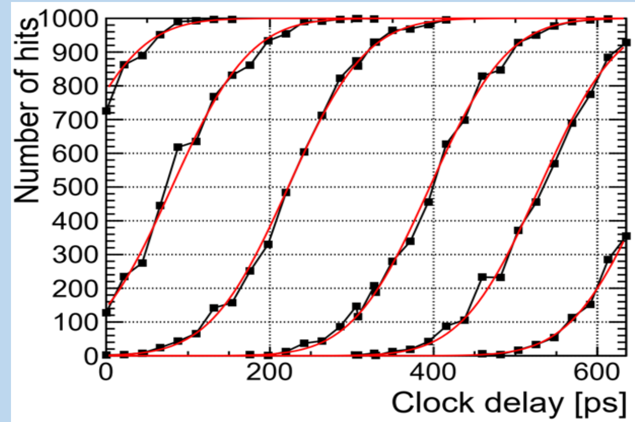


X. Llopart (CERN)

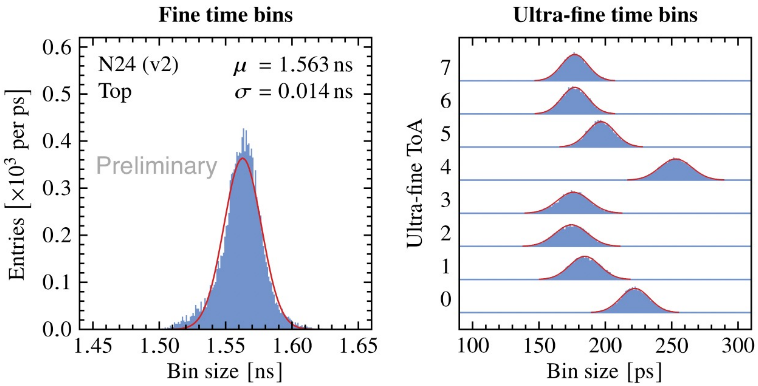
Timing with test pulse measurements

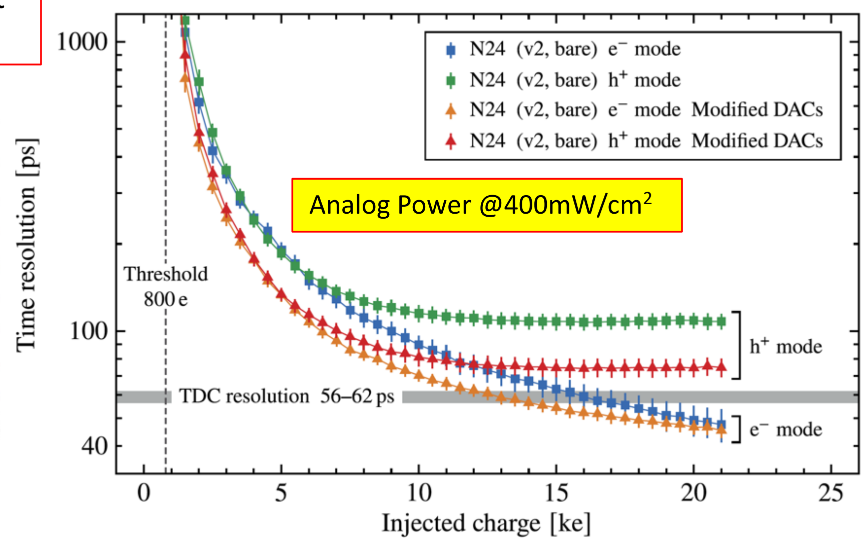
- Timepix4v2
- Using DDLL in bypass mode:
  - Controlled delay step of ~5.1ps
- Test on first 4 rows of pixels of both edges
- Allows for precise UFTOA measurement

K. Heijhoff (Nikhef)



UFTOA bins shows a small non uniformity at bin 4 and 0





X. Llopart (CERN)