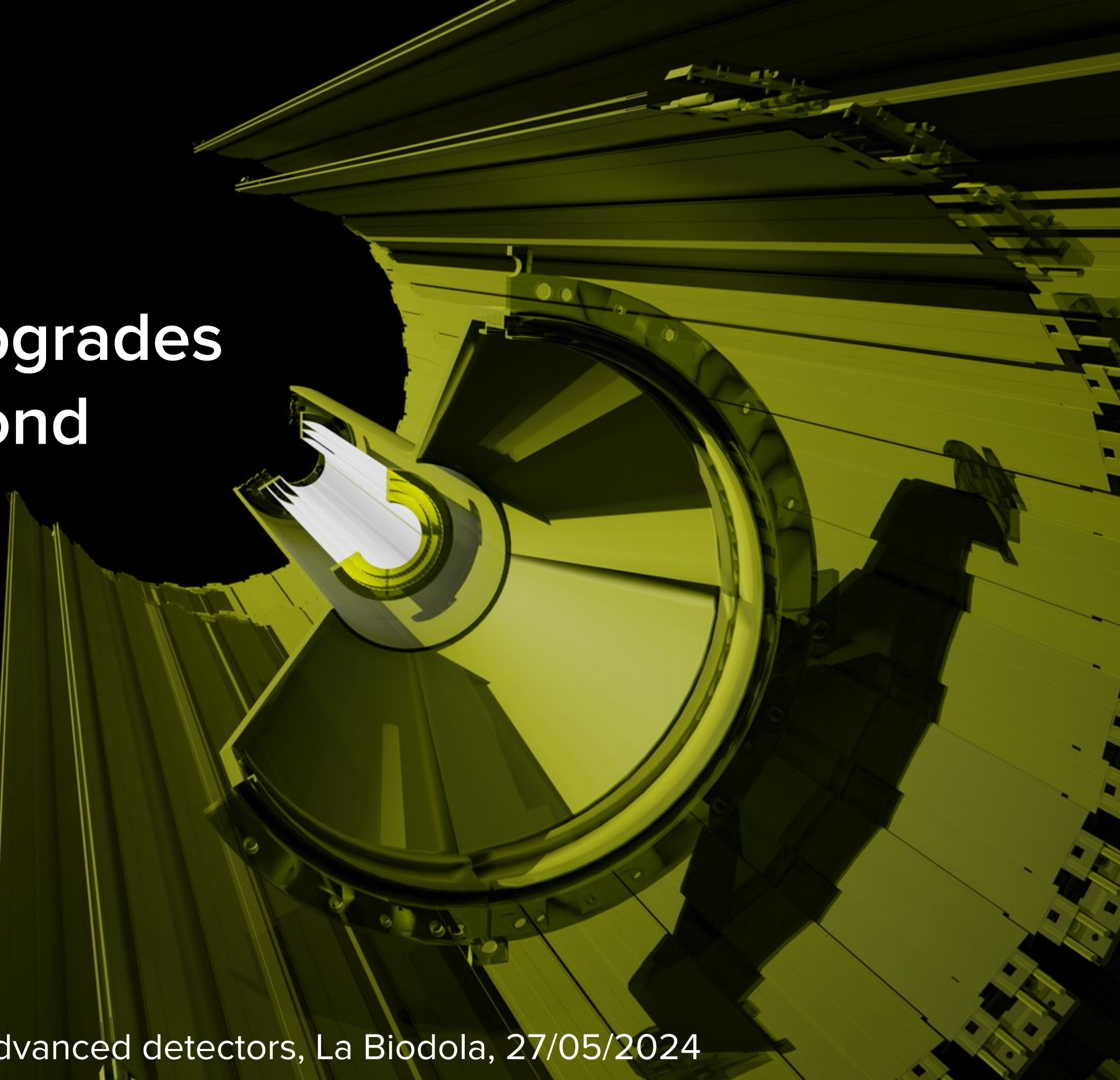
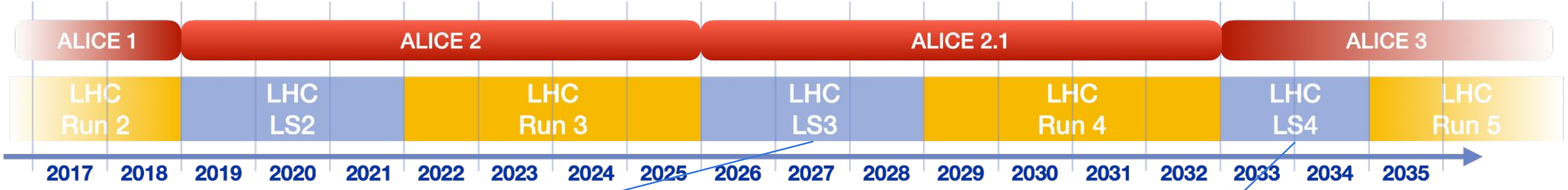
ALICE Silicon Tracker Upgrades for LHC RUN4 and Beyond



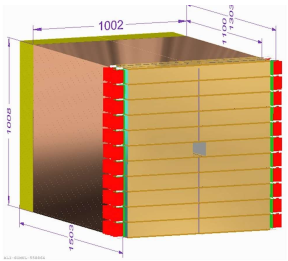
Luca Aglietta on behalf of the ALICE collaboration

16th Pisa Meeting on Advanced detectors, La Biodola, 27/05/2024

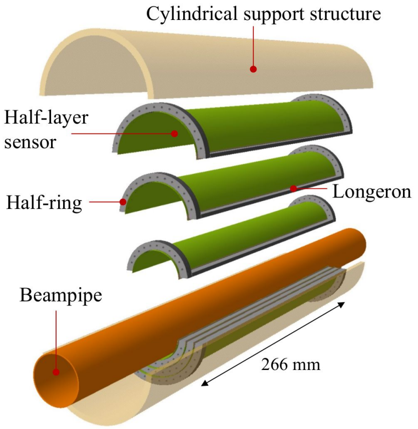
ALICE Upgrades timeline



ALICE 2.1



Forward Calorimeter
LOI: CERN-LHCC-2020-009
TDR: CERN-LHCC-2024-004
Not in this talk:
➔*See **M. Inaba** poster in Calorimetry session!*



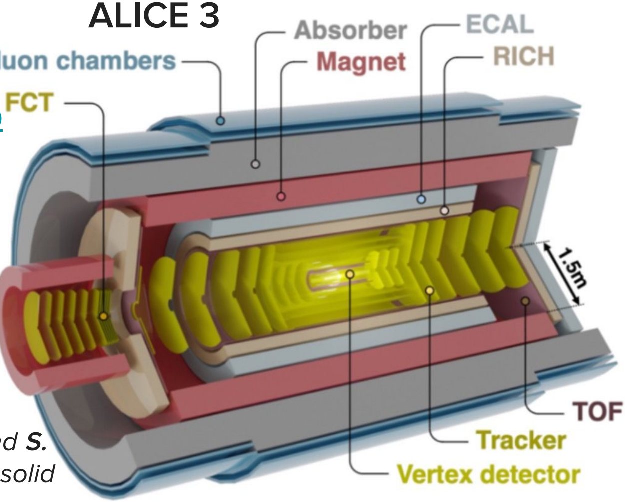
Inner Tracking System 3 (ITS3)
LOI: CERN-LHCC-2019-018
TDR: CERN-LHCC-2024-003

ALICE 3

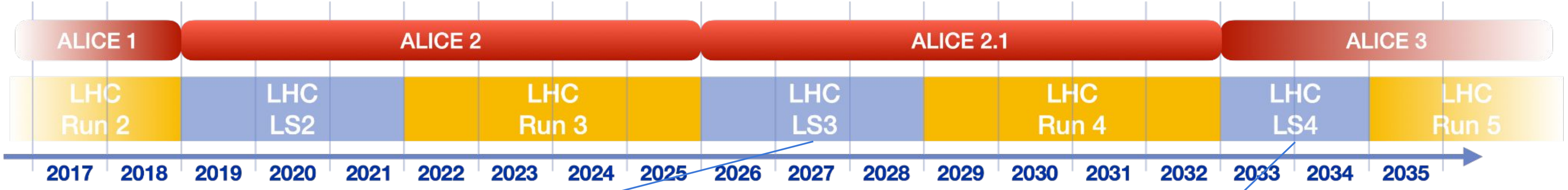
LOI: CERN-LHCC-2022-009
Scoping document in preparation

In this talk:
- Vertex Detector
- Outer Tracker

➔ *TOF: see **G. Gioachin** and **S. Strazzi** posters in PID and solid state detectors sessions!*



ALICE Upgrades timeline



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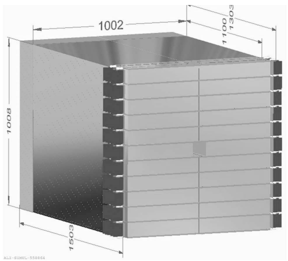

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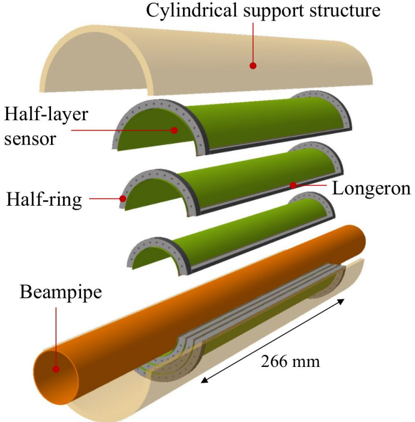

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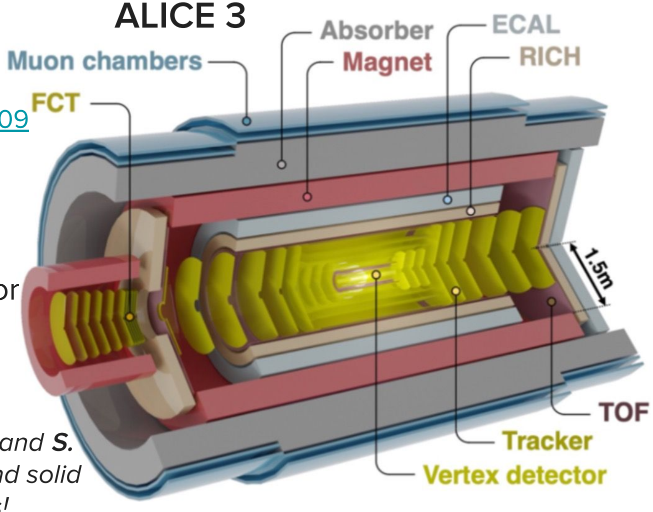


*➔ **TOF:** see **G. Gioachin** and **S. Strazzi** posters in PID and solid state detectors sessions!*

Upgrades motivations and requirements

Physics Motivations:

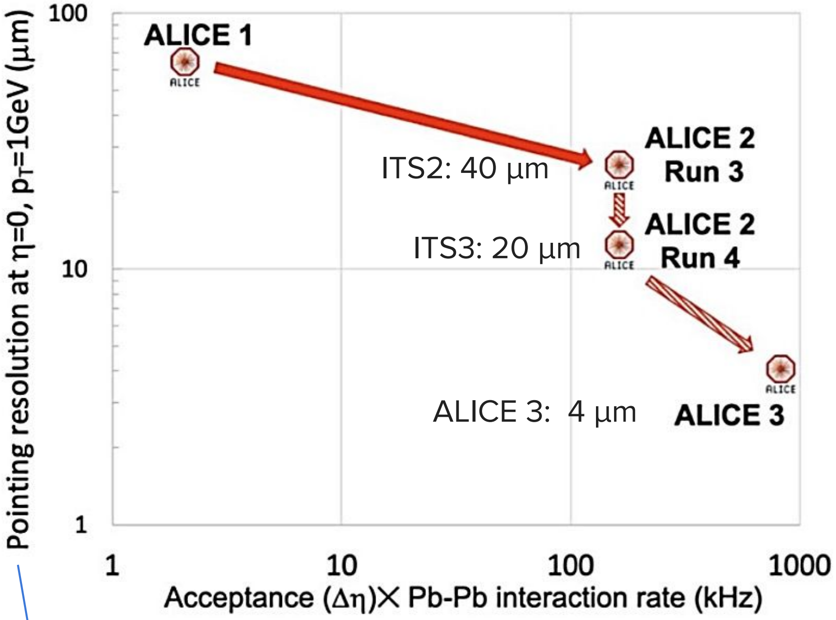
Study of QGP in ultra-relativistic heavy-ions collisions search for rare, low momentum probes, reconstruction of displaced decay topologies: →

- Heavy flavour hadrons at low p_T
- Thermal dileptons
- Precision measurements of light (hyper)nuclei and searches for charmed hypernuclei

Tracker upgrade requirements:

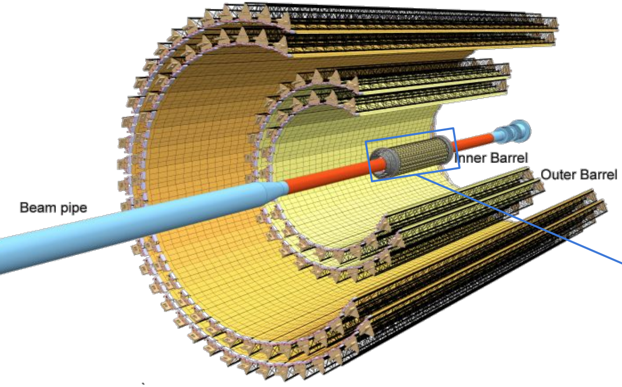
- Increase of effective acceptance (acceptance x readout rate)
- Improve tracking and vertexing performance low p_T for combinatorial background suppression

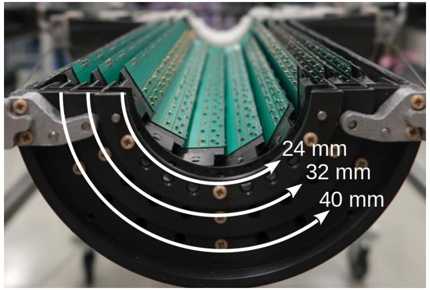
→ Excellent spatial resolution, minimal inner radius and low material budget are needed



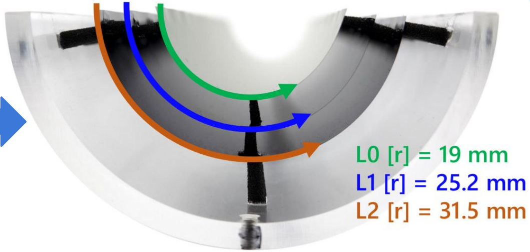
$$\sigma_{DCA} \approx A\,\sigma_{xyz} \oplus B\,\frac{r_0}{p}\sqrt{\frac{X}{X_0}}\cosh\eta$$

The ITS3 Upgrade

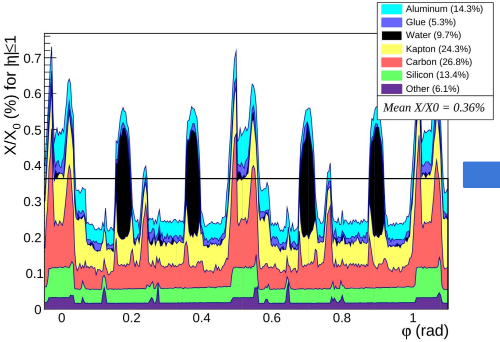


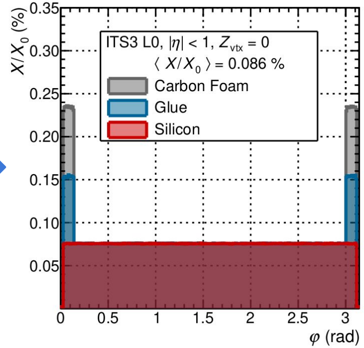


ITS2 Inner Barrel



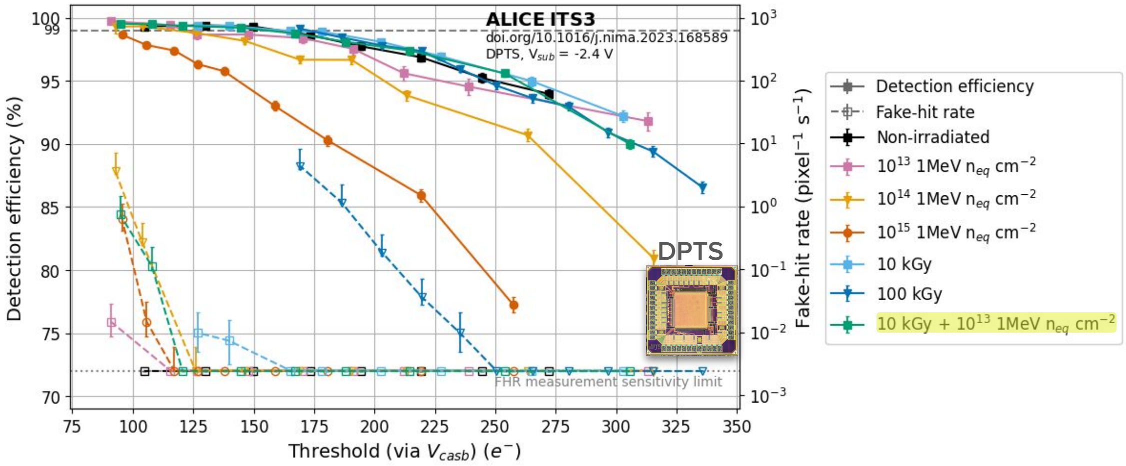
ITS3 Engineering Model 1

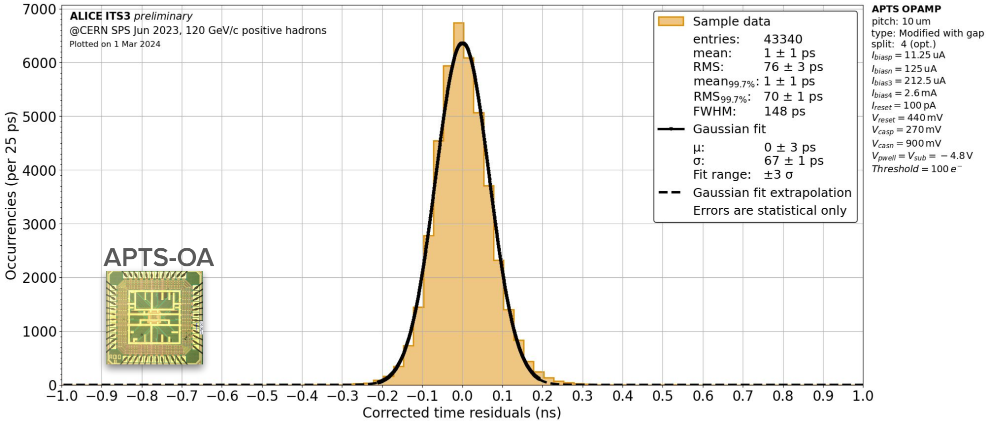




- Replacement of the Inner Barrel of the ITS2 with 3 layers of **curved, 50 μm thick, wafer-scale** MAPS in **65nm** CMOS process
- **Air cooling** and ultra-light mechanical supports (carbon foam)
- Reduction of L_0 radius:
  → from **24 mm** to **19 mm**
- Reduction of material budget per layer:
  → from **0.36%** X/X_0 to **0.09%** X/X_0

Technology qualification: MLR1





Digital Pixel Test Structure (DPTS):

- Efficiency > 99% and FHR < $2 \cdot 10^{-3}$ $pix^{-1}s^{-1}$ after irradiation at ITS3 requirements

j.nima.2023.168589

Analog Pixel Test Structure (APTS-SF):

- Efficiency maintained until 10^{15} 1MeV n_{eq} cm^{-2} at 15°C

arXiv:2403.08952

Analog Pixel Test Structure (APTS-OA):

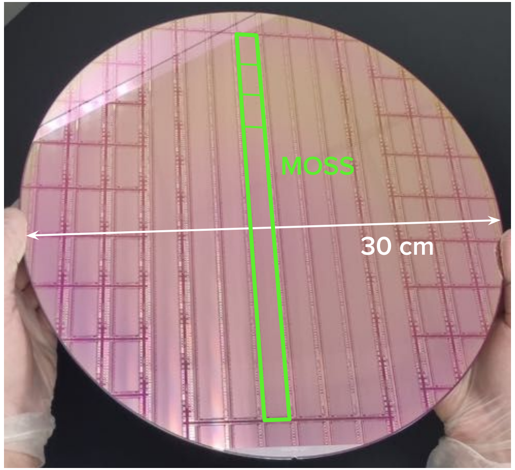
- Sensor time resolution ≤ 70ps

→ *More details?*
*See **K. Gautam (APTS)** and **A. Villani (DPTS)** posters in Solid State detectors session!*

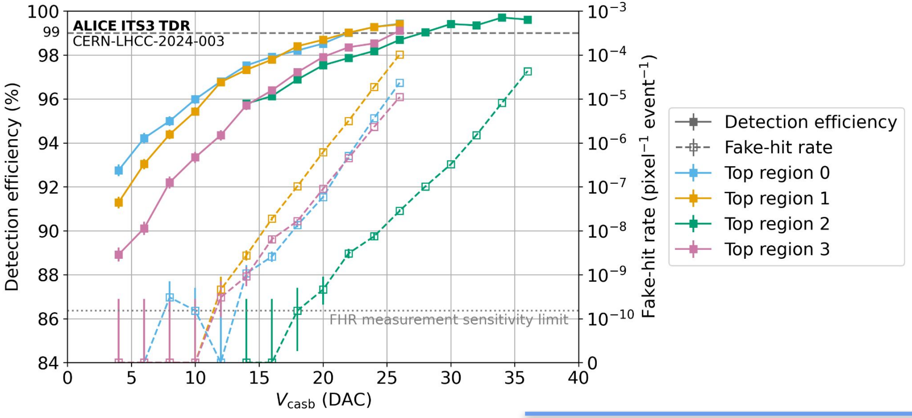
Stitched MAPS: ER1

Wafer	Row	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
Wafer 17	1-TOP	LIMIT	OK - I	OK - I	LIMIT	LIMIT	LIMIT	LIMIT	OK - I	OK - I	OK - I
	1-BOT	OK - II	OK - II	OK - II	OK - II	LIMIT	LIMIT	LIMIT	OK - II	OK - I	OK - II
	2-TOP	mechanically broken									
	2-BOT										
	3-TOP	OK - II	OK - II	OK - II	OK - II	LIMIT	LIMIT	LIMIT	OK - II	OK - I	OK - I
	3-BOT	LIMIT	OK - I	OK - II	LIMIT	LIMIT	LIMIT	LIMIT	LIMIT	OK - II	LIMIT
	4-TOP	OK - I	OK - I	OK - I	LIMIT	LIMIT	LIMIT	LIMIT	OK - I	OK - II	OK - I
	4-BOT	OK - I	LIMIT	OK - I	LIMIT	LIMIT	LIMIT	LIMIT	OK - I	OK - II	LIMIT
	5-TOP	OK - I	LIMIT	OK - I	LIMIT	OK - II	LIMIT	LIMIT	LIMIT	OK - II	OK - I
	5-BOT	OK - II	OK - I	OK - II	LIMIT	LIMIT	OK - II	LIMIT	OK - I	OK - I	LIMIT
	6-TOP	OK - I	LIMIT	OK - II	OK - II	LIMIT	LIMIT	LIMIT	LIMIT	OK - I	OK - I
	6-BOT	OK - II	OK - II	OK - I	OK - II	OK - II	LIMIT	LIMIT	OK - II	OK - II	OK - II
Wafer 23	1-TOP	OK - II	OK - I	OK - II	LIMIT	OK - II	OK - II	OK - I	LIMIT	OK - II	OK - II
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - II	LIMIT	OK - II	OK - I	OK - II	OK - II
	2-TOP	OK - II	OK - I	LIMIT	LIMIT	LIMIT	OK - II	OK - II	OK - II	OK - II	OK - II
	2-BOT	OK - II	OK - II	OK - II	OK - II	OK - I	LIMIT	OK - II	OK - I	OK - II	OK - I
	3-TOP	OK - II	OK - I	LIMIT	LIMIT	LIMIT	LIMIT	LIMIT	OK - I	OK - II	LIMIT
	3-BOT	OK - II	OK - I	OK - I	OK - II	OK - II	LIMIT	OK - II	OK - I	LIMIT	OK - II
	4-TOP	OK - II	LIMIT	LIMIT	LIMIT	OK - I	OK - II	OK - II	OK - II	OK - I	OK - I
	4-BOT	OK - II	OK - I	OK - II	OK - II	OK - I	OK - II	LIMIT	LIMIT	OK - I	OK - II
	5-TOP	OK - I	OK - II	OK - II	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	5-BOT	LIMIT	OK - II	LIMIT	OK - I	LIMIT	LIMIT	OK - II	OK - II	OK - I	OK - II
	6-TOP	OK - I	OK - I	OK - I	OK - II	LIMIT	OK - I	OK - II	OK - II	OK - II	OK - I
	6-BOT	OK - I	OK - I	OK - I	OK - II	OK - II	LIMIT	OK - II	OK - I	LIMIT	OK - I
Wafer 24	1-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	2-TOP	OK - II	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - I	OK - II	OK - I
	2-BOT	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
	3-TOP	to be tested									
	3-BOT										
	4-TOP	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - I
	5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
	5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-TOP	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I

Powering Yield

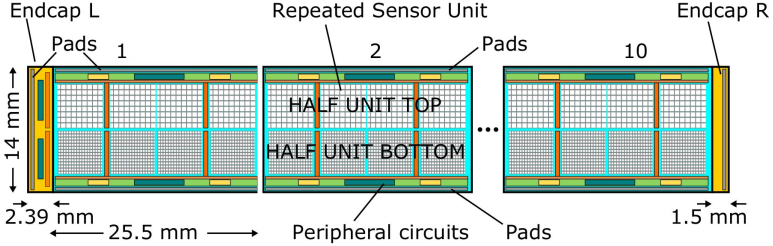


ER1 wafer

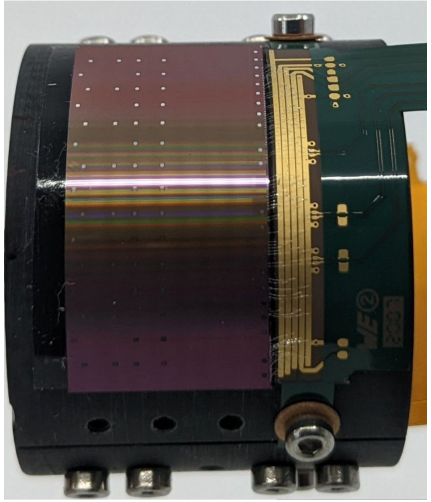


MOnolithic Stitched Sensor (MOSS):

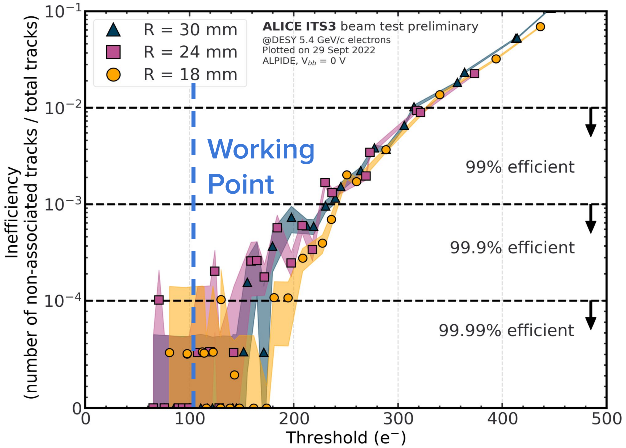
- 10 Repeated Sensor Units stitched together: 259 mm x 14 mm per sensor
- 2 pixel pitches (18 µm and 22.5 µm) and 5 front-end variants
- Chip is **operational** and reaches **full efficiency**
- **Yield:** currently under study with extensive characterization campaign with wafer prober. Target < 2% dead pixels per layer

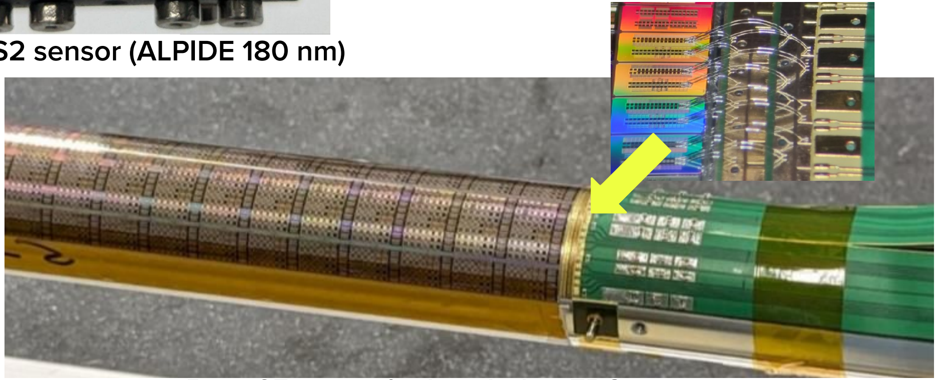


Performance of bent MAPS



Bent ITS2 sensor (ALPIDE 180 nm)



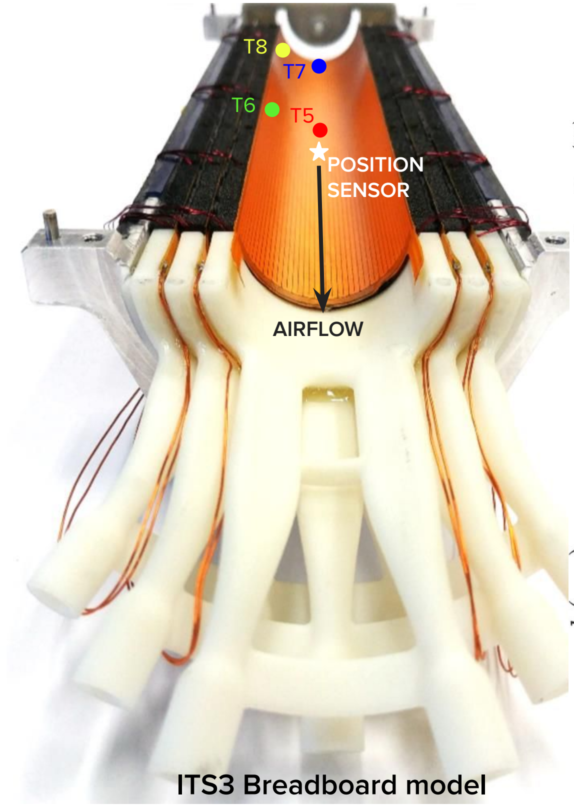


Bent 65 nm wafer bonded to FPC

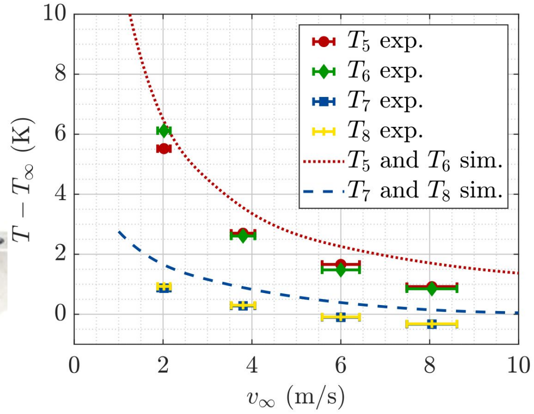
- 50 µm thick silicon sensors can be be bent to ITS3 target radius without breaking
- Test on bent ALPIDE chips show performance is unaffected → No efficiency loss
- Results validated on bent 65 nm pixel test structures
- Electrical interconnections to FPC after bending through wire bonding

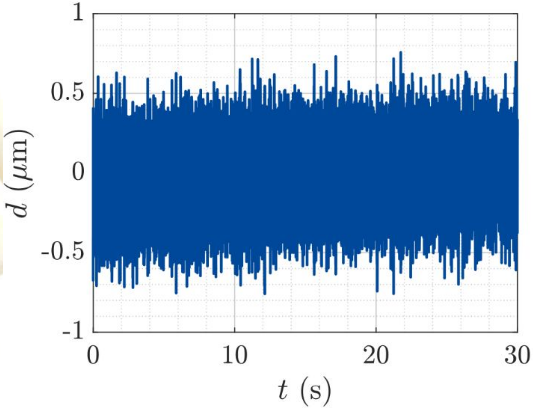
First results on bent MAPS: j.nima.2021.166280

Thermo-mechanical characteristization



ITS3 Breadboard model

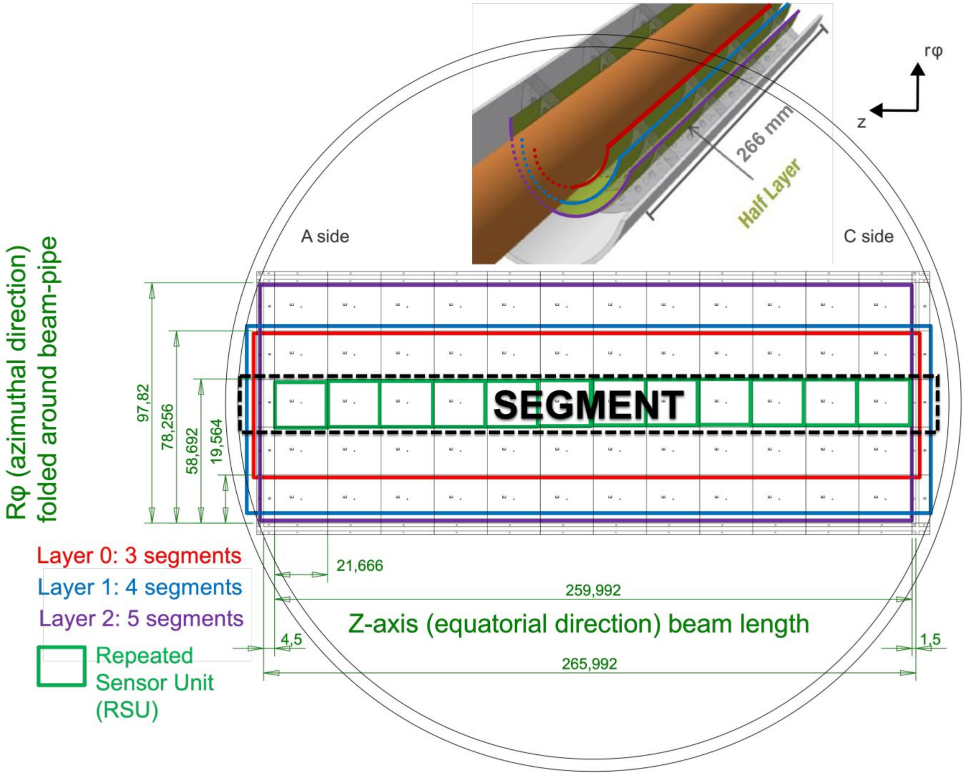




Baseline cooling solution ➔ **air cooling**.

- Tests in wind tunnel on breadboard model: dummy silicon sensor with copper serpentine heater
- Temperature differences in the sensor below 5°C with of 8 m/s airflow. (Thermal load: 25 mW cm^{-2} in matrix, 1000 mW cm^{-2} in end-caps)
- Mechanical assembly with carbon foam half rings keeps vibrations within ± 0.5 µm with 8 m/s airflow

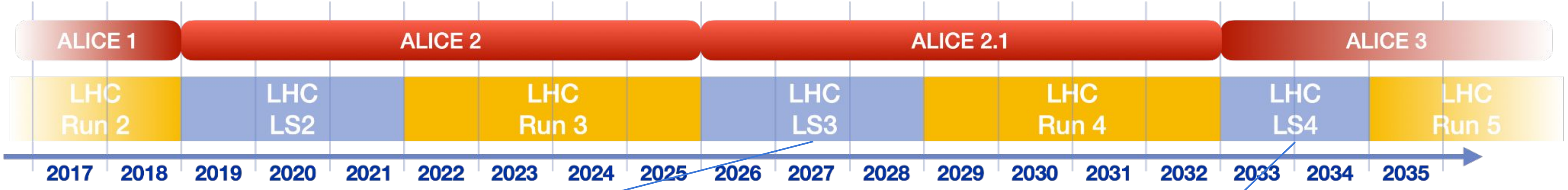
ITS3 Final Sensor Design: ER2 submission



Design of **full-size** and **full-functionality** prototypes of the final sensor is being finalised incorporating learnings from MOSS testing:

- **Modular design**: each sensor is divided into 3, 4, or 5 segments with 12 RSUs.
- Each RSU is divided in turn in 12 fully independent tiles (powering, control and readout)
- Left end cap acts as a separate readout circuit on the same silicon wafer ➔ interface with off detector electronics
- Submission to the foundry in fall 2024

ALICE Upgrades timeline



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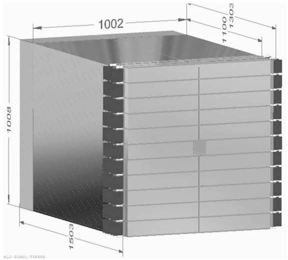

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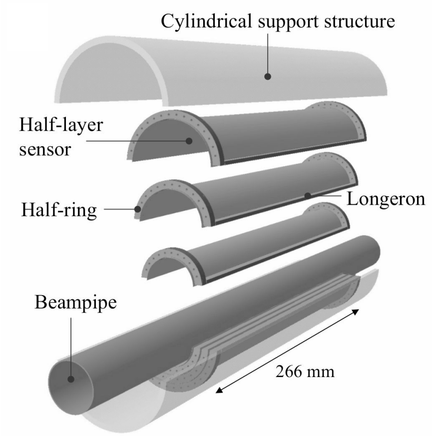

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ALICE 3

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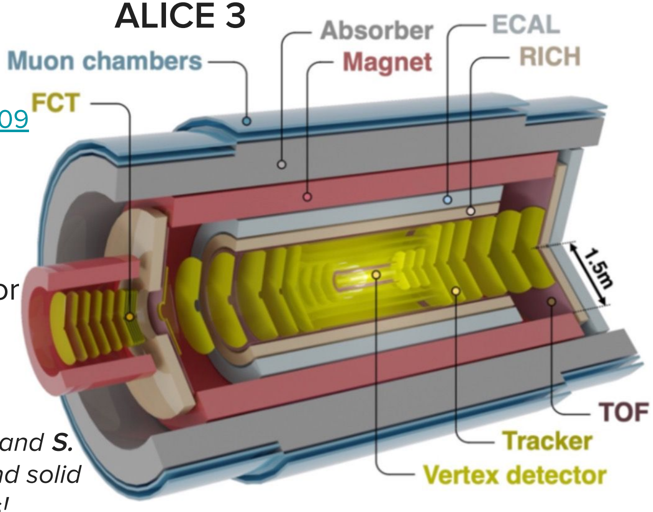

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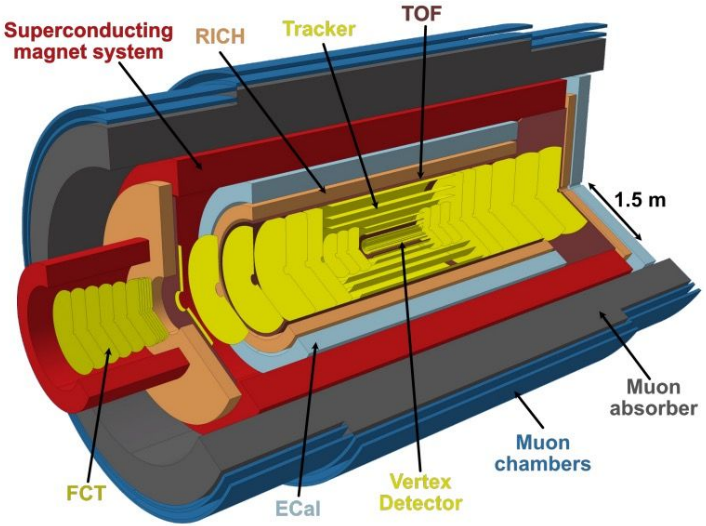
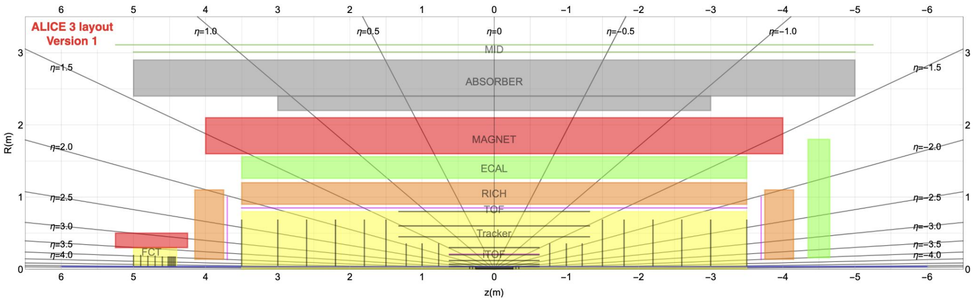
ALICE 3 (LS4: 2033-2034)



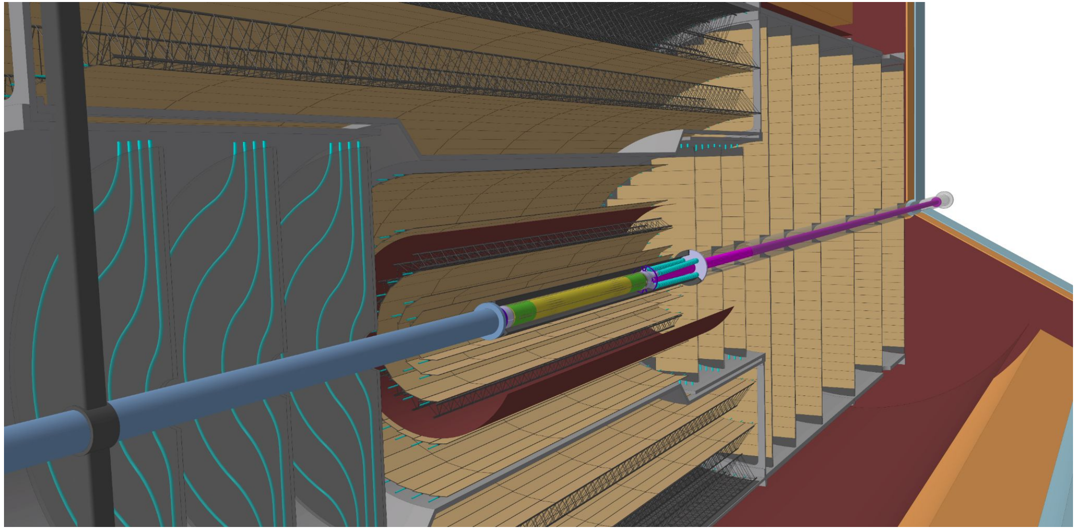


Next generation compact experiment based on advanced silicon detectors

- Centered around a $60m^2$ low-mass silicon tracker fully made of MAPS
- Retractable vertex detector for unprecedented pointing resolution
- Excellent PID capabilities thanks to TOF and RICH detectors
- Superconducting magnet (2T)
- Large acceptance: $-4 < \eta < 4$
- Continuous readout and online data processing to access rare signals
- Muon Identification system, large acceptance Ecal and Forward Conversion Tracker for ultra-soft photons

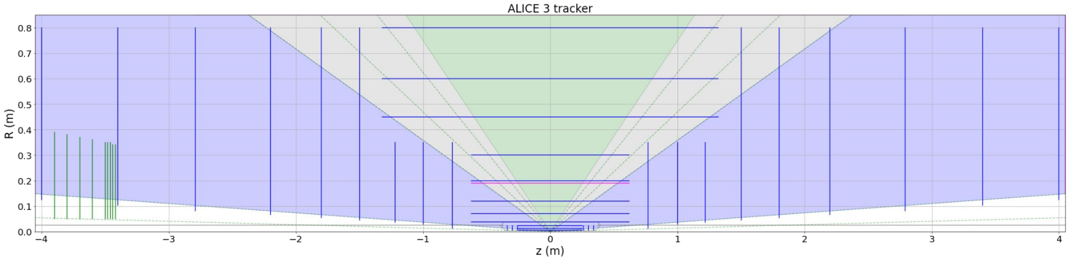
ALICE 3 Outer Tracker

- 8 barrel layers (3.5 cm < R < 80 cm) and 2 x 9 end-cap disks
- Material budget: 1% X/X_0 per layer
  ➔ **< 10%** $\boldsymbol{X/X_0}$ for entire tracker
- Space resolution: 10 µm ➔ 50 µm pixel pitch
- Low power consumption: **20 mW/cm^2**
- **100 ns** time resolution to mitigate pileup

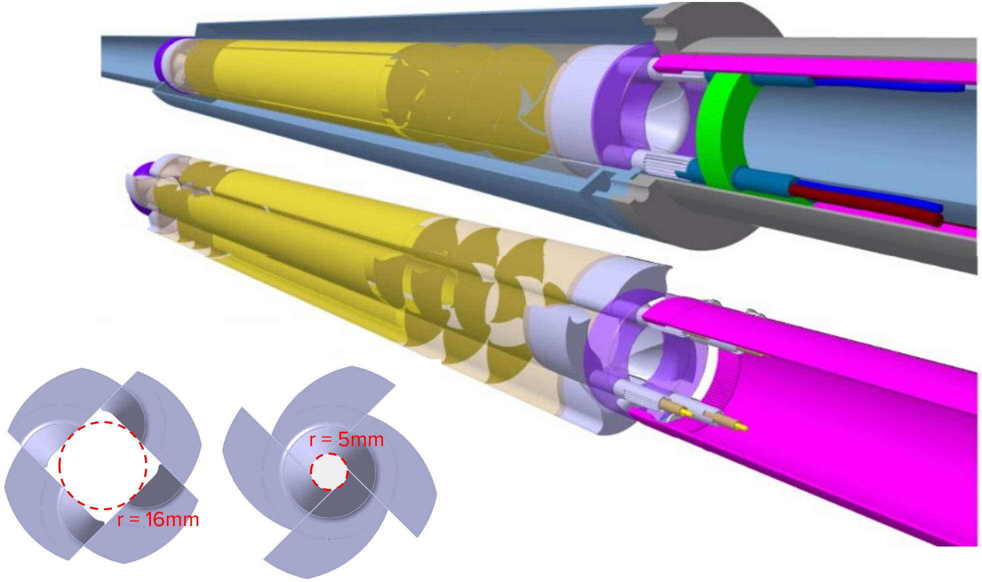


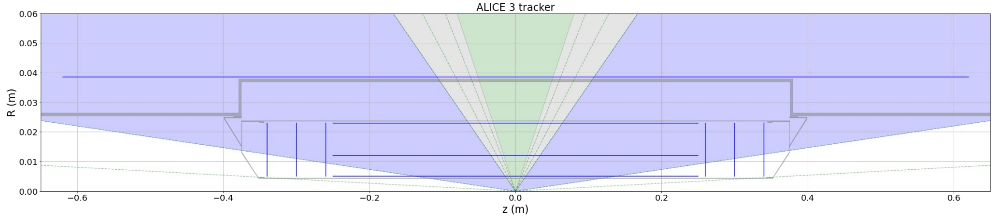
Main R&D challenges:

- Modules integration for mass industrialization
- Power consumption while preserving timing performance



ALICE 3 Vertex Detector





- 3 barrel layers and 2 x 3 end-cap disks of **ultra-thin, curved, wafer-scale MAPS**
- Retractable structure inside the beam pipe in secondary vacuum: **Iris Tracker**
- First detection layer at **5 mm** from the interaction point
- Unprecedented spatial resolution: **2.5 µm**
- Extremely low material budget: **0.1%** X/X_0
- Hit rate: **35 MHz cm^{-2}**

Main R&D challenges:

- Radiation hardness: **10^{16} 1MeV n_{eq} cm^{-2}** + **300 Mrad** (LOI values)
- Mechanics and cooling
- **10 µm** pixel pitch
- Data and power distribution

➜ R&D will build up on ITS3 experience

Summary and Outlook

ALICE ITS3 project is on track for being installed in LS3 :

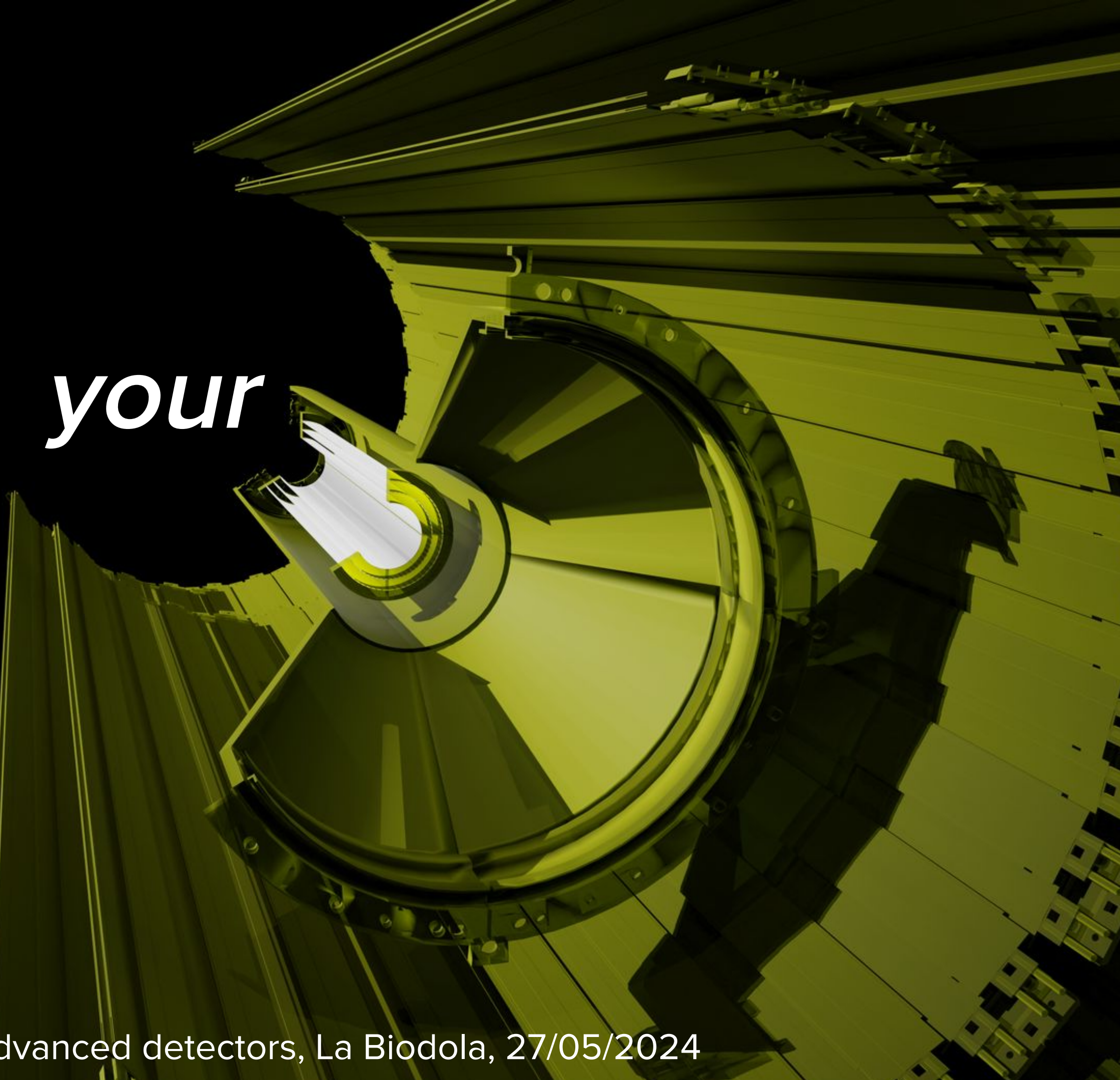
- bent MAPS performance demonstrated in beam
- 65 nm process qualified with MLR1 pixel structures
- stitched design exercised, testing is ongoing
- assembly procedure with curved wafer-scale sensors defined
- air cooling solution validated
- TDR reviewed by LHCC and approved by Research Board: CERN-LHCC-2024-003

ALICE 3, proposed for LHC run 5, will further push the limits of MAPS technology:

- LOI: CERN-LHCC-2022-009
- large-scale integration (60 m^2 outer tracker)
- increased spatial resolution, radiation hardness and rate capabilities + in-vacuum operation (vertex detector)
- Scoping document is being redacted: submission to the LHCC in fall 2024

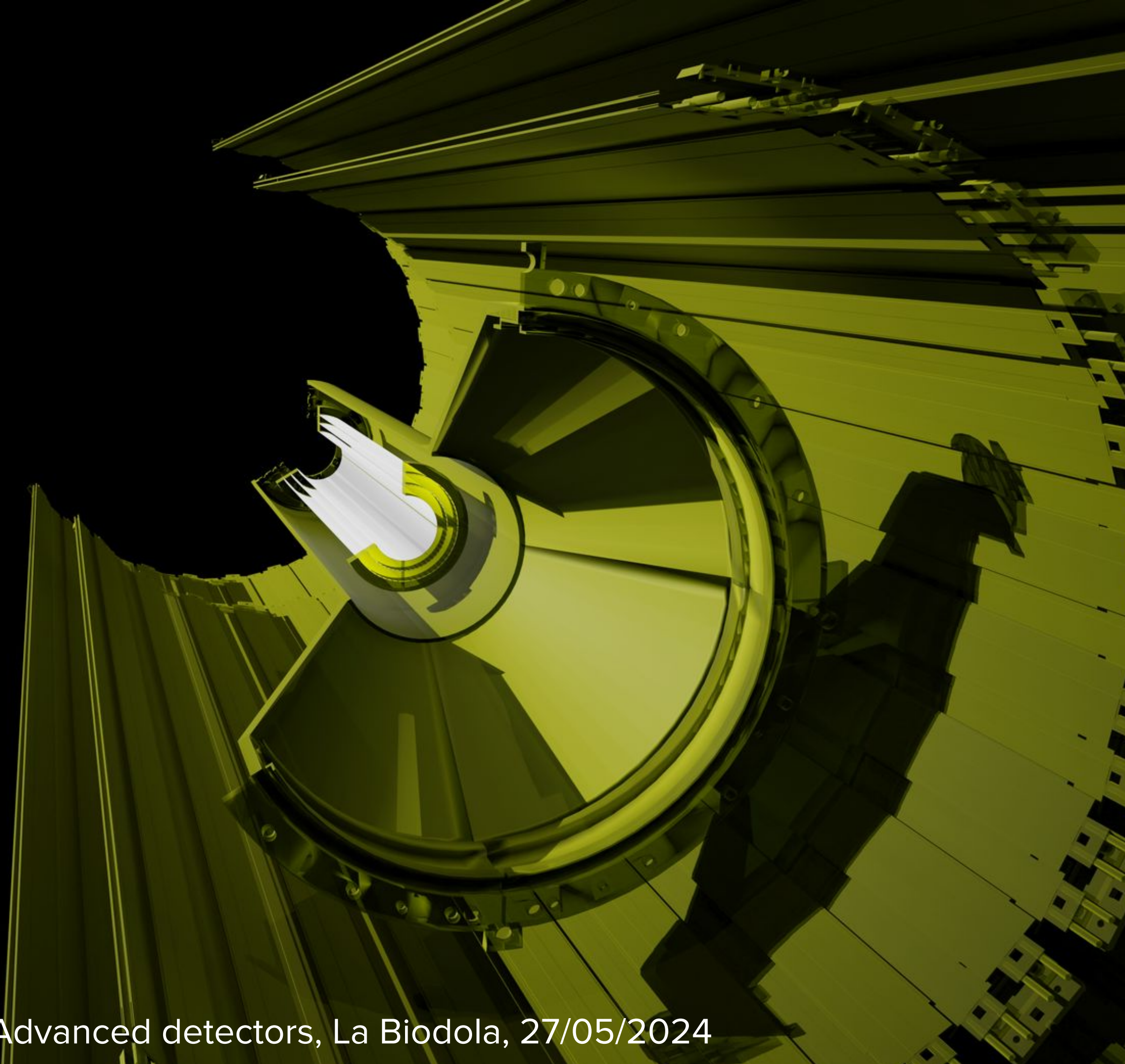
ITS3 Engineering Model 2

Thank you for your attention!

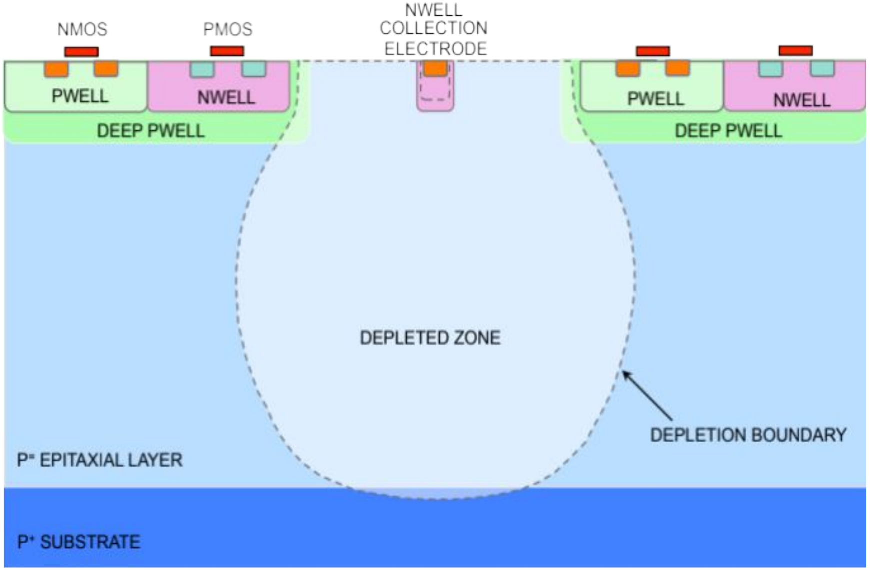


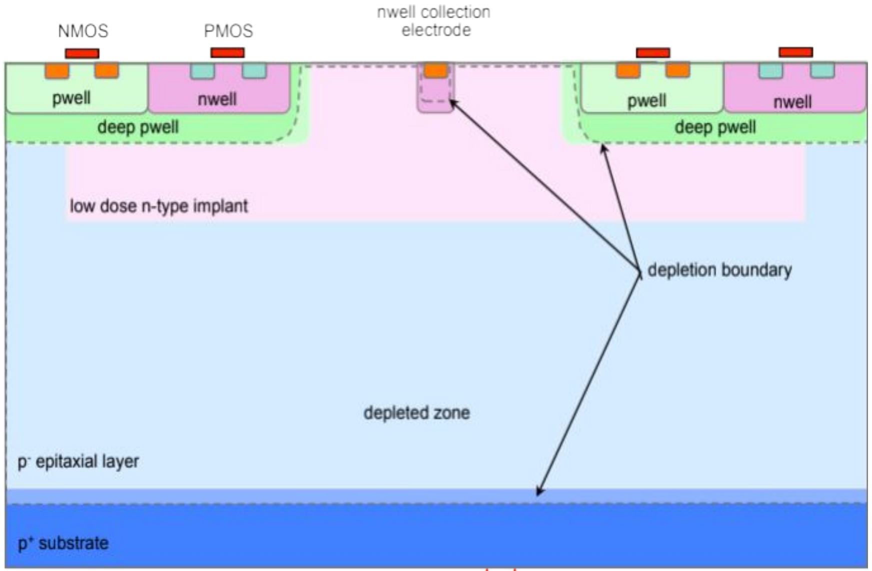
In the background: *Render of the full ITS3 geometry implemented in ALICE simulation and reconstruction software (O2)*

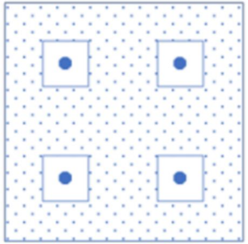
Backup



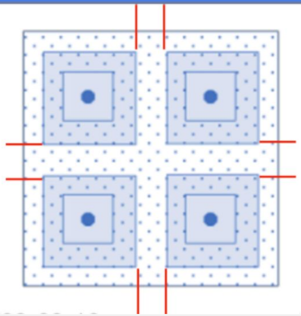
Modified MAPS production process



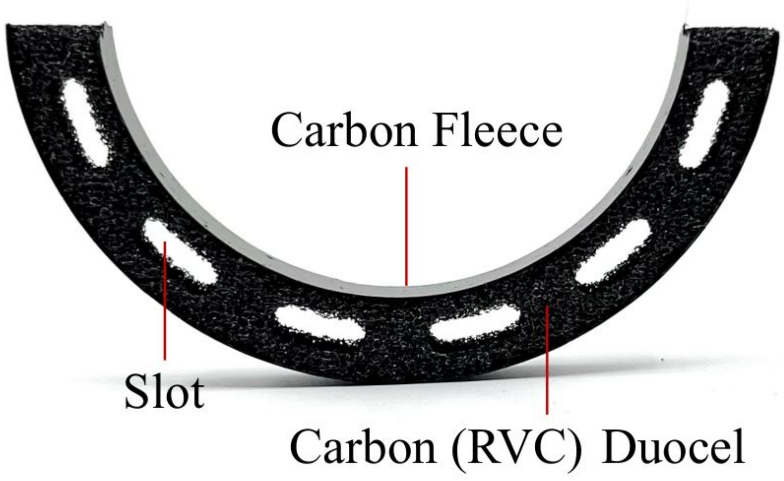


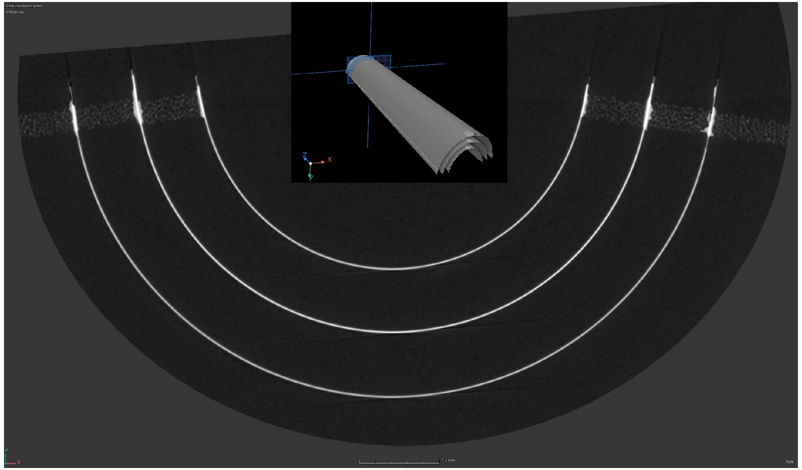


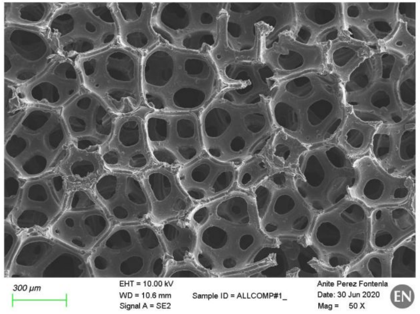
[Snoeys, W., et al. "Optimization of a 65 nm CMOS imaging process for monolithic CMOS sensors for high energy physics." *PIXEL 2022*.](#)



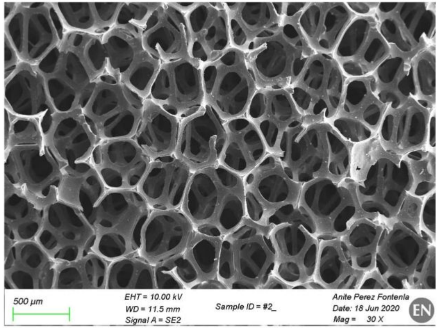
Ultra-light detector mechanics





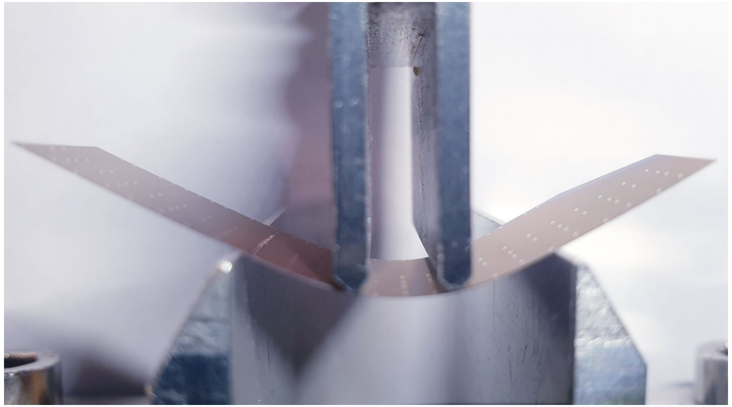


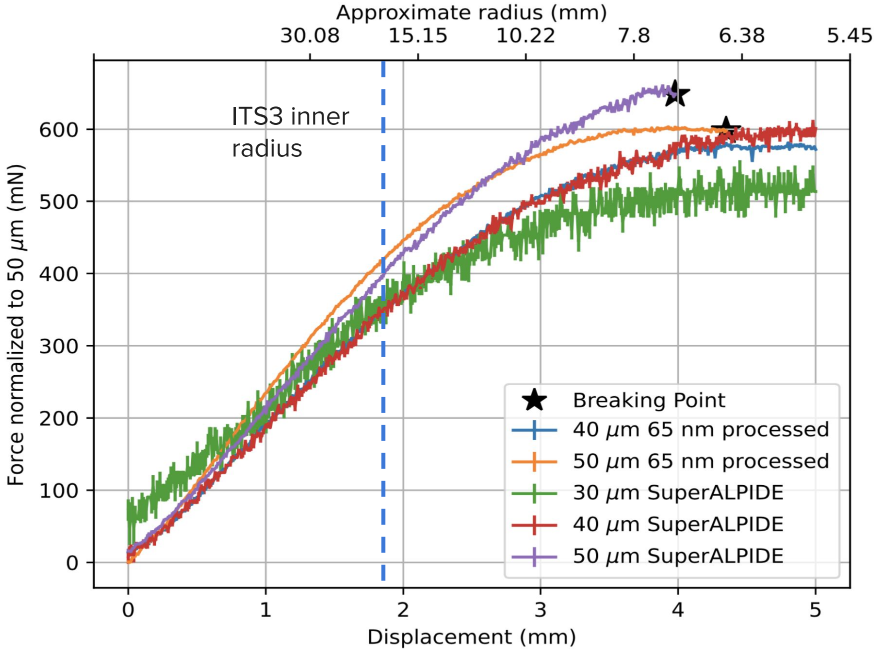
(b) Allcomp K9 standard density



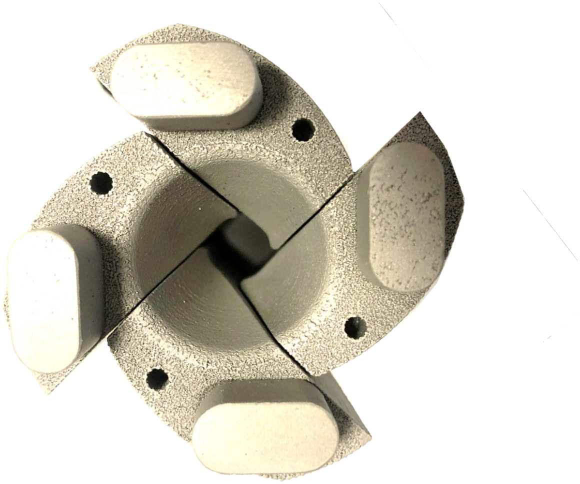
(a) Carbon (RVC) Duocel®

Bending Force

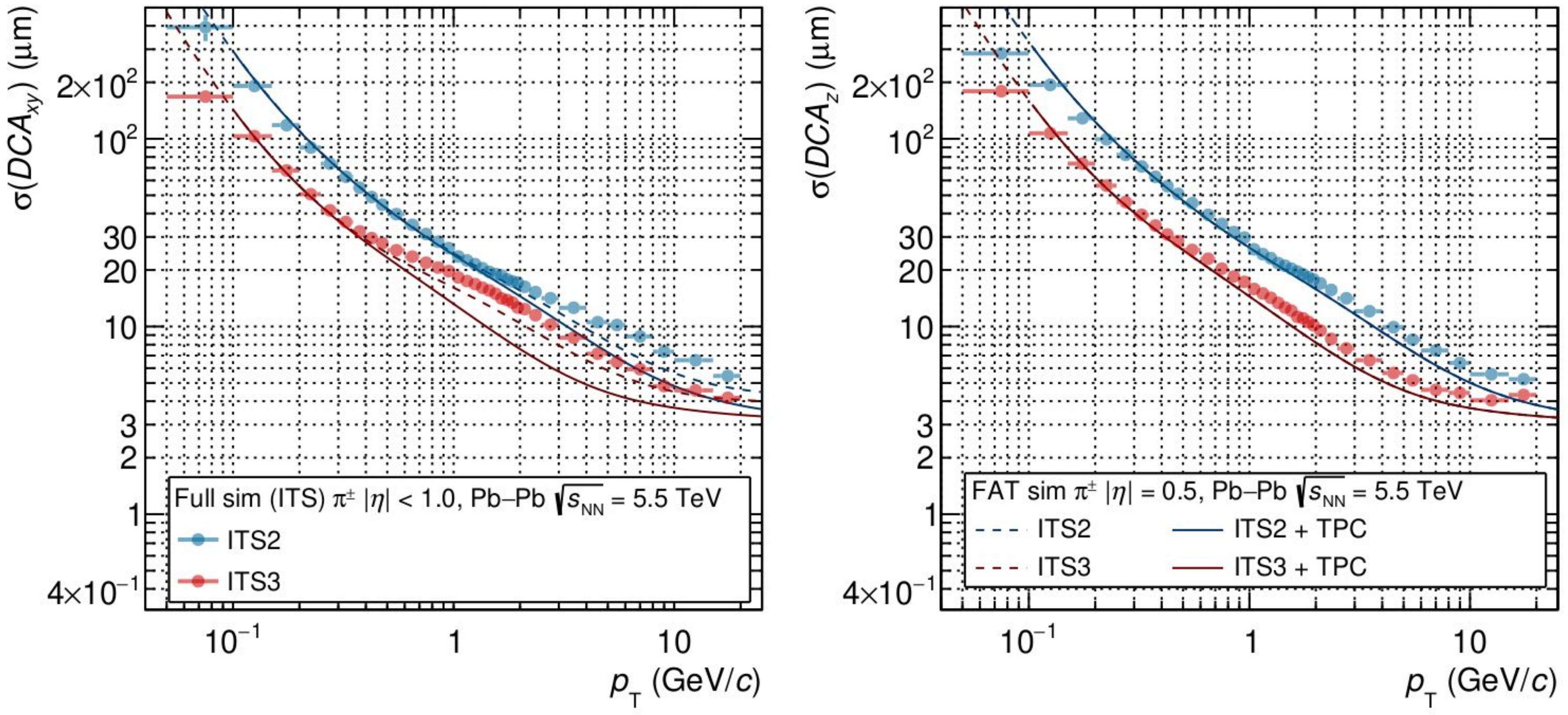




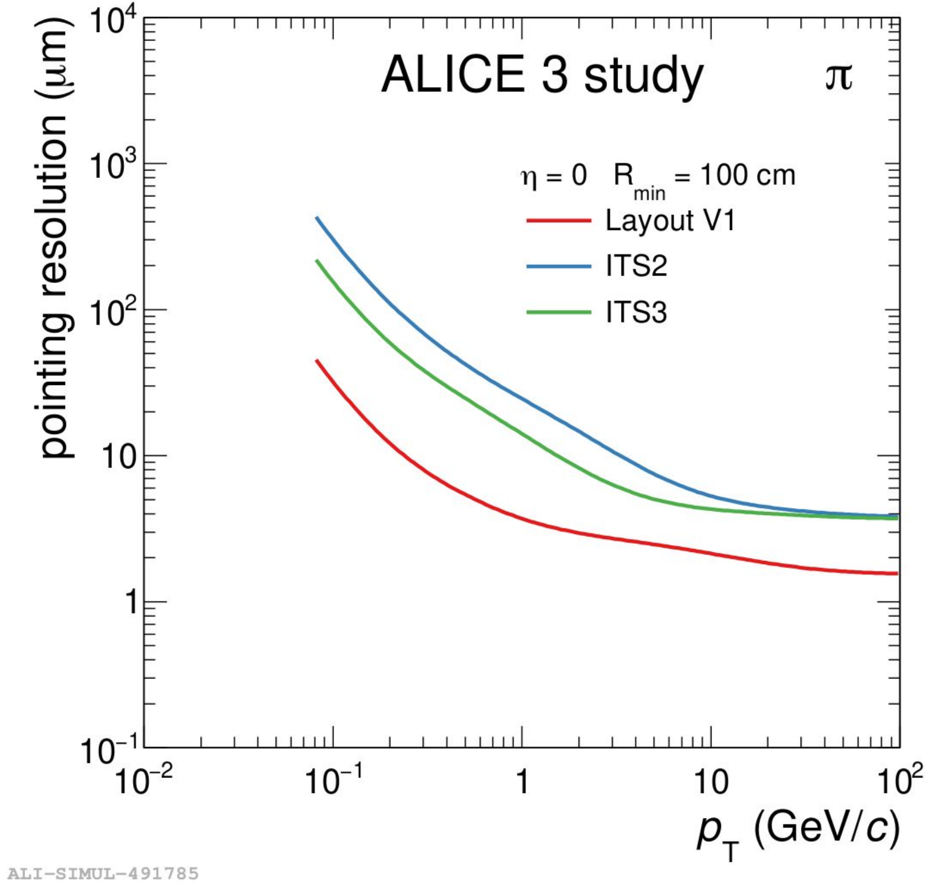
Iris Bread Board Model

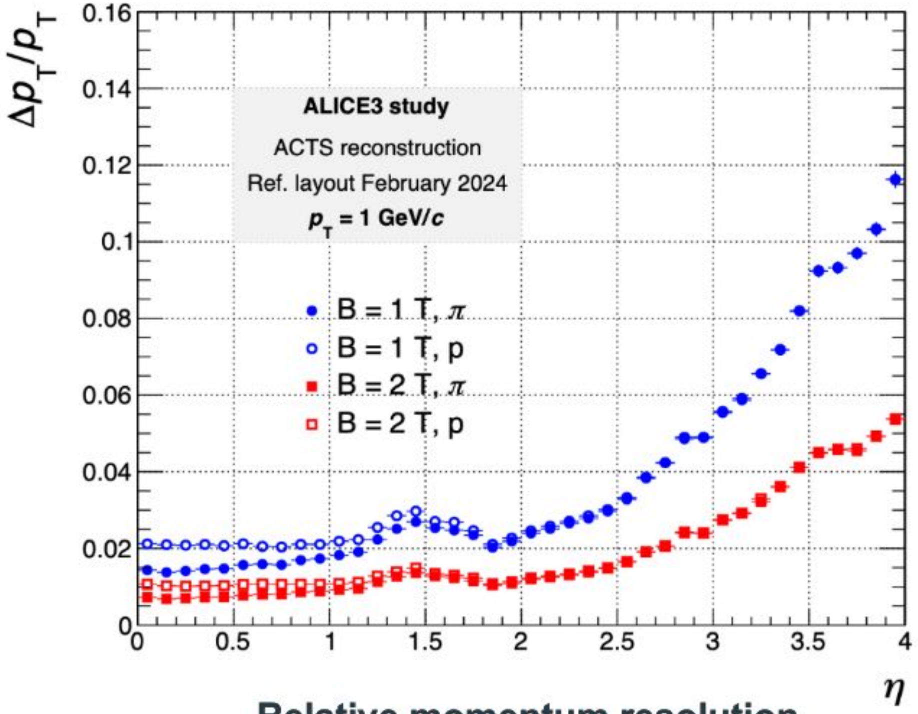


ITS3 Pointing resolution



ALICE 3 Tracking performance





Relative momentum resolution