

# Exploring XPOL-III: Advancements in CMOS VLSI ASIC for X-ray Detection

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We report on the design, implementation and initial tests of XPOL-III, a cutting-edge, 180nm CMOS VLSI ASIC integrating over 100K pixels at 50  $\mu\text{m}$  pitch (over a hexagonal grid) with an active area of 15 x 15 mm squared. Based on the readout chip successfully operating in the Gas Pixel Detectors onboard the Imaging X-ray Polarimetry Explorer (IXPE) since December, 2021, XPOL-III is designed to be used as a charge collecting anode, with a low-noise (30 e) spectroscopic electronics chain integrated within each pixel. The new ASIC significantly improves over its predecessor over all the relevant performance metrics, featuring a better uniformity of response, a significantly lower minimum trigger threshold, and a much higher (x10) throughput.

When coupled to a suitable solid-state pixel sensor, XPOL-III might open exciting perspectives for the implementation of a new class of event-driven, hybrid X-ray detectors providing excellent spatial and energy resolution with full single-photon sensitivity. In addition to the polarimetric applications for which the chip was initially conceived, we report on the initial R&D activity in this new direction.

## Collaboration

IXPE Imaging X-ray Polarimetry Explorer

## Role of Submitter

I am the presenter

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