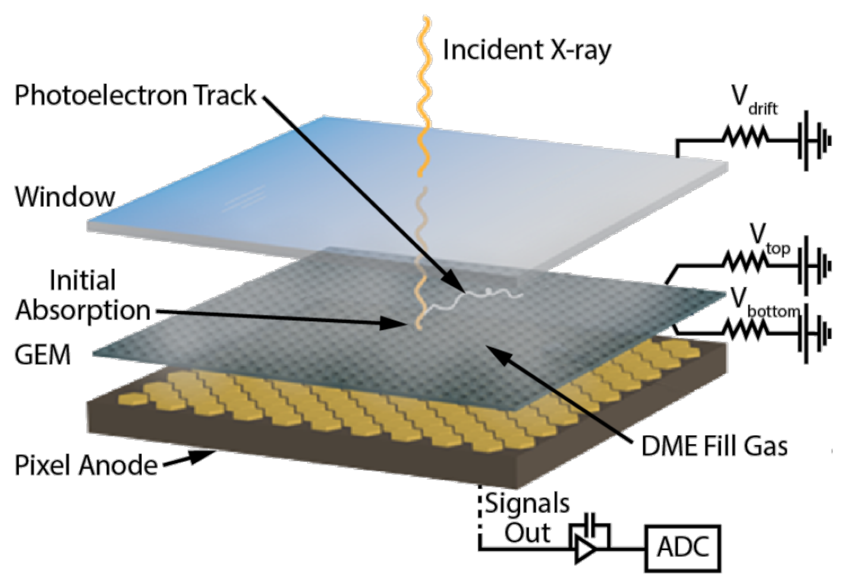
Exploring XPOL-III: Advancements in CMOS VLSI ASIC for X-ray Detection

M. Minuti[1]

[1]Istituto Nazionale di Fisica Nucleare, Sezione di Pisa, Italy

Abstract: *We report on the design, implementation and initial tests of XPOL-III, a cutting-edge, 180 nm CMOS VLSI ASIC integrating over 100k pixels at 50 μm pitch (over a hexagonal grid) with an active area of 15×15 mm^2. Based on the readout chip successfully operating in the Gas Pixel Detectors onboard the Imaging X-ray Polarimetry Explorer (IXPE) since December, 2021, XPOL-III is designed to be used as a charge collecting anode, with a low-noise ($30\ e^-$) spectroscopic electronics chain integrated within each pixel. The new ASIC significantly improves over its predecessor over all the relevant performance metrics, featuring a better uniformity of response, a significantly lower minimum trigger threshold, and a much higher (x10) throughput. When coupled to a suitable solid-state pixel sensor, XPOL-III might open exciting perspectives for the implementation of a new class of event-driven, hybrid X-ray detectors providing excellent spatial and energy resolution with full single-photon sensitivity. In addition to the original applications for which the chip was initially conceived, we report on the initial R&D activity in this new direction.*

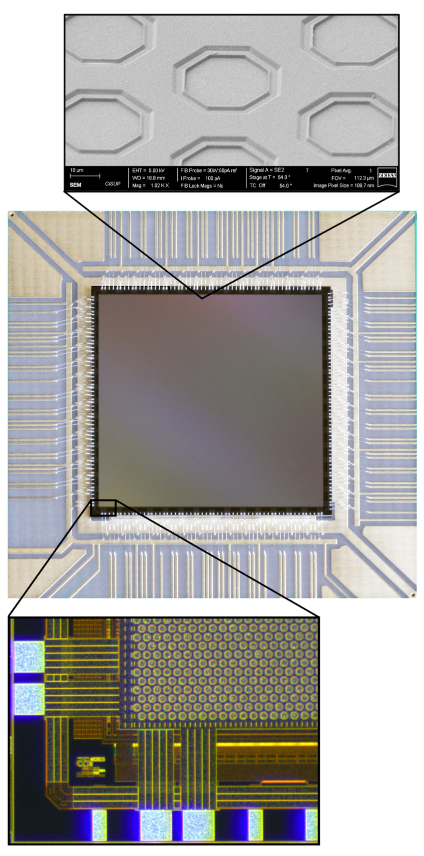
X-ray polarimetry



Photoelectron track in low pressure DME carries out the information on X-ray photon polarization. Track imaging has been made possible in the 2-8 keV range, coupling a thin-film GEM to a full-custom finely pixelated readout ASIC [1].

- A full-custom ASIC (XPOL) with over 100k 50 μm pixels for track imaging
- Successful operation onboard the IXPE and Polarlight observatories [2, 3, 4] Currently in LEO (IXPE), and SSO (Polarlight) since almost 3 years.
- XPOL is the starting platform for any further development in this field

XPOL-III ASIC Specification

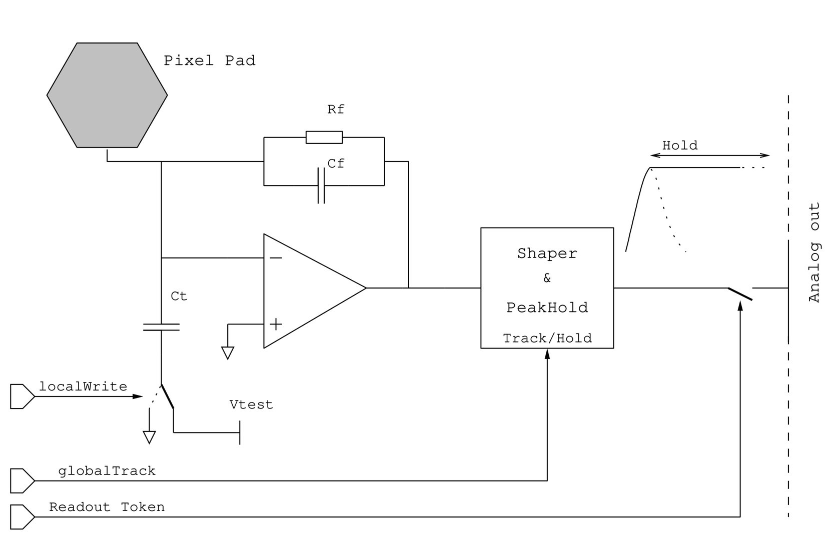


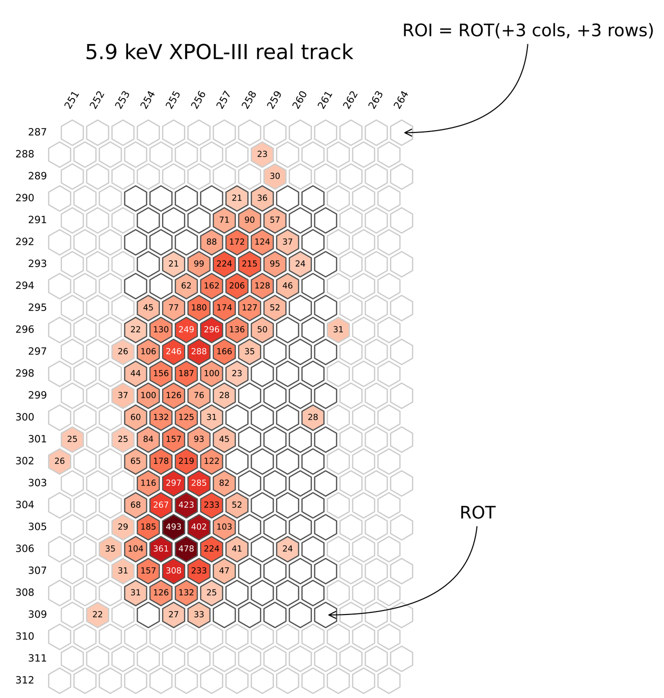
- Standard 180 nm CMOS process
- Hex pattern of 304×352 pixels, with 50 μm pitch
- Each pixel with metal electrode (charge collection) and amplification chain
  - Charge-sensitive amplifier, shaping circuit, and a peak-detector
- Single photon Self-triggering
  - Automatic localization of the region of interest (ROI)
  - Sequential readout of all the pixel in the ROI

XPOL-III ASIC [5] designed to improve single event readout speed

- Increase the frequency of the serial readout clock
  - Tested up to 10 MHz (~5 MHz in XPOL)
- Streamline the readout sequence
  - Used to be an important dead time contribution
- Reduce the ROI average size (see below)

XPOL-III Principle of Operation

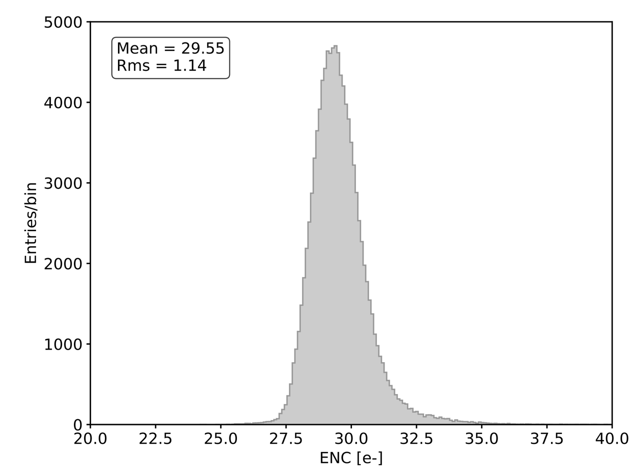




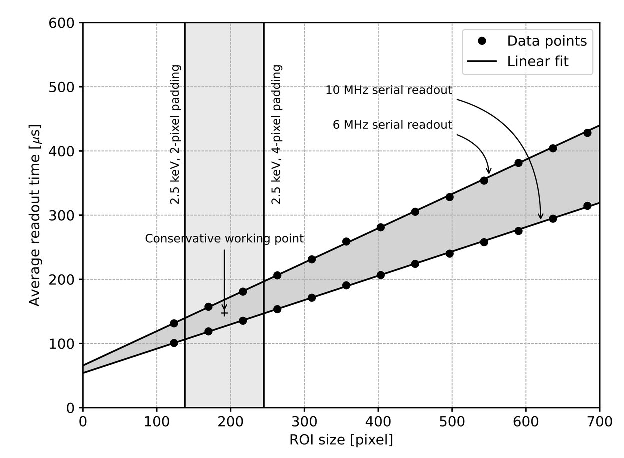
Trigger is based on the (analog) sum of the signals for 4 adjacent pixels (mini-clusters).

- Upon the detection of a trigger
  - Peak detectors are activated
  - A dedicated on-chip logic identifies the region of trigger (ROT) containing all the triggering mini-clusters
- Readout
  - A programmable margin is added to form the region of interest (ROI)
  - The readout is mastered by the external electronics and consists in a sequential readout of the peak detectors for all the pixels belonging to the ROI

Performance



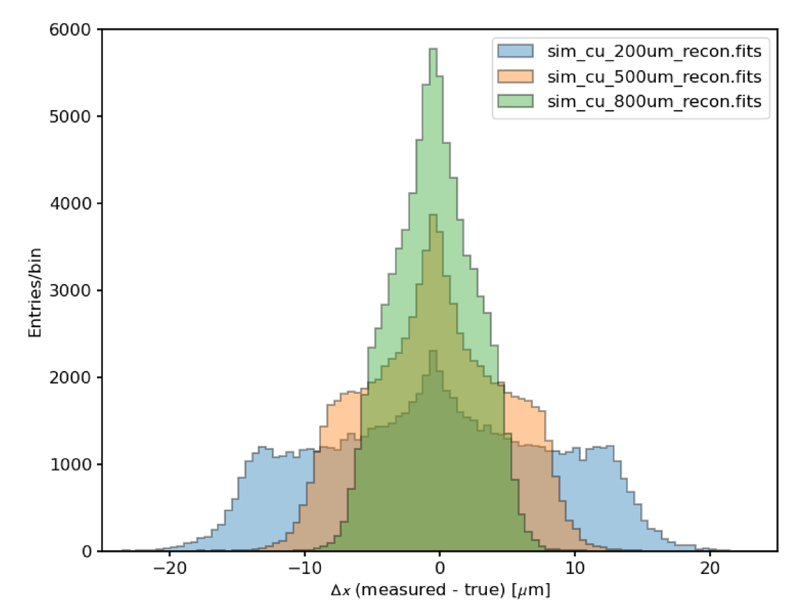
- Typical pixel noise is $\sim 30e^-$ ENC
- Minimum threshold $\sim 150e^-$
- Measured by reading externally selected ROI multiple times
  - New feature introduced in XPOL-III
- Same readout sequence as for real events



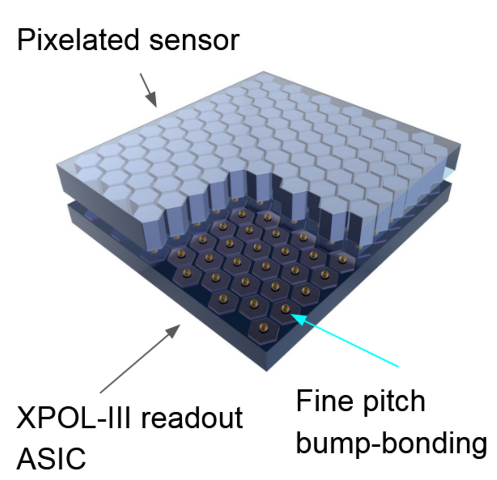
- Overall dead-time depends on the readout clock frequency and on the ROI size which in turns depends on the photon energy
- When compared with XPOL, at the 2.5 keV reference energy, dead time is 7× shorter
- Can go 10× with further DAQ electronics optimization

Towards High Resolution Spectral Imaging

Coupling a solid state sensor to the XPOL-III readout ASIC might open the way to a new class of devices. Exciting results emerged from preliminary GEANT-4 simulations with various sensor geometries. Exceptional position and energy resolutions are achievable by combining an appropriate sensor with a fine pitch and very low-noise analog readout.



The plot shows the distributions of the offset between the reconstructed charge cluster centroid and the MC photon absorption point for 200 μm, 500 μm and 800 μm Silicon sensors with 50 μm hexagonal pixel. (Cu $K_{\alpha 1,2}, K_\beta$)



- In-progress coupling to a solid state pixel planar sensor
  - 50 μm pitch, 300 μm n-o-p Silicon (2-10 keV)
  - 100 μm pitch, 750 μm tSchottky type CdTe (≥ 10 keV)
- Goal: spatial and energy resolution better than 10 μm and 400 eV @ 8 keV
  - Mainly limited by sub-optimal matching of the FE
  - To be drastically improved in next generation readout ASIC

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