Aggiornamento ALICE ITS3 2021-22

S. Beolé

21 Luglio 2022

OUTLINE

- ITS organization and INFN responsibilities
- ITS status and plans
- ITS3 status and plans

Project Organization

Institute Board

Team Leaders, Project Leader, Deputy Project Leader, ITS3 sub-project leaders, Technical Coordinator

Project Leader

S. Beolè (12/23)

Deputy Project Leader

A. Di Mauro

New Project Leader:

F. Reidt (1/1/2024-31/12/2026)

ITS3 sub-project

Sub-project Leaders

A. Kluge, M. Mager

Work Packages Conveners

Physics and Performance/A. Kalweit, **A, Rossi**

Chip Design/G. Aglieri, W. Snoeys

Chip Characterization/M. Suljic, S. Senyukov

Thinning, Bending and Interconnection/

G. Contin, **D.Colella**

Mechanics and Cooling/C. Gargiulo

Read-out/ O.Groettvik, F.Reidt

ITS2

Technical Coordinator

F. Reidt

Deputy: M.Keil

System Run Coordinator

N. Valle (12/23)

A. Isakov (12/23)

Electronics Coordinator

G. Aglieri

Software Coordinator

M. Concas

Sub-system Coordinators

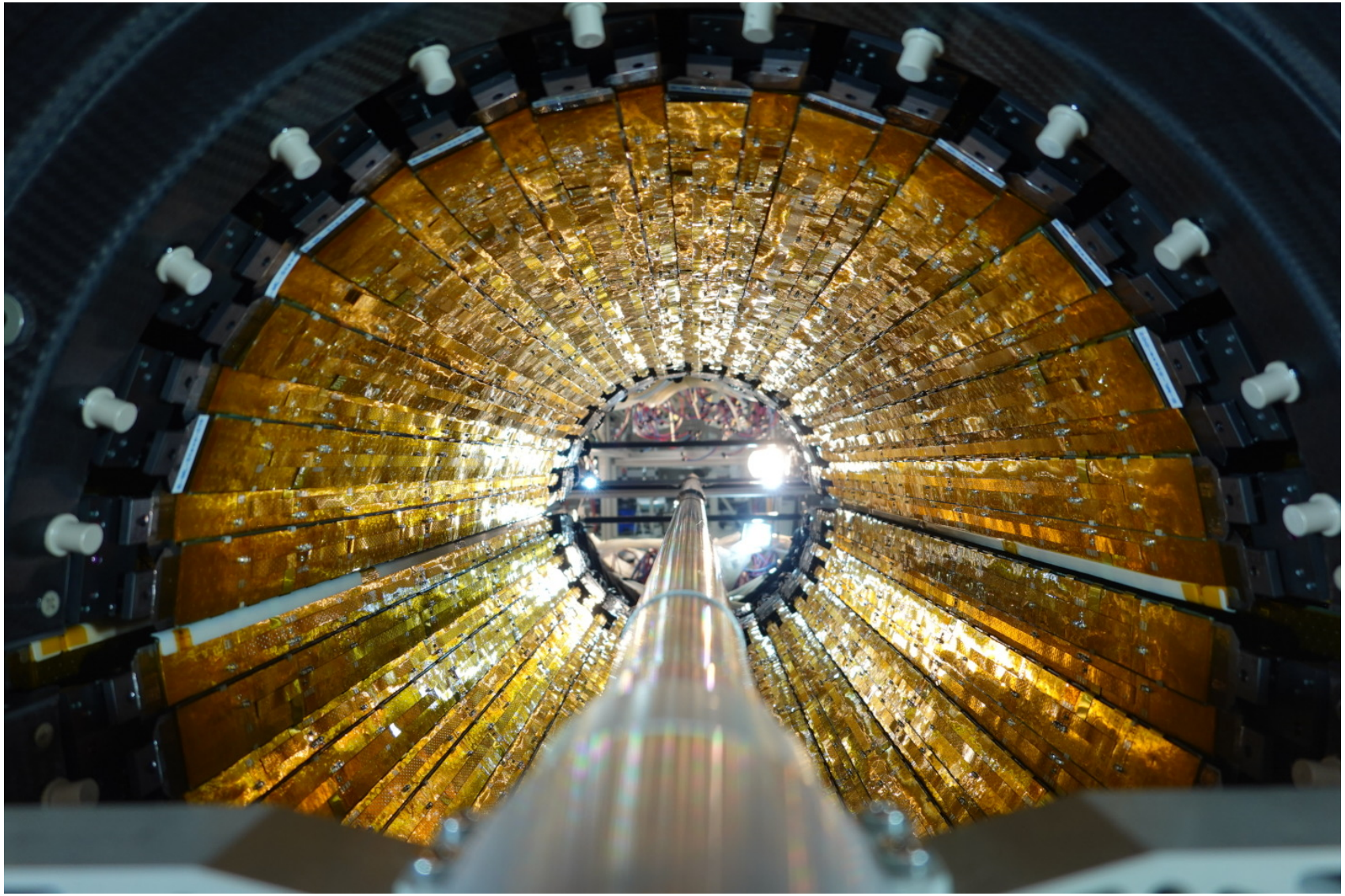
DCS/M. Keil

ITS2S/P. Martinengo

Cooling/S. Senyukov

ITS2

Slide da:
Nicolo’ Valle
Matteo Concas
Ivan Ravasenga
Mattia Faggin



Presa dati 2022

ottimizzazione tools di QC

issues

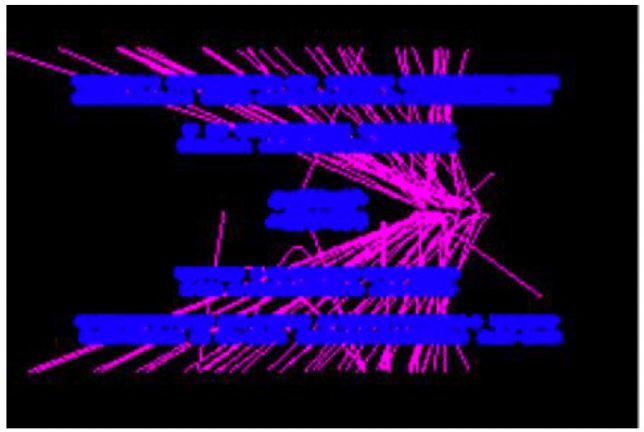
in-run recovery

overall performance

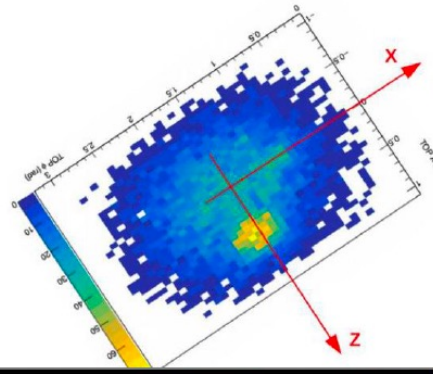
Global commissioning

Effort to finalize the sytems readiness and the new software chain.

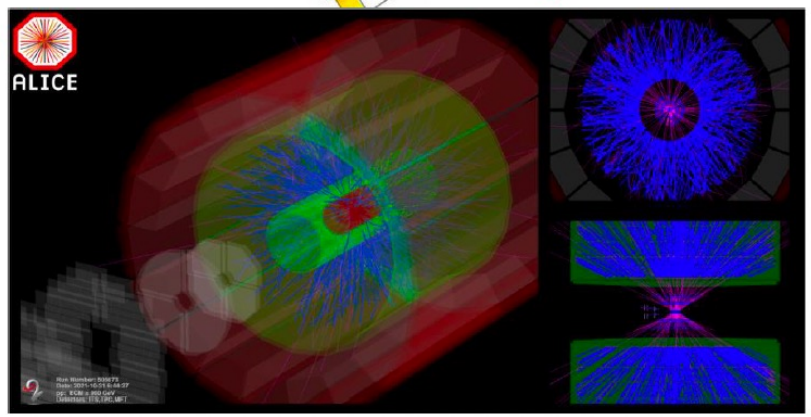
- ✓ Cosmic muons: pre alignment (O(100um)) and combined reconstruction with other detectors.
- ✓ Emulated events by injecting pulse patterns in the chips → readout and processing under realistic load.
- ✓ TED shots
- ✓ pp collisions at 900 GeV



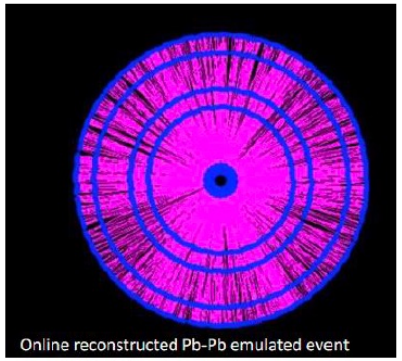
40 cm vertex displacement in first pilot collission, ITS still able to find it.



Cosmics distribution, "ITS knows where it is"



Emulated PbPb event



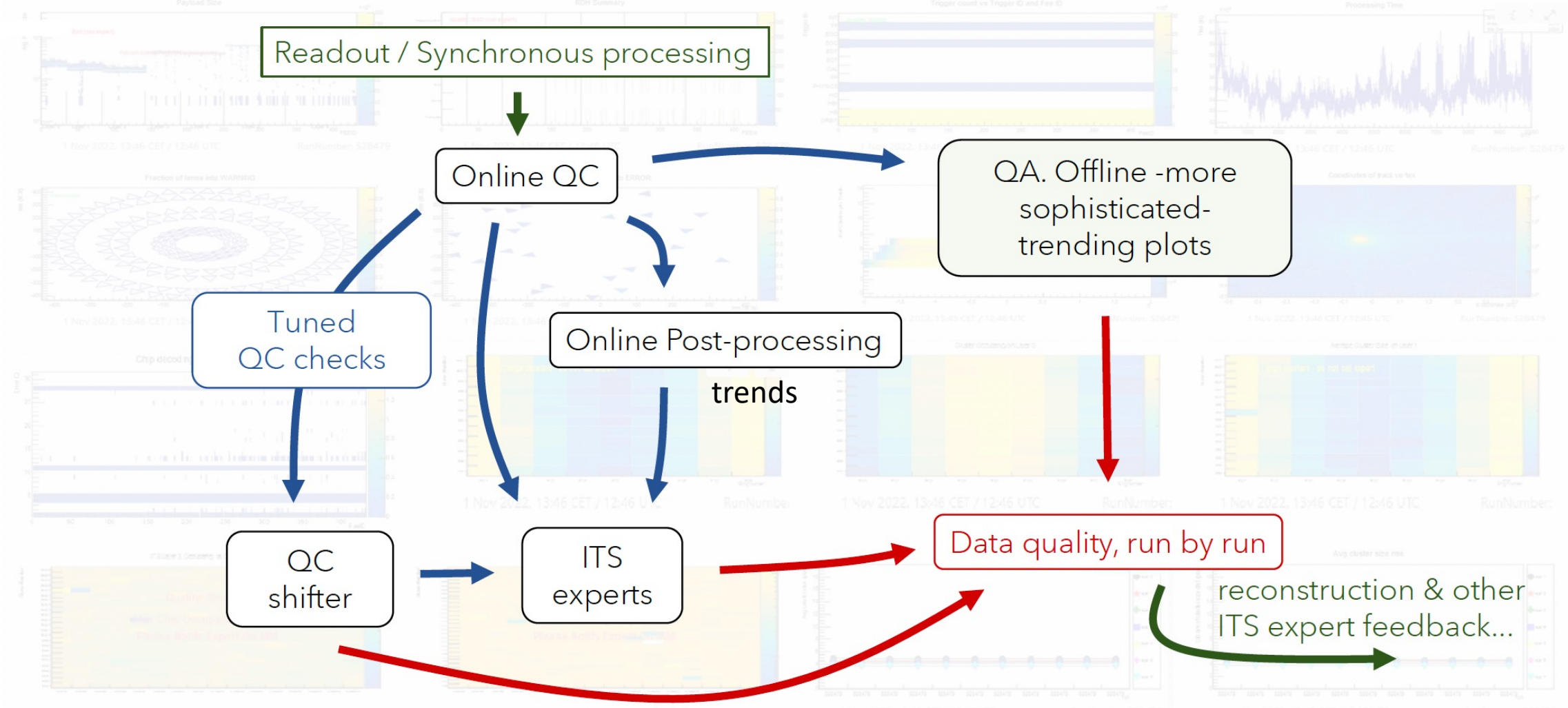
2022 at top LHC energy

- ITS crucial detector for vertexing and tracking in the barrel
  - ITS data quality drives ALICE data quality

DEETECTORS IN GOOD QUALITY GLOBAL RUNS

https://evsel-qa.web.cern.ch

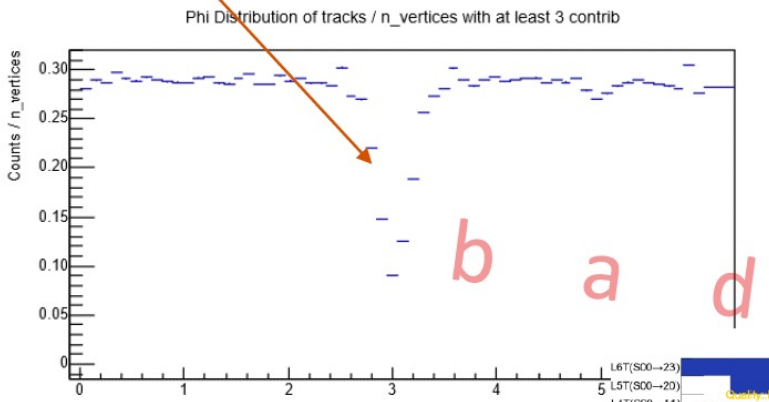
Data Quality Control & Assurance



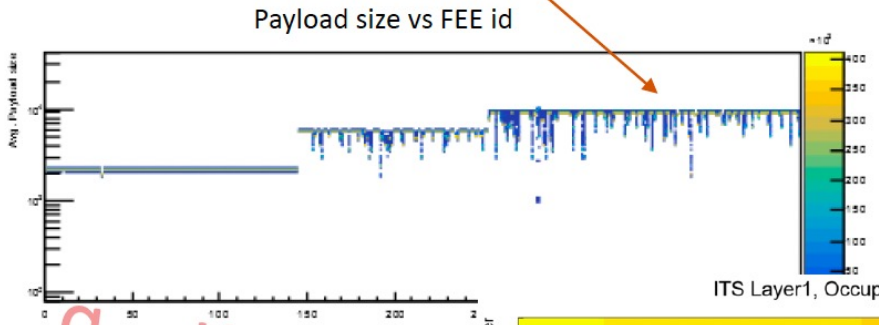
Data Quality Control & Assurance
Online QC

Complete and in-deep view on data quality thanks to advanced QC workflows.

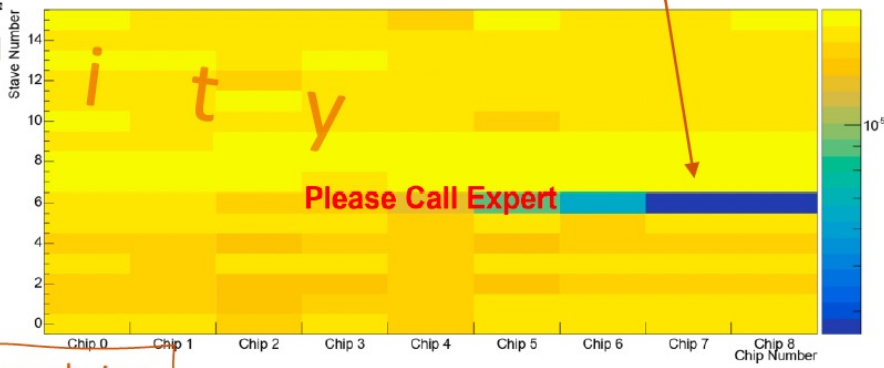
Track distribution.
Hole (on L3)



Data integrity check
degraded readout rate

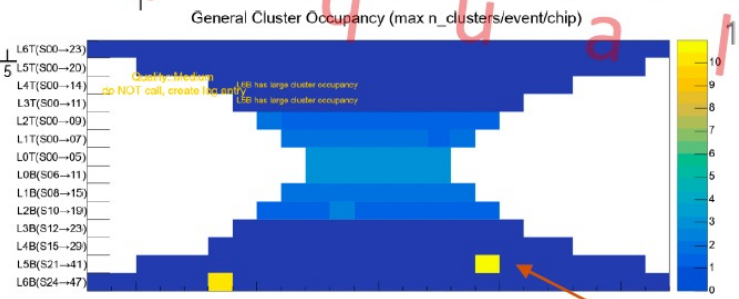


Hit occupancy
Chips stopped sending data during the run



b a d q u a l i t y

5 tasks running online during data taking
Front-end electronic disgnostics
Hit occupancy
Cluster occupancy/size
Track distributions
Decoding errors



Cluster occupancy and size
Noisy elements

DATA QUALITY

Main issues during RUN3 data taking

Data corruption

Not only originating from ITS front-end. Mostly mitigated by now

Radiation-induced errors: new robust FPGA scrubbing under implementation

Misconfiguration

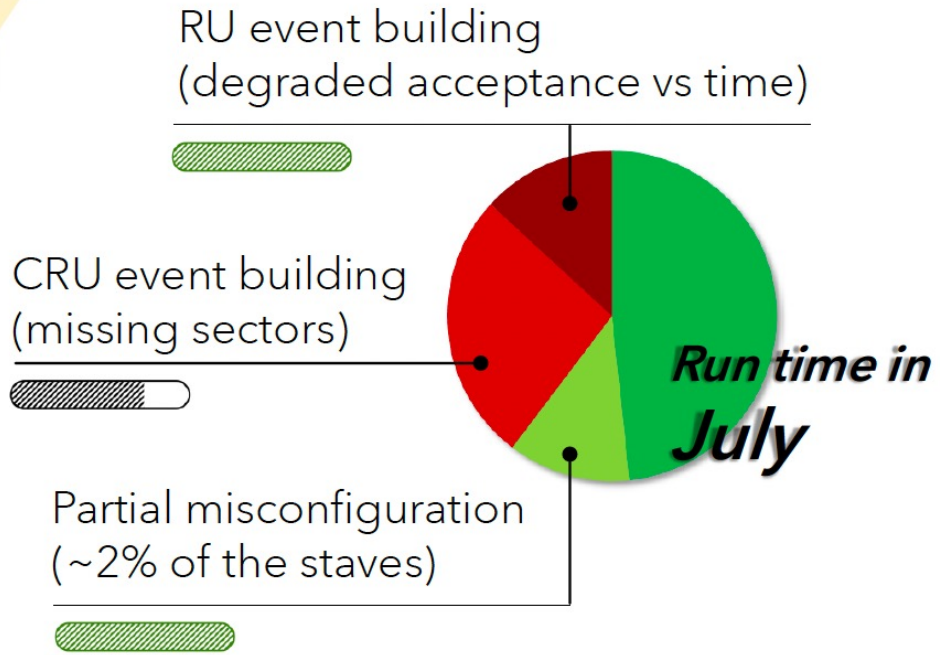
Made negligible by improved DCS / backend software

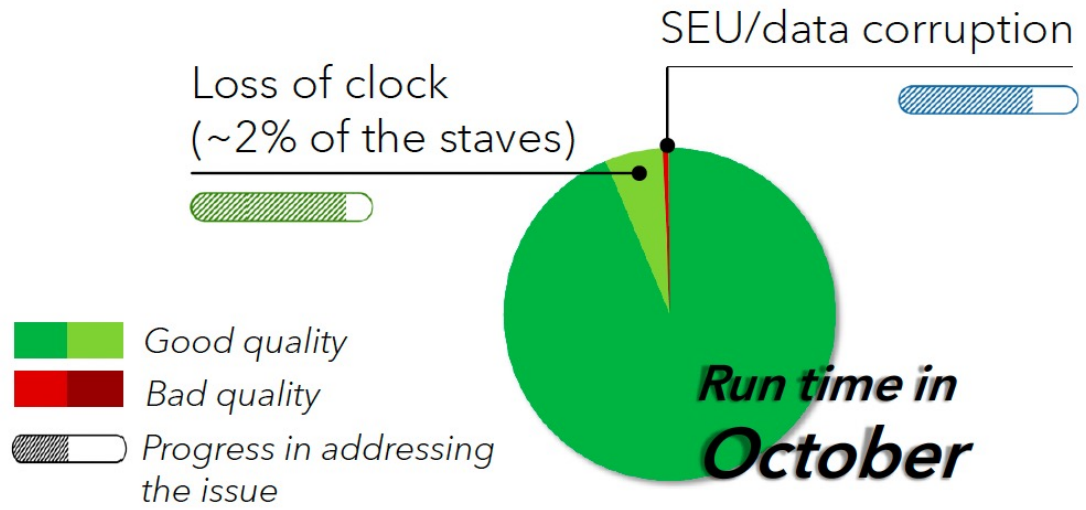
Loss of clock
Loss of chip links

In-run recovery minimizes the averaged loss of acceptance

Next slide ;)

Few chips showing unrecoverable errors, better understading in progress (low priority, for data quality)





In-run recovery

Readout through high-speed links
IB: 1 link = 1 chip
OB: 1 link = 7 chips

~1% loss of acceptance already reached with a non-finalized recovery logic

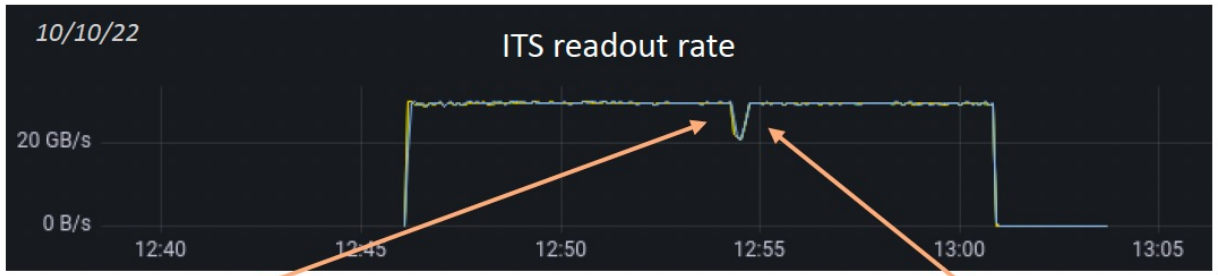
Links lost during run at a rate of ~2.5% per hour.
Most of them traceable to (unavoidable) beam-induced events.

Automatic recovery allows for a minimal data loss.

Dector and RU receiving logic reconfigured while trigger forwarding is supended.

Loss of clock

~1 event/day, i.e. 1 stave/day when a run is ongoing
In-run recovery testes successfully

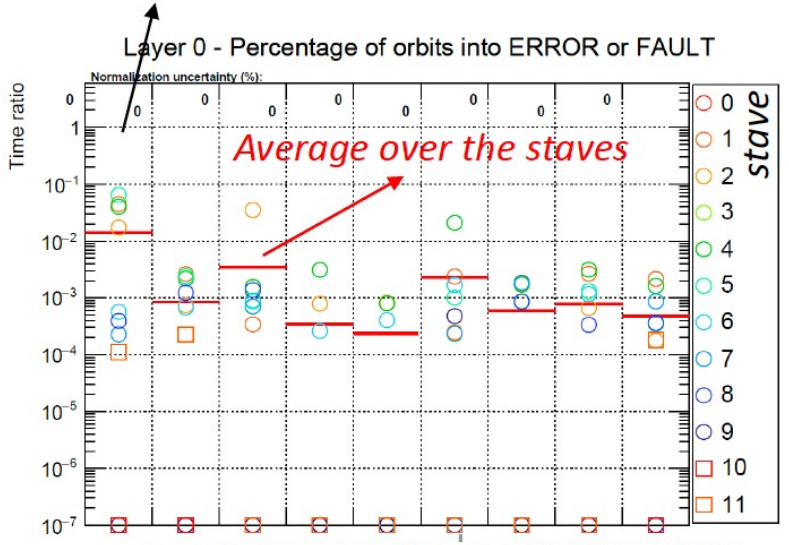


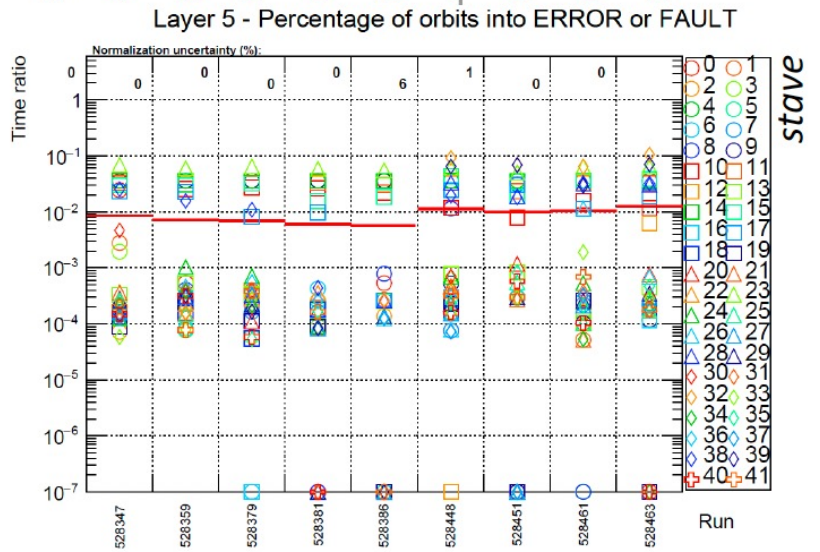
Massive event, all the IB/ML chips lost

links automatically recovered

6-hours run

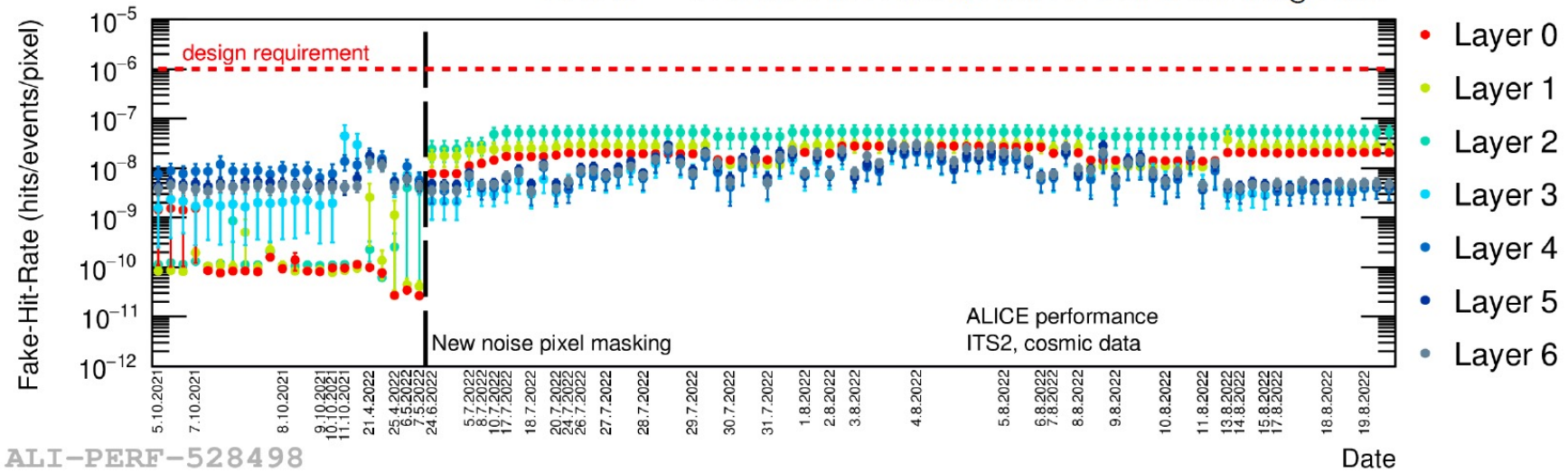
pp 500 kHZ
202 kHz ROF rate





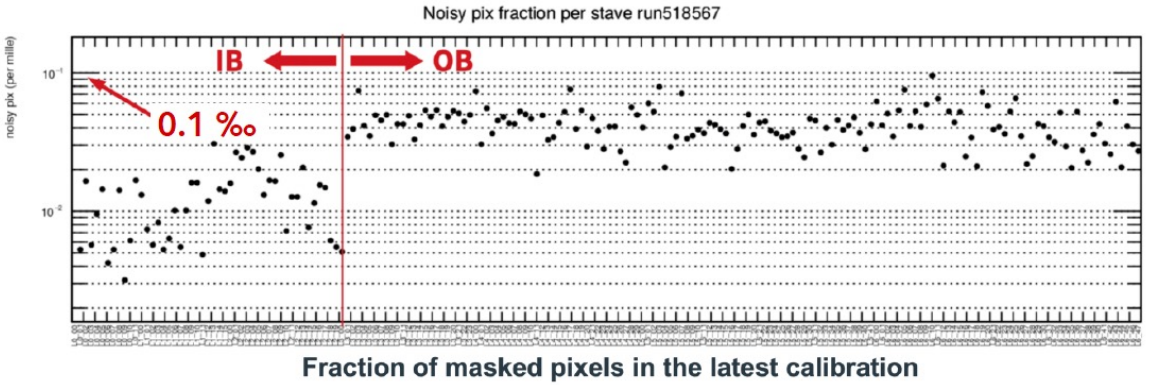
Fake-Hit Rate

Hits/event/pixel measured during cosmic runs.
«Event» = 1 ReadOut Frame, with 200 kHz framing rate.



Fake-hit-rate stable and well below the design requirement of 10^{-6} hits/pixel/event.

Inner barrel masking logic (since June):
- Only stuck and very noisy pixels are masked.
- Prioritization of efficiency over data-rate reduction.



Data quality

2022

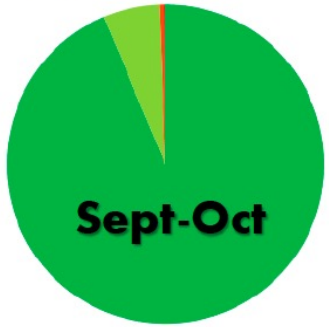
Percentage of run time
(BAD runs included)

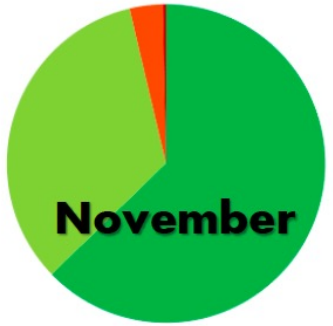
OK

O(1 to 2) staves missing out of 192 → O(2%)

Missing sectors ~ ¼ to 1 layer out

Other major problems





- RU timing issue before fw 1.17.2 (July 08th)
- CRU packaging and readout config before fw 3.15
- ML O-side, cooling tuning on July 11th
- Misconfiguration (missing FSM commads)
- L4_17 short

- Operator error (misconfiguration)
- Remaining data corruption @ SOR
- L6_17 configured with NOSCAN (ITS2-44)
- Invalid data from staves with no scrubbing.

- Remaining data corruption @ SOR
- Ivalid data from RUs with no scrubbing
- Clock errors
- Invalid data form RUs with no scrubbing.

- Detector configured with wrong timeout
- Detector configured with wrong run type (bookkeeping)
- L1/IB ecluded for threshold tuning investigation
- Invalid data from RUs with no scrubbing
- Clock errors
- Invalid data from staves with no srubbing (high percentage: L0_10 during a fill with long runs)

All the cases are now spotted by QC in < 3mins.

Presa dati 2023

overall performance

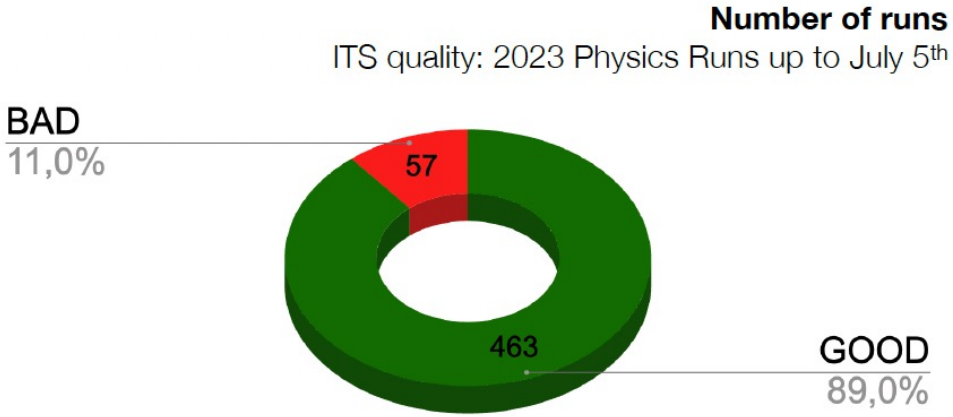
detector ageing

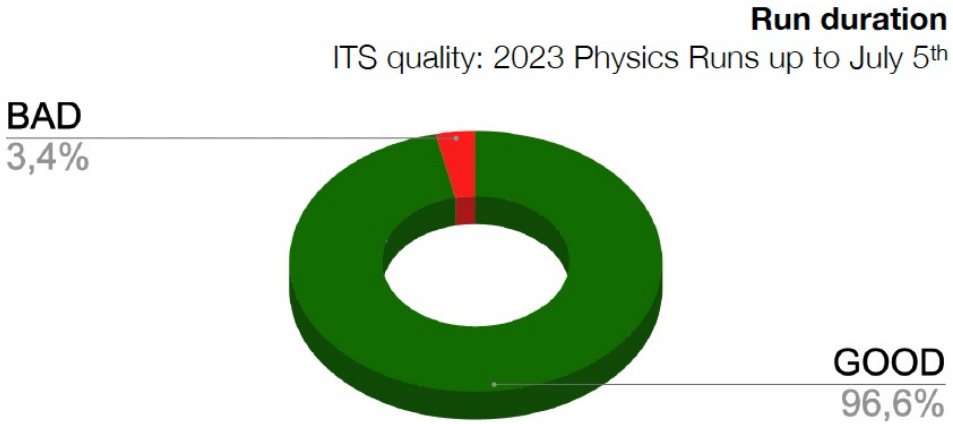
calibrazione

Overview of data taking in 2023

2023

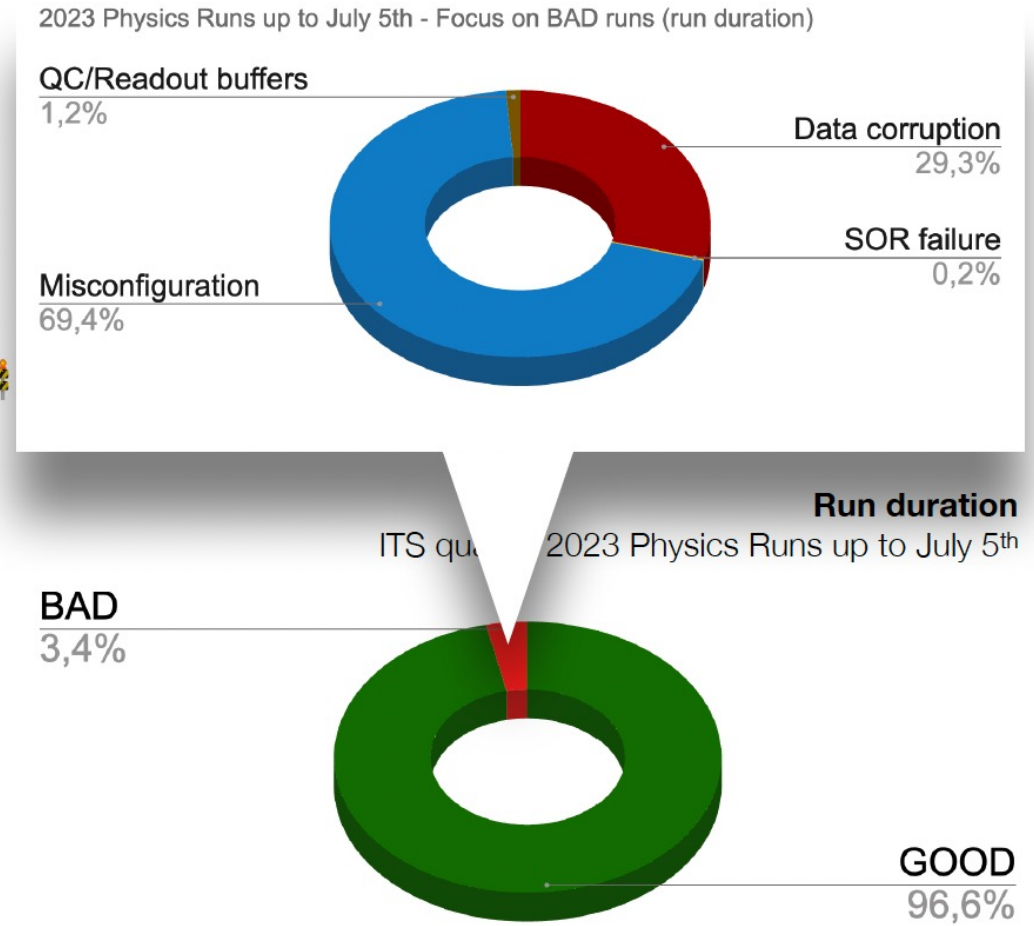
- This year: **~500** hours of **GOOD** *pp* data
- ALICE Inner Tracking System is a crucial detector
  - BAD ITS Run → BAD Global run





Overview of data taking in 2023

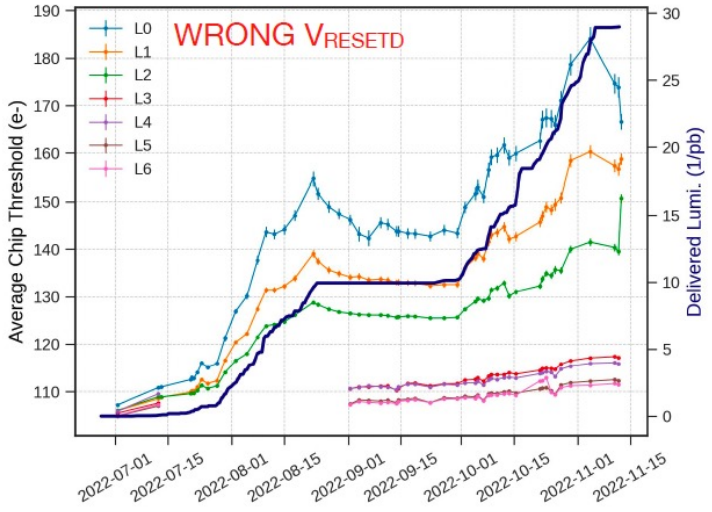
- This year: **~500** hours of **GOOD** *pp* data
- ALICE Inner Tracking System is a crucial detector
  - BAD ITS Run → BAD Global run
- Status of leading causes for BAD ITS runs
  - **Misconfiguration**: human error, fully addressed in DCS[1] ✅
  - **Data issues**: investigations ongoing to fully understand the issue 🚧
  - **External events**: sporadic and low in duration ☮️

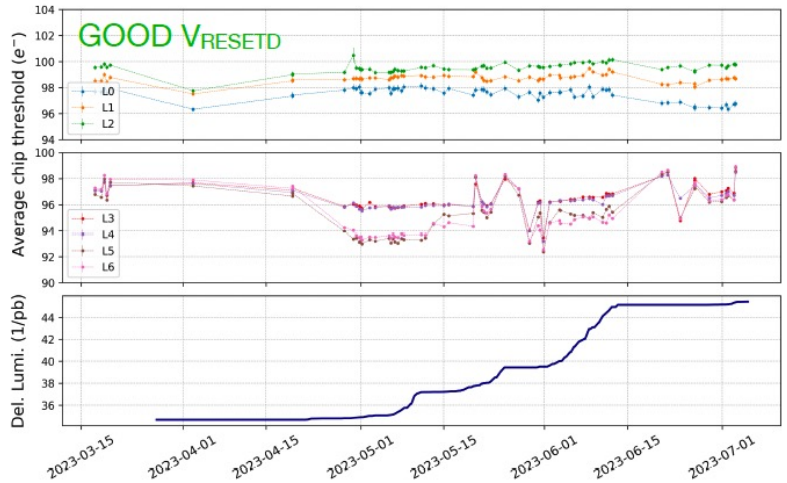


[1] Improved interface for shifter and ability to automatically set run type at "*prepare for run*" stage, not in production yet

Detector ageing: under control

- Q3-Q4 2022
  - Constant settings from late June to October
  - **Threshold monotonously increasing** with radiation load
  - Tuning to **100 e⁻** was **no longer possible**: could this become an issue?
  - Thorough investigation started[1]
- End of 2022 (YETS)
  - **Discrepancy** found in resulting calibration using surface commissioning tools
  - Pixel reset voltage **V_{RESETD}** configuration prevented the correct functioning
- Restart of data taking 2023
  - V_{RESETD} **corrected**: current tune very close to the June 2022 one
  - It should be ok until end of operations (based on single-chip radiation tests)
  - **Ad-hoc calibration scan** for V_{RESETD}



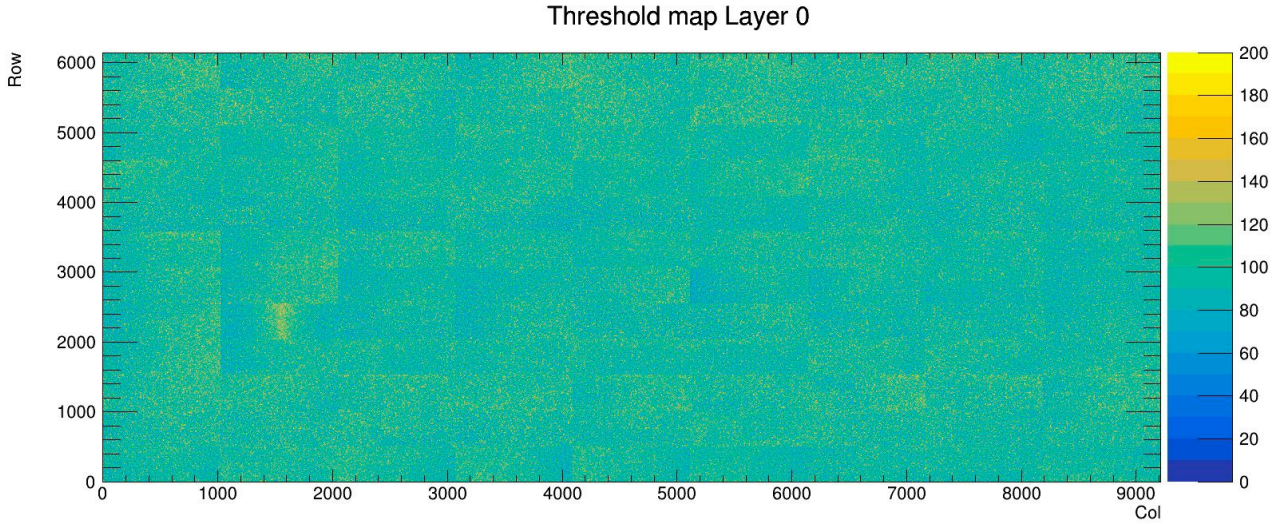


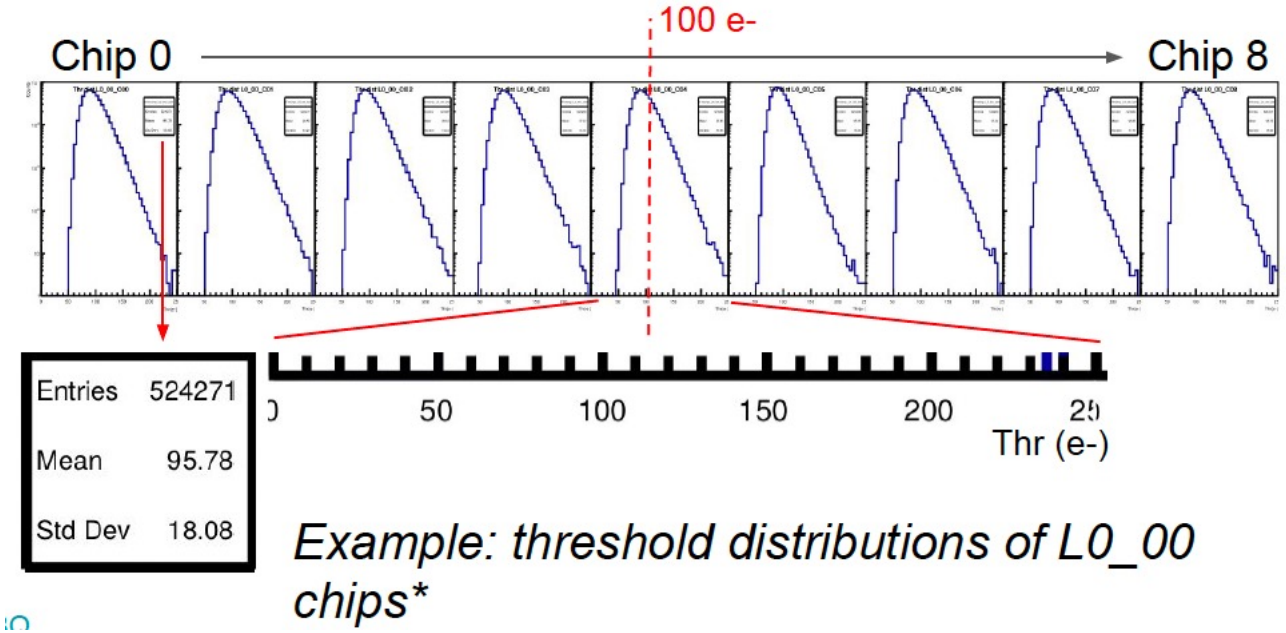
Thresholds in 2023: with correct V_{RESETD} remain constant

[1] Detailed explanation in this talk

Calibrazione

- FULL Threshold scan su tutto il rivelatore (24000 chip): esempio Layer 0
- tuned to 100e$^-$

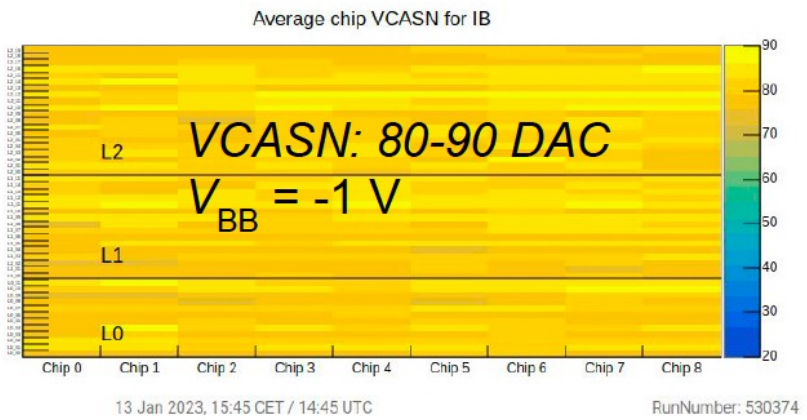


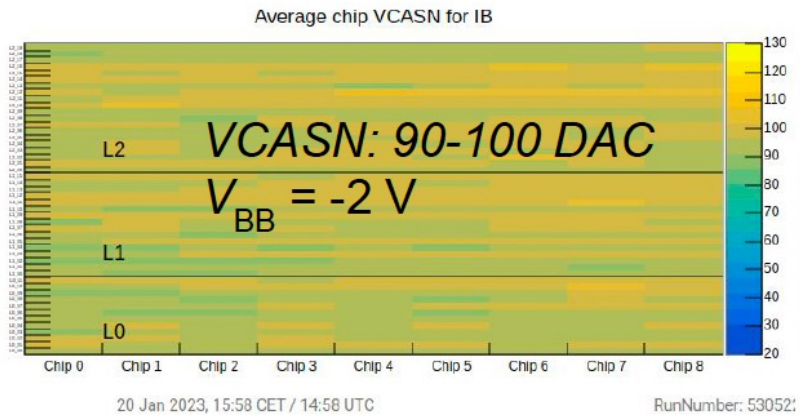


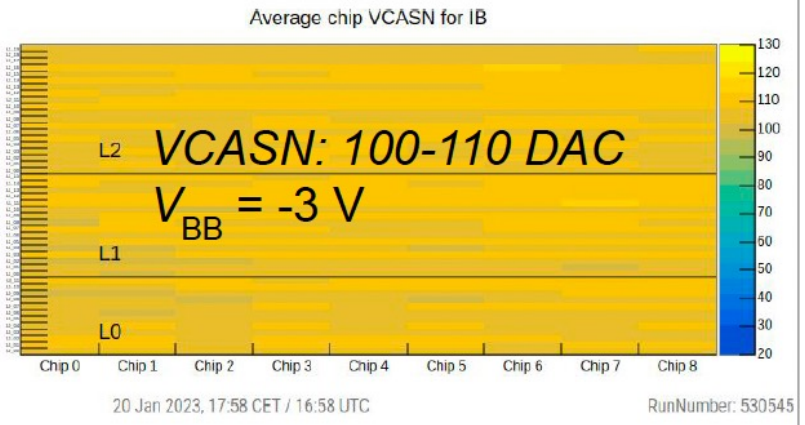
*Example: threshold distributions of L0_00 chips**

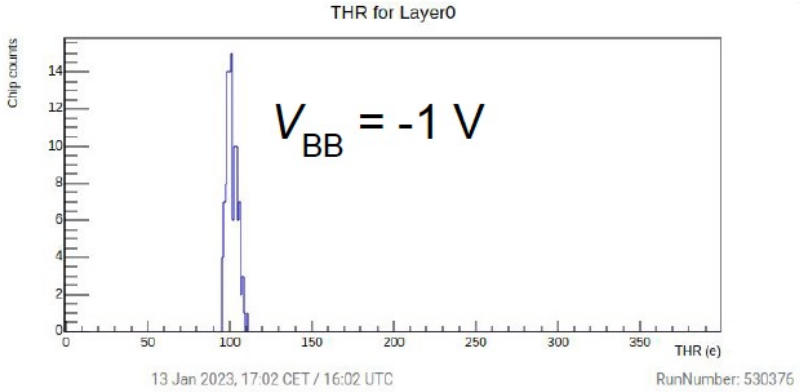
Calibration of IB with back-bias (2)

- Calibration with BB achieved: tuning to 100 e- ⟶ Examples below ⟶ L0, 1, 2 fully comparable

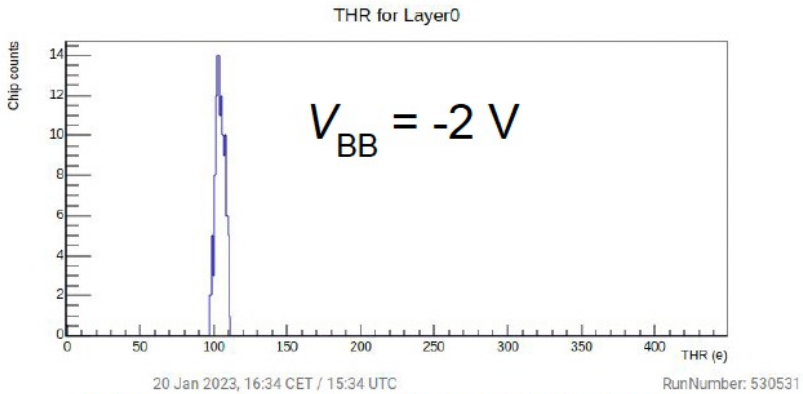




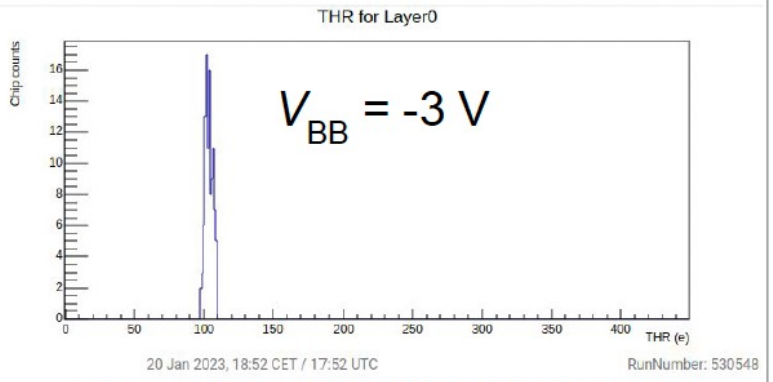




Example: avg. thr of L0 chips



Example: avg. thr of L0 chips



Example: avg. thr of L0 chips

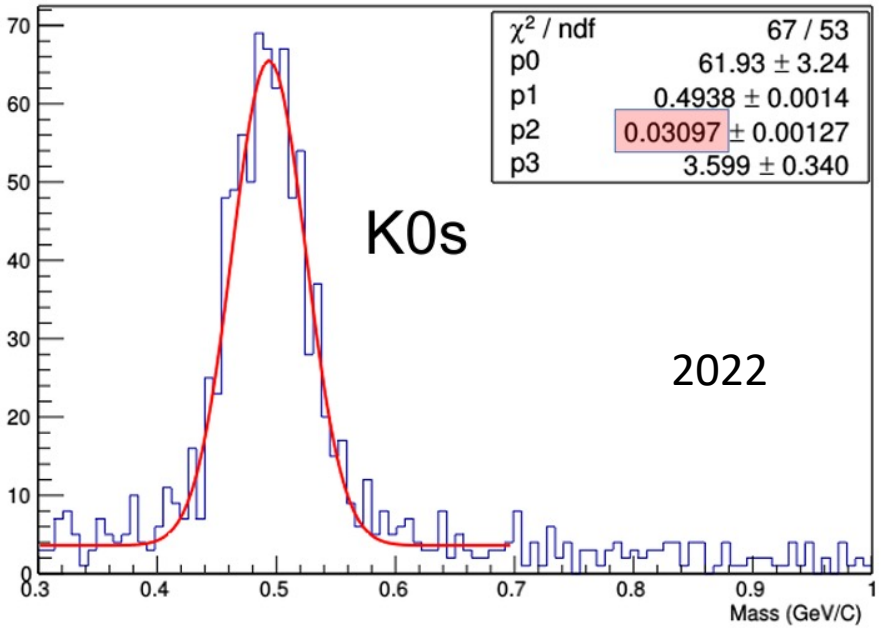
ITS Performance

Allineamento

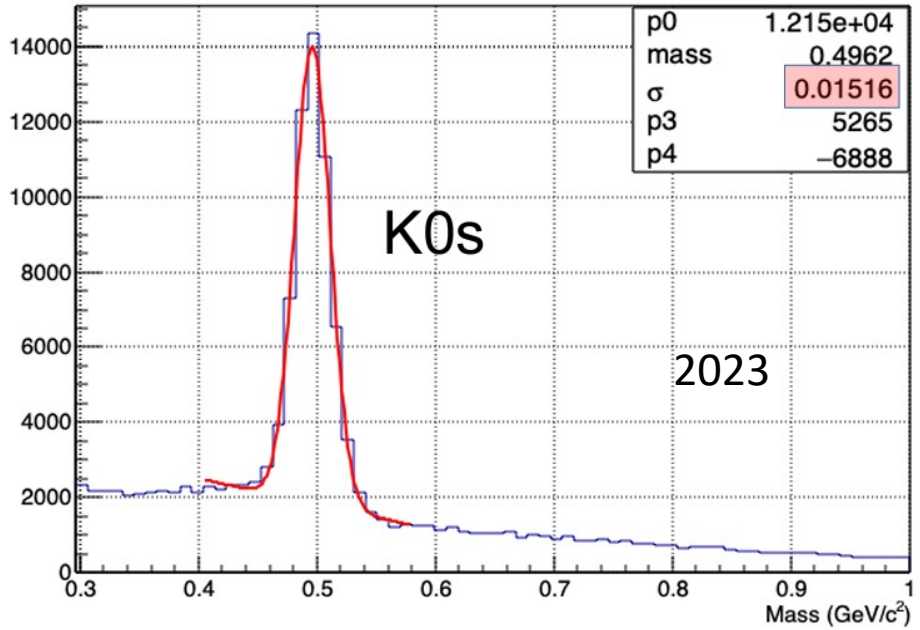
Impact parameter resolution

Allineamento: confronto 2022-2023

Pre-aligned



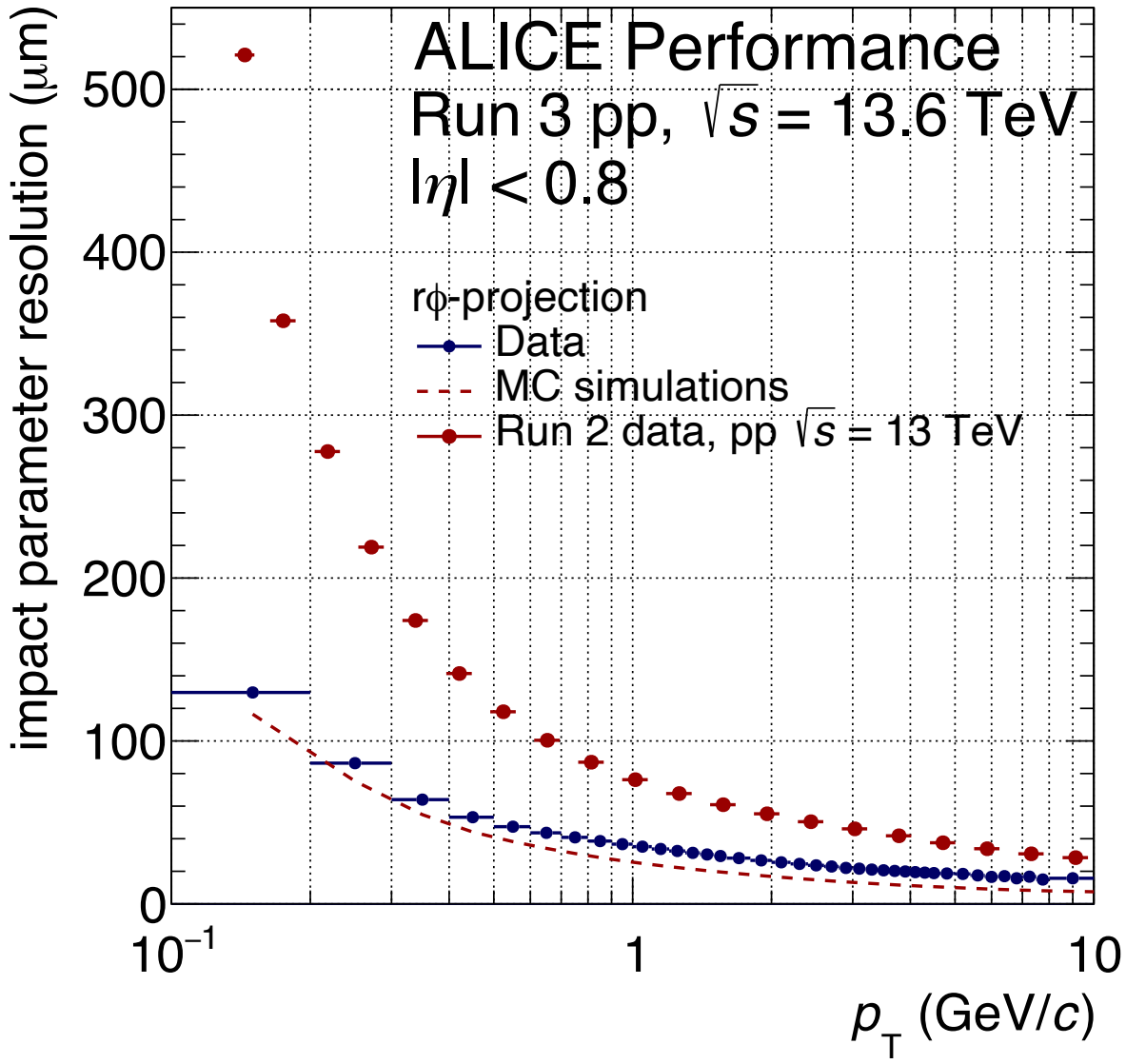
Aligned



- The width of the aligned K0s peak is **15 MeV**. This is **2x better** than last year

Impact parameter resolution: confronto Run2-Run3

MC anchoring ancora non ottimale, discrepanza residua ~10um



PbPb readiness

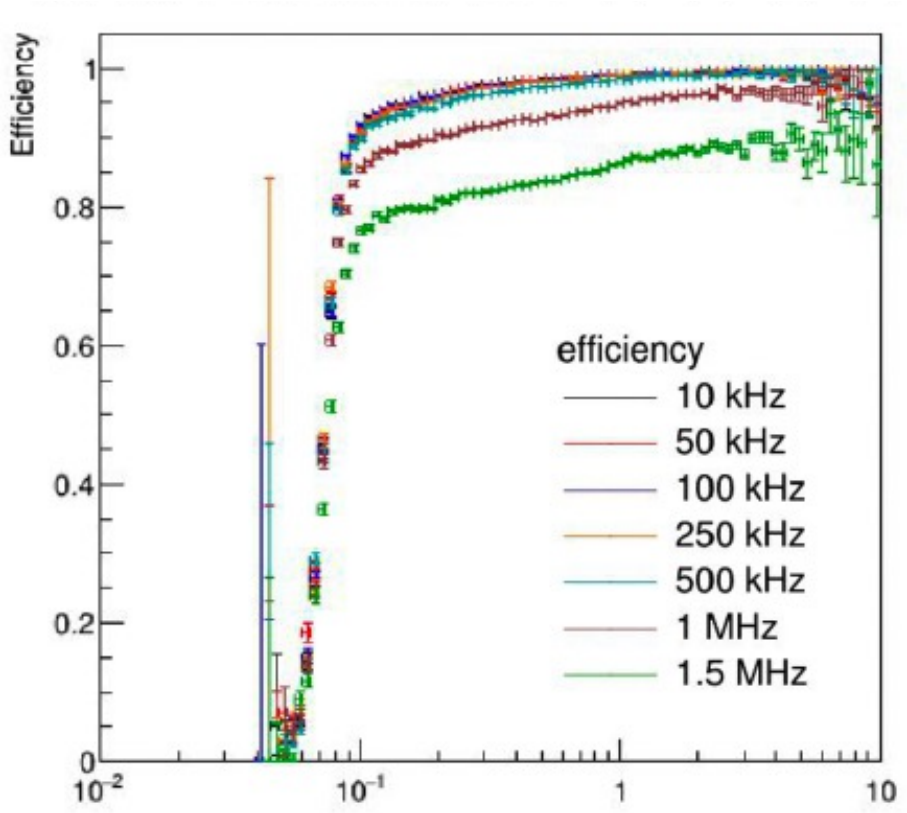
Controllo tracking performance

Data taking in PbPb

To do list

Better understanding our data

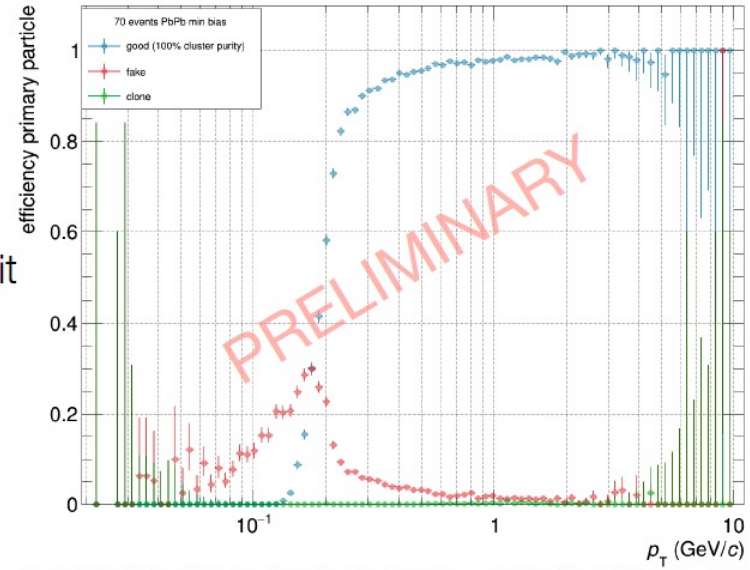
- ITS **standalone performance** to inspect data and evaluate MC
  - A systematic check of offset stability for ITS data transmission wrt TOF/TPC
  - Average cluster size vs η from identified pions in MC and data
  - Seeding vertices purity
  - Impact parameter estimation using ITS-only tracks
- Performance vs **interaction rate**
  - Tracking efficiency vs p_T, η, Φ. Interesting to evaluate the limits of our setup
  - Duplicate fraction estimation in & average number of tracks/ROF
- Good opportunity to **get acquainted** with ITS software and data
  - We use **data from central productions** as much as we can, **not always possible**
  - Idea: collect all efforts in a **single entry point** rather than multiple ROOT macros
  - **Collaborators** develop their **independent tasks** with simplified I/O



tracking efficiency vs IR

ITS data taking conditions in Pb-Pb

- LHC will deliver **PbPb** collisions up to **50kHz** of interaction rate (IR)
- ITS takes data in **continuous-readout** mode
  - Target framing rate to operate is **67kHz** (45kHz as fallback) to **minimise pileup**
  - **Readout Frame** (ROF) duration is extended to **594** (891) bunch crossings ~6(4) ROF/orbit
- No further change in detector working conditions is required/foreseen
- Synchronous reconstruction
  - By design, **1% of primary tracks** are fully reconstructed to allow for TPC calibration
  - Reconstruction and tracking **software is the same** used for *pp* sync
  - **Configuration** slightly **changes** due to the **higher** average **multiplicity**
  - Software is generally **ready** for sync data taking; improvements are on the way



Current tracking efficiency for primaries in sync reconstruction of Pb-Pb minbias.
Tracks with at least one fake cluster are marked as fake

	Event processing time (s)
AMD Ryzen 9 7950X	0.44

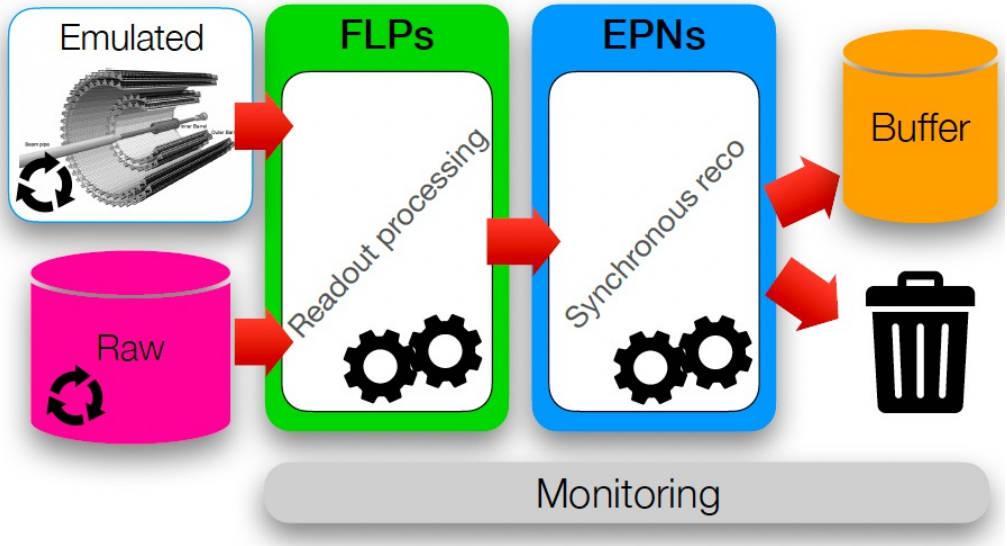
Benchmarks from run with O2DPG full simulation workflow

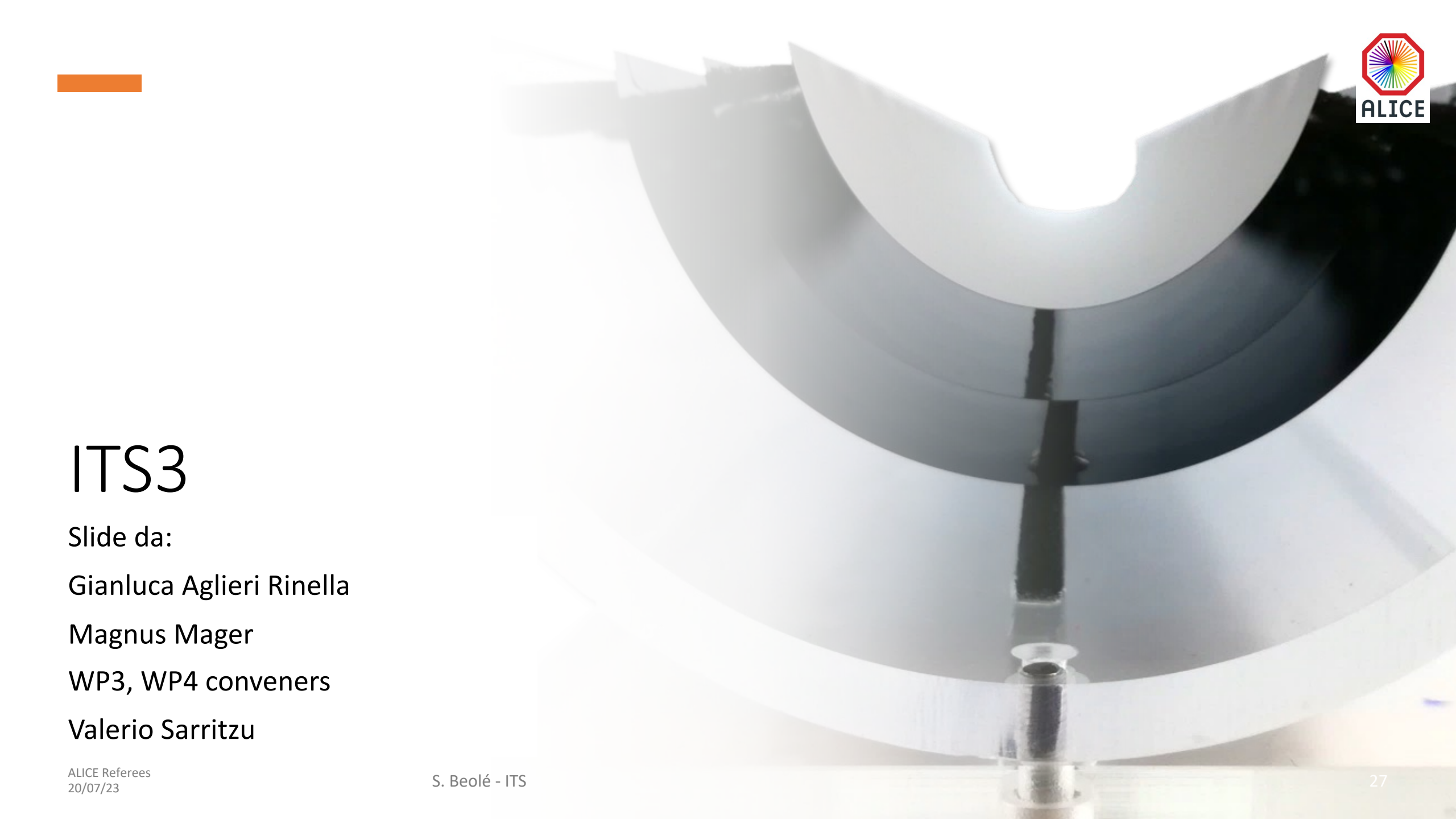
To do list

- Simulations in the working environment
  - Extensive test of the whole operation machinery and pipelines
- Emulated patterns (detector included)
  - **Injected** pixel response: **realistic measurement** from simulation
  - Sensible to the **real state of the chip/links**
  - **Reproduce** readout rate, **chip** and **detector occupancy**
  - Next weeks: **update** the emulated **patterns** with **new Pb-Pb events**

ready

- Synthetic runs (detector excluded):
  - **Replay of RAW** chip data starting from readout nodes
  - Instrumental to **test data processing** on FLP and EPN
  - **Validate** processing **pipeline**, stress tests
  - Next weeks: **update** RAW chip data with **same emulated Pb-Pb events**





ITS3

Slide da:

Gianluca Aglieri Rinella

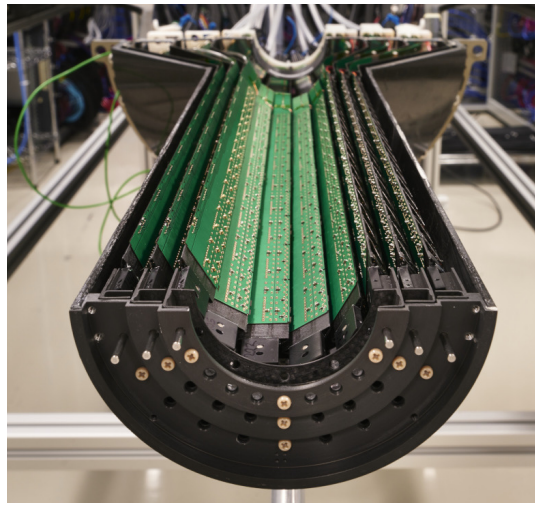
Magnus Mager

WP3, WP4 conveners

Valerio Sarritzu

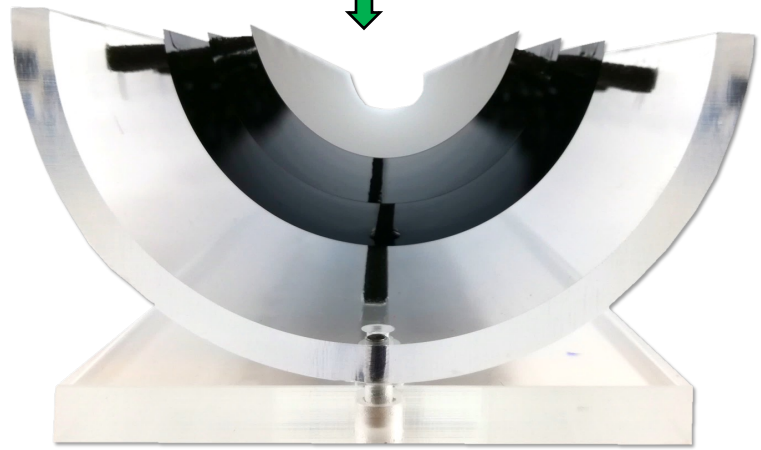
ITS3: all silicon new vertexer

LOI: CERN-LHCC-2019-018



- New detector technology:
  - three truly cylindrical Si pixel layers based on ultra-thin wafer-sized curved sensors (65 nm CIS technology)
  - no external connections nor cooling
  - new beam pipe
  - new concept for future detectors
- Performance:
  - Pointing resolution improves by a factor 2 compared to ITS2 in the full p_T range
  - Tracking efficiency increases by a factor 1.2-2 compared to ITS2 in p_T < 100 MeV/c

inner layers	ITS1	ITS2	ITS3
X/X_0	1.14%	0.36%	0.05%
innermost radius	39 mm	22 mm	18 mm
pixel size	50x425 μm^2	30x30 μm^2	O(15x15 μm^2)



ITS3 road map

- large area
- stitched
- bent

Can we test each feature independently?

bend existing chips (ALPIDE)

caveat: ALPIDE technology 180nm CIS -> need to test bending on 65nm

large area wafers: 65 nm CIS

port charged particle CIS from 180 to 65nm -> MLR1

stitching in CIS for charged particles sensors (widely used for imaging sensors) -> ER1+ER2

Towards the wafer-scale sensor

timeline (ITS3/LHC)

MLR1

MLR1 | ER1 | ER2 | ER3 — ITS3

- MLR1: technology characterisation — submitted and tested
- ER1: stitching verification
- ER2: full sensor
- ER3: final sensor

- **MLR1:** technology qualification
  - charge detection
  - radiation hardness
- **ER1:** stitching prototype
  - first time stitching is done in HEP
  - different defect mitigation strategies
  - stitching in one direction
- **ER2 + ER3:** final size (2D) stitched sensor

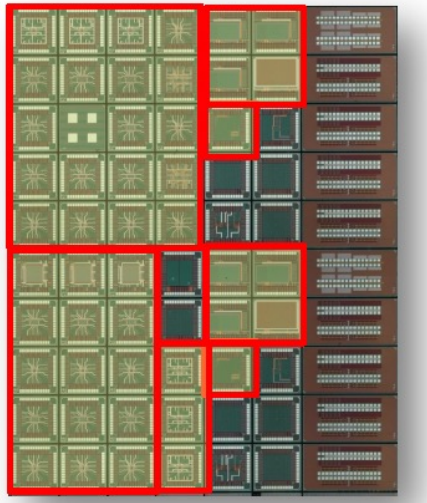
MLR1 test set-up developed by INFN
APTS and DPTS test structures tested @ INFN
DPTS paper: published
https://arxiv.org/abs/2212.08621
APTS papers: 2 in preparation (SF & OA)

Pixel Prototype Chips

APTS, DPTS, CE65

Variants of collection diodes

Variants of Front-End



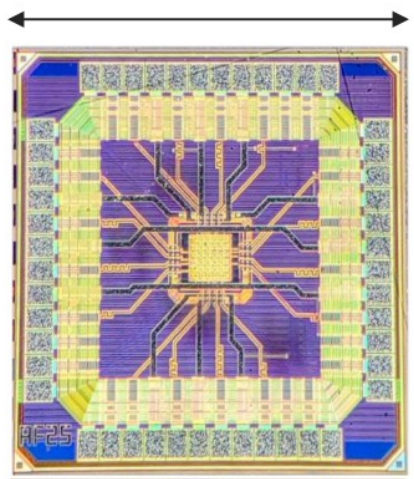
Front-End prototype

Charge Shaping Amplifier

Process Optimisation

Increase margins on sensing performance

Silicon proven pixels and DPTS front-end used as basis for stitched chip sensors in ER1



EP R&D

APTS

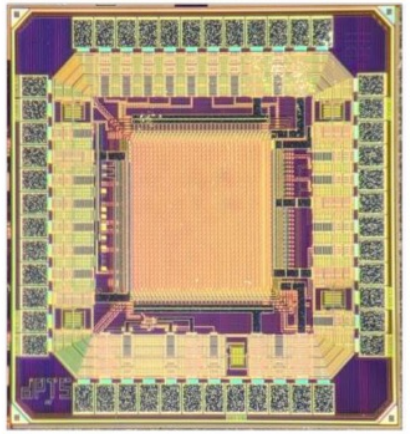
4x4 pixel matrix

10, 15, 20, 25 µm pitches

Pixel variants

Direct analogue readout

tested @ INFN



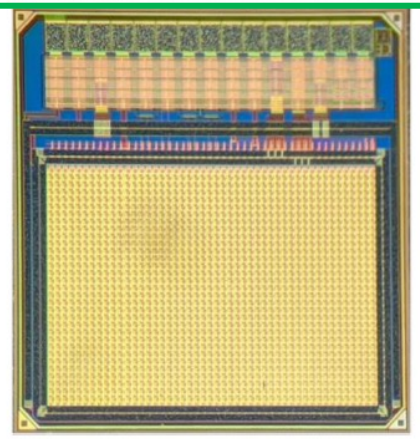
DPTS

32 × 32 pixels

15 µm pitch

Asynchronous digital readout

ToT information



CE65

64 × 32, 15 um pixels

48 × 32, 25 um pixels

Rolling shutter analog readout

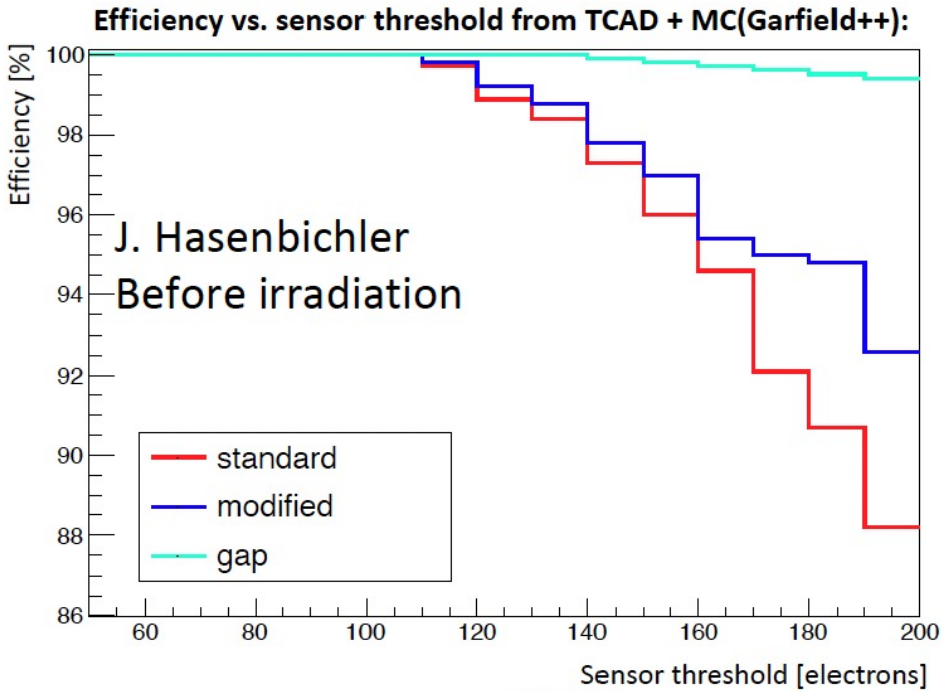
3 pixel front-end architectures

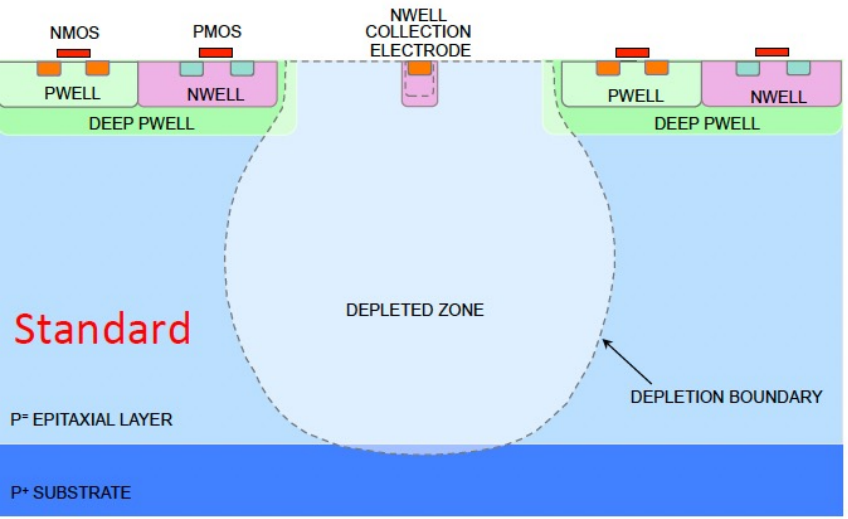
SPLITS for Multi Layer per Reticle MLR1

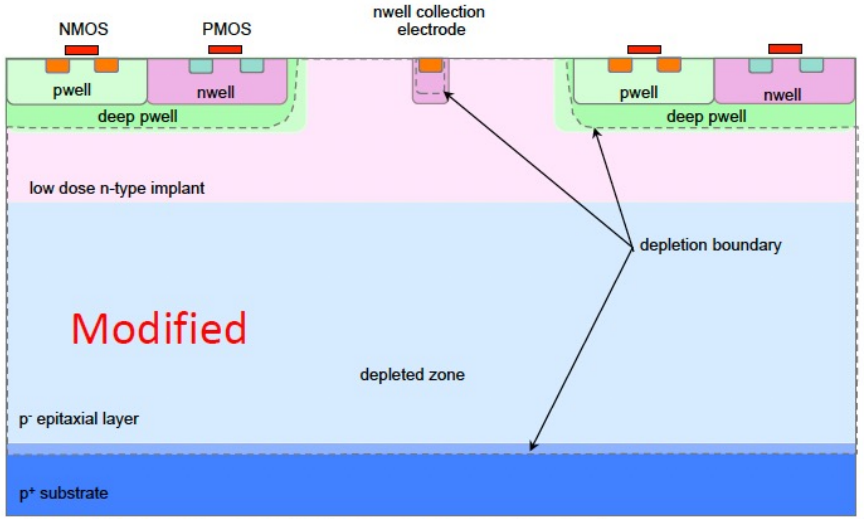
applying same optimization principles to 65 nm as in 180 nm

- 4 process splits, 3 wafers each
  - **Split 1: default process**
  - Split 2: first intermediate process
  - Split 3: second intermediate process
  - **Split 4: optimized process**
- 3 main pixel designs implemented in all splits
  - Standard similar in all splits, Modified, Gap

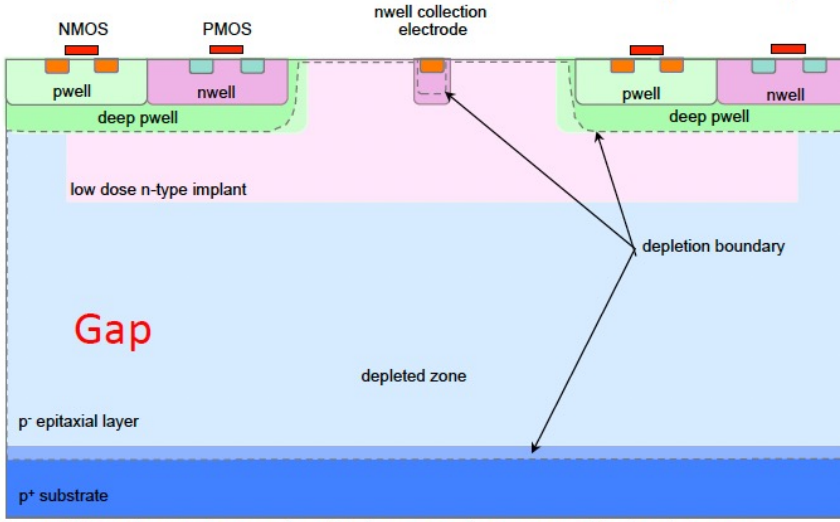
modifications more needed in 65 nm for good charge collection.







https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

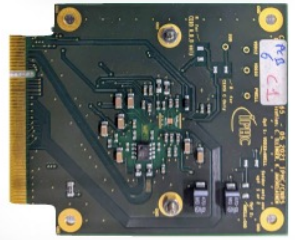
Charge collection speed

Charge sharing

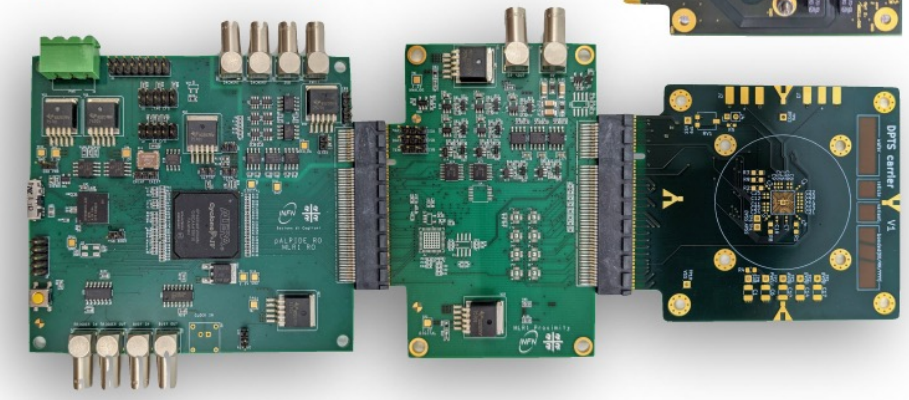
Readout system

ITS3 development

developed @ INFN CA-TO-TS (85k€ in 2021)



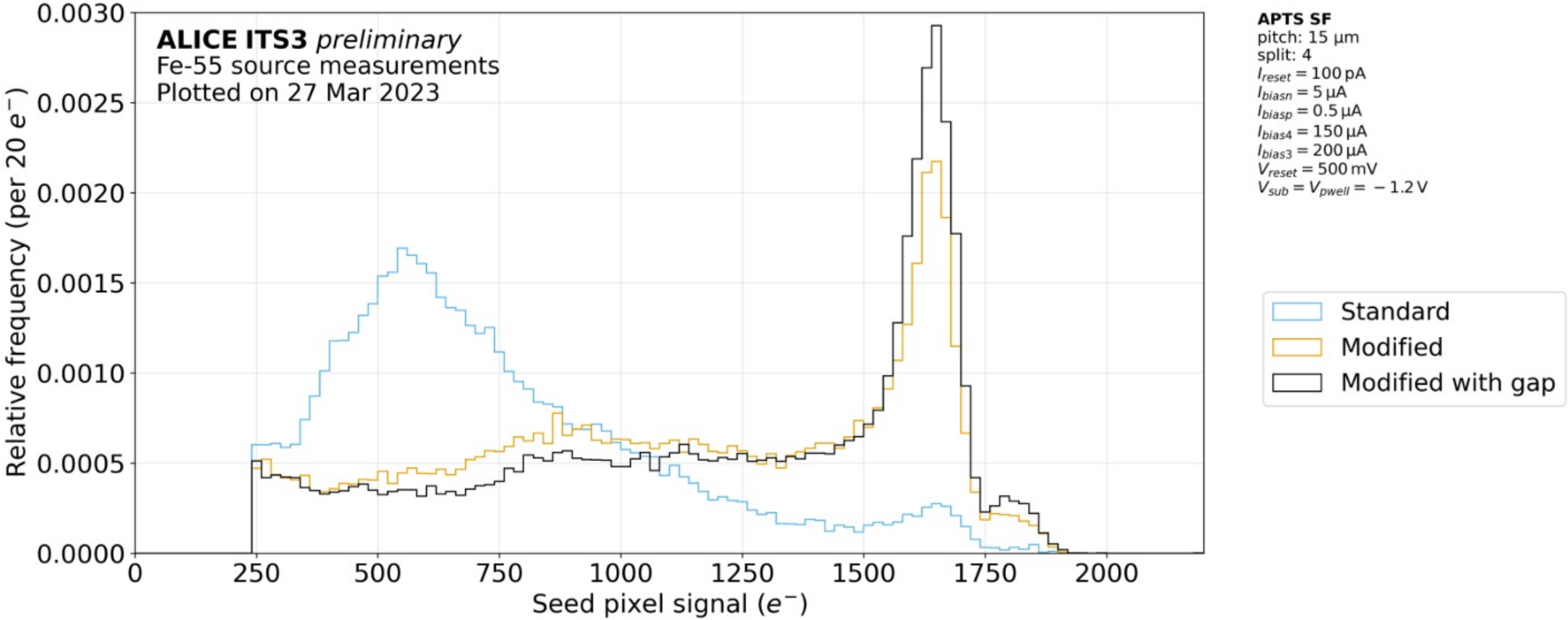
- Adaptation of existing readout system based on the DAQ boards that were used for ITS2 and ALPIDE
  - compatible with existing ALPIDE telescopes
  - affordable
- Newly produced proximity boards allow to set biases and read analog signals
- Uses simple chip carriers that are produced in large quantities (few hundreds)
  - essential to study large parameter space
- Distributed to a number of institutes



CERN + INFN (CA, CT, TO, TS) + IHPC (Strasbourg): pilot sites
BA+BO+PD + Nikhef + Liverpool + Birmingham: extensive test sites

MLR1 selected results: APTS

Catania-Padova-Bologna

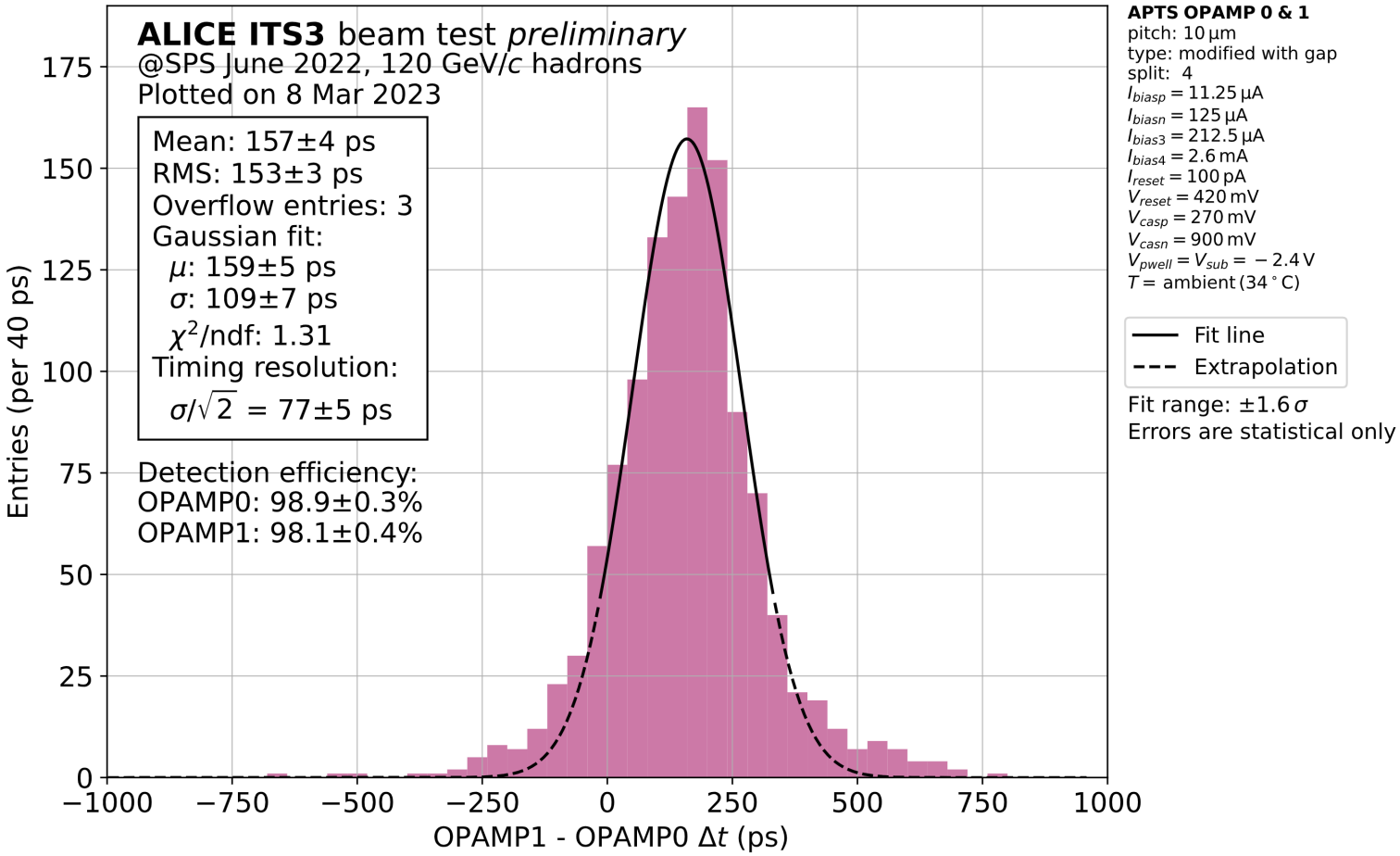


APTS SF: charge detection

Charge collection by the seed pixel is optimised in the “modified with gap” process

MLR1 selected results: APTS

Torino-Bari



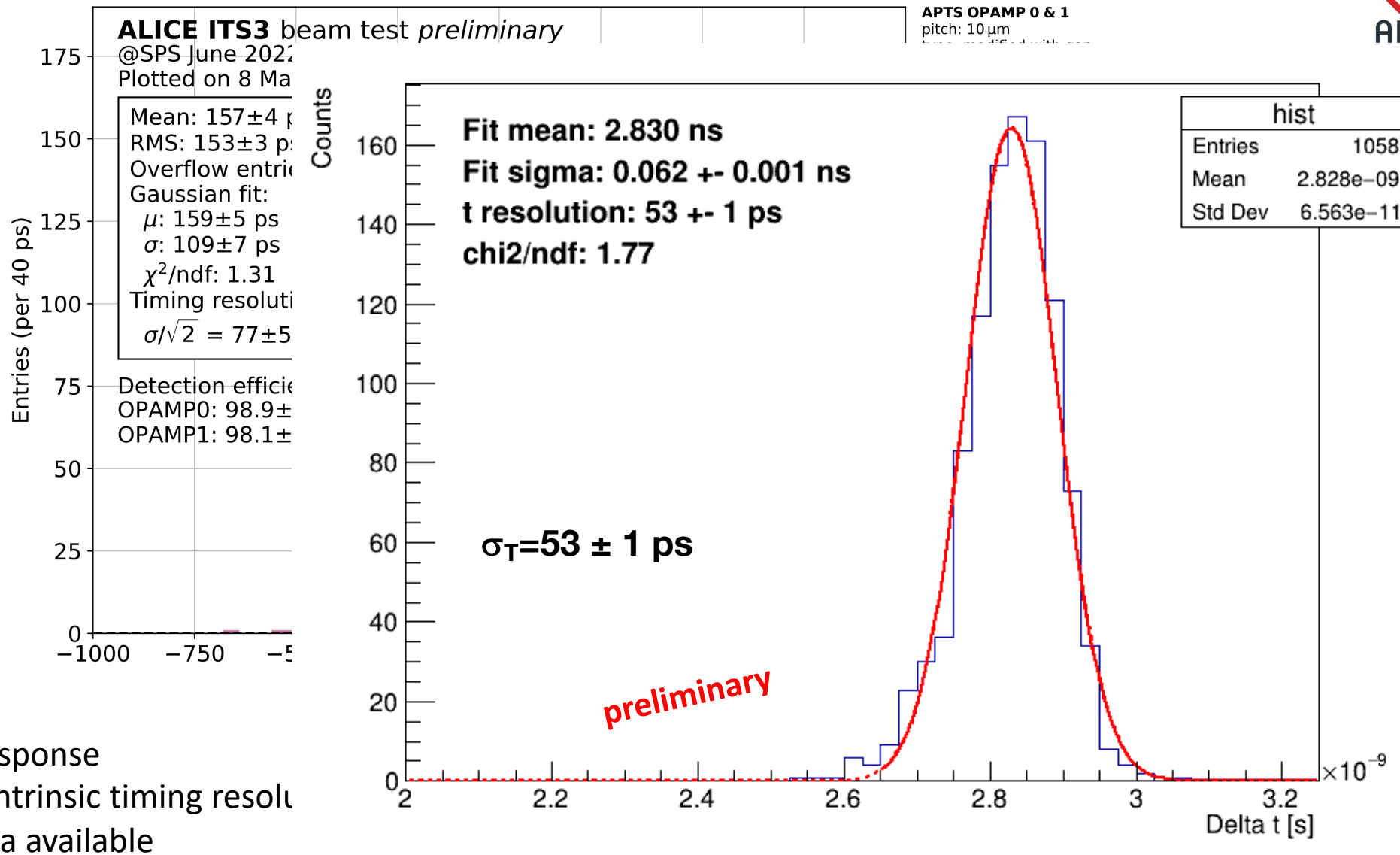
APTS OA: timing response

First results show intrinsic timing resolution below 80ps

New beam test data available, analysis ongoing

MLR1 selected results: APTS

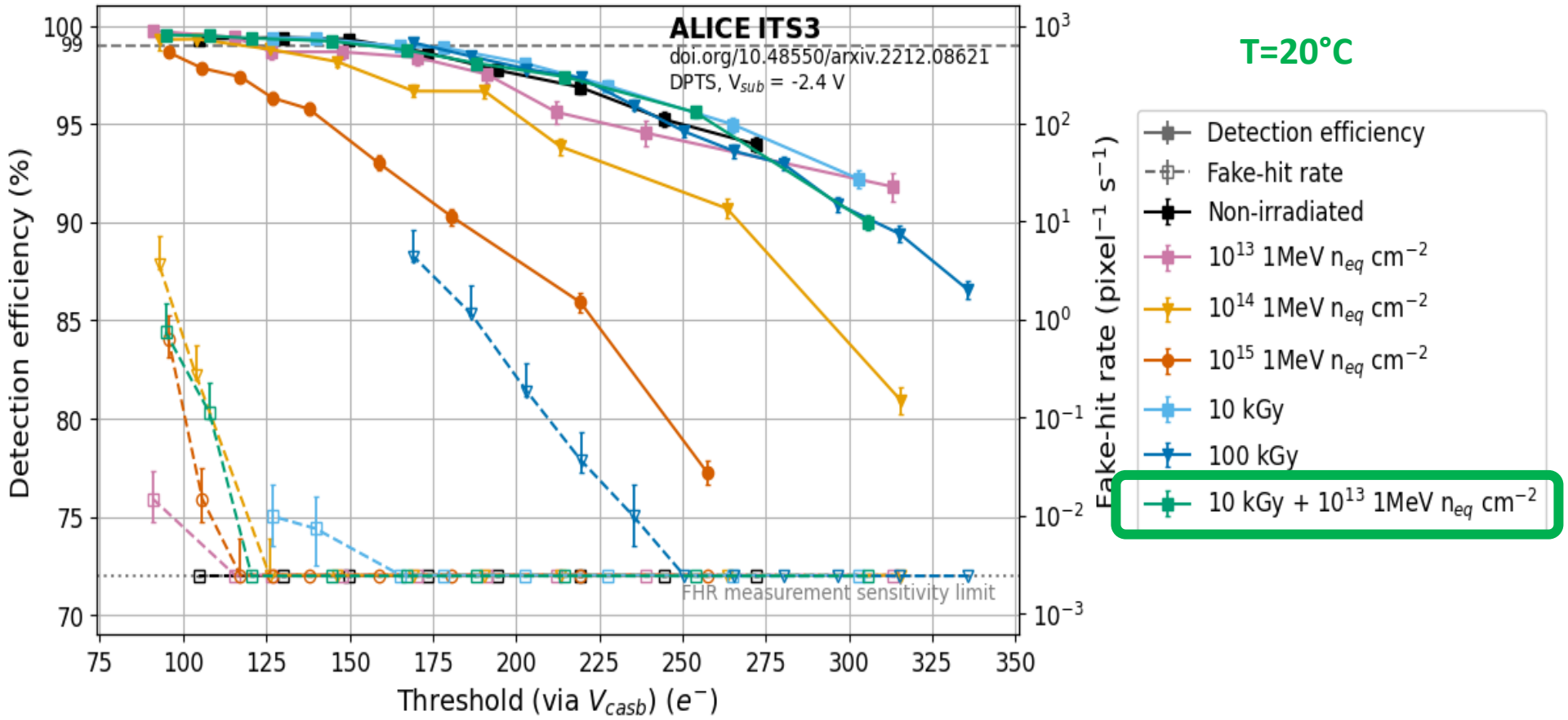
Torino-Bari



APTS OA: timing response
First results show intrinsic timing resolu
New beam test data available

MLR1 selected results: DPTS

Trieste



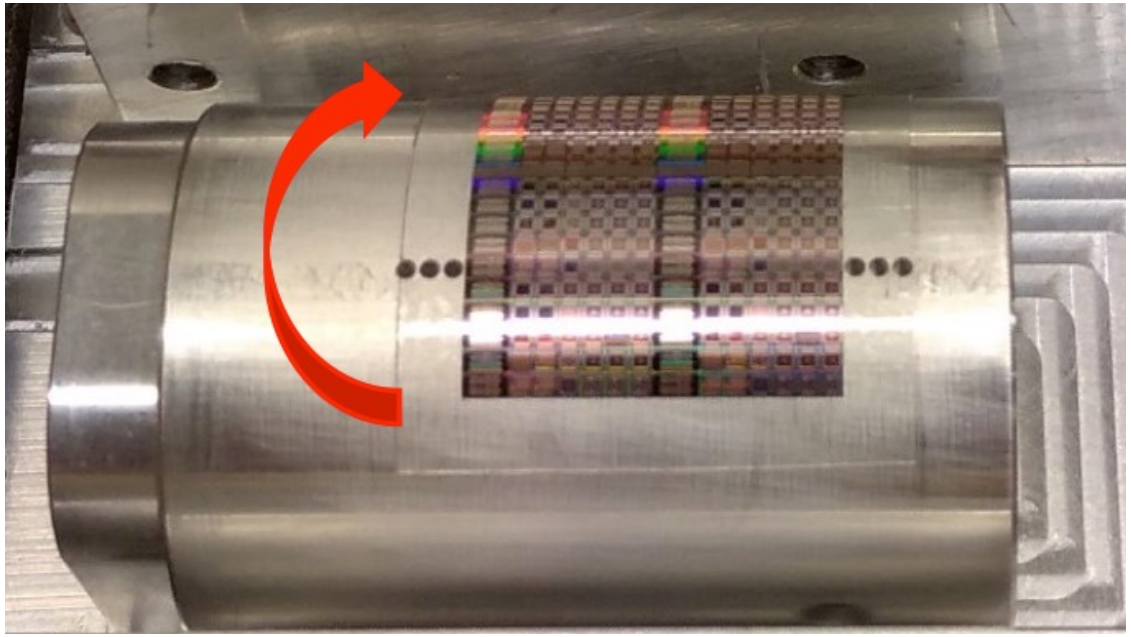
DPTS: radiation hardness

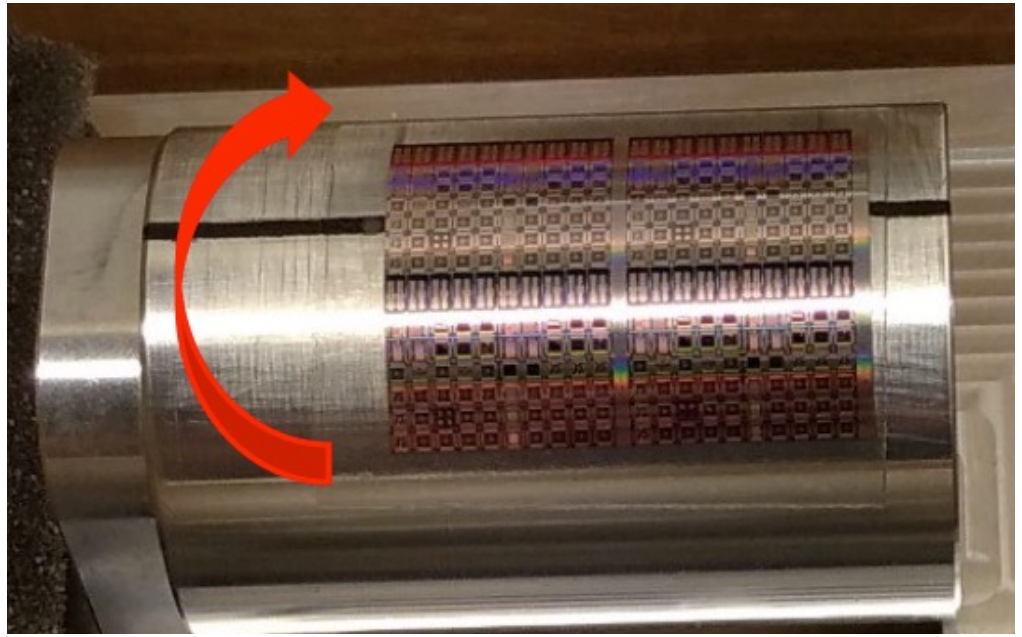
Detection efficiency well above 99%, in the desired threshold region, up to NIEL 10^{14} 1MeV n_{eq} cm^{-2}, with very low noise, at room temperature

Bent 65nm test structures

Trieste

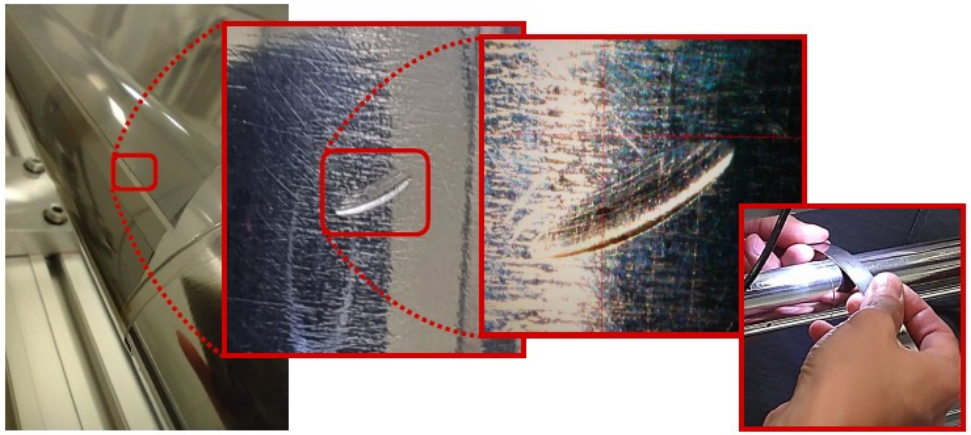
- Larger pieces from fully processed 65nm wafers are bent to R = 18 mm and electrically characterised
- They work nicely (tested with a Fe-55 source)
- More comprehensive study ongoing
- Very important cross-check: underlying CMOS processing is different in several aspects (ALPIDE, 180 nm vs MLR1, 65 nm)





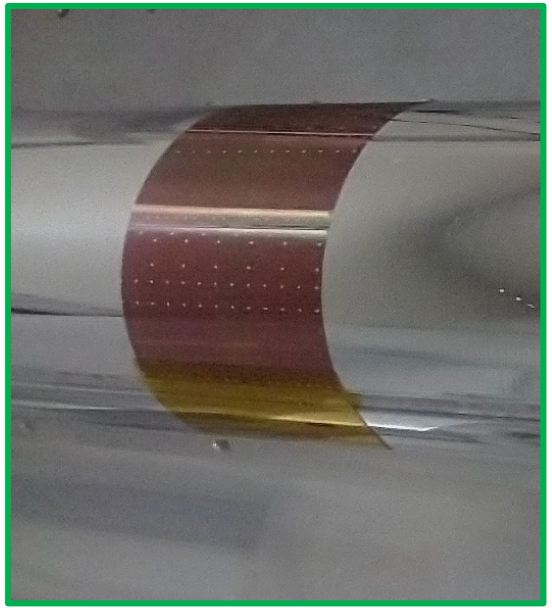
SuperALPIDE update

Bari



October 2022

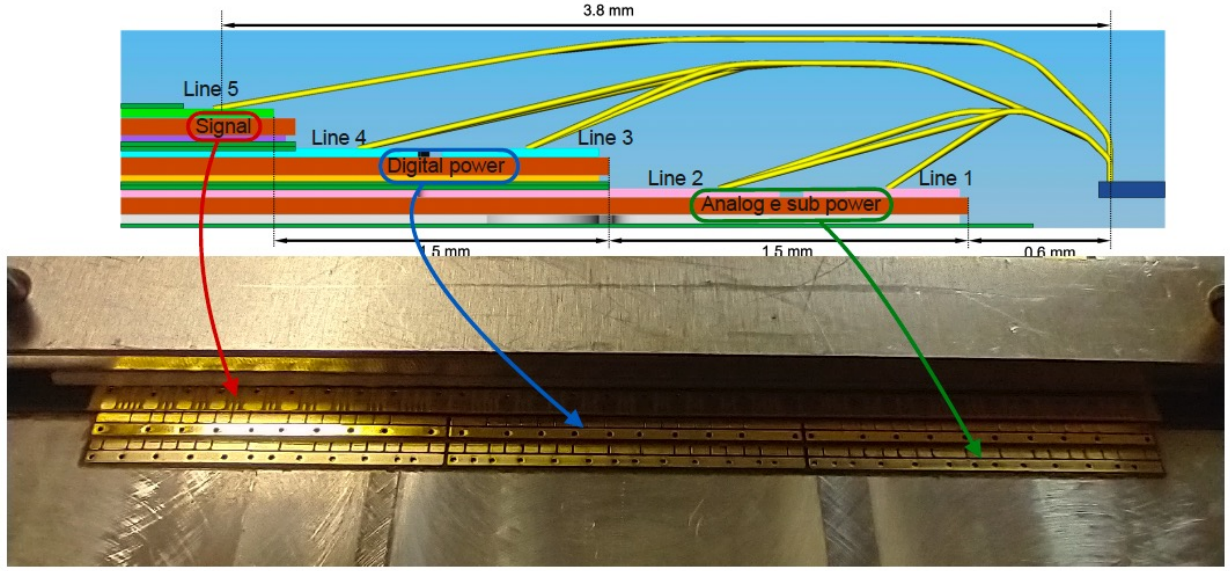
- Scratch found on the mandrel surface
- Improved by gently scrubbing
- At least 6 silicons, 40 µm thick, successfully bent

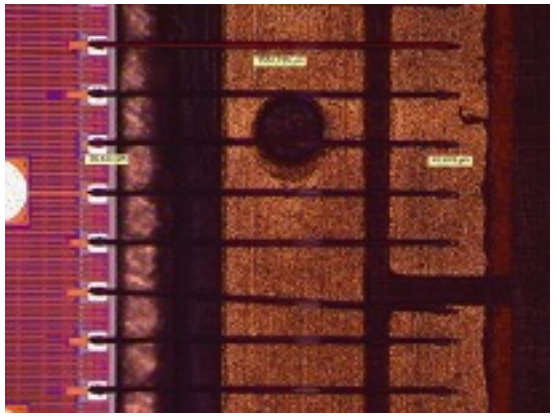


2023:

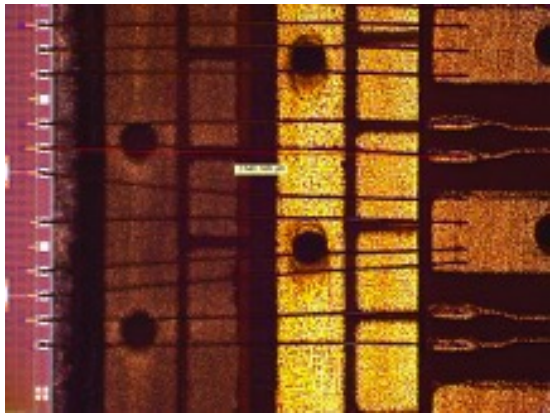
- Two bending attempts of recovered pieces of processed super-ALPIDE (30 µm thick) from break:
- 1. In the scratch region (silicon size: ~4.7 cm, ~2.5 cm) → Success!
- 2. Outside of the the scratch region (silicon size: ~1.5 cm, ~6.2 cm), longitudinal bending → Success!

Wire bonding to edge FPC

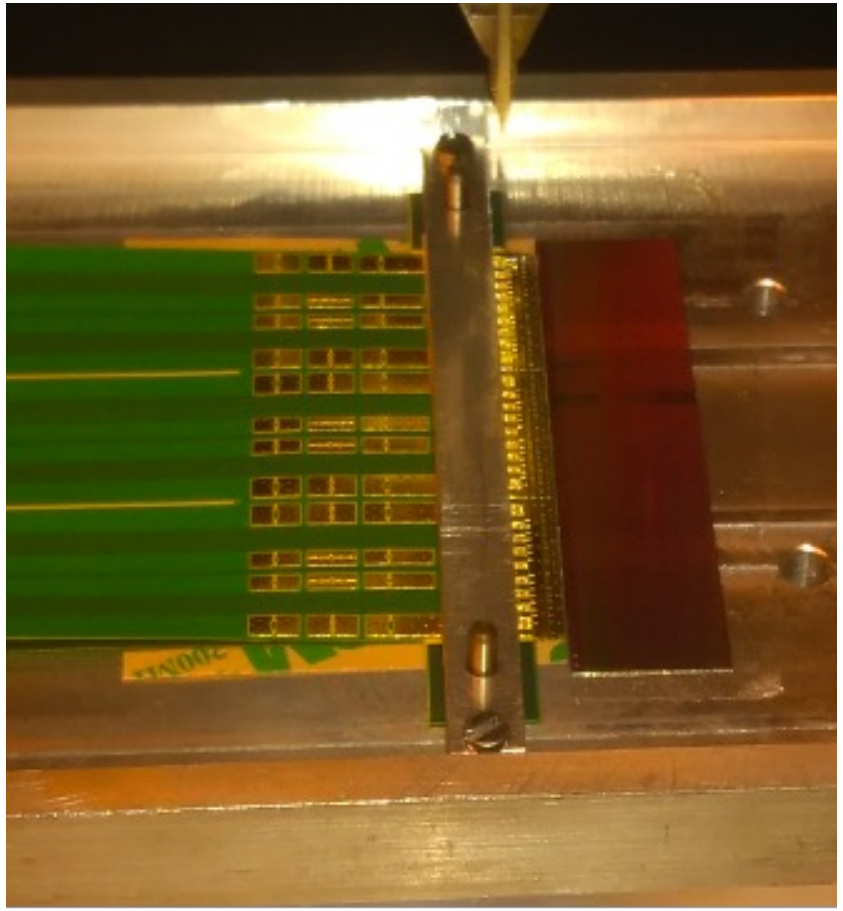




Bottom layer, line 2, wire examples



Upper layer, line 5, wire examples



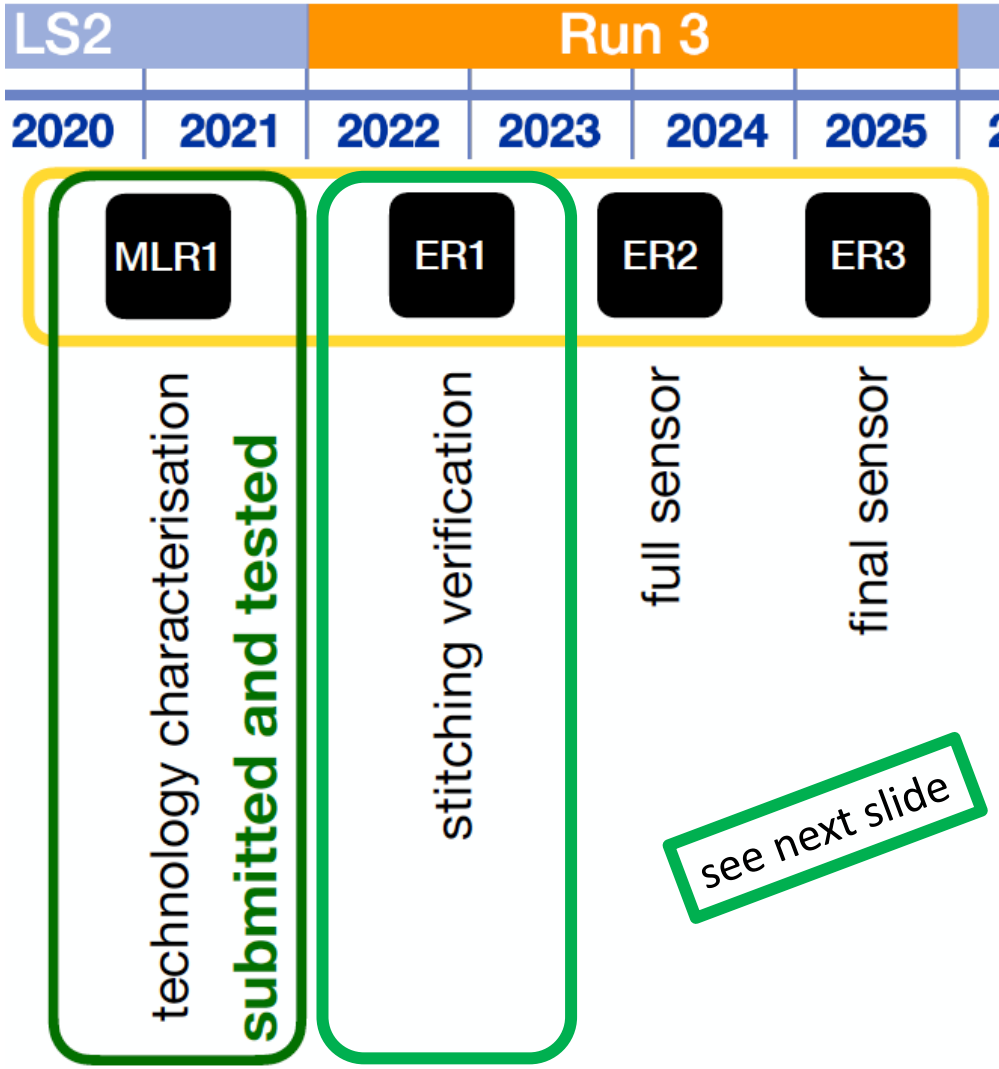
Two ALPIDE sensors used as ITS3 sensor simulator

500 µm distance between FPC and sensor

Towards the wafer-scale sensor

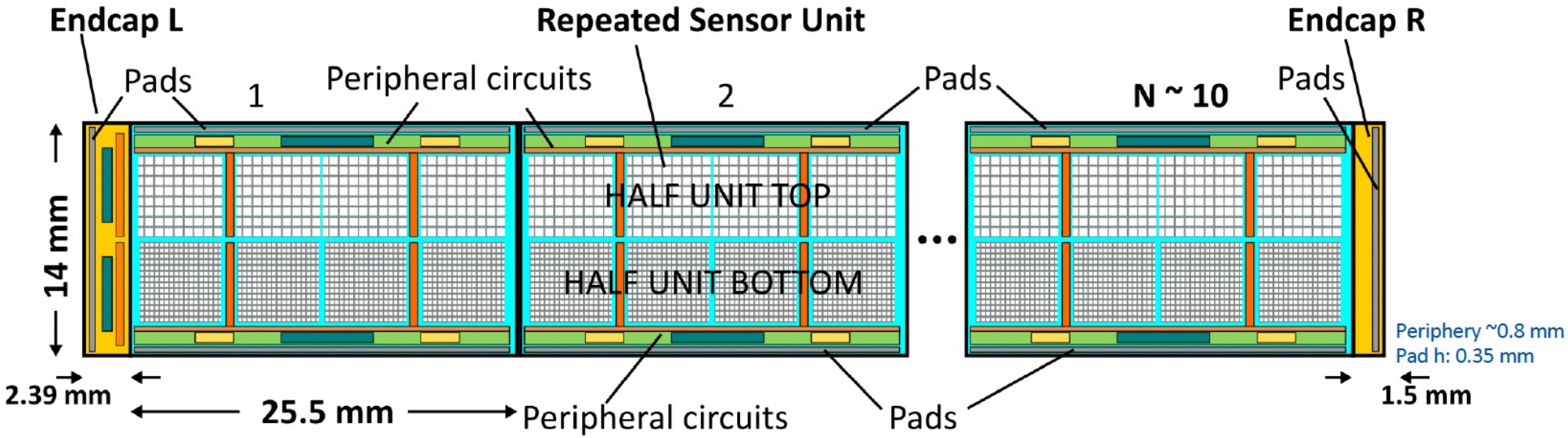
timeline (ITS3/LHC)

ER1



- **MLR1:** technology qualification
  - charge detection
  - radiation hardness
- **ER1:** stitching prototype
  - first time stitching is done in HEP
  - different defect mitigation strategies
  - stitching in one direction
- **ER2 + ER3:** final size (2D) stitched sensor

MOSS Monolithic Stitched Sensor Prototype



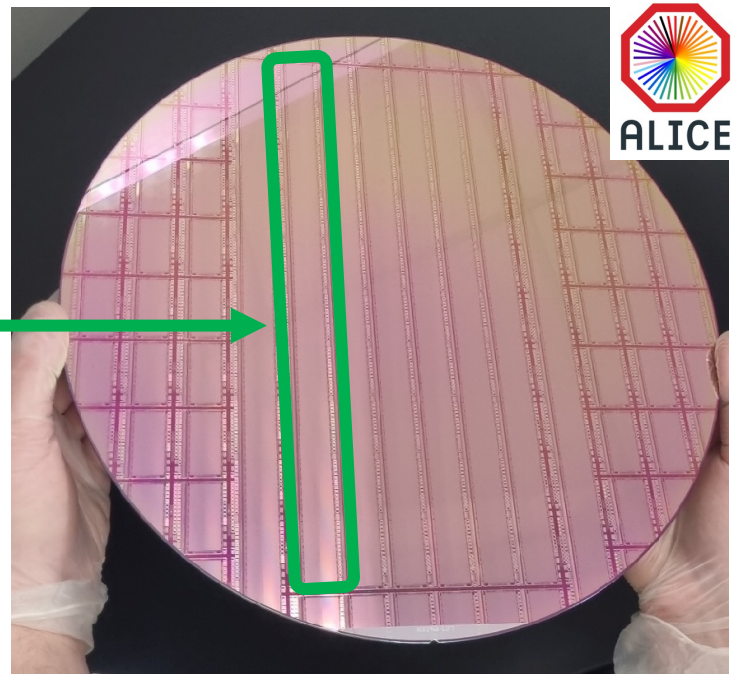
Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

Repeated units abutting on short edges

- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

ER1: wafer-scale sensors

- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips
- **"MOSS": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm^2)**
  - **conservative design, different pixel pitches**
- "MOST": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm^2)
  - more dense design
- Plenty of small chips (like MLR1)



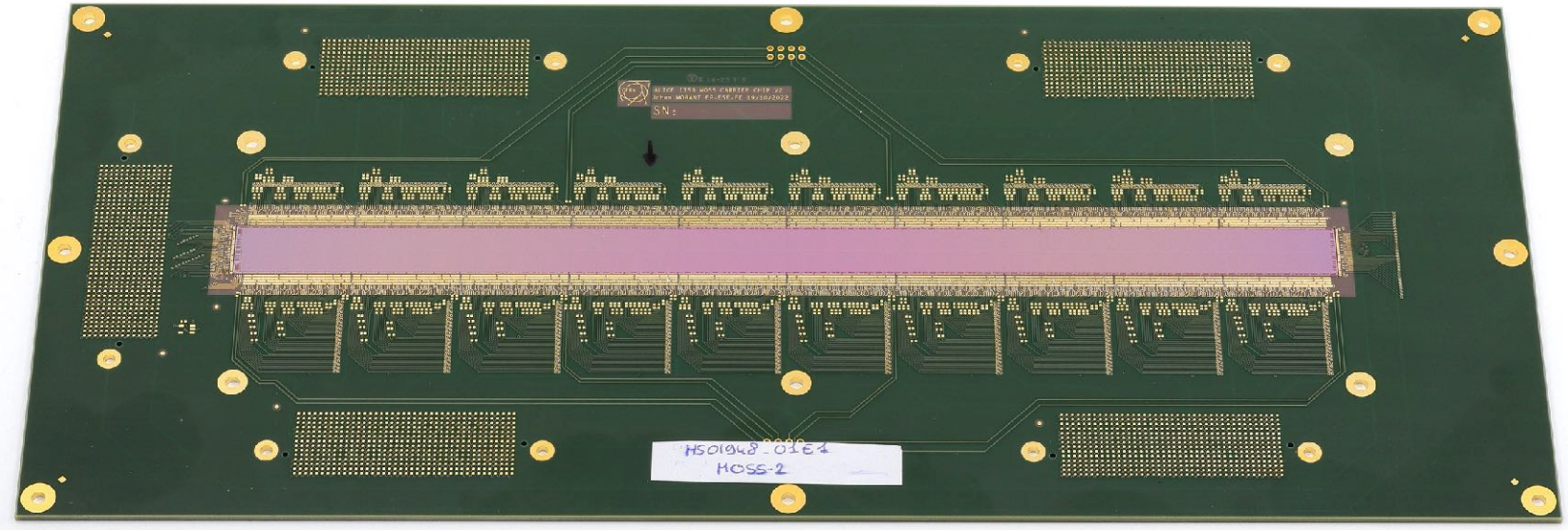
STATUS

‣ **Production:** Both pad wafers and **fully processed** wafers **are available @CERN since end of May**

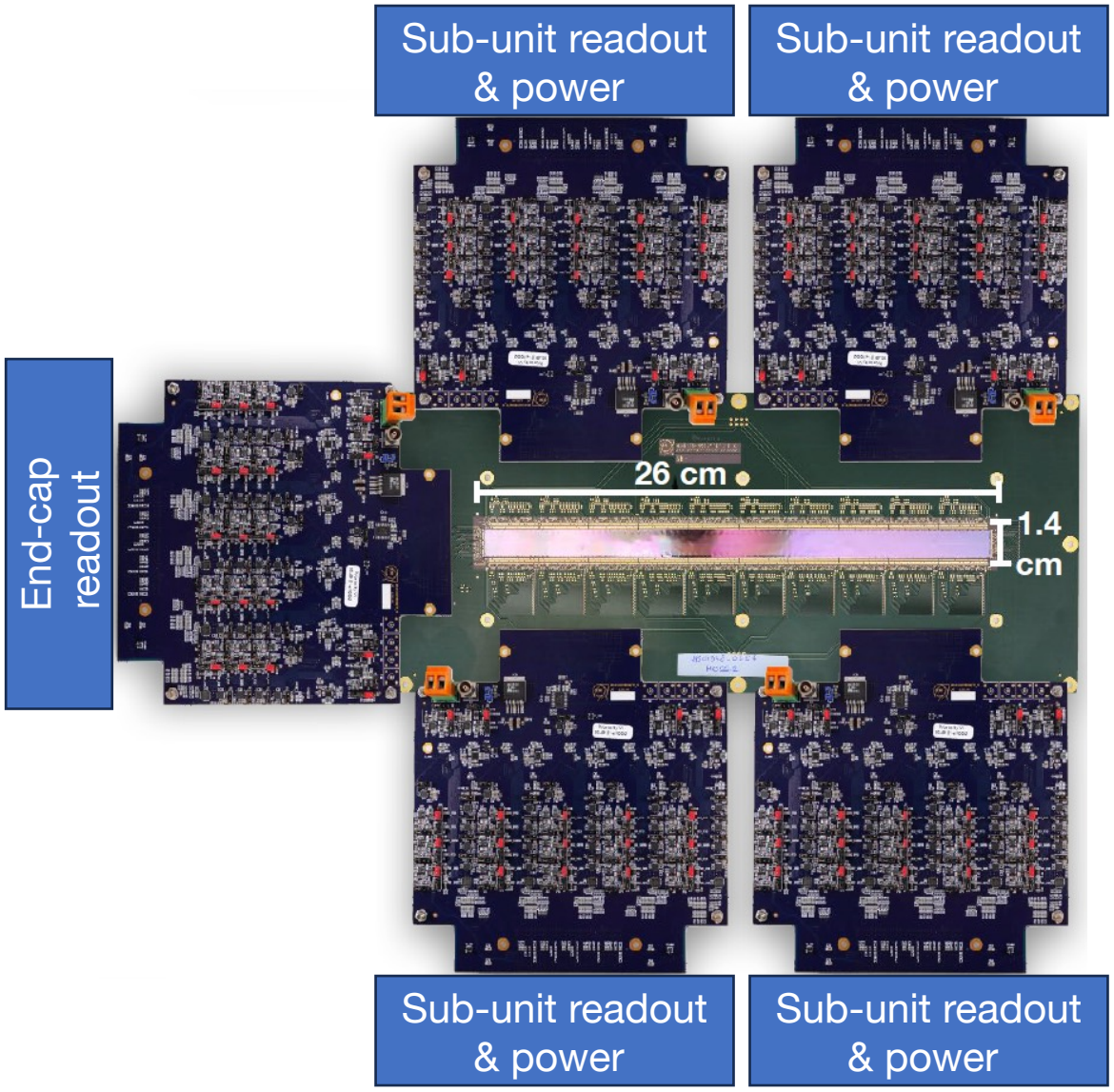
‣ **Thinning and dicing:**

- **done** for large chips (first 2 wafers), in preparation for small chips

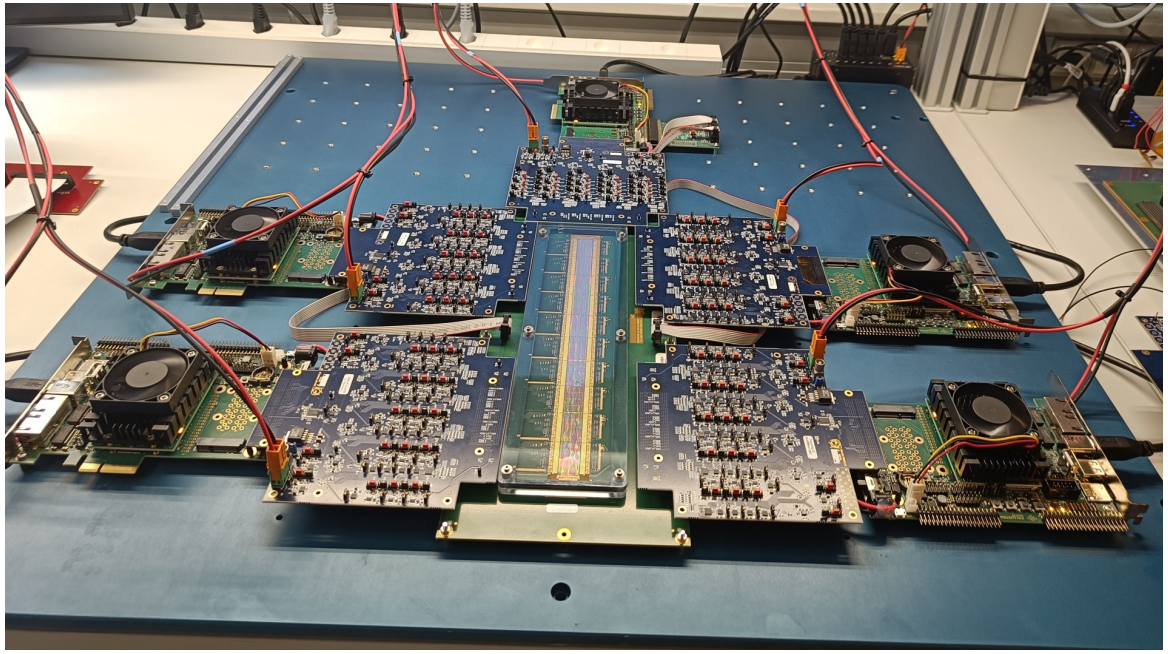
TESTING: see next slide



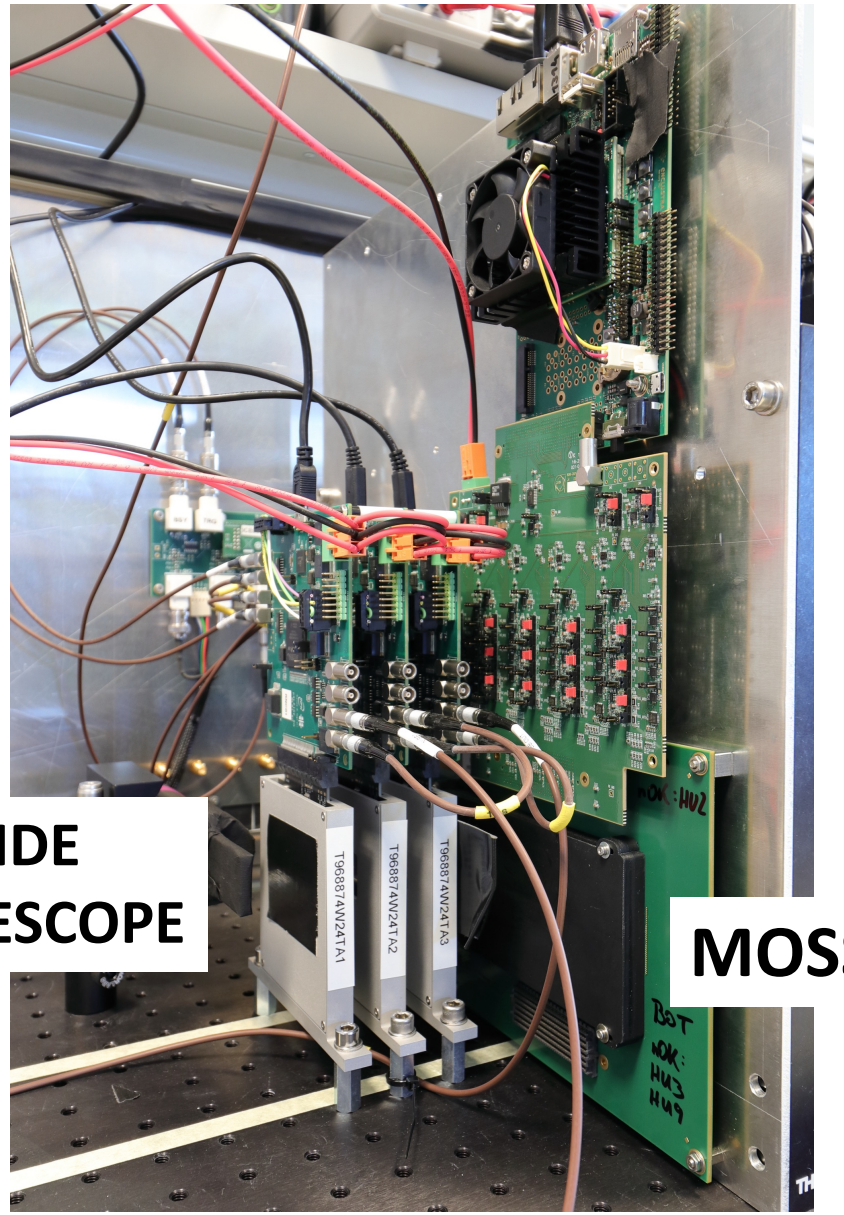
Bonded sensor tests in laboratorio

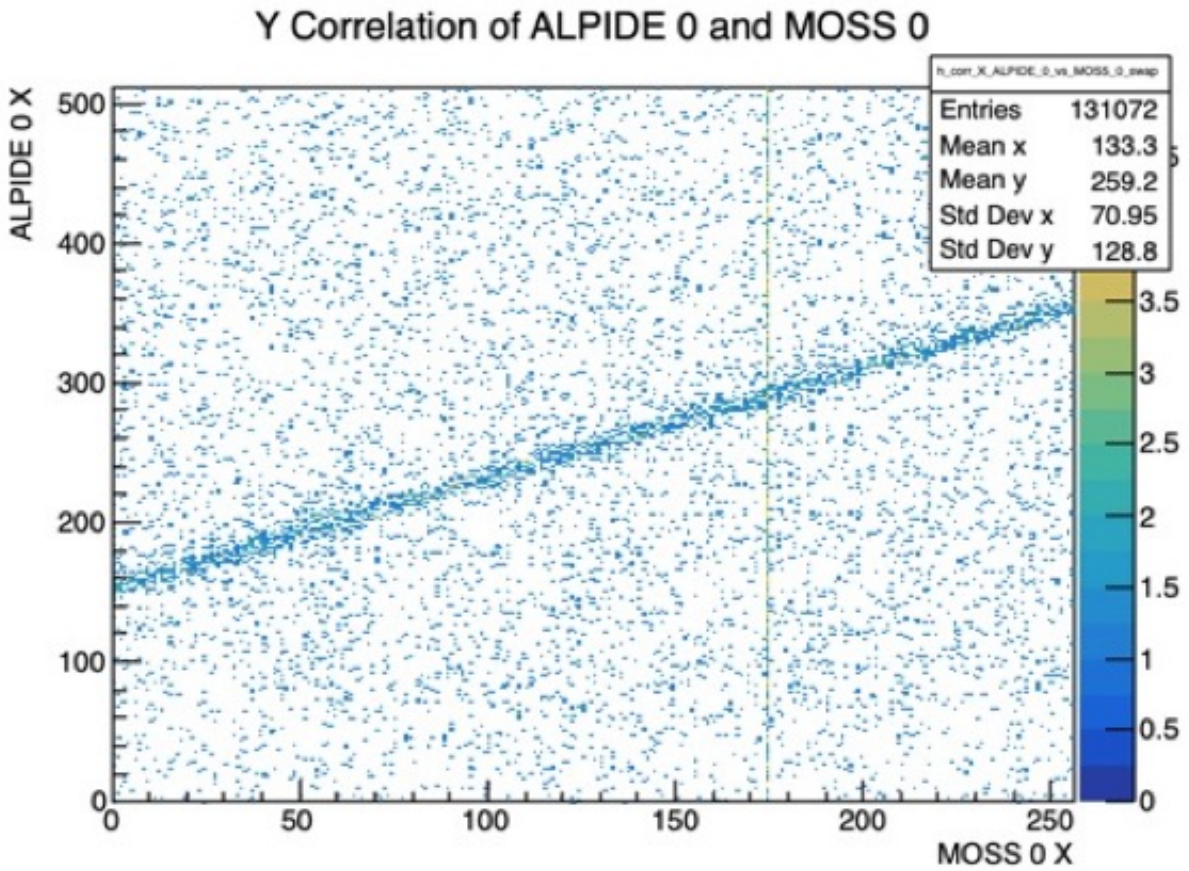


- 1 MOSS bonded
- 20 sub-units ≅ 20 ITS2 chips
  - Each sub-unit can be tested independently
- 16 sub-units tested (4 are not connected to this set-up)
  - 16 powering → no shorts!
  - 16 responding to register access
  - 1 tested for readout and working as expected!



MOSS beam test: primo test su fascio disensore large area





Primissimi risultati da beam test

What next

ER2 Stitched Sensor

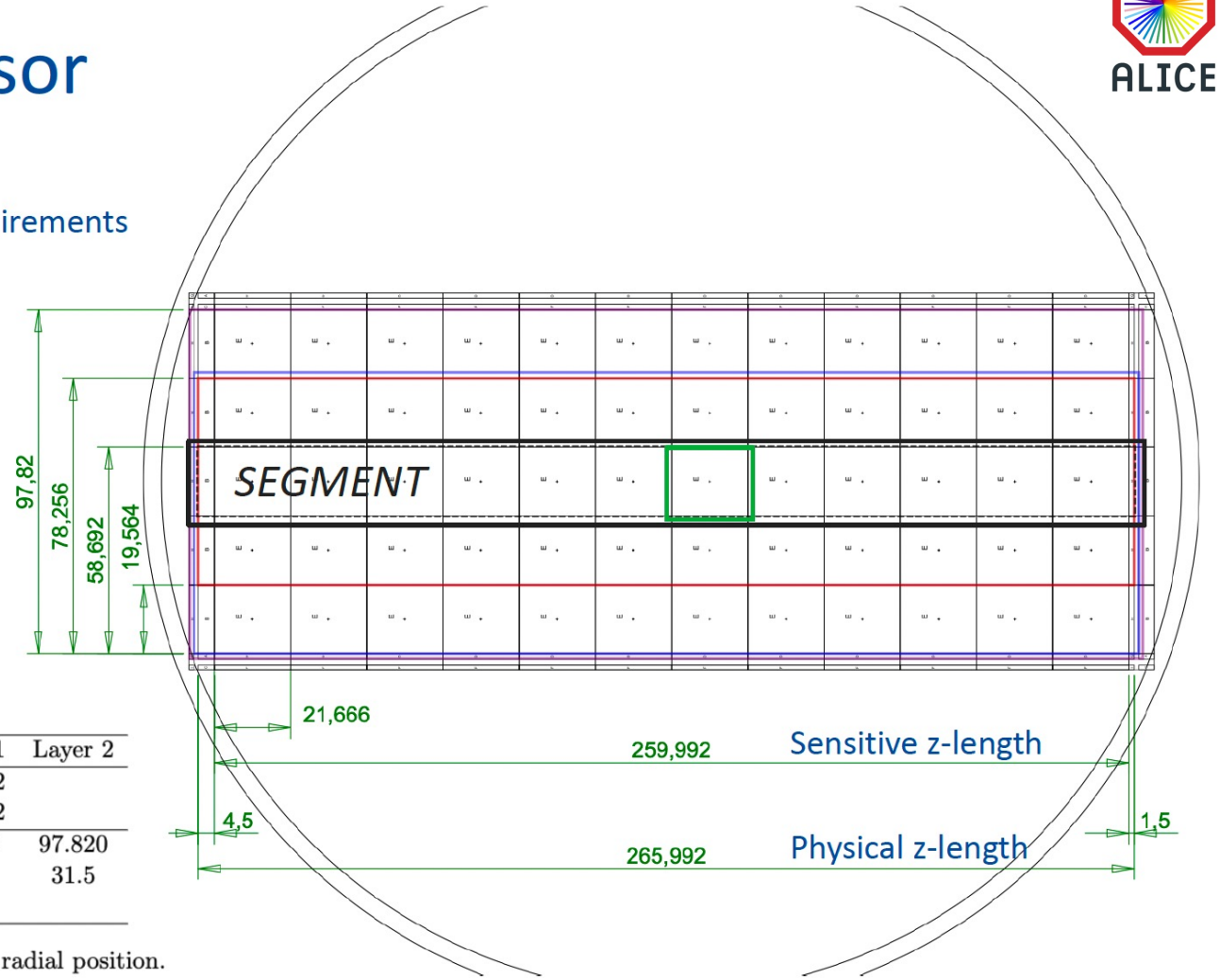
ER2 Sensor aims to meet the ITS3 requirements

Layer 0: 12 x 3 repeated units+endcaps

Layer 1: 12 x 4 repeated units+endcaps

Layer 2: 12 x 5 repeated units+endcaps

Repeated (Stitched) Sensing Unit

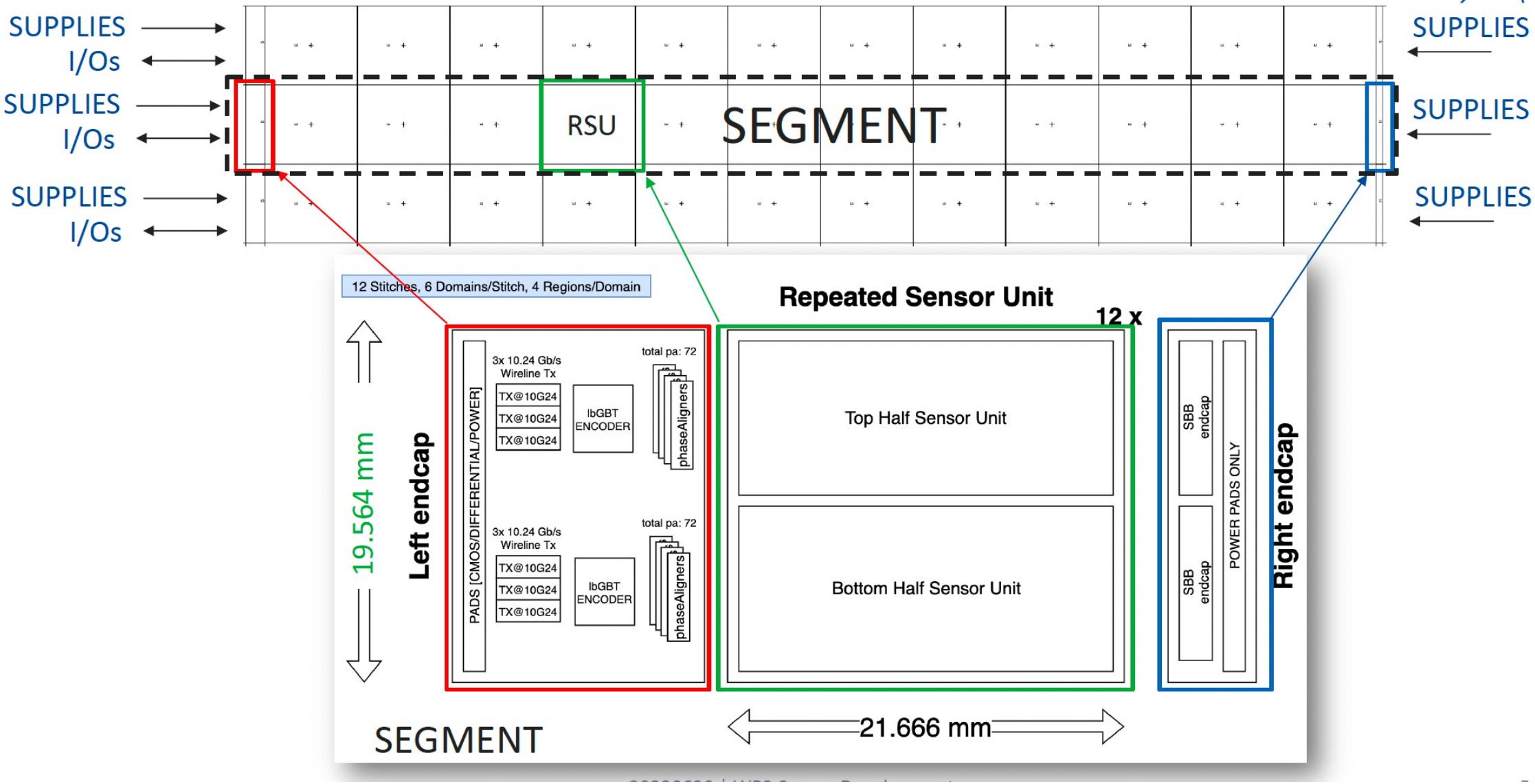


AZIMUTHAL WIDTH UPDATED

IB Layer Parameters	Layer 0	Layer 1	Layer 2
Sensor length [mm]		265.992	
Sensitive length [mm]		259.992	
Sensor azimuthal width [mm]	58.692	78.256	97.820
Radial position [mm]	19.0	25.2	31.5
Equatorial gap [mm]		1.0	

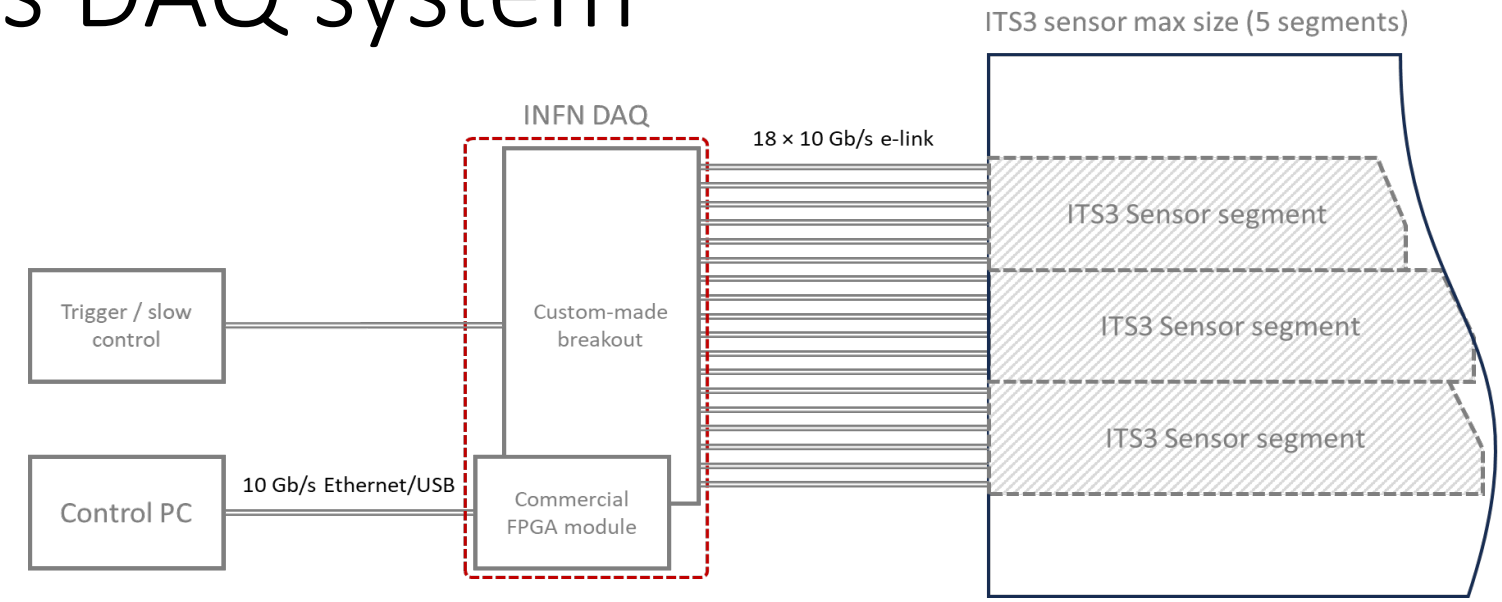
Table 3.2: Design dimensions of the sensor dies and radial position.

Top Integration Diagram



Large area sensors DAQ system

Bari, Cagliari, Padova, Trieste



Proposal: **table-top like DAQ system** capable of

- reading (through high-speed e-links)
- controlling (through slow lines)

Considering the size and number of outputs of an ITS3 sensor (12x3 minimum repeated single sensing unit)
it is foreseen using a few boards in parallel to read a full sensor, where data are aggregated on the back-end computer through standard ethernet/USB link topology.

GOAL: responsabilità INFN su sistema di lettura di ITS3 like sensor, per portare in Italia il test set-up e i sensori large area
Interesse sinergico con ALICE3 tracker, EIC, NA60+

ITS3 attività INFN

2023:

- WP2: Design e sottomissione ER2 sottomissione rimandata a inizio 2024 (contributo INFN 250k€)
- WP3: Test di strutture bent + large area (sviluppo di nuovo test system per MOSS chip); caratterizzazione di strutture irraggiate
- WP4: continuazione attività bending e bonding su strutture bent di piccola e grande area
- WP5: studio di materiali per supporti e cooling

FINE 2023: pubblicazione ITS3 TDR -> fondi CORE

*contributo CORE al progetto: suddivisione di compiti e contributi inclusi in tabella TDR

2024

- WP2: Sottomissione ER2 (MOSS2: ITS3 compliant sensor e nuova versione test structures)
- WP3: sviluppo di sistema di read-out per MOSS2*
- WP4: continuazione attività bending e bonding su strutture bent di grande area, test di FPC e interconnessioni
- WP5: produzione di supporti per replica ITS3*

OVERVIEW RICHIESTE ITS3 2021-2025

tipo attività	2021 (k€)	2022 (k€)	2023 (k€)	2024 (k€)	2025 (k€)	2026 (*)?	totale richiesta INFN (k€)	totale ITS3 (k€)
R&D	200	300	150 WP3=100 WP4+5=50				700 (**)	2500
Costruzione (CORE)			ER2: 250	400	400	100	1100	3500
totale	200	300	400	400	400	100	1800	6000
viaggi			50	50				

RICHIESTE ITS3 2024

tipo attività	2024 (k€)
R&D	0
Costruzione (CORE)	400
totale	400
viaggi	50

Richieste 2024: Core (k€)	Destinazione	Sede
330	sottomissione ER2+ER3 e thinning and dicing	Torino
60*	large area sensor read-out setup	Padova
10*	bending mandrels	Bari

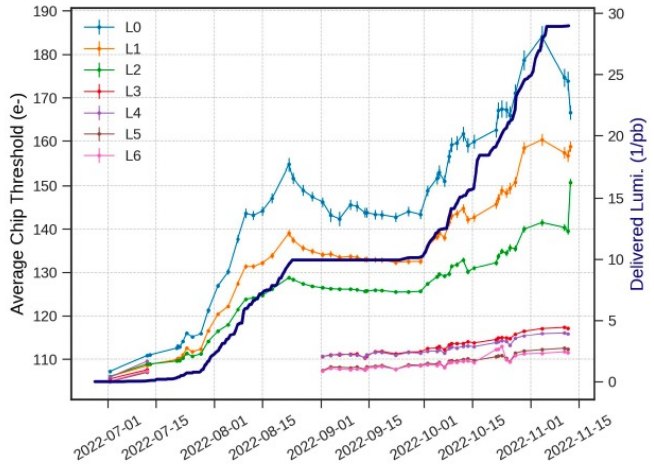
le richieste * devono essere formalmente confermate dal management ITS3

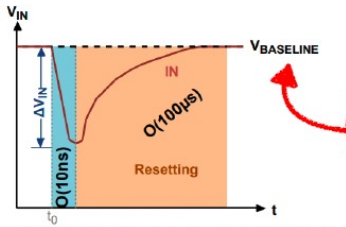
Richieste 2024: Viaggi	Destinazione	Sede
50	Test Beam e Test MOSS @ CERN	BA, BO, CA, CT, PD, TO, TS

BACKUP SLIDES

Detector ageing: under control

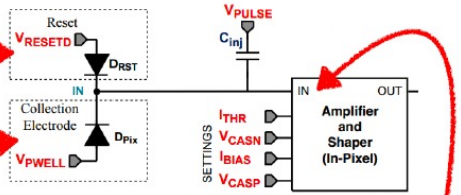
- Q3-Q4 2022
  - Constant settings from late June to October
  - **Threshold monotonously increasing** with radiation load
  - Tuning to **100 e⁻** was **no longer possible**: could this become an issue?
  - Thorough investigation started[1]
- End of 2022 (YETS)
  - **Discrepancy** found in resulting calibration using surface commissioning tools
  - Pixel reset voltage **V_{RESETD}** configuration prevented the correct functioning





Voltage excursion during charge collection (blue) and resetting (orange)

Baseline of V_{IN} depends on V_{RESETD} and the leakage current in the pixel



Input section of the ALPIDE Front-End

Pixel leakage current increased by NIEL

Transistor properties altered by TID

Working range found to be shifted to higher V_{RESETD}

[1] Detailed explanation in this talk

ER1 Submission

August 2022

EP R&D

Aim: learn and prove **stitching**

Two large *stitched* sensor chips (MOSS, MOST)

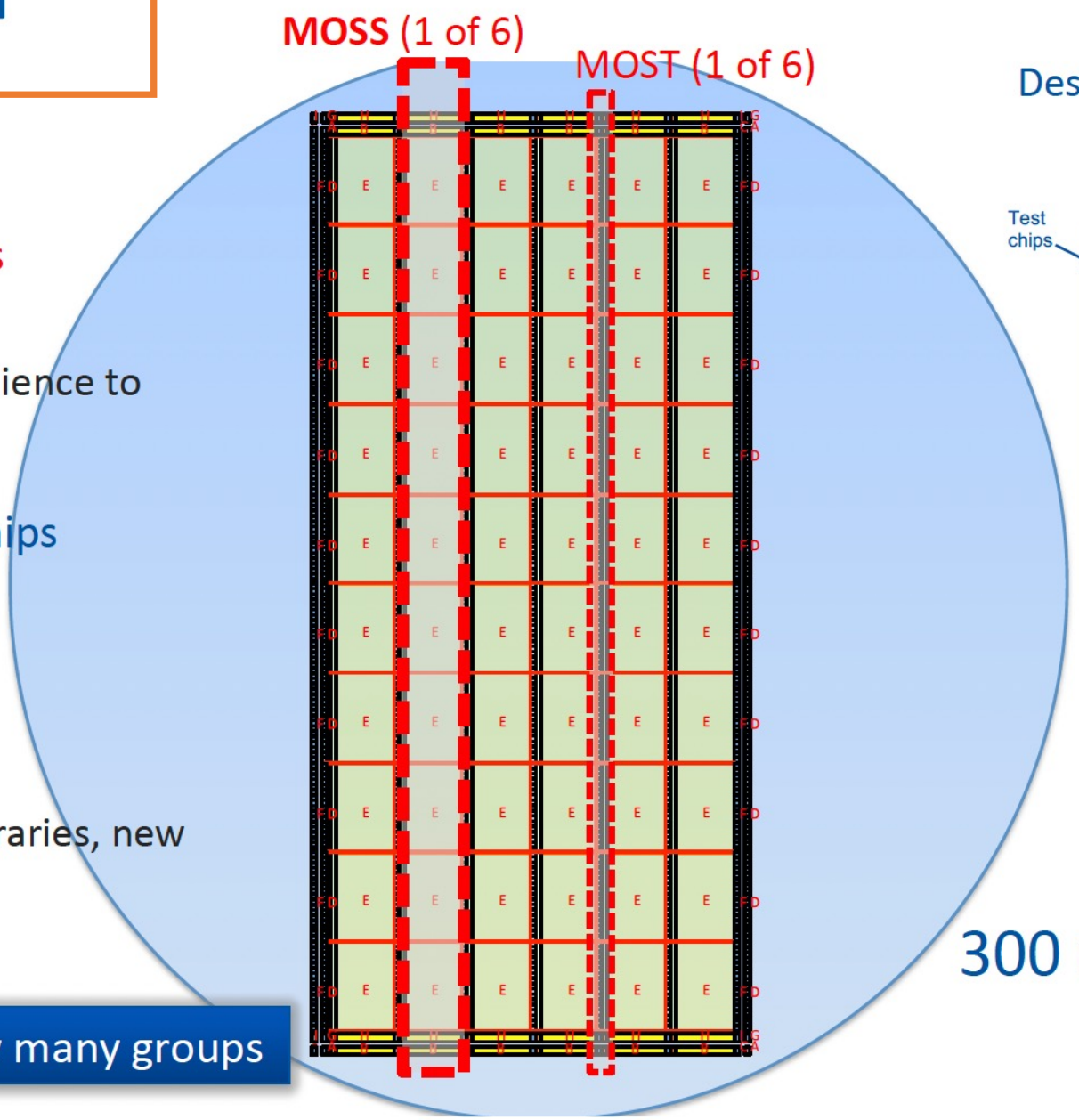
- Different approaches for resilience to manufacturing faults

Small test and development chips

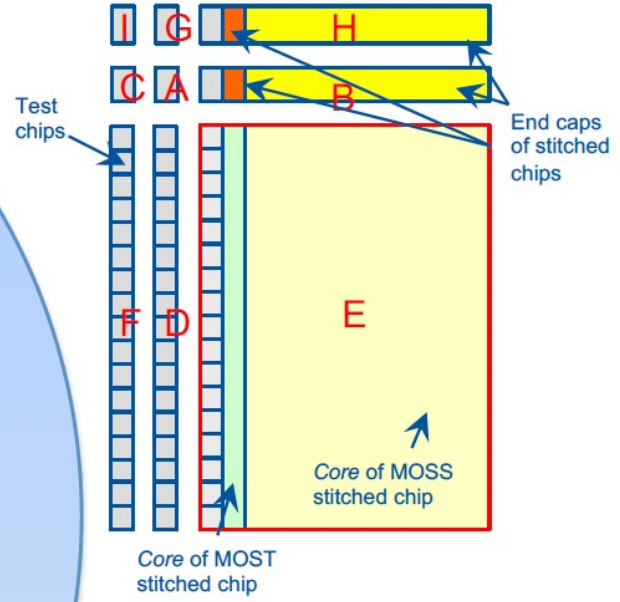
- Pixel Prototypes
- Fast Serial Links

Technology and Support

- New metal stack, new I/O libraries, new PDKs



Design Reticle



300 mm wafer

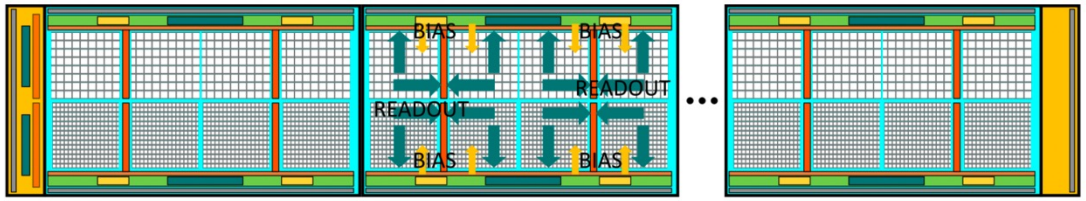
Intense design effort shared by many groups

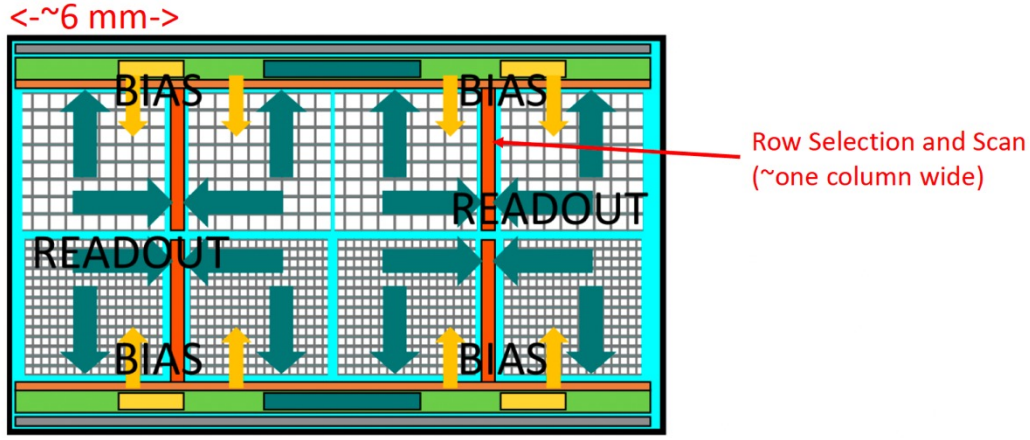
MOSS: Monolithic stitched sensor

First large are sensor designed for high energy particles detection → main goal:

- test basic features of designing with stitching and aspects like yield

DESIGN DI INTERESSE COMUNE A:
ALICE
NA60+
EIC





Basic subsensor unit 25 m long, replicated 10 times through stitching, for an o length of about 25 cm

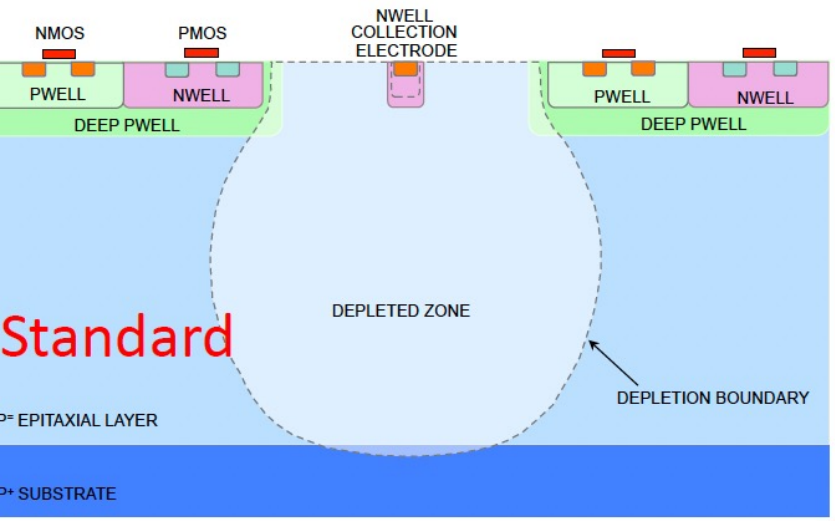
Readout architecture and powering:

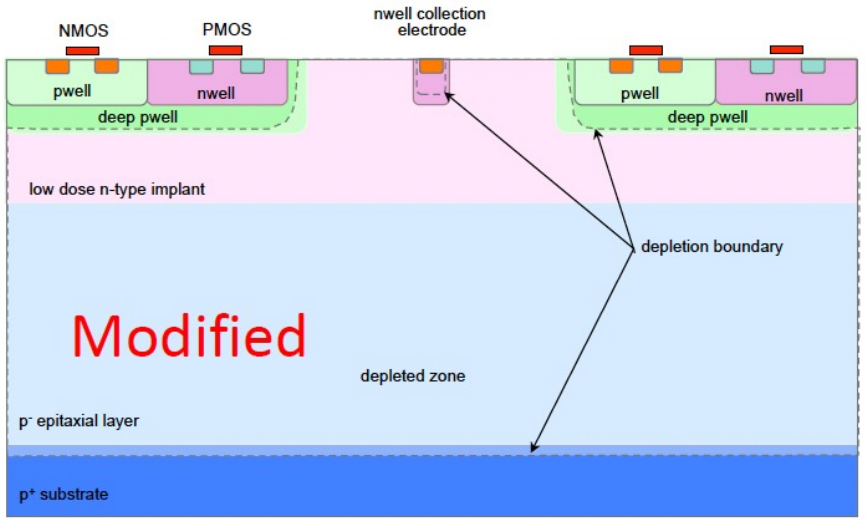
- readout performed locally independently for each subsensor and also from left end as foreseen for ALICE ITS3 (simple parallel ports, no high speed serial links)
- separate powering for each subsensor →minimize shorts affecting the others

Process modifications

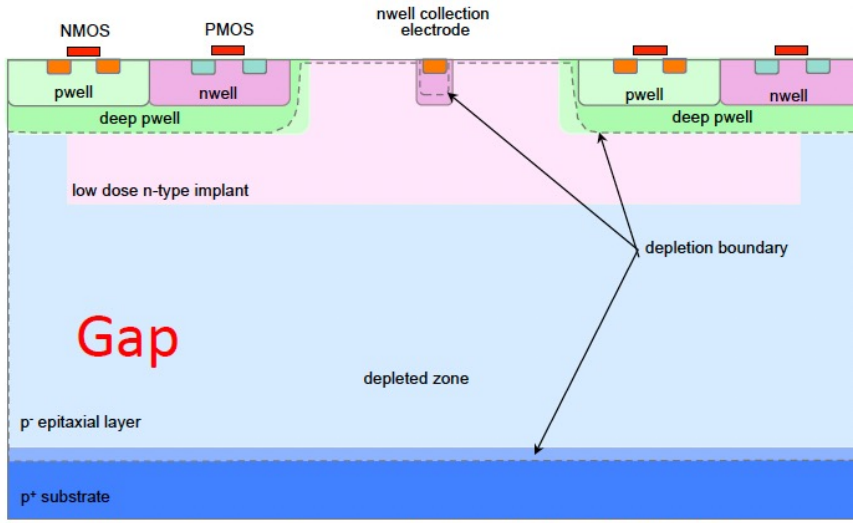
Similar optimization as in 180nm

Implant modifications needed even more in 65 nm for good charge collection





https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

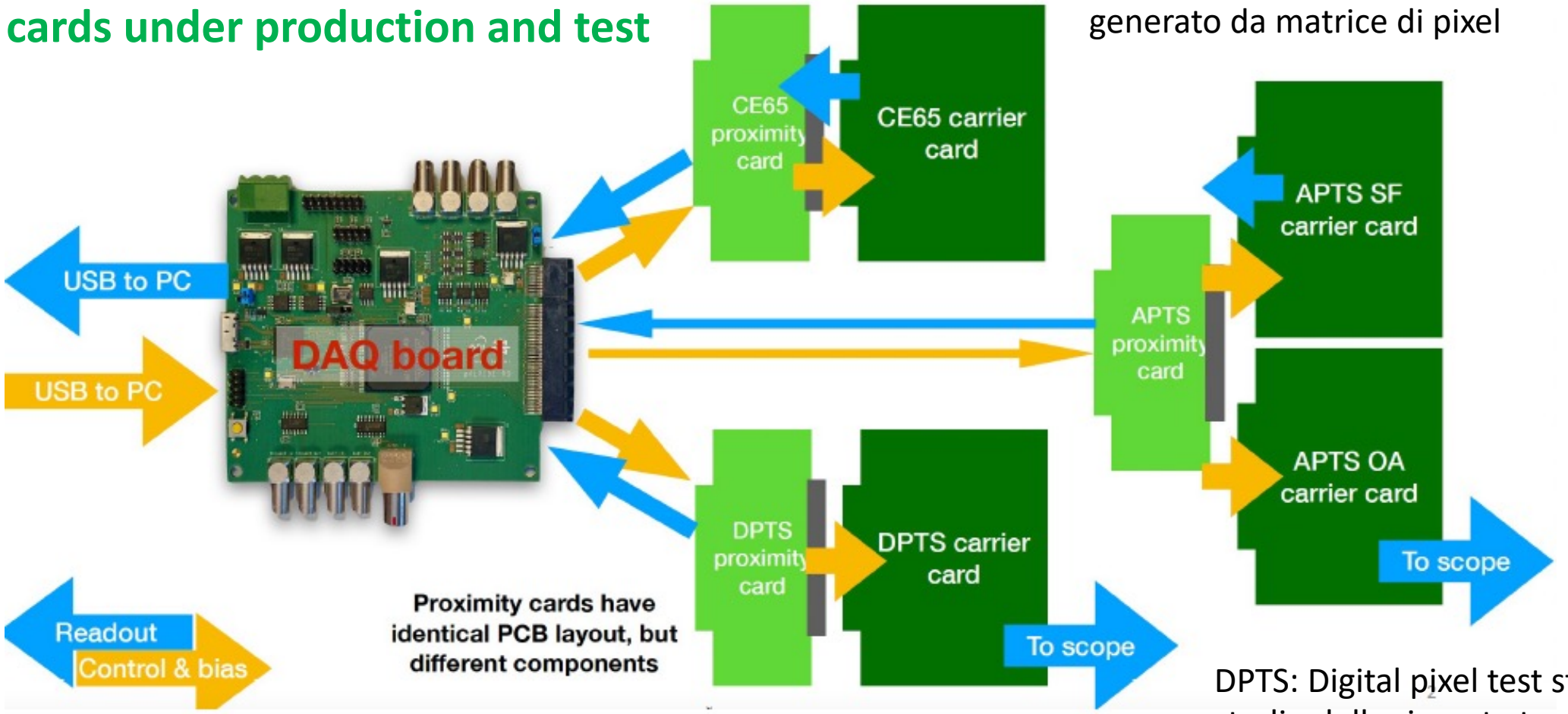
Charge sharing

MLR1 Test system concept

System fully designed

Presently **cards under production and test**

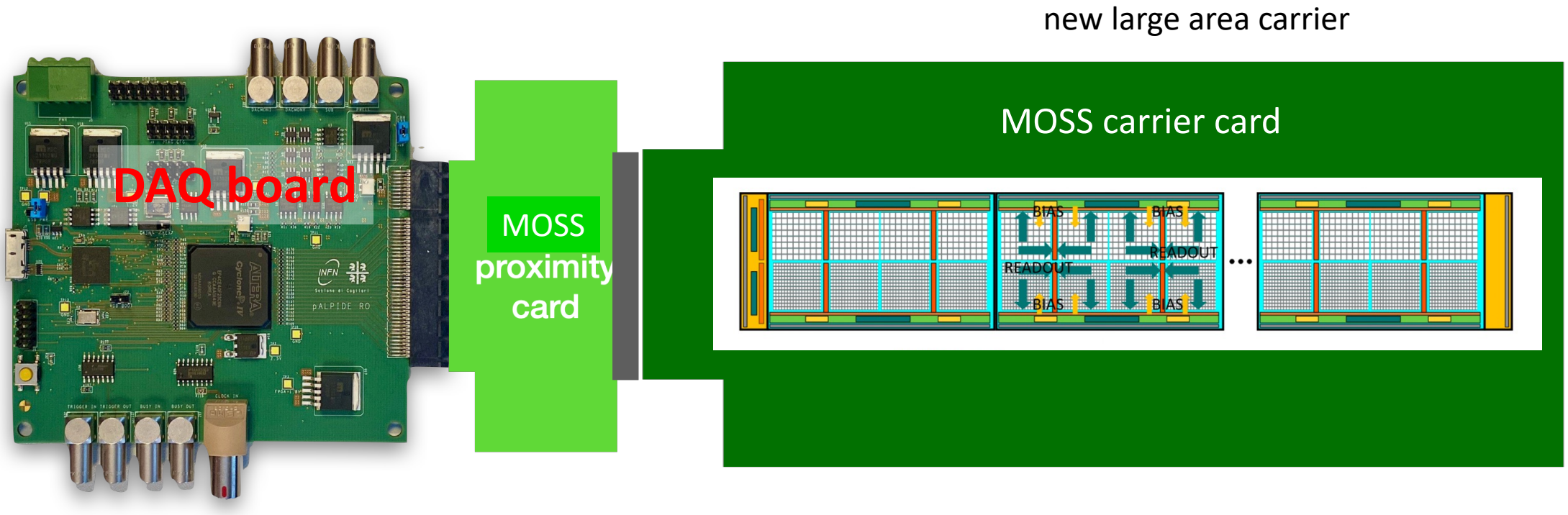
APTS: Analog pixel test structure
studio della forma del segnale generato da matrice di pixel



DPTS: Digital pixel test structure
studio della risposta temporale de pixel

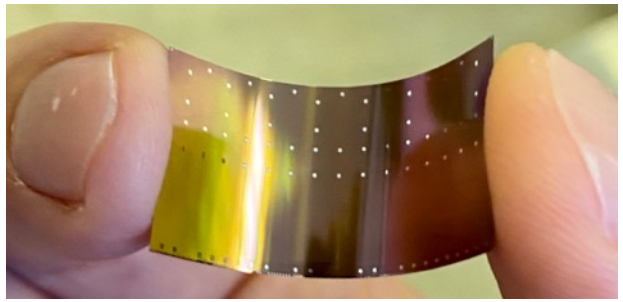
MOSS Test system concept

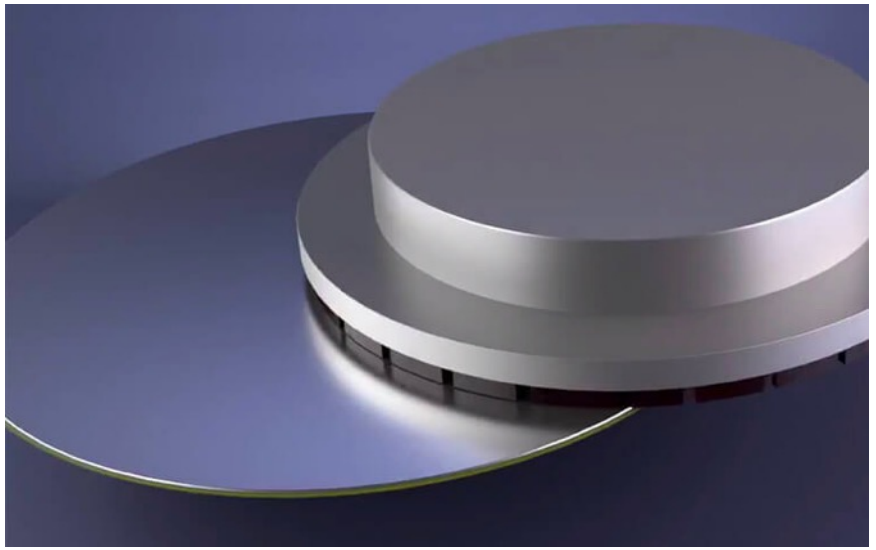
Extension of concept developed for MLR1

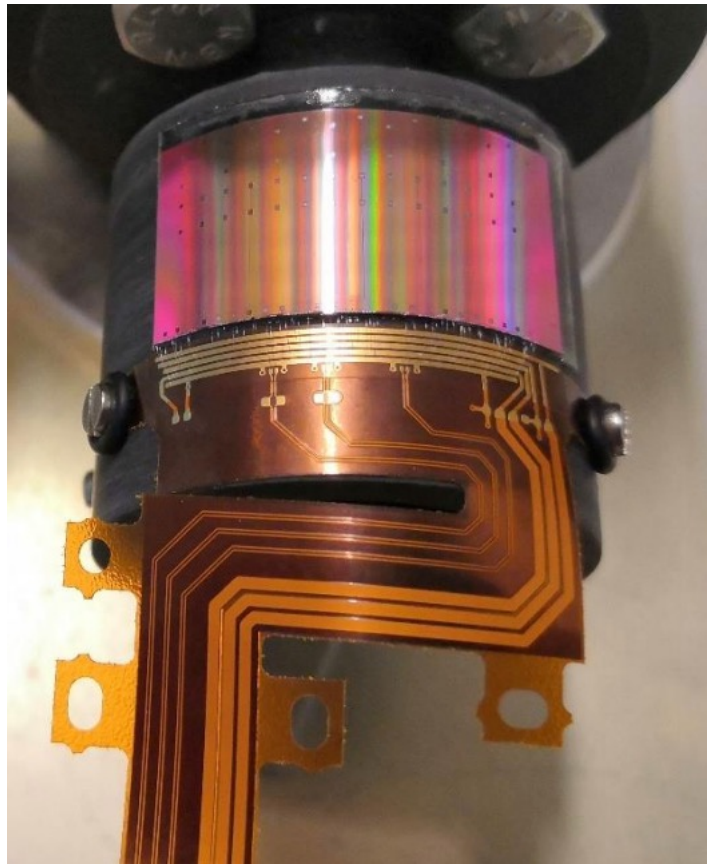


ITS3 - WP4: sensor thinning, bending and interconnections

convener: **G. Contin** – M. Mager





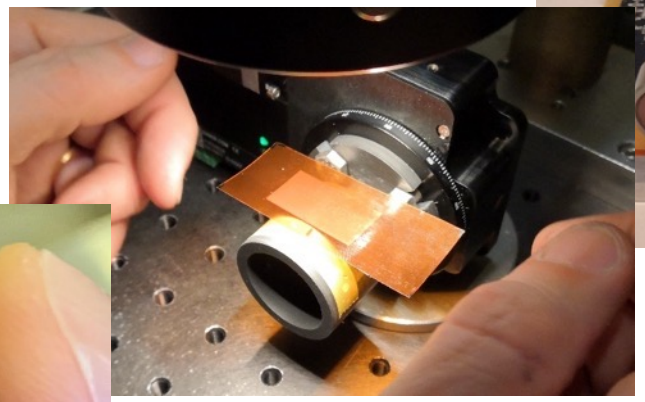


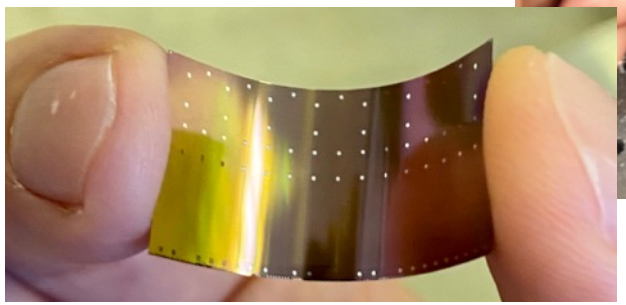
interesse da diverse sedi INFN:

- Bari/Bologna: wire bonding
- Trieste: thinning, bending, wire bonding
- Torino: spTAB bonding

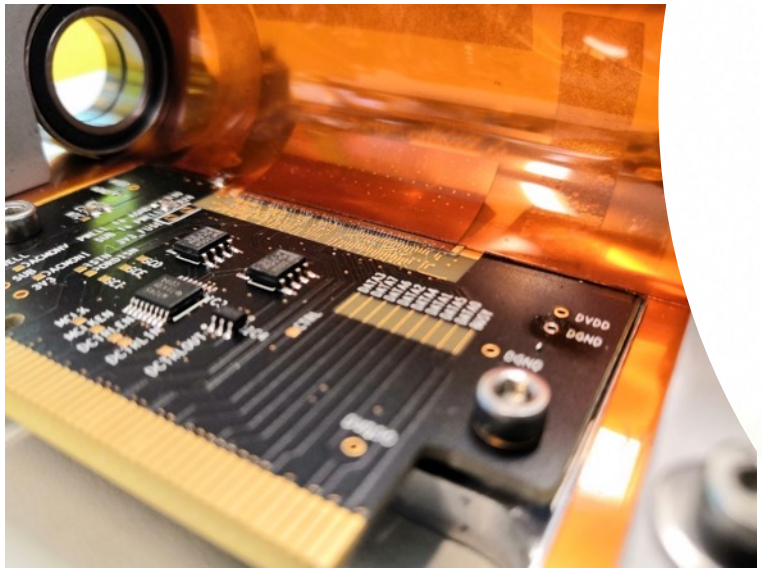
Sensor bending

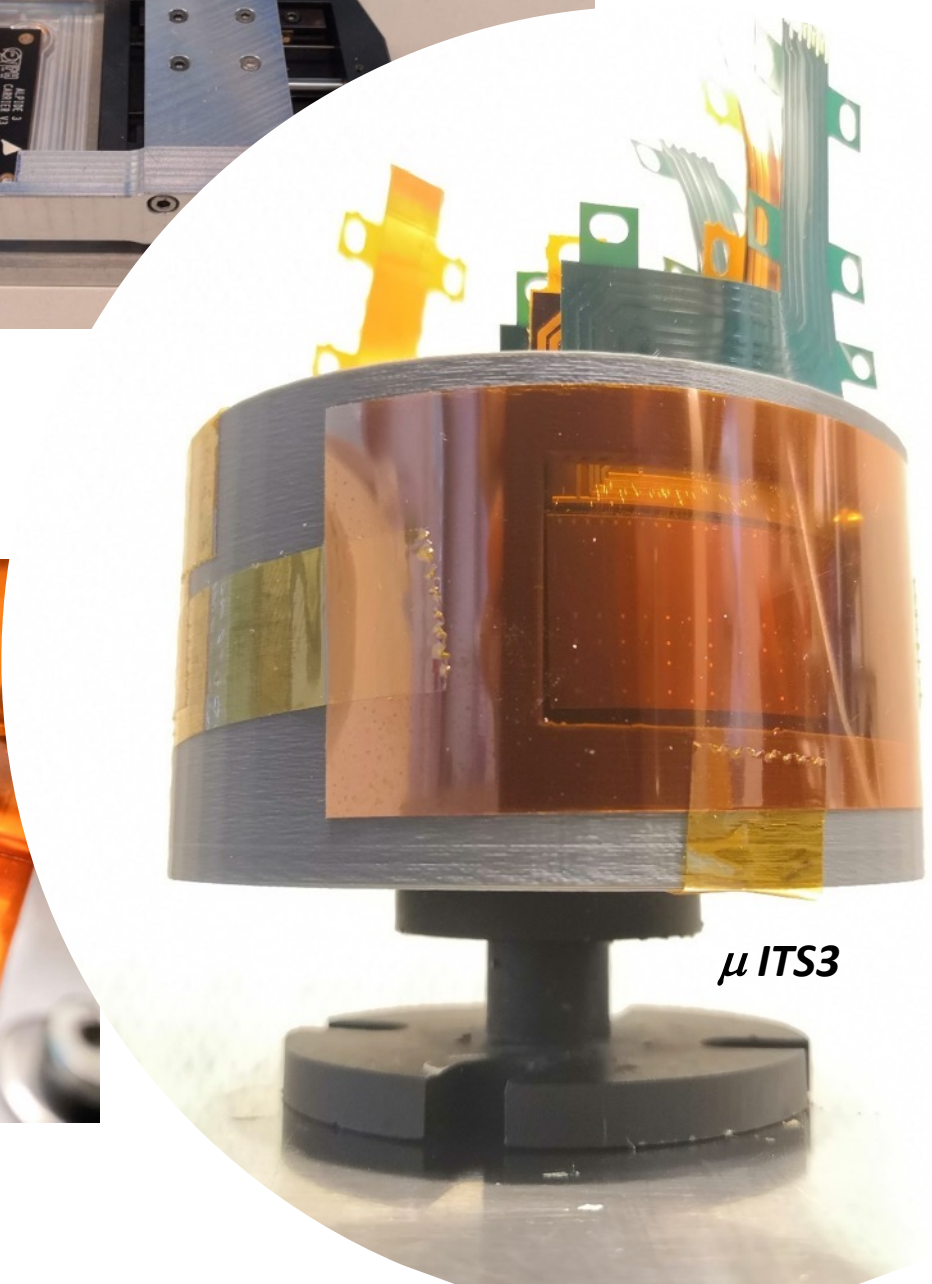
Manual bending





Controlled bending

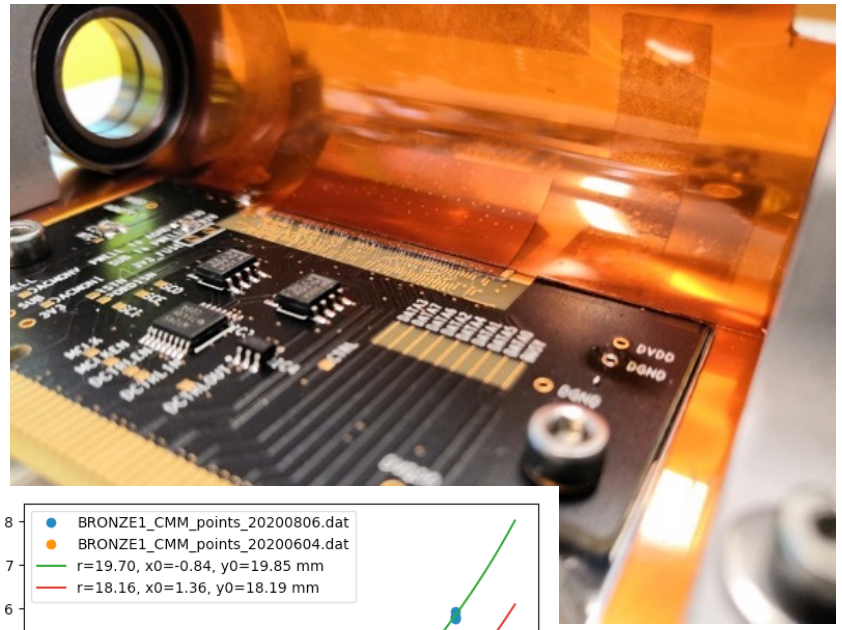


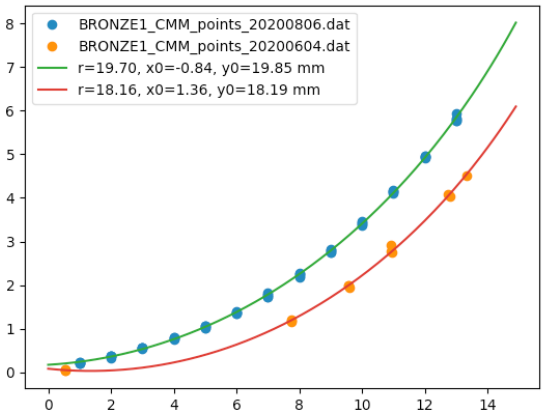


μ ITS3

- Measured curvature radius:
  - DUT1: ~ 16mm
  - DUT2: ~ 18mm
- **Test beam performed at Desy, no possibility to participate due to COVID-19 (article ready for publication)**

Preparazione DUTs e telescopi per testbeams





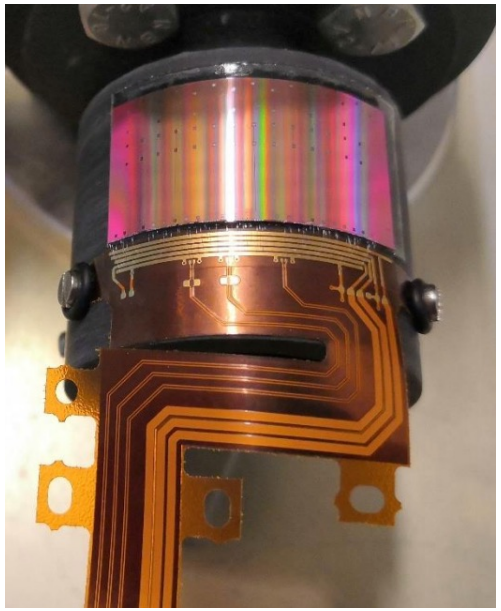
Monitoraggio della curvatura

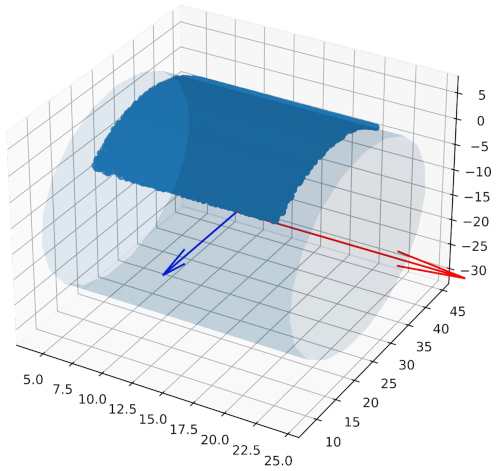
Preparazione DUTs per diversi Testbeam 2020-2021 avvenuta principalmente a Trieste e al CERN

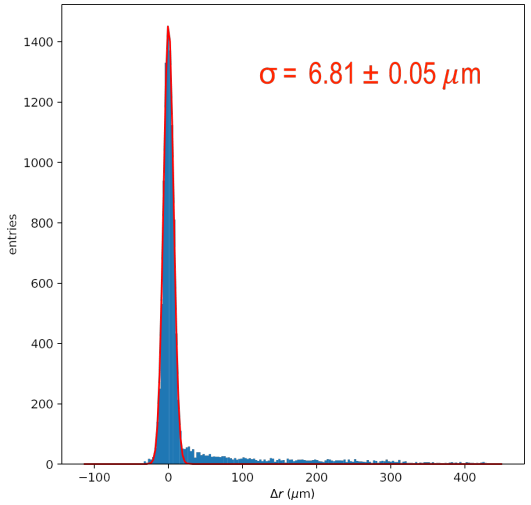
R&D su:

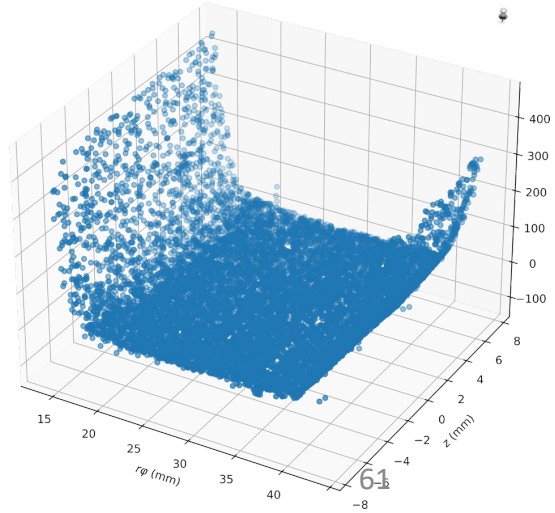
- Meccaniche e procedure per curvatura
- Wire-bonding su superfici curve
- Misura di precisione della curvatura (CMM)
- Primi test elettrici in laboratorio

→ Risultati pubblicati in [arXiv:2105.13000]

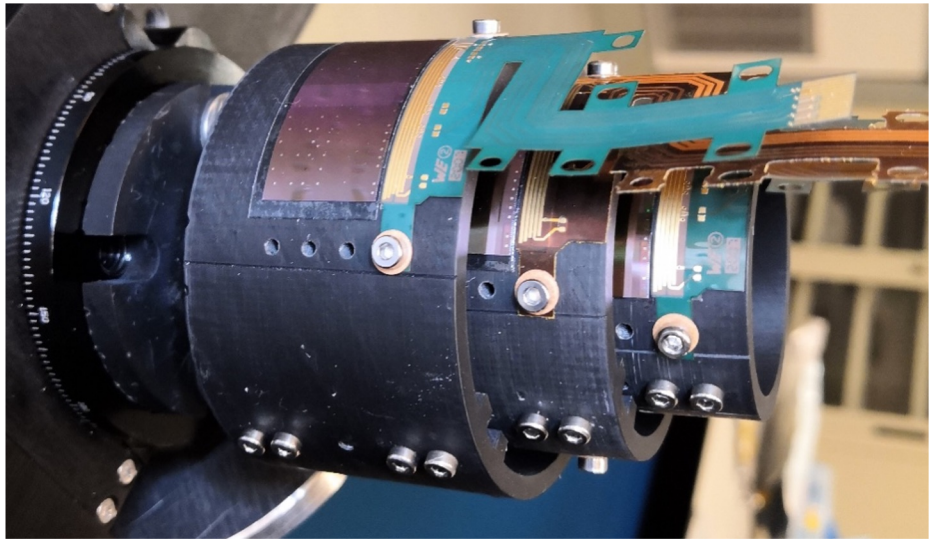








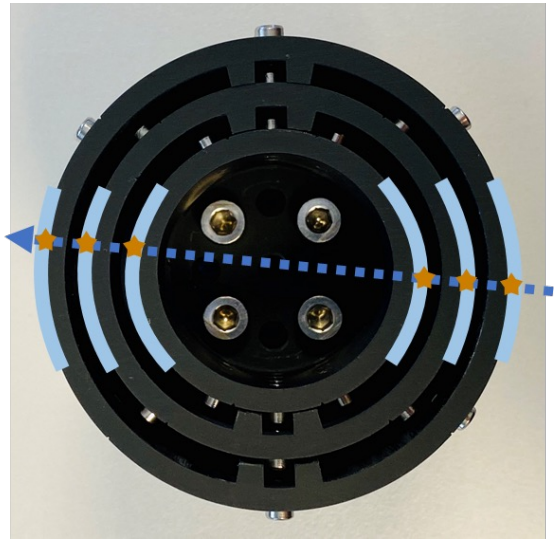
Preparazione μITS3 e prossimi DUTs



μITS3

3 strati di ALPIDE curvati con raggio di curvatura nominale dell'ITS3

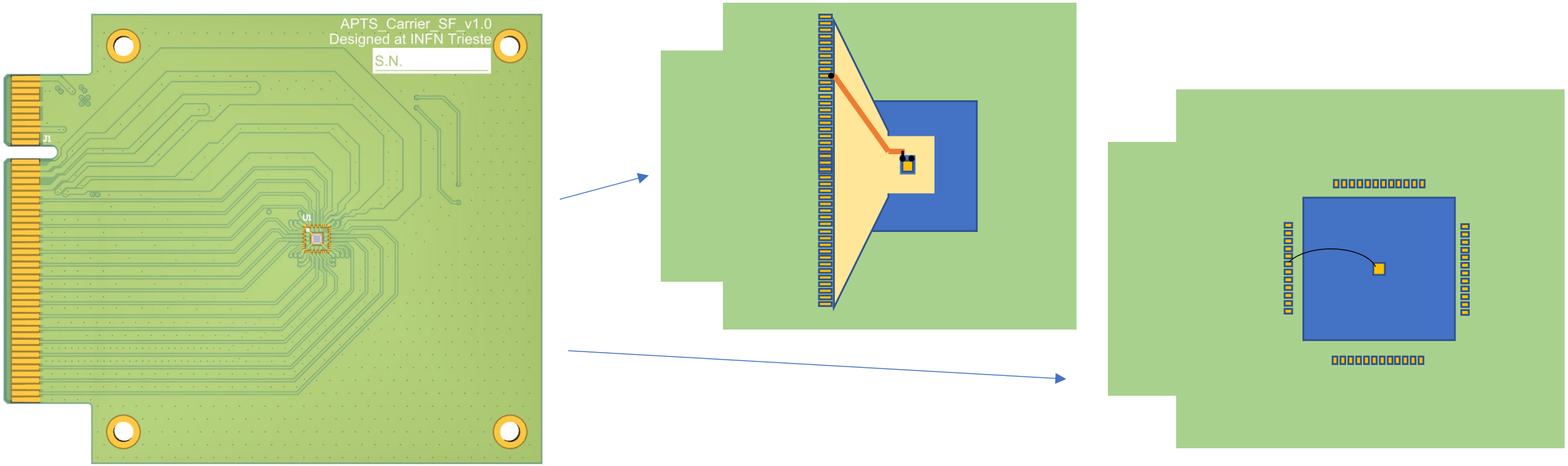
- Tracciamento con 6 punti registrati da strati di silicio curvo!



Piani 2022 per WP4 INFN (TS)

- Preparazione DUTs basati su ALPIDE e strutture di test MLR1
- Sviluppo meccaniche di curvatura di chip di media grandezza
- Sviluppo elettroniche di caratterizzazione segnali veloci per prossime sottomissioni
- Costruzione telescopi per caratterizzazione prestazioni DUTs

Piani per curvare strutture di test MLR1



Le carrier board sviluppate a Cagliari, Torino, Trieste saranno modificate per poter ospitare chip flessibili di area 3x3 cm^2 contenenti le strutture di test MLR1

Opzioni considerate: wire bonding e SpTAB bonding
Attualmente allo studio:

- Sviluppo FPC/chipcable e interconnessioni
- Miglior layout di tracce e piani di alimentazione
- Connessione meccanica e elettrica

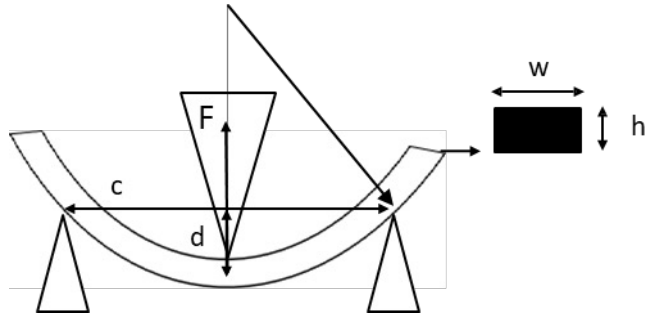
Thinning e caratterizzazione meccanica

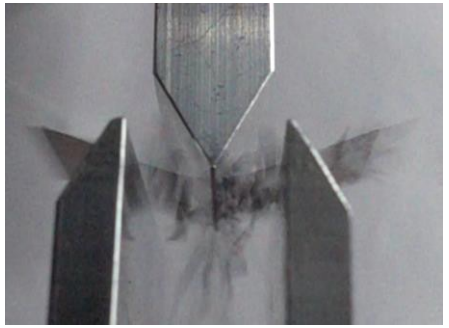
- Automated 3-p test setup

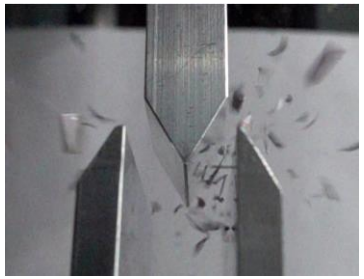
Planned measurements:

- Bending modulus
- Elastic – plastic region
- Breaking point
- Minimum radius

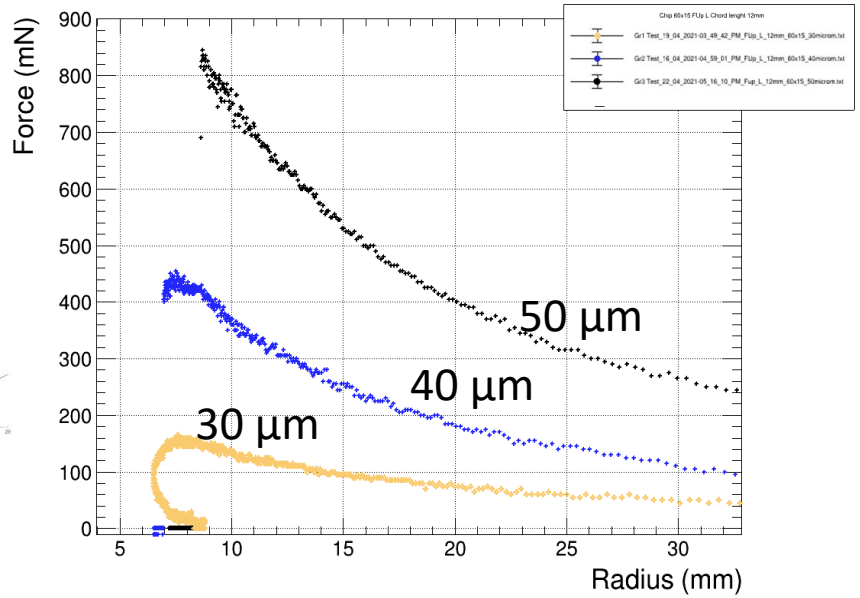
- **At 30-40-50 µm thickness!**





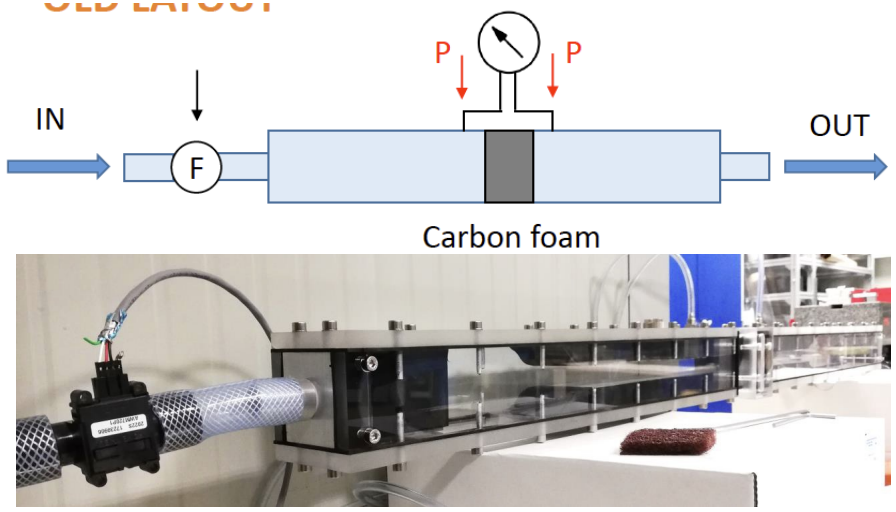


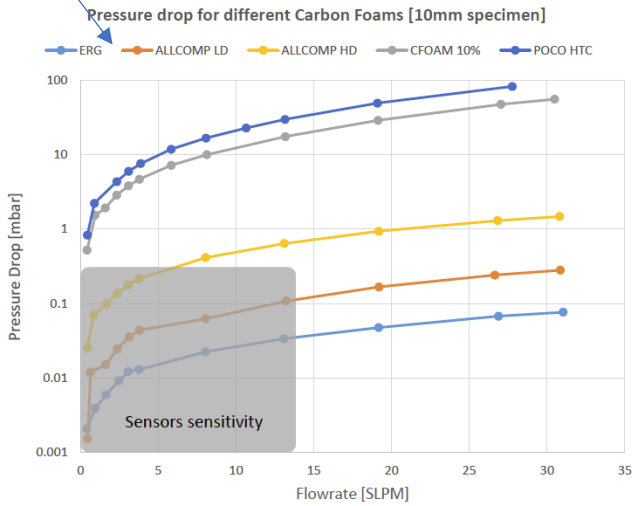
ALICE ITS3 Bending Test

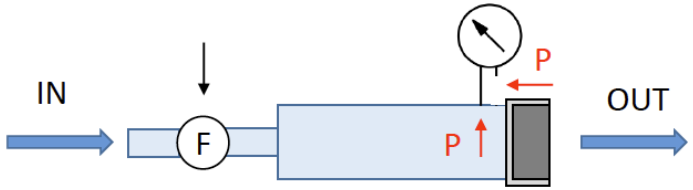


Caratterizzazione proprietà Carbon Foam (CF)

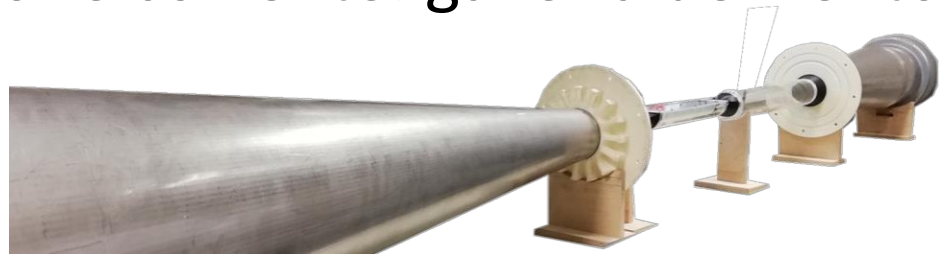
- Pressure drop test
  - Diversi layout provati nel 2021
  - Misure su diversi tipi di CF



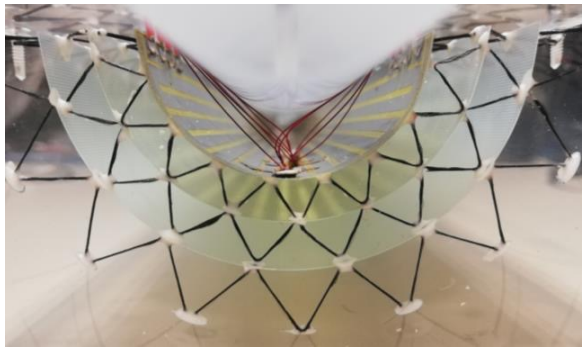




- Versione corrente: galleria del vento



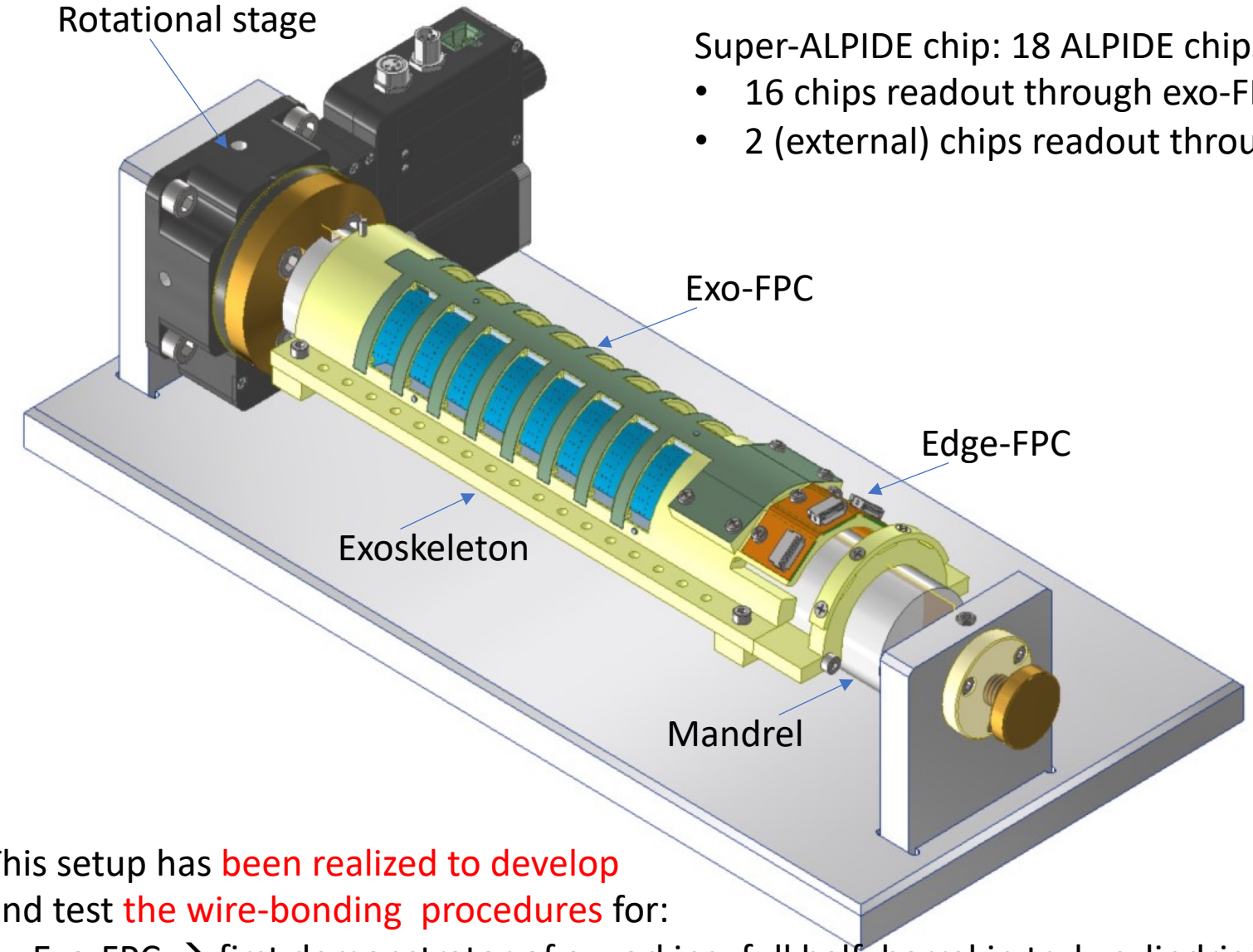
L0 equipped with 3 PT1000 temperature sensors



Studio del raffreddamento a valle del primo supporto (ring) in fibra di carbonio

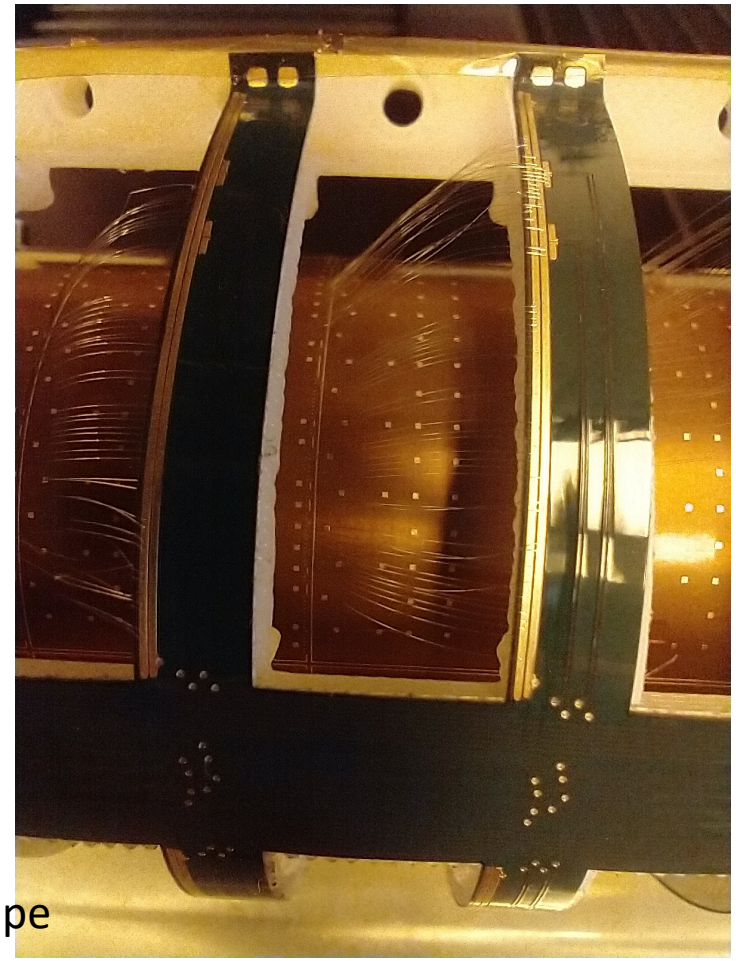
2022: attività di simulazione ed ottimizzazione

Super-ALPIDE (mock-up) setup: development of the wire-bonding procedure and FPC design



Super-ALPIDE chip: 18 ALPIDE chips over 2 rows in one big structure

- 16 chips readout through exo-FPC [bond over 7 mm pads vertical distance]
- 2 (external) chips readout through edge-FPC [bond at the same quota]



This setup has been realized to develop
and test the wire-bonding procedures for:

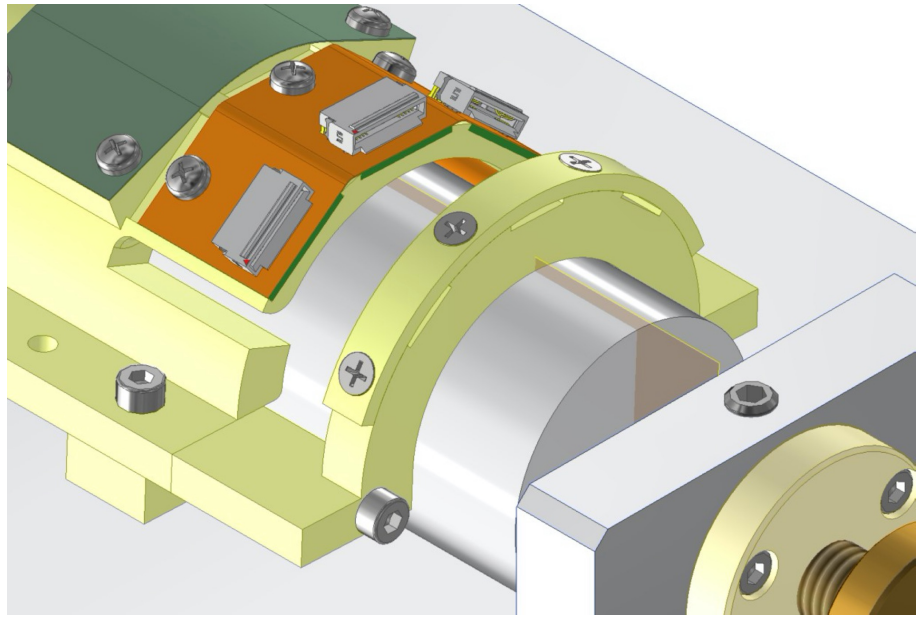
- Exo-FPC → first demonstrator of a working full half barrel in truly cylindrical shape
- Edge FPC → main interest for the further developments (final detector)

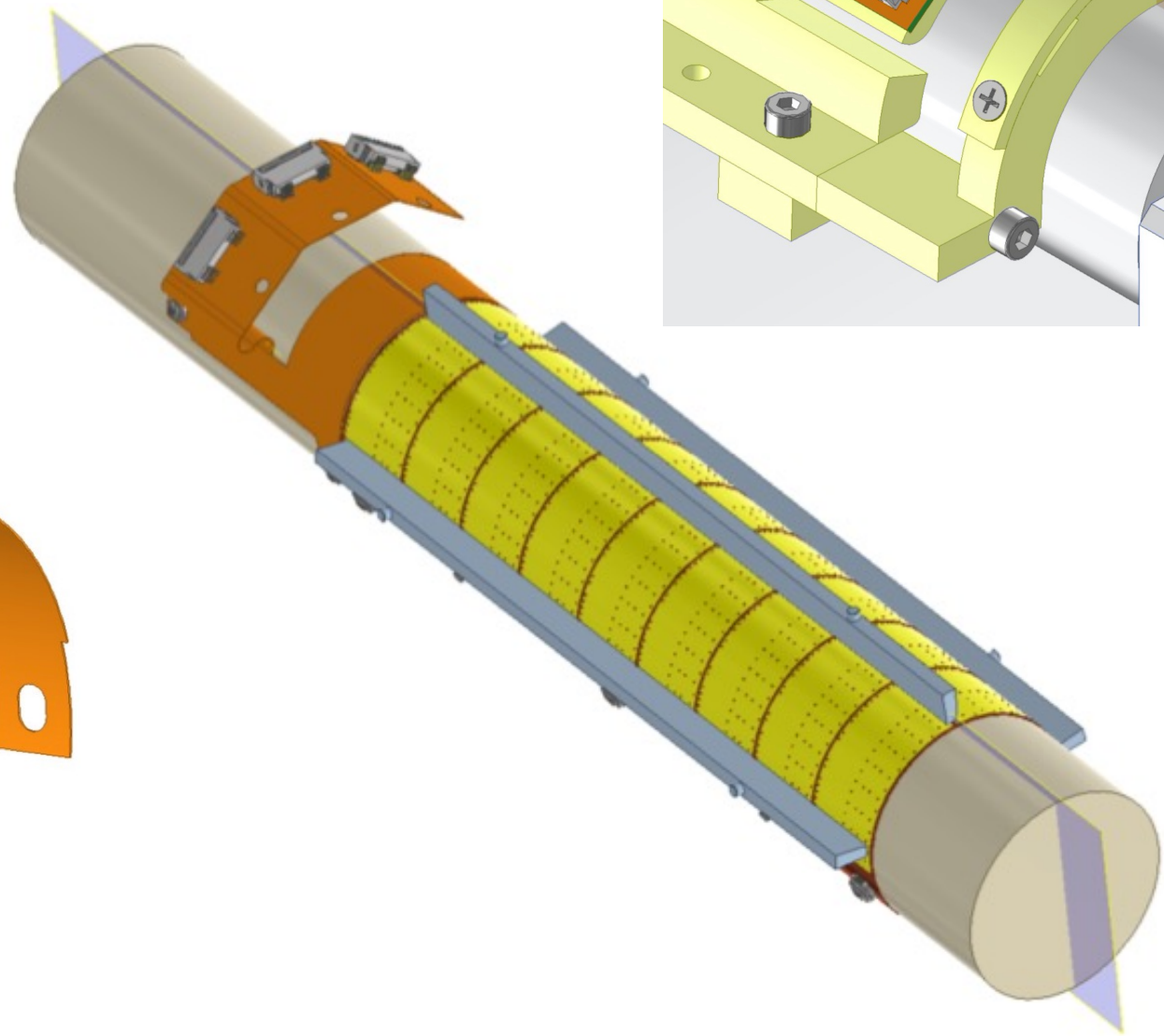
The present mandril holds a mock-up of the bended super-ALPIDE

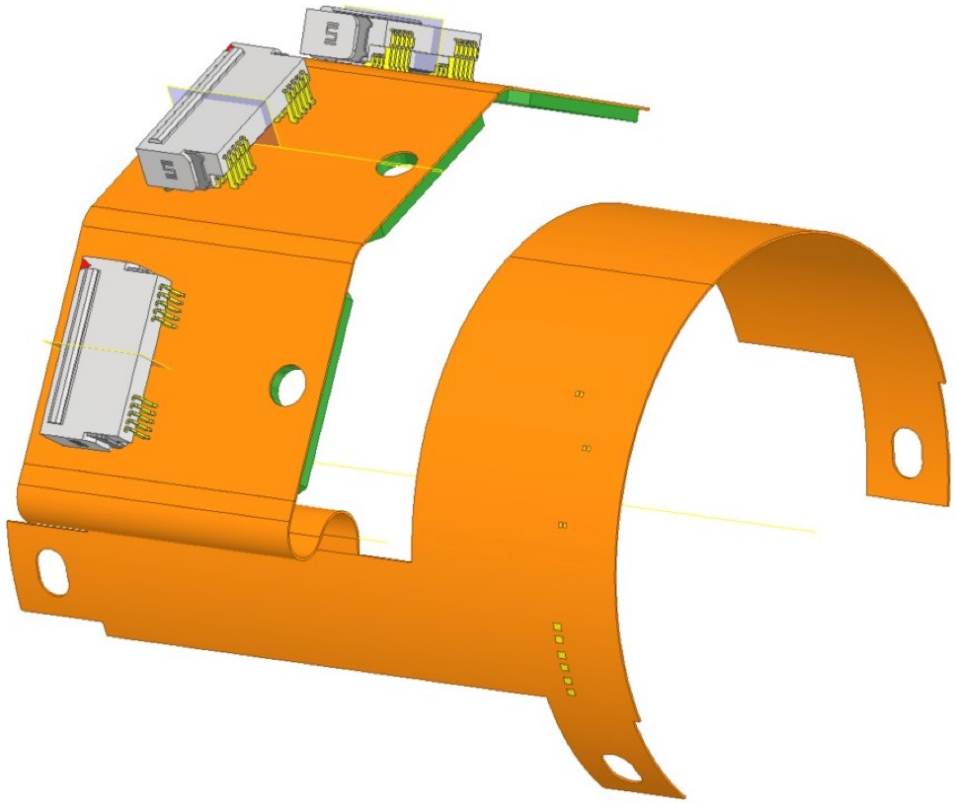
Super-ALPIDE setup

Edge-FPC

- Prototype of the final detector FPC
- Designed and integrated in Bari
- Under production
- Continue design toward next generation of large-area chips in 2022
  - new productions in 2022



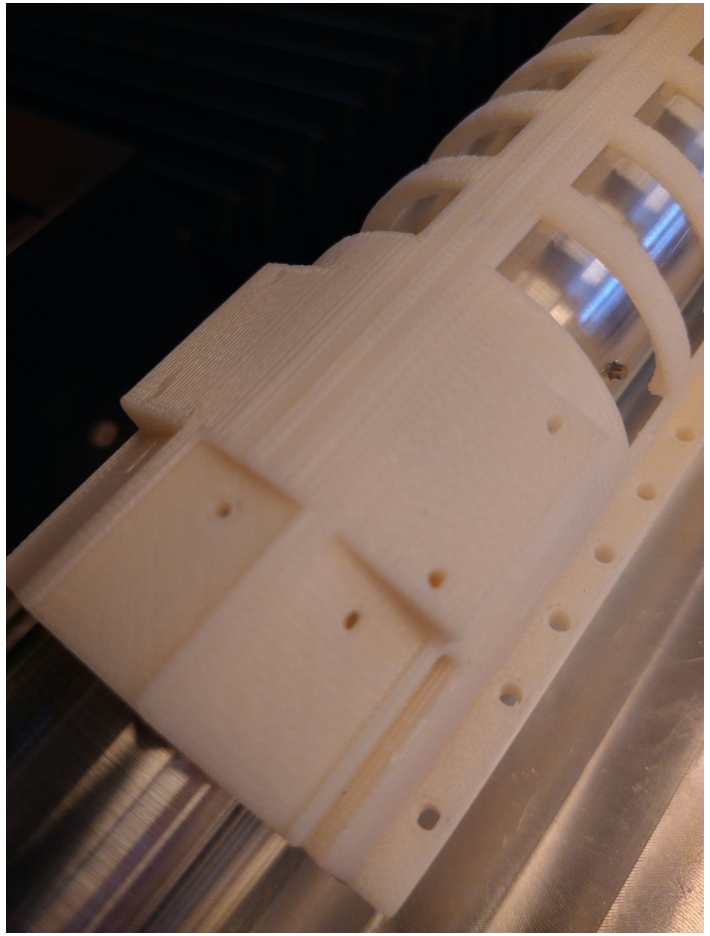


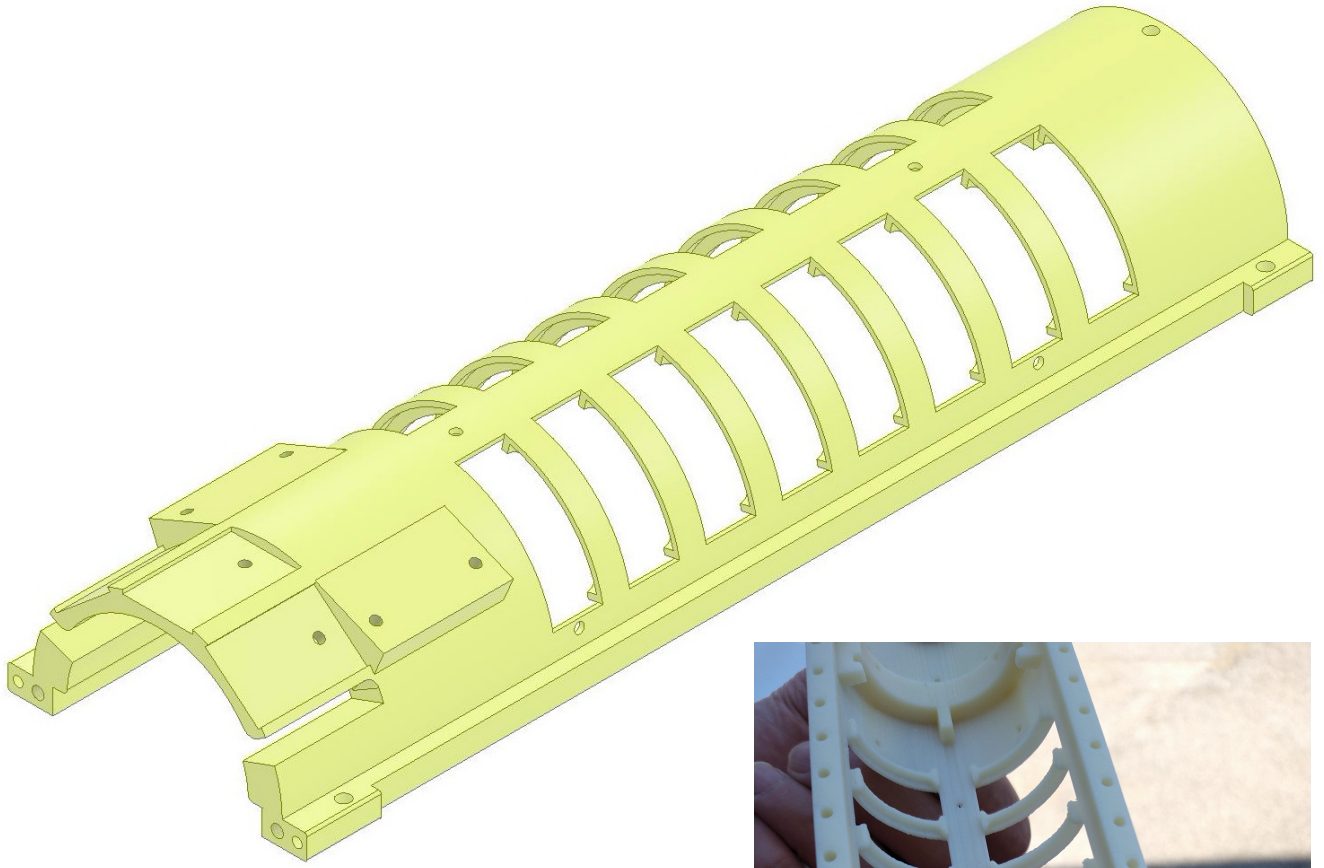


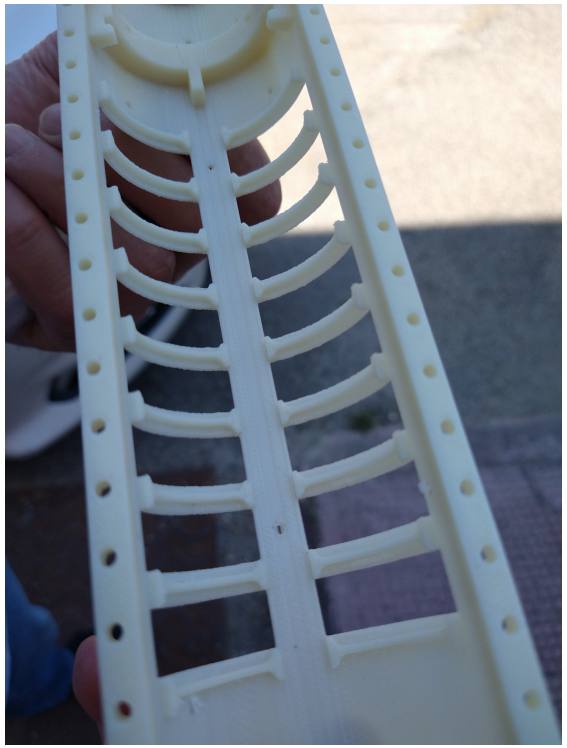
Super-ALPIDE setup

Exoskeleton

- First version designed by Magnus Mager
- Design finalization in Bari
  - edge-FPC integration
  - Bonding machine compatibility

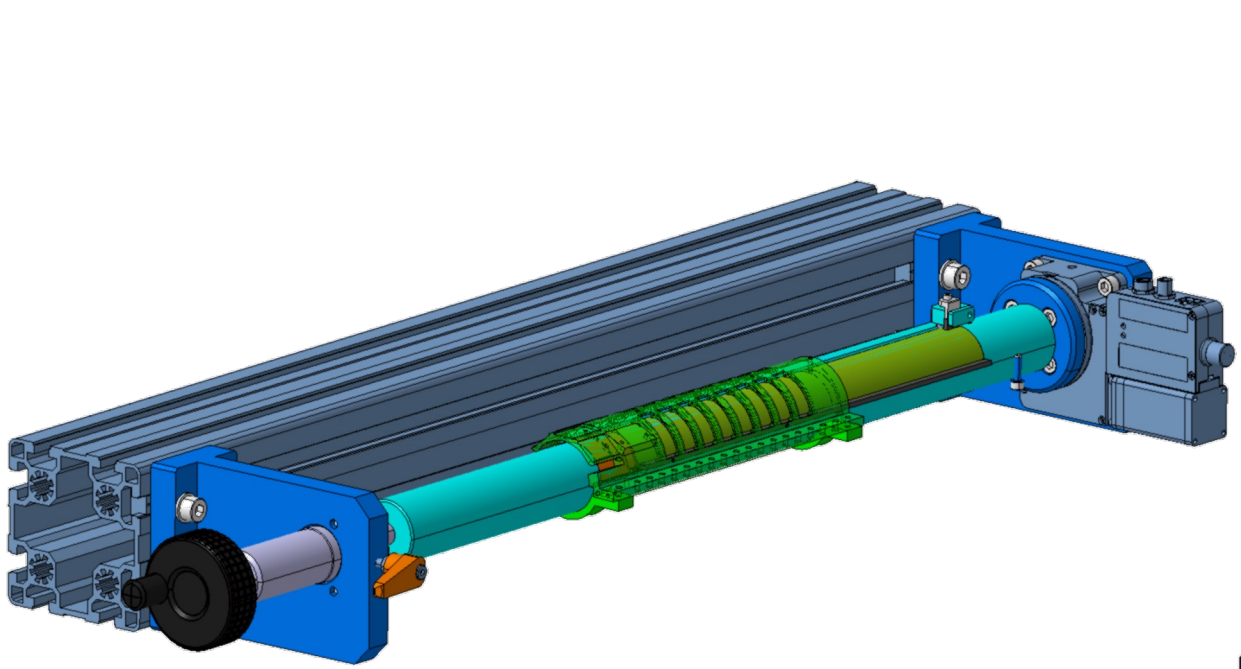


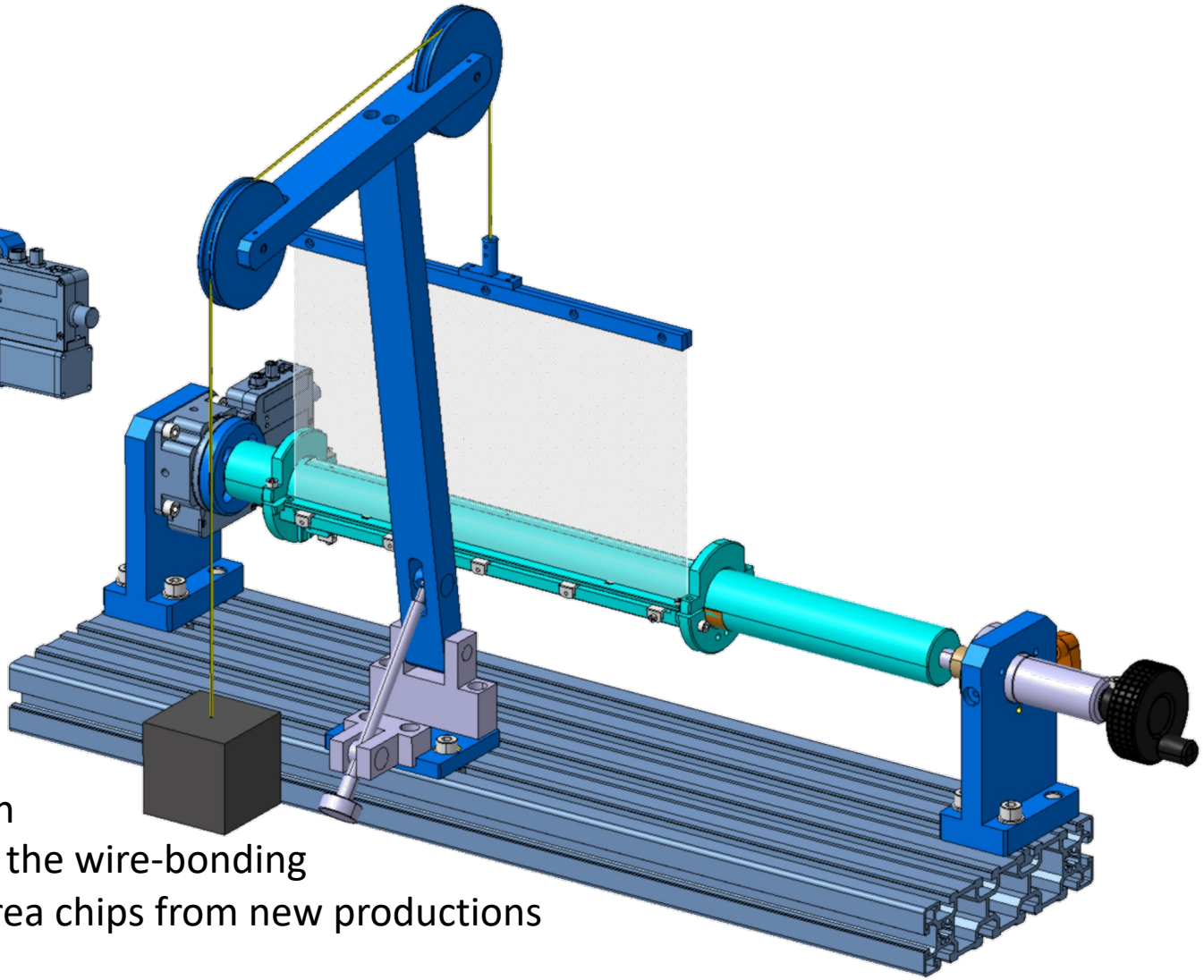




Super-ALPIDE setup - Bending tools

- Being designed at CERN
- Integration with the other components (exoskeleton and FPCs) in collaboration with Bari
- Next: full setup for complete super-ALPIDE assembly in Bari





The activity on the design of the edge FPC, its integration with the bending and assembly procedure of large area chips, and the wire-bonding procedure will be the focus of next year (2022), using large area chips from new productions