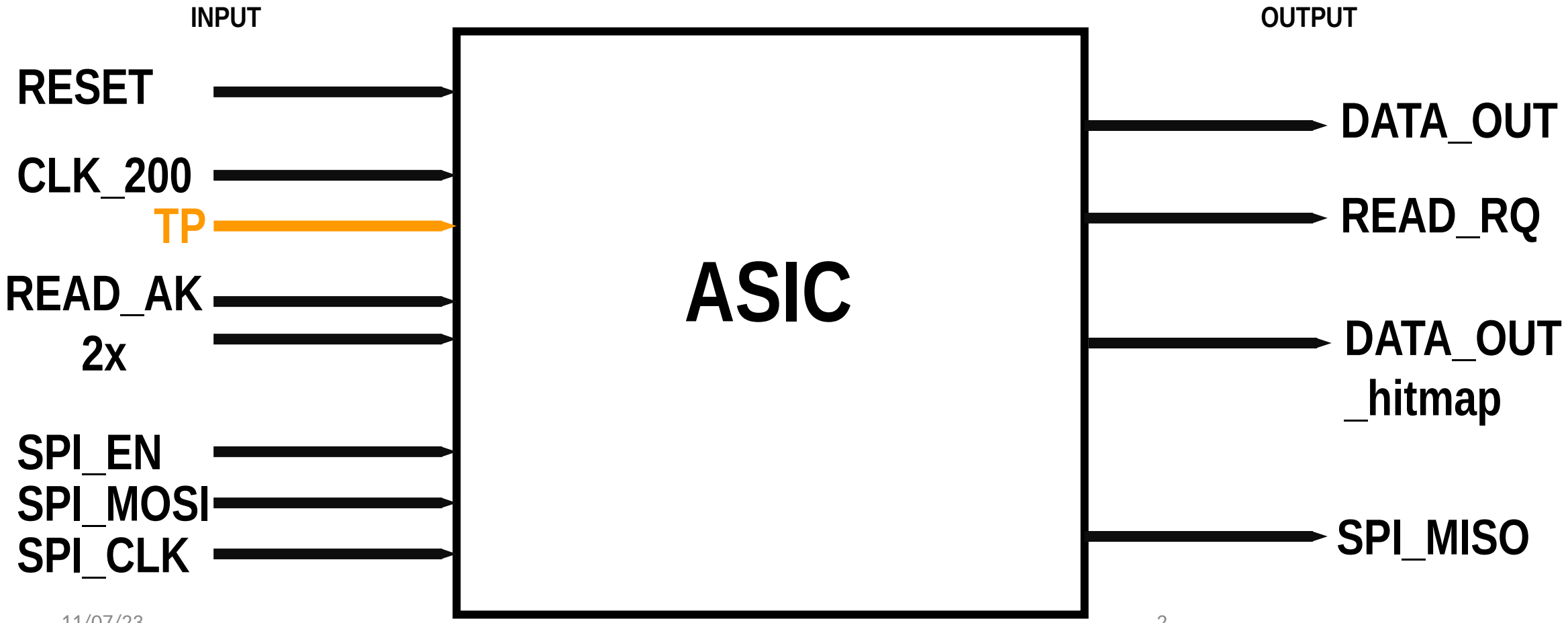
TERZINA FIRMWARE DEVELOPMENT: Status and features

Istituto Nazionale di Fisica Nucleare

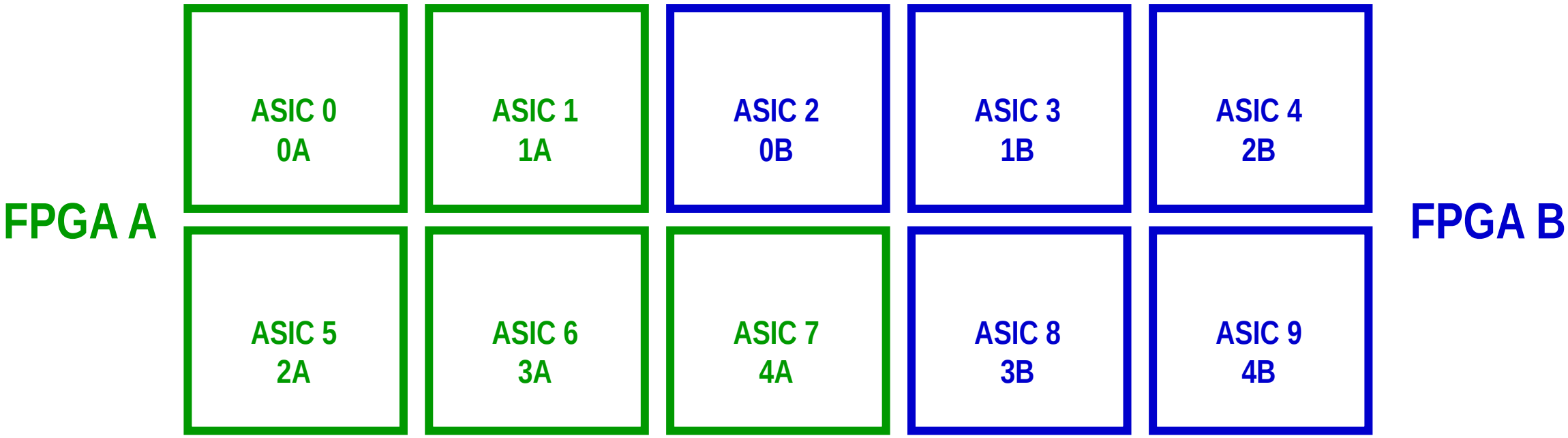
2023-07-11

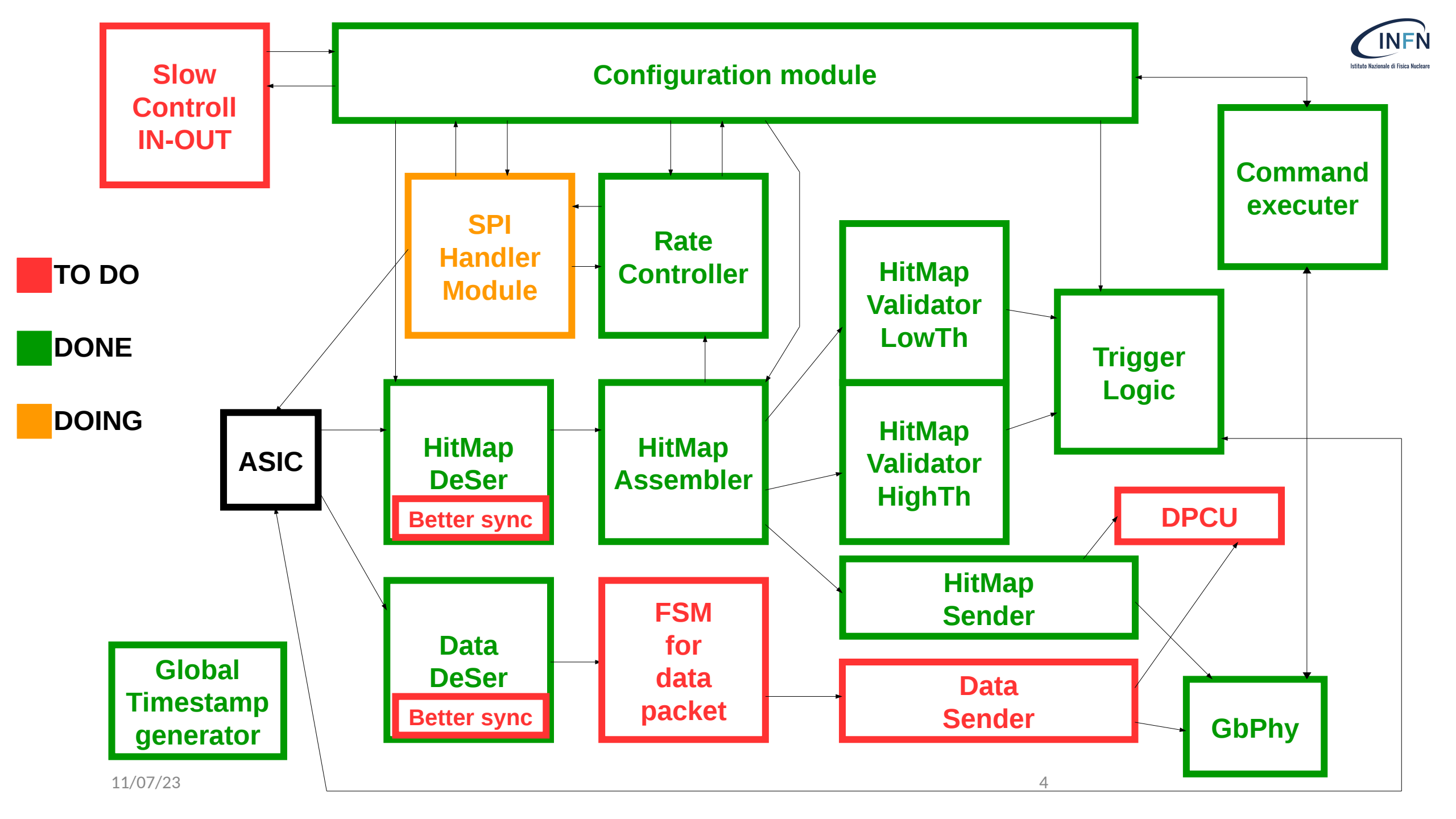
ASIC I-O

Every port is LVDS_25, this means that the actual number of ports is double

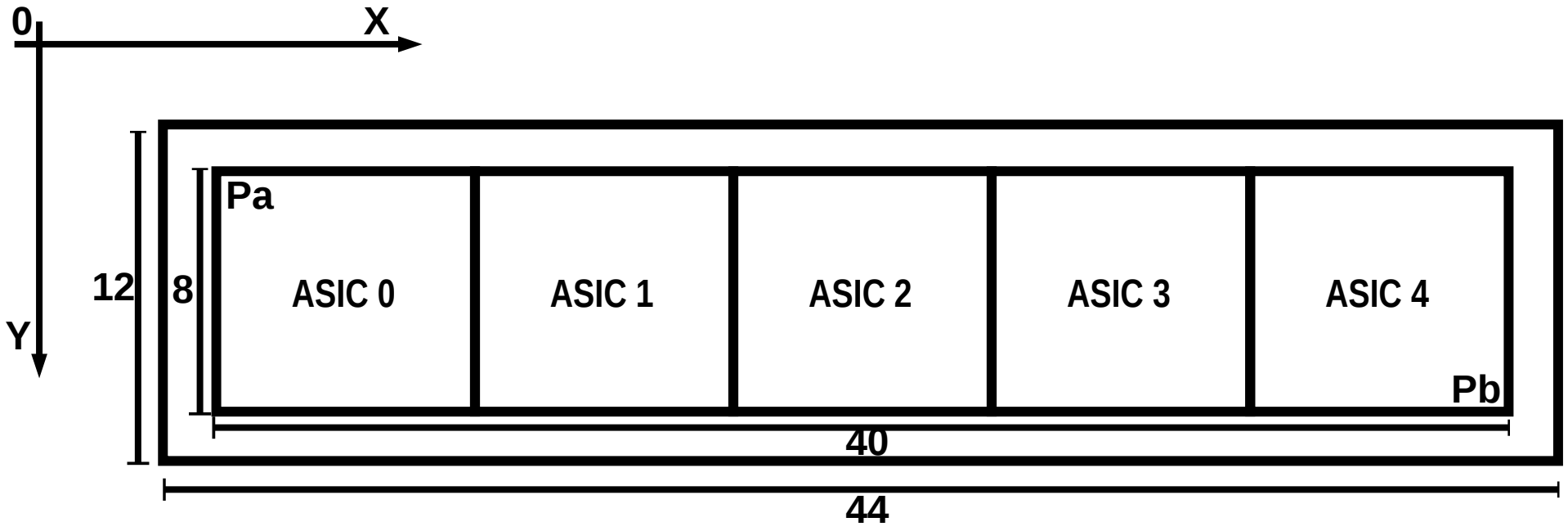


ASIC PLACEMENT




Slow Controll IN-OUT
Configuration module
Command executer
SPI Handler Module
Rate Controller
HitMap Validator LowTh
HitMap Validator HighTh
Trigger Logic
TO DO
DONE
DOING
ASIC
HitMap DeSer
Better sync
HitMap Assembler
DPCU
HitMap Sender
Data DeSer
Better sync
FSM for data packet
Data Sender
GbPhy
Global Timestamp generator

HITMAP VALIDATOR ALGORITHM

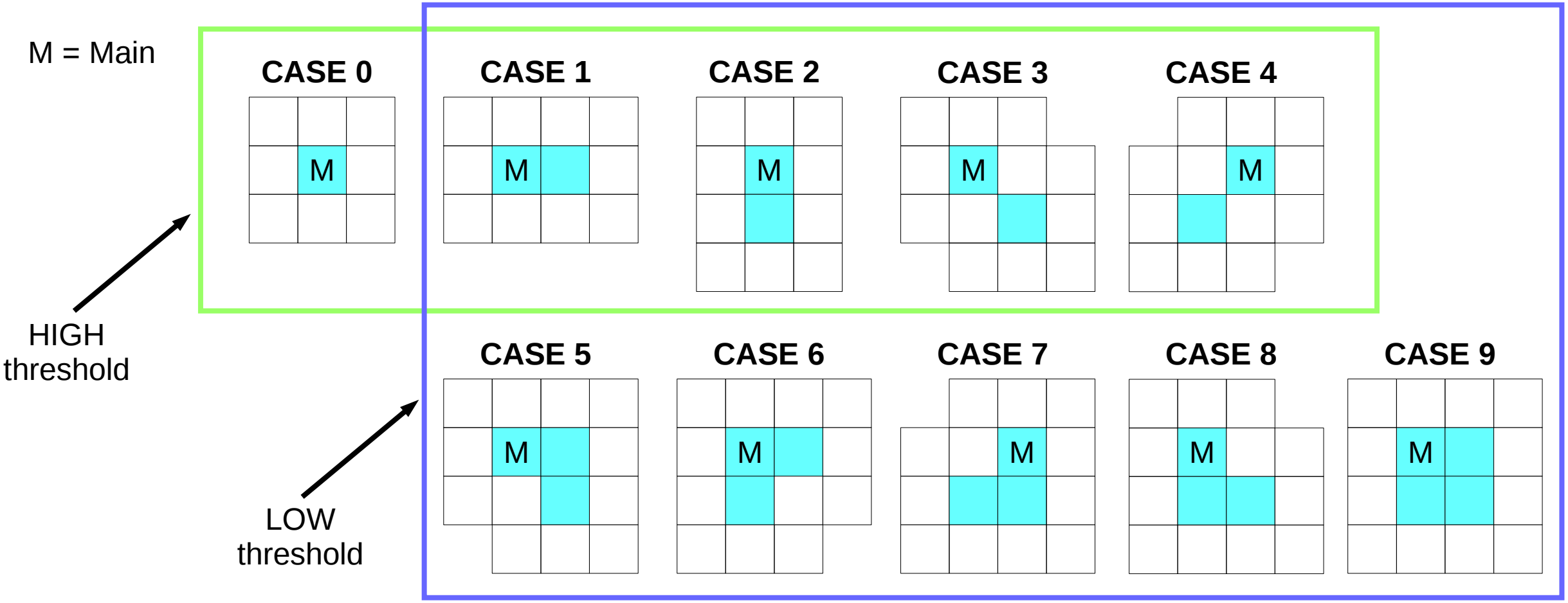


P = X + 44*Y
Pa = 2 + 44*2
Pb = 41 + 44*9

(527 downto 00) → 528 bit | 320 bit hitmap | 208 bit padding

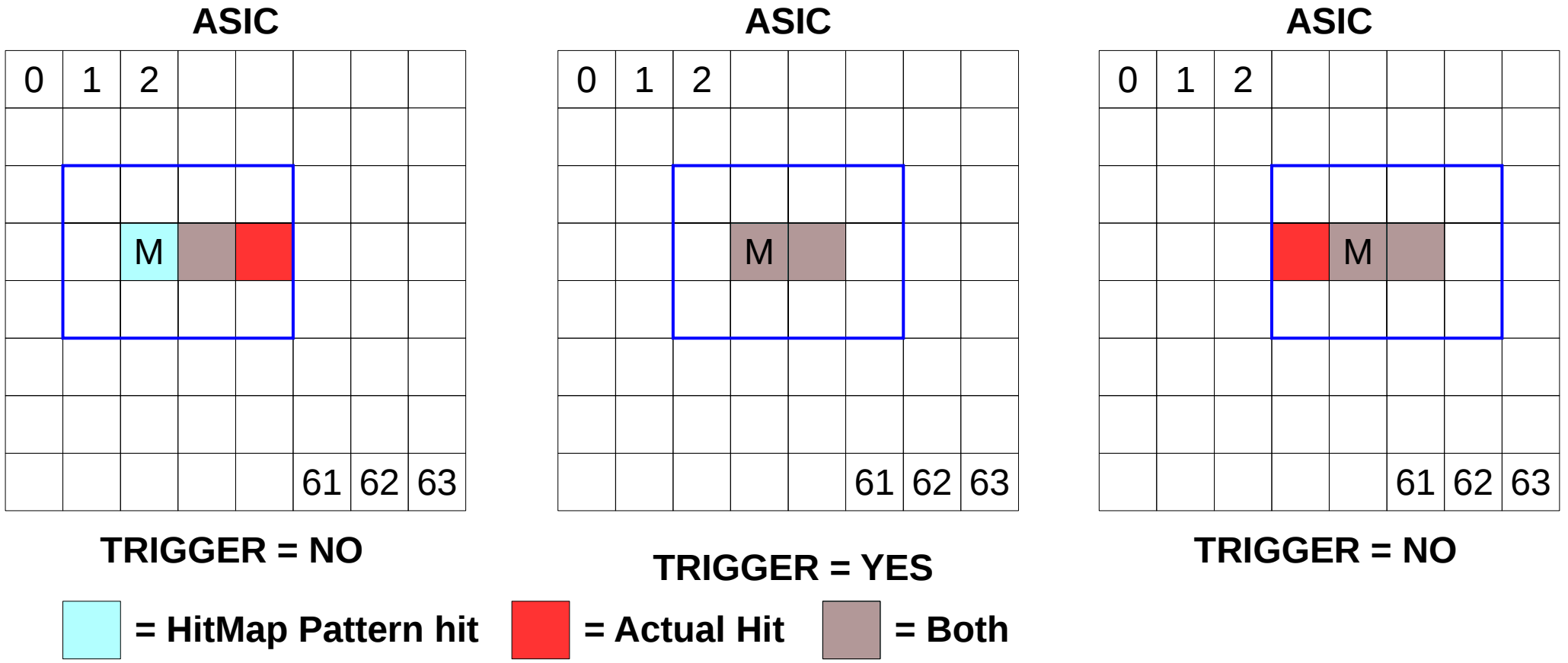
(437 downto 90) → 348 bit Main

HITMAP VALIDATOR PATTERN CASES



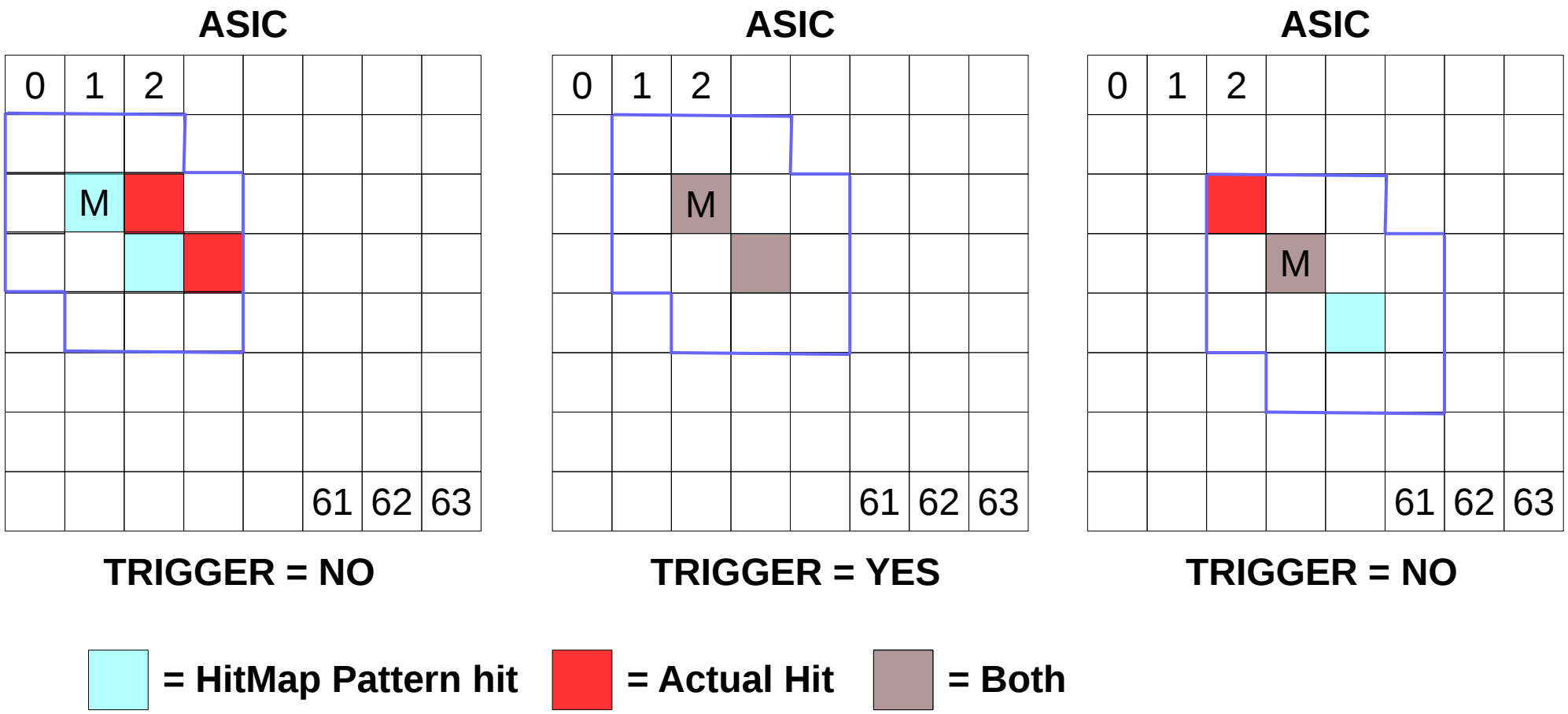
PATTERN SEEKING ALGORITHM

- Each pixel (in this case from 0 to 63) is considered as MAIN (M) and the pattern fingerprint is checked.
- This procedure is done in parallel for every pixel and every pattern case.
- Duration → 1 clock cycle.



EXAMPLE

- The case “Main + high left” can be mapped as “case 3” → “Main + low right”



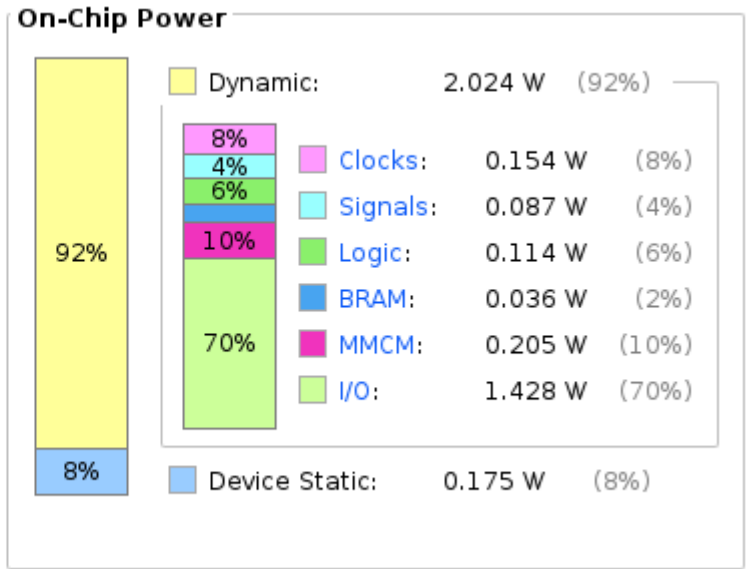
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.094 ns	Worst Hold Slack (WHS):	0.049 ns	Worst Pulse Width Slack (WPWS):	0.264 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94057	Total Number of Endpoints:	94012	Total Number of Endpoints:	36058

All user specified timing constraints are met.

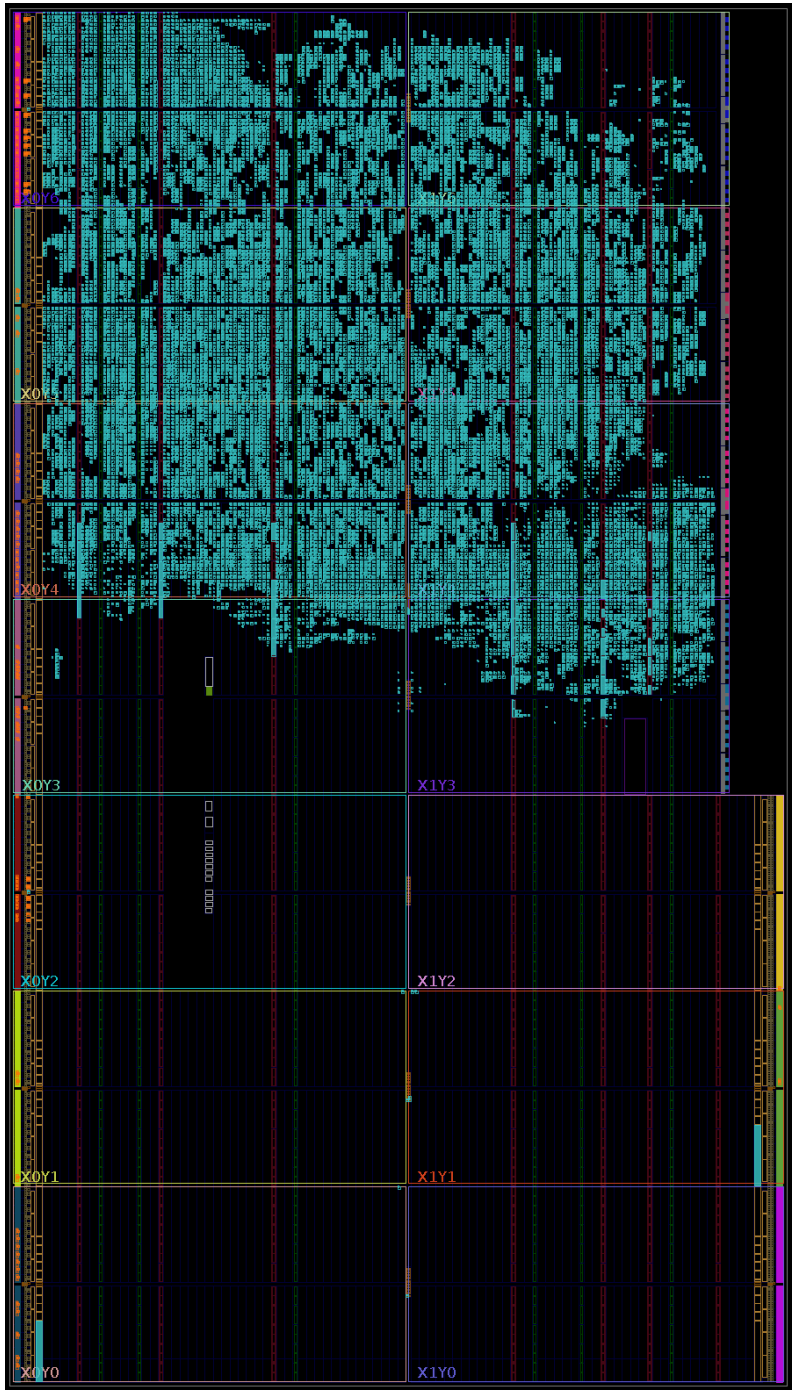
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

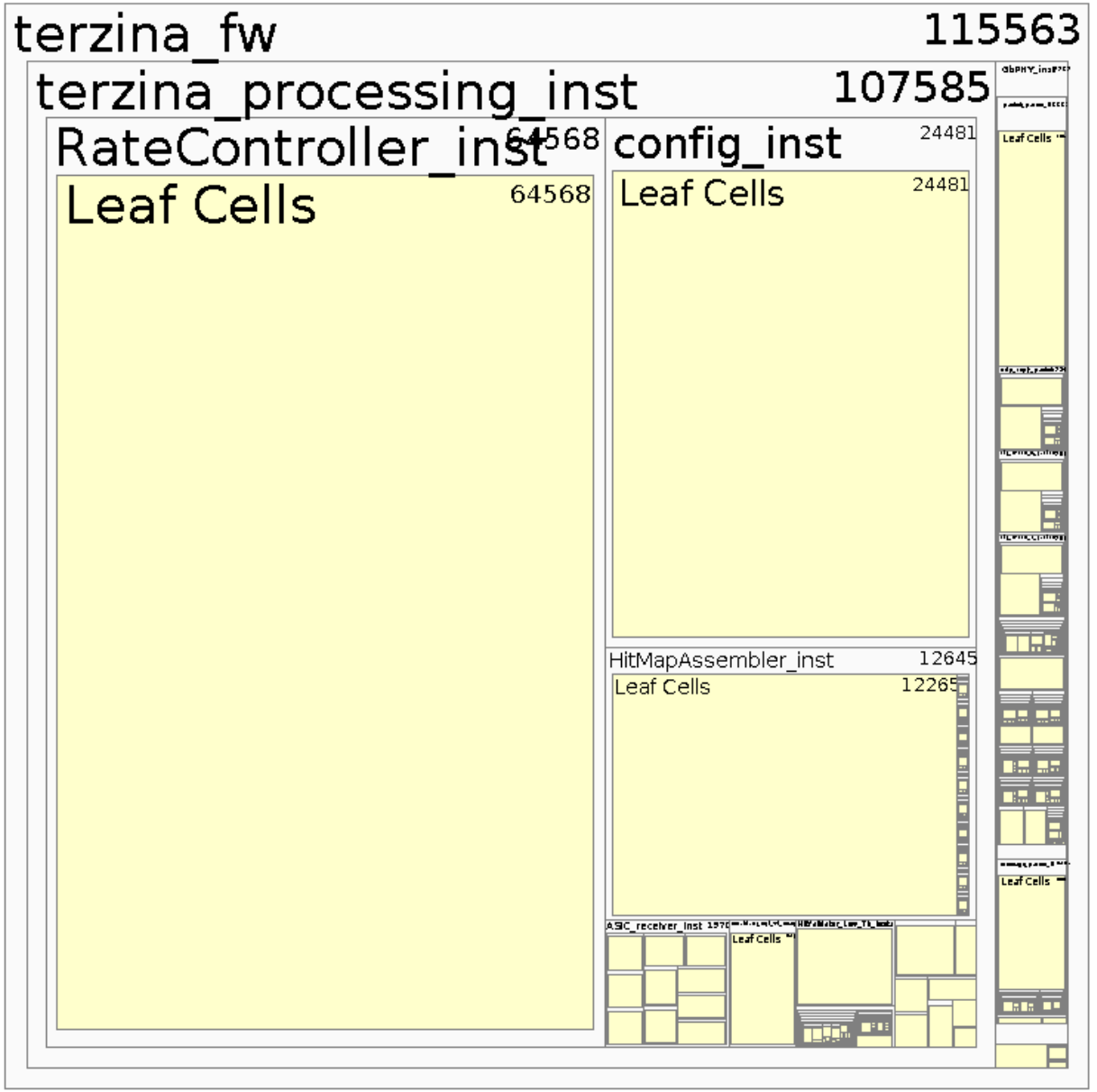
Total On-Chip Power:	**2.199 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.9°C**
Thermal Margin:	56.1°C (30.8 W)
Effective ϑJA:	1.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

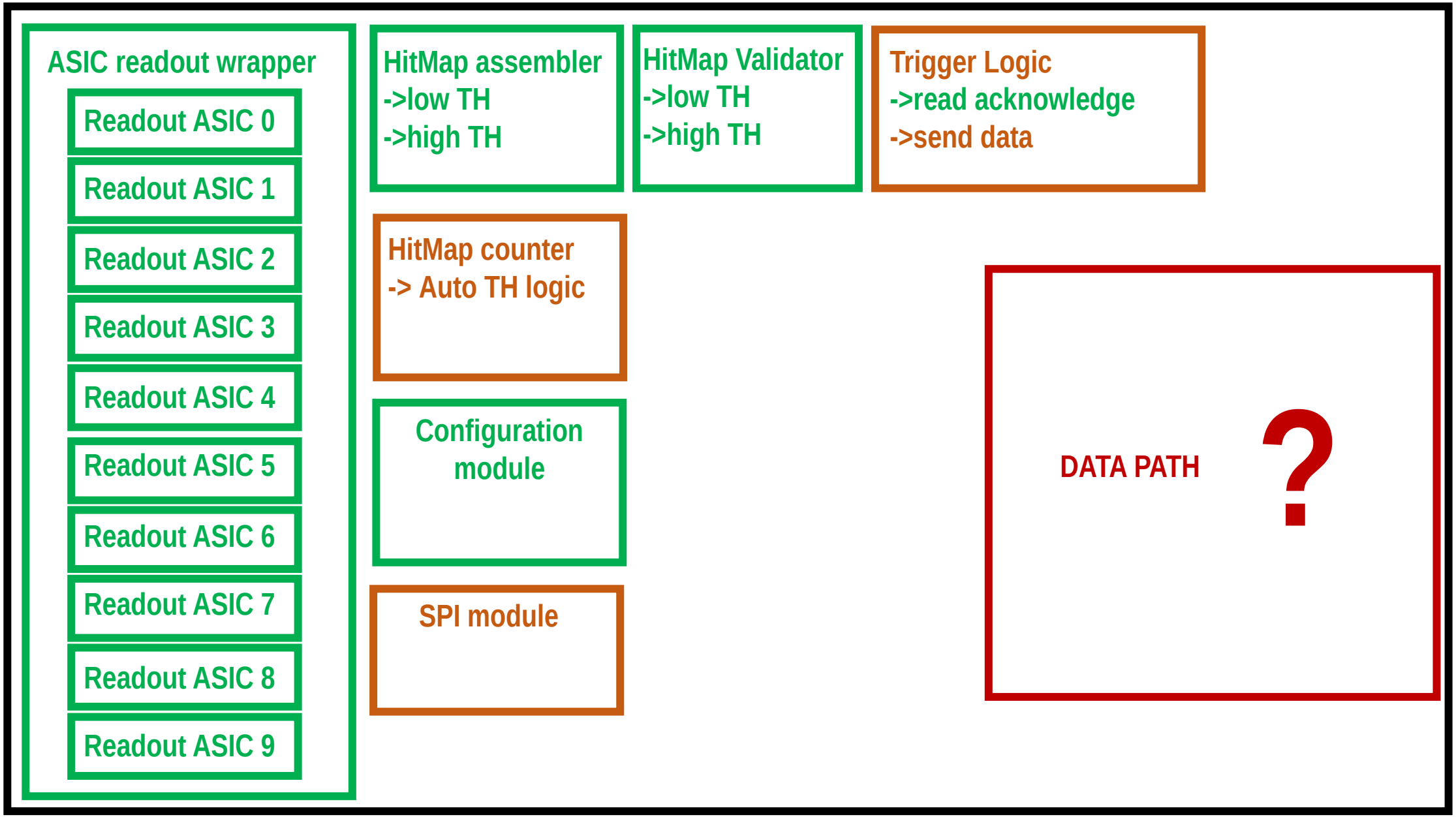


Name	Slice LUTs (203800)	Slice Registers (407600)	F7 Muxes (101900)	F8 Muxes (50950)	Slice (50950)	LUT as Logic (203800)	LUT as Memory (64000)	Block RAM Tile (445)	Bonded IOB (500)	IDELAYCTRL (10)	IBUFDS (480)	IDELAYE2/IDELAYE2_FINEDELAY (500)	ILOGIC (500)	OLOGIC (500)	BUFGCTRL (32)	MMCME2_ADV (10)	BUFHCE (168)
terzina_fw	42517	35849	789	289	17735	42484	33	34.5	128	2	16	21	20	1	7	2	4
clk_generator (clk_wiz_0)	0	24	0	0	3	0	0	0	0	0	1	0	0	0	4	1	3
clk_generator_GbPHY (clk_wiz_GbPHY)	0	8	0	0	1	0	0	0	0	0	0	0	0	0	3	1	1
GbPHY_inst (GbPHY)	2684	3874	51	0	1438	2684	0	12	0	0	0	11	0	1	0	0	0
terzina_processing_inst (terzina_processing)	39799	31902	738	289	16552	39766	33	22.5	0	0	10	10	20	0	0	0	0
ASIC_receiver_inst (ASIC_receiver)	1191	510	0	0	384	1191	0	0	0	0	10	10	20	0	0	0	0
command_executer_inst (command_execute	159	224	4	0	193	159	0	0	0	0	0	0	0	0	0	0	0
config_inst (config)	15561	381	28	0	4506	15561	0	0	0	0	0	0	0	0	0	0	0
HitMapAssembler_inst (HitMapAssembler)	7958	2990	98	1	3517	7928	30	20	0	0	0	0	0	0	0	0	0
HitMapSender_inst (HitMapSender)	120	279	0	0	126	117	3	2.5	0	0	0	0	0	0	0	0	0
HitValidator_High_Th_inst (HitValidator__par	259	741	0	0	578	259	0	0	0	0	0	0	0	0	0	0	0
HitValidator_Low_Th_inst (HitValidator)	261	739	0	0	615	261	0	0	0	0	0	0	0	0	0	0	0
RateController_inst (RateController)	22193	25641	608	288	10893	22193	0	0	0	0	0	0	0	0	0	0	0
SpiController_generate[0].SpiController_inst	52	59	0	0	31	52	0	0	0	0	0	0	0	0	0	0	0
SpiController_generate[1].SpiController_inst	52	59	0	0	30	52	0	0	0	0	0	0	0	0	0	0	0
SpiController_generate[2].SpiController_inst	53	59	0	0	27	53	0	0	0	0	0	0	0	0	0	0	0
SpiController_generate[3].SpiController_inst	52	59	0	0	30	52	0	0	0	0	0	0	0	0	0	0	0
SpiController_generate[4].SpiController_inst	52	59	0	0	29	52	0	0	0	0	0	0	0	0	0	0	0
TriggerLogic_inst (TriggerLogic)	20	35	0	0	16	20	0	0	0	0	0	0	0	0	0	0	0


X0Y5
X1Y5
X0Y4
X1Y4
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


terzina_fw
115563
terzina_processing_inst
107585
RateController_inst
64568
Leaf Cells
64568
config_inst
24481
Leaf Cells
24481
HitMapAssembler_inst
12645
Leaf Cells
12265
Leaf Cells

BACKUP


ASIC readout wrapper
Readout ASIC 0
Readout ASIC 1
Readout ASIC 2
Readout ASIC 3
Readout ASIC 4
Readout ASIC 5
Readout ASIC 6
Readout ASIC 7
Readout ASIC 8
Readout ASIC 9
HitMap assembler
->low TH
->high TH
HitMap Validator
->low TH
->high TH
Trigger Logic
->read acknowledge
->send data
HitMap counter
-> Auto TH logic
Configuration module
SPI module
DATA PATH
?

TO DO LIST

- Trigger logic
- HitMap assembler and HitMap validator
- Configuration Module
-
- Auto Rate Calculator and Threshold setting
- Data path and data selector

FIRMWARE REPORTS

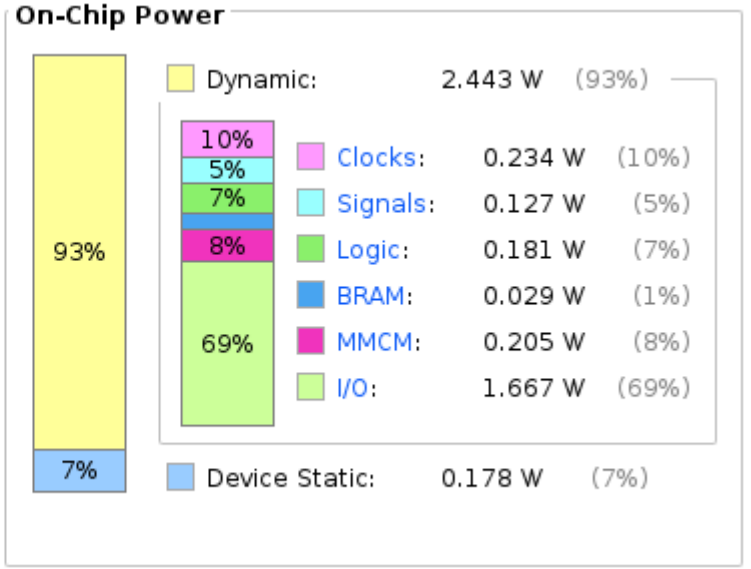
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.079 ns	Worst Hold Slack (WHS):	0.043 ns	Worst Pulse Width Slack (WPWS):	0.264 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	168155	Total Number of Endpoints:	168113	Total Number of Endpoints:	63617

All user specified timing constraints are met.

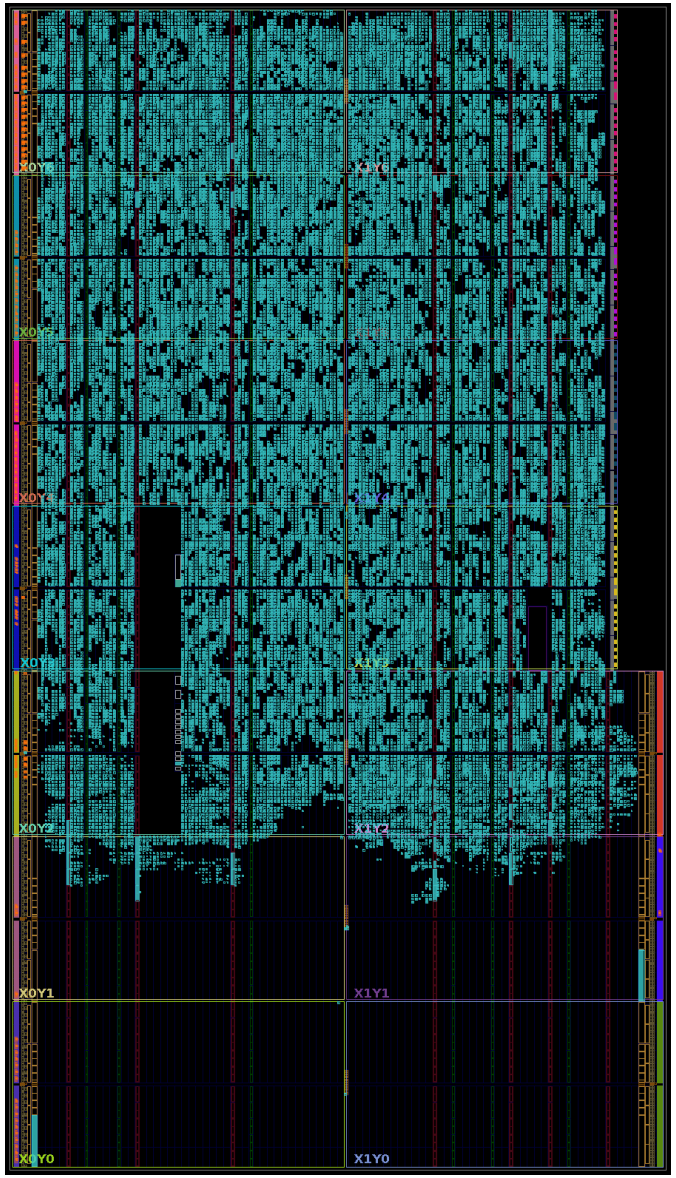
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.621 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.7°C**
Thermal Margin:	55.3°C (30.4 W)
Effective ϑJA:	1.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



FIRMWARE DESIGN HIERARCHY



FIRMWARE RESOURCES UTILIZATION

Name	Slice LUTs (203800)	Slice Registers (407600)	F7 Muxes (101900)	F8 Muxes (50950)	Slice (50950)	LUT as Logic (203800)	LUT as Memory (64000)	Block RAM Tile (445)
terzina_fw	34.54%	15.47%	1.38%	1.32%	59.49%	34.45%	0.29%	7.75%
clk_generator (clk_wiz_0)	0.00%	<0.01%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%
clk_generator_GbPHY (clk_wiz_GbPHY)	0.00%	<0.01%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%
dbg_hub (dbg_hub)	0.22%	0.18%	0.00%	0.00%	0.48%	0.21%	0.04%	0.00%
GbPHY_inst (GbPHY)	1.29%	0.92%	0.05%	0.00%	2.61%	1.29%	0.00%	2.70%
terzina_processing_inst (terzina_processing)	33.03%	14.36%	1.33%	1.32%	56.65%	32.95%	0.25%	5.06%
ASIC_receiver_inst (ASIC_receiver)	1.15%	0.25%	0.00%	0.00%	1.79%	1.15%	0.00%	0.00%
command_executer_inst (command_execute	0.42%	0.39%	<0.01%	0.00%	1.13%	0.36%	0.20%	0.56%
config_inst (config)	9.71%	0.06%	0.01%	<0.01%	10.20%	9.71%	0.00%	0.00%
HitMapAssembler_inst (HitMapAssembler)	3.69%	0.73%	0.00%	0.00%	6.58%	3.68%	0.05%	4.49%
HitValidator_High_Th_inst (HitValidator__par	0.07%	0.16%	0.00%	0.00%	1.04%	0.07%	0.00%	0.00%
HitValidator_Low_Th_inst (HitValidator)	0.06%	0.16%	0.00%	0.00%	1.10%	0.06%	0.00%	0.00%
RateController_inst (RateController)	23.03%	12.57%	1.32%	1.32%	43.43%	23.03%	0.00%	0.00%
SpiController_inst (SpiController)	0.02%	0.01%	0.00%	0.00%	0.04%	0.02%	0.00%	0.00%
TriggerLogic_inst (TriggerLogic)	0.01%	0.02%	0.00%	0.00%	0.09%	0.01%	0.00%	0.00%