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Terzina: camera architecture meeting
ASIC update

A. Di Salvo[1], S. Garbolino[1], S. Zugravel[1, 2],
A. Rivetti[1], M. E. Bertaina[1, 3], Antonio Palmieri[1, 3]

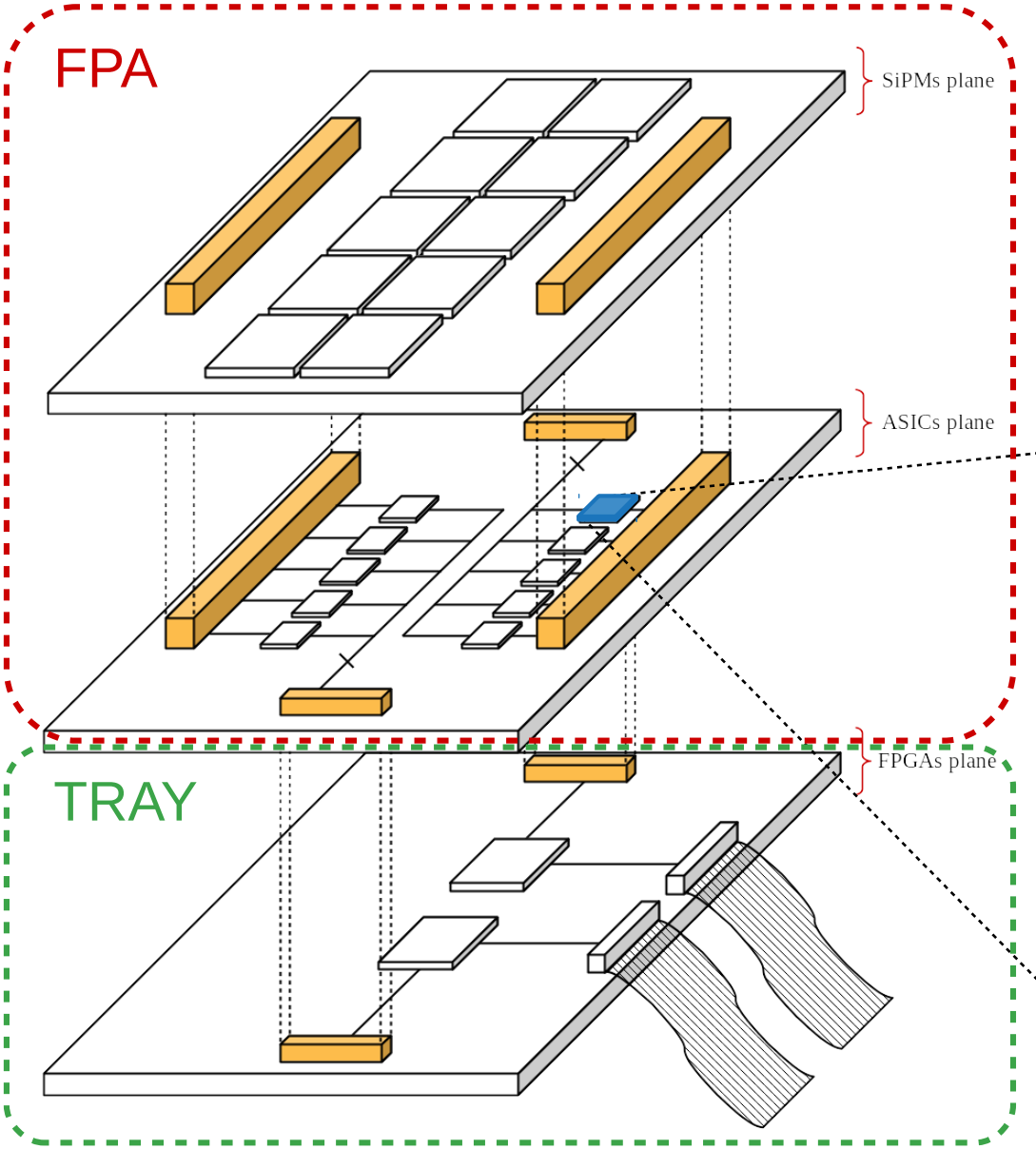
Politecnico di Torino

[1] National Institute for Nuclear Physics, Section of Torino, Torino, Italy

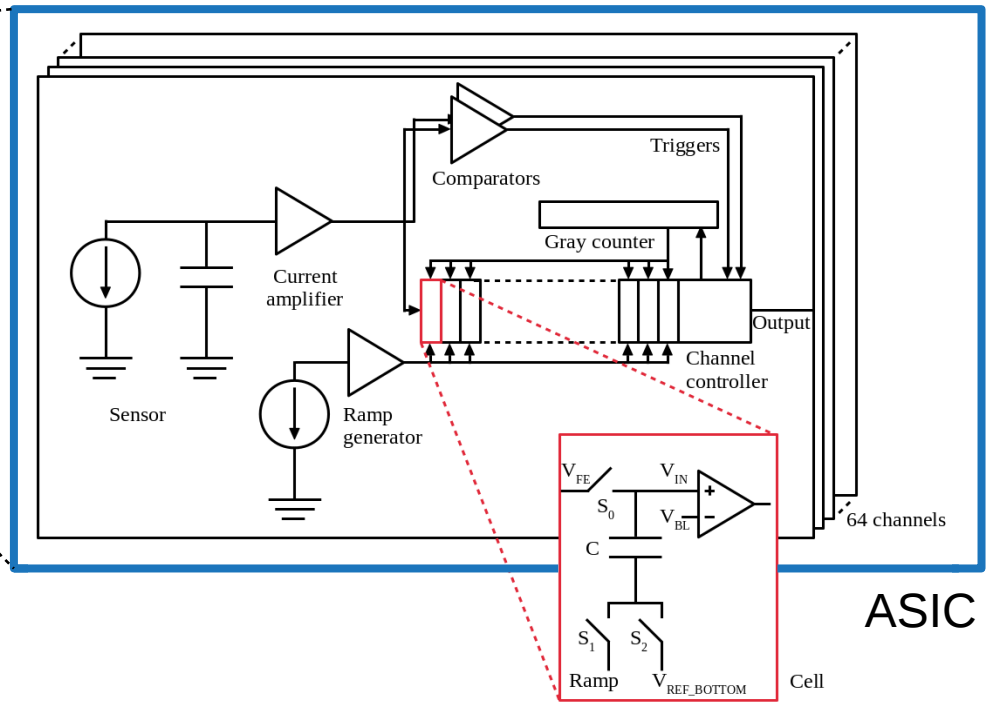
[2] Politecnico di Torino, Dipartimento di Elettronica e Telecomunicazioni, Torino, Italy

[3] University of Torino, Physics, Torino, Italy

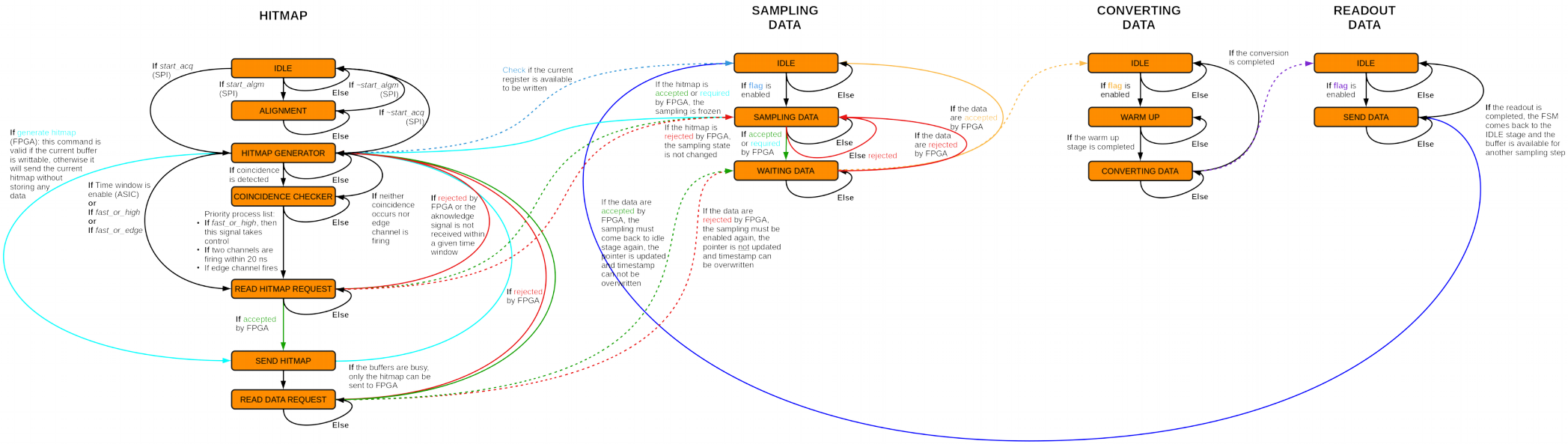
Camera and ASIC architecture



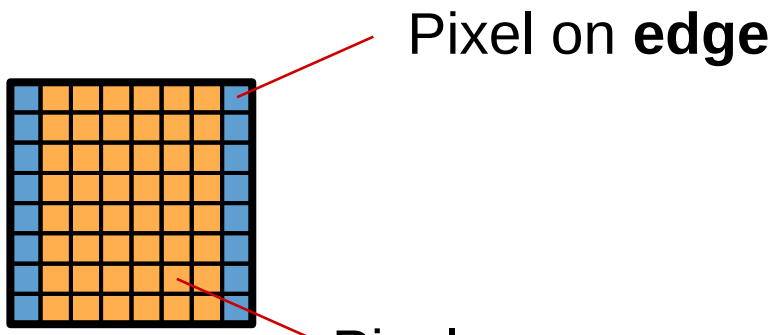
- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.



Hitmap logic

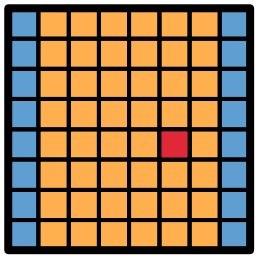


- New hitmap logic.
- Pixel configurability: core or edge.
- **Core**: dedicated combinatorial circuit based on fast-OR chains to detect ≥ 2-pixels coincidence.
- **Edge**: programmable fast-OR chain reserved to the edge detection.



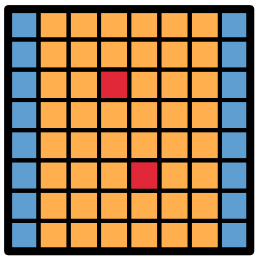
Hitmap logic

- High threshold (core + edge)



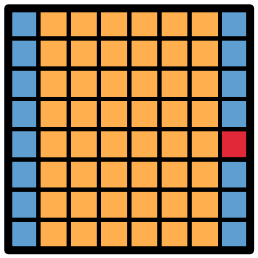
- Condition continuously checked.
- If verified, a read hitmap request is generated.

- Low threshold (core)



- Condition to verify: ≥ 2 pixels on the core.
- Coincidence checked within a programmable window (~20 ns).

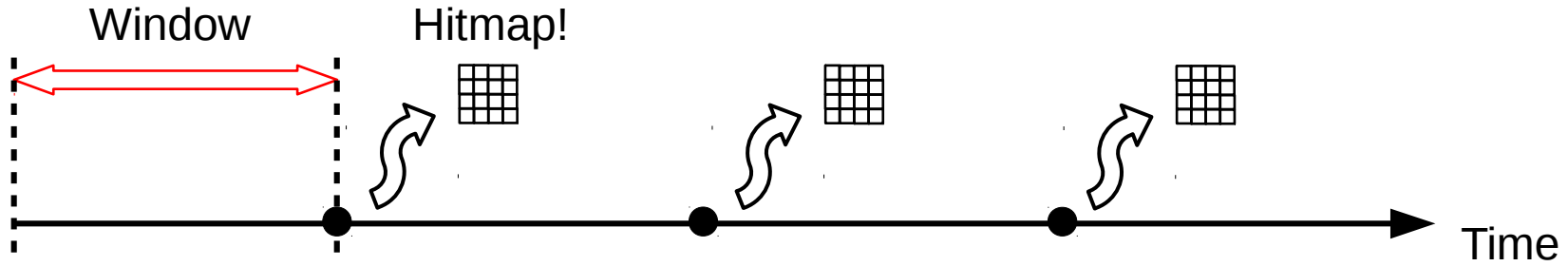
- Low threshold (edge)



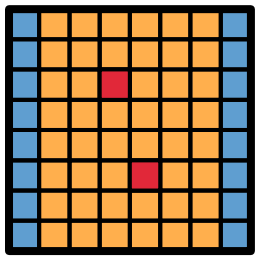
- Condition to verify: 1 pixel firing on the edge.
- An electrical scheme of the physical connection with the SiPMs is required.

Hitmap logic

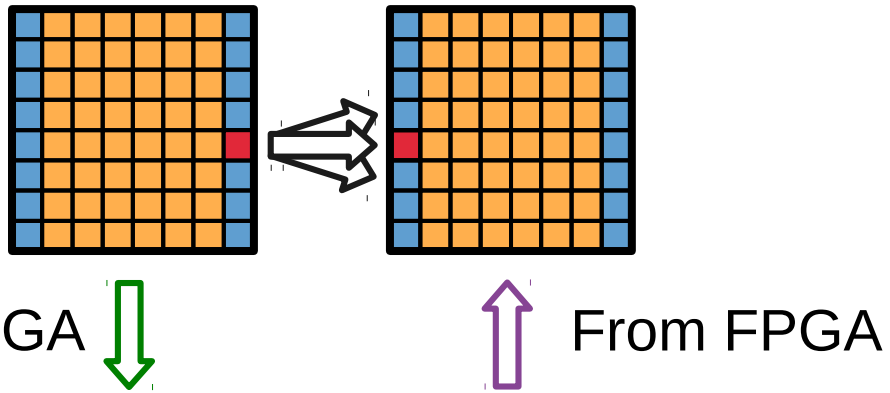
- **TIME WINDOW**



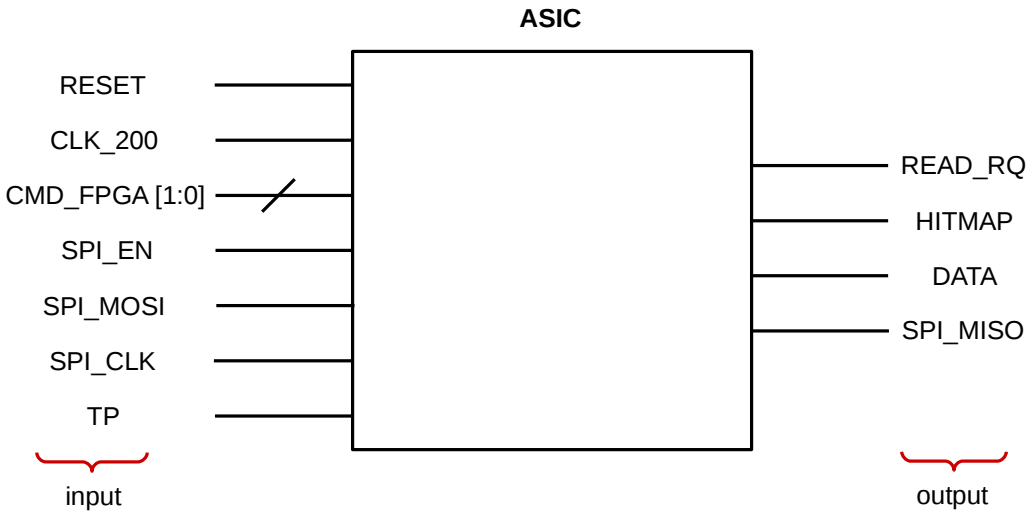
- **HIGH THRESHOLD + COINCIDENCE + EDGE DRIVEN**



- **FPGA REQUEST**



Serial bus



- **12** differential LVDS lines.
- Communication with a clock at **400 MHz** in DDR.
- To configure the ASIC: 1 dedicated **SPI**.
- 240 communication lines for the ASIC board + 640 connections with SiPMs.

PIN name	Description	Total LVDS lines
	From FPGA to ASIC	
RESET	Reset signal	20
CLK_200	Clock signal	20
CMD_FPGA	Read acknowledge signal	40
SPI_EN	SPI enable	20
SPI_MOSI	SPI mosi	20
SPI_CLK	SPI clock	20
T_P	Test Pulse	20
	From ASIC to FPGA	
SPI_MISO	SPI miso	20
READ_RQ	Read request from ASIC	20
DATA	Physics data	20
HITMAP	Hitmap data	20
	From FPGA to DPCU	
CLK	DATA PORT (MASTER)	4
CS	DATA PORT (MASTER)	4
MOSI 0	DATA PORT (MASTER)	4
MOSI 1	DATA PORT (MASTER)	4
MOSI 2	DATA PORT (MASTER)	4
MOSI 3	DATA PORT (MASTER)	4
CLK	SLOW CONTROLL (SLAVE)	2
CS	SLOW CONTROLL (SLAVE)	2
MOSI	SLOW CONTROLL (SLAVE)	2
MIS0	SLOW CONTROLL (SLAVE)	2
CLK	SYNC	4
TRG OUT	SYNC	4
TRG IN	SYNC	4
VALIDATION	SYNC	4
BUSY	SYNC	2
TRG	SYNC	2

Total number of lines ASIC-FPGA	240
Total number of lines FPGA-DPCU	52
Total number of FPGA I/O lins	292

Roadmap

- To complete behavioural simulations with frozen specifics.
- Circuital synthesis.
- Place & Route.
- Analog blocks integration.
- Signoff + verification.

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