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# Hardware acceleration for fast MRF map reconstruction: FPGA porting of a deep learning algorithm

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Magnetic Resonance Fingerprinting (MRF) is an MR imaging technique that allows for the reconstruction of brain parameters within the same acquisition session. Despite its strengths, MRF implies a large amount of data to be processed and a complex analytical function that is not well defined. Recently, a neural network (NN) has been proposed to reconstruct brain quantitative maps starting from the MRF signal. While the NN offers rapid parameter estimation once trained, its training demands substantial computational resources and time. To address this challenge, hardware accelerators like Field-Programmable Gate Arrays (FPGAs) are increasingly replacing traditional software-based tools, significantly enhancing processing speed and reducing power consumption in MR image analysis. By redesigning the original NN onto an FPGA, the project aims to dramatically reduce reconstruction time for both simulated and real clinical MR parameter maps. The NN needs to be quantized to meet the available hardware resources of an FPGA without affecting the accuracy of the model. This multidisciplinary approach has the potential to outperform traditional software in speed and energy efficiency, paving the way for real-time brain analysis, even on mobile devices. This could revolutionize clinical decision-making and telemedicine by enabling faster, more efficient, and potentially more accessible brain imaging.

## Field

Software and quantification

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