Recent developments of CMOS pixel sensors and their applications to high energy physics experiments

Giornate di Studio sui Rivelatori

Cogne

June 26th - 30th, 2023

Manuel Rolo (INFN)

Si Pixel sensors: where&when to start? …

ISSCC

FRIDAY, FEBRUARY 11, 1966 … UNIVERSITY MUSEUM/UNIV. OF PENNSYLVANIA … 1:30-4:30 P.M.

SESSION XI: Digital Applications of Field-Effect Transistors

FPM 11.4: A Thin-Film Solid-State Image Sensor*

P. K. Weimer, G. Sadasiv, H. Borkan, L. Meray-Horvath, J. Meyer,

RCA Laboratories

Princeton, N. J.

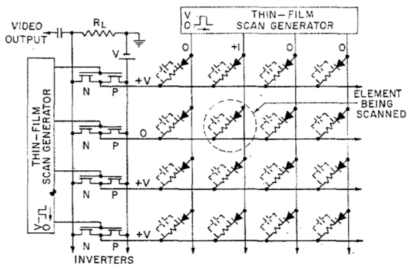


FIGURE 6—One method of coupling out the video signal from an array of photoconductor-diode elements. Alternatively, the complementary inverters can be replaced by a single column of transistors.

1965 International Electron Devices Meeting

4.5 A MONOLITHIC MOSAIC OF PHOTON SENSORS FOR SOLID STATE IMAGING APPLICATIONS, M. A. Schuster and G. Strull, Westinghouse Electric Corp., Baltimore, Md.

Monolithic silicon mosaics of photosensor elements have been developed for solid state imaging applications. The physical structure, design features, and performance characteristics of these electro-optical devices will be presented.

IEEE ELECTRON DEVICE LETTERS, VOL. EDL-1, NO. 9, SEPTEMBER, 1980

Amorphous-Silicon Image Sensor IC

M. MATSUMURA, MEMBER, IEEE, H. HAYAMA, Y. NARA AND K. ISHIBASHI

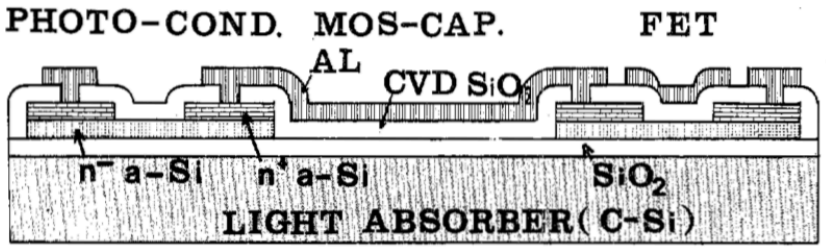


Figure 1. The unit cell structure of the proposed image sensor IC.

IEEE TRANSACTIONS ON PARTS, HYBRIDS, AND PACKAGING, VOL. PHP-10, NO. 3, SEPTEMBER 1974

A Hybrid Integrated Silicon Diode Array for Visible Earth-Horizon Sensing

FRANK J. BACHNER, MEMBER, IEEE, RONALD A. COHEN, MEMBER, IEEE, ROBERT W. MOUNTAIN, WILLIAM H. MC GONAGLE, AND ARTHUR G. FOYT, MEMBER, IEEE

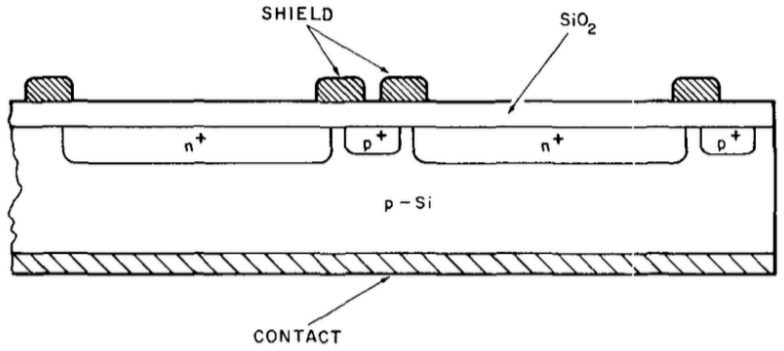


Fig. 2. Cross-section of a portion of an eight diode array showing the n^+ active region, the p^+ channel stop, the passivating oxide and the metal edge-shields.

Si Pixel sensors: where&when to start?…

Semiconductor
Nuclear Particle Detectors

Proceedings of an Informal Conference

Asheville, N. C., September 28-30, 1960

Foreword

The progress of science has always followed the development of the experimental arts, and this has been as true in nuclear physics as it has been in astronomy, chemistry and biology. One has only to mention the ionization counter, the cloud chamber, the scaling circuit, nuclear emulsions, magnetic spectrometers, the modern scintillators, and the bubble chamber to bring to mind the historical framework of experimental nuclear physics. To this distinguished lineage we may now have to add the semi-conductor detector. Certainly it looks like a worthy candidate for such a position; its speed and generosity of response, linearity of pulse height with particle energy, small size, cheapness and modest requirement as to power supply, place it in a class by itself, and anything in a class by itself is likely to go a long way.

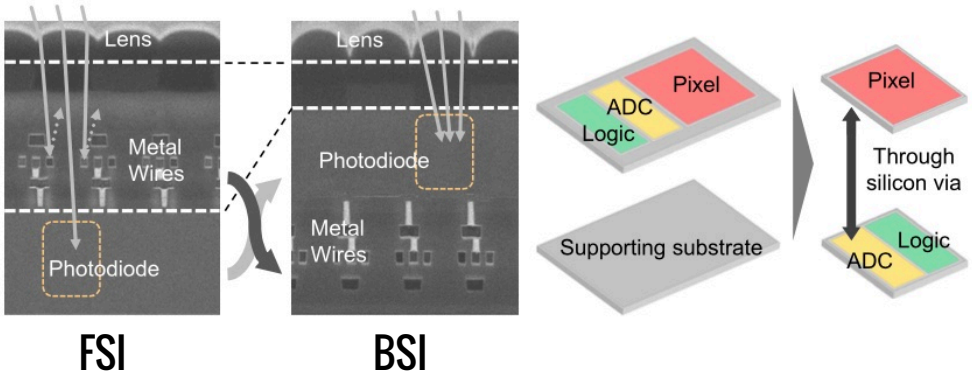
Arthur H. Snell
Chairman, Subcommittee on
Instruments and Techniques

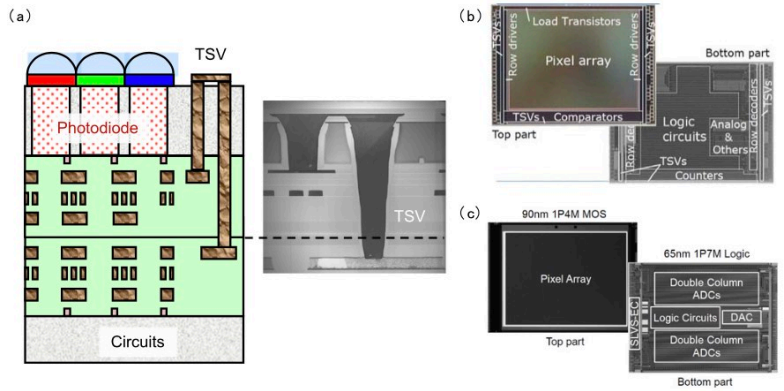
CMOS image sensors

in Cogne (GSR School) 6 years ago...

CMOS image sensors… are everywhere!

- CMOS Active Pixel Sensor is today a mature technology and a steady leader in the image sensor market
- Front-side-illumination on state-of-the-art CMOS imager pixels O(1μm) limits light incidence
- BSI devices have BEOL below the photodiode region, avoiding reflection of the incident light
- Ramping up interest on 3D stacked sensors, using TSVs and employing vertical integration of sensor and readout&processing tiers
- Combination of BSI, 3D integration and CMOS deep sub-micron technologies should allow for 100% fill-factor, high-speed signal digitisation and processing on CMOS sensors

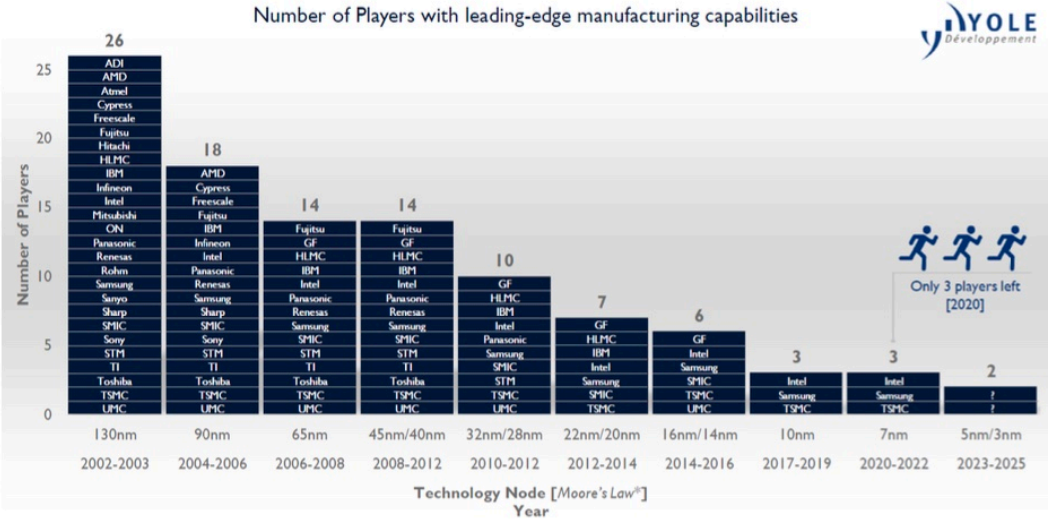




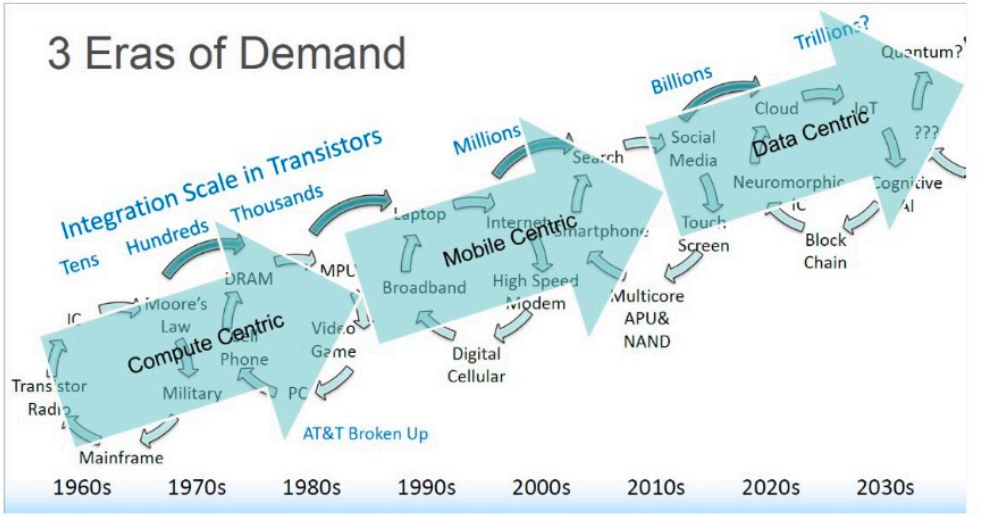
Y. Oike, "Evolution of Image Sensor Architecture With Stacked Device Technologies," in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2021.3097915

Drivers for 3D Integration

2D-Moore's law is slowing down



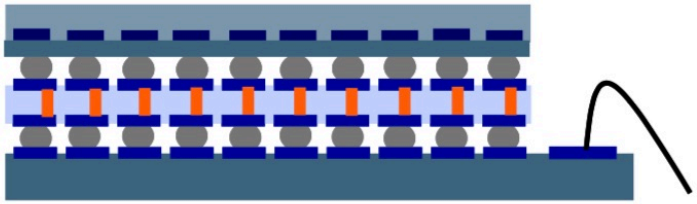
- **Technical issues and associated costs to:**
  - **Produce the chips:**
    - 2-3nm fab. => CAPEX: 30B$
    - EUV Litho: 120-150M$ for 7nm
  - **Design the chips:**
    - 7nm => 300M$
    - 5nm => 550M$



Move to a System Approach (SoC or SiP)

ECFA Detector R&D Roadmap Symposium of Task Force 7 Electronics and On-detector Processing, Christophe Wyon

3D Integration - concept



- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
    - Example: passive photodetector layer + analog ROIC + digital image processor
  - Using high density bumping + area redistributed TSVs
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

P. De Moor (IMEC)

Stacked chips and interconnection

- **C4**: **c**ontrolled-**c**ollapse **c**hip **c**onnection
- developed by IBM in the 1960s and widely used for high-I/O-count applications
  - solder is placed on a conductive pad in electrical connection with the integrated circuit (IC) of the semiconductor die
  - semiconductor die heated to bond the solder to the pad
  - the solder then forms a spherical shape due to the surface tension of the solder
  - in conventional C4 structures, spherical solder deposits are referred to as "solder bumps."

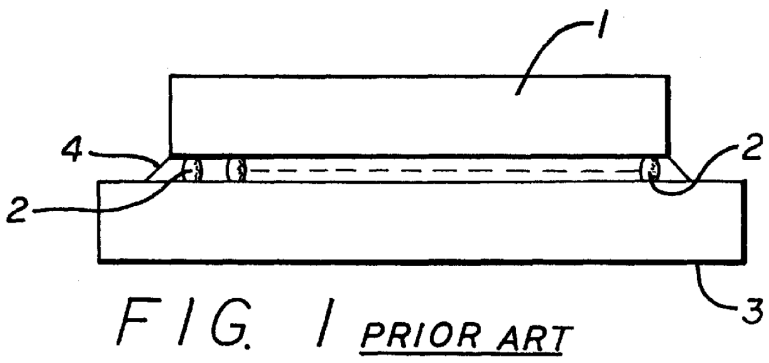
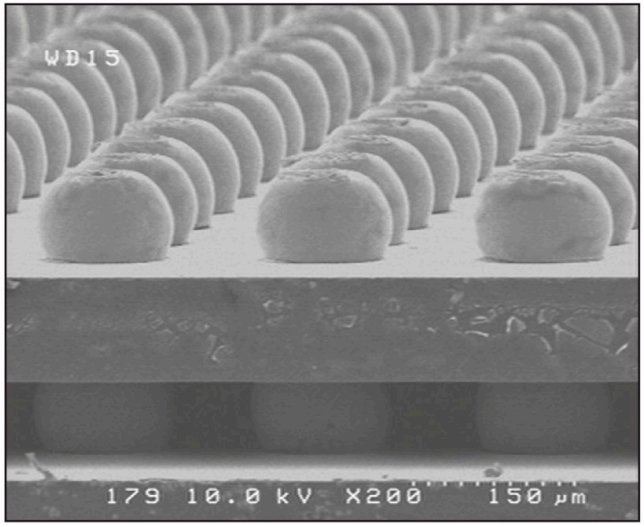
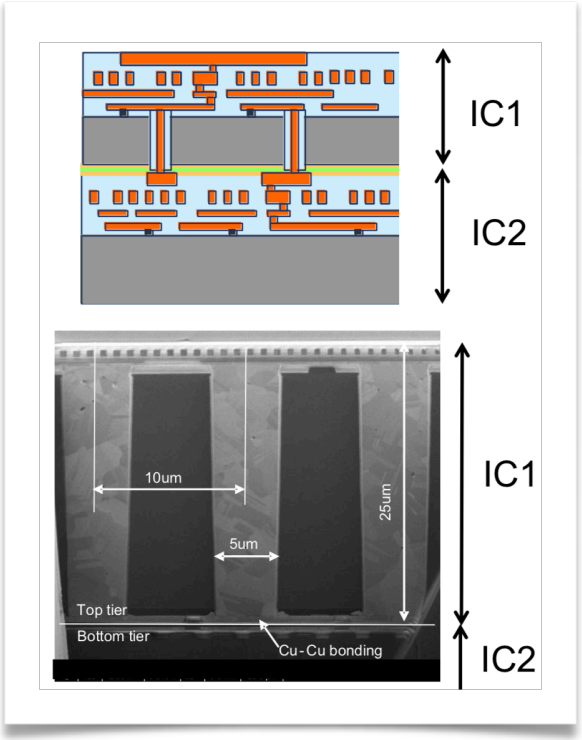


FIG. 1 PRIOR ART



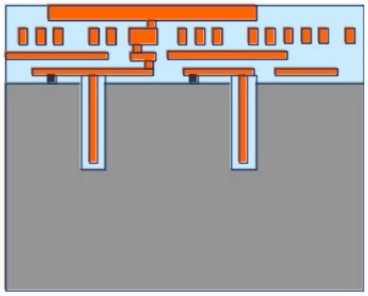
3D IC Process Flow

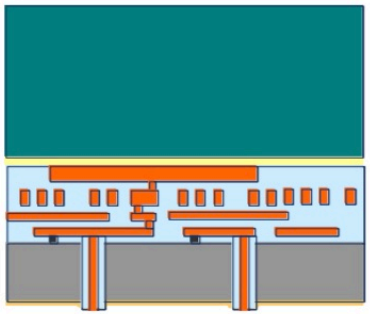


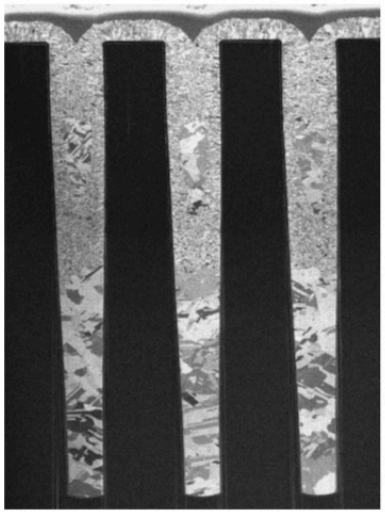
P. De Moor (IMEC)

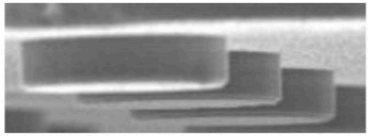
Via processing

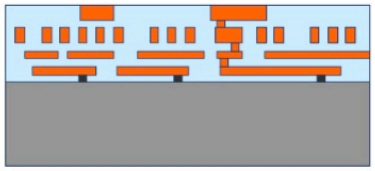
Extreme thinning (on carrier)



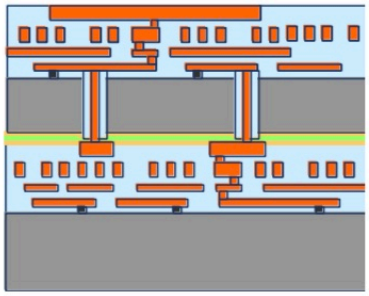


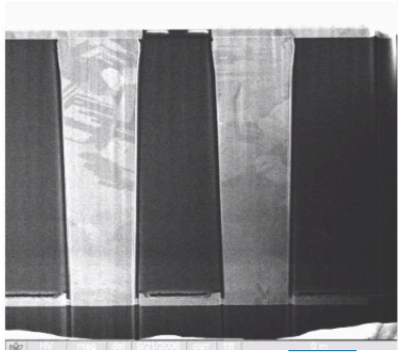






Mixed polymer and Cu-Cu thermocompression bonding





Advanced 3D Integration

ISSCC 2019 / SESSION 5 / IMAGE SENSORS / 5.7

5.7 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

Robert K. Henderson[1], Nick Johnston[1], Sam W. Hutchings[1], Istvan Gyongy[1], Tarek Al Abbas[1], Neale Dutton[2], Max Tyler[3], Susan Chan[3], Jonathan Leach[3]

[1]University of Edinburgh, Edinburgh, United Kingdom
[2]STMicroelectronics, Edinburgh, United Kingdom
[3]Heriot-Watt University, Edinburgh, United Kingdom

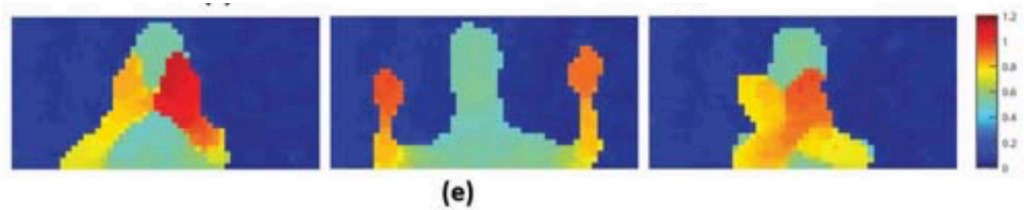
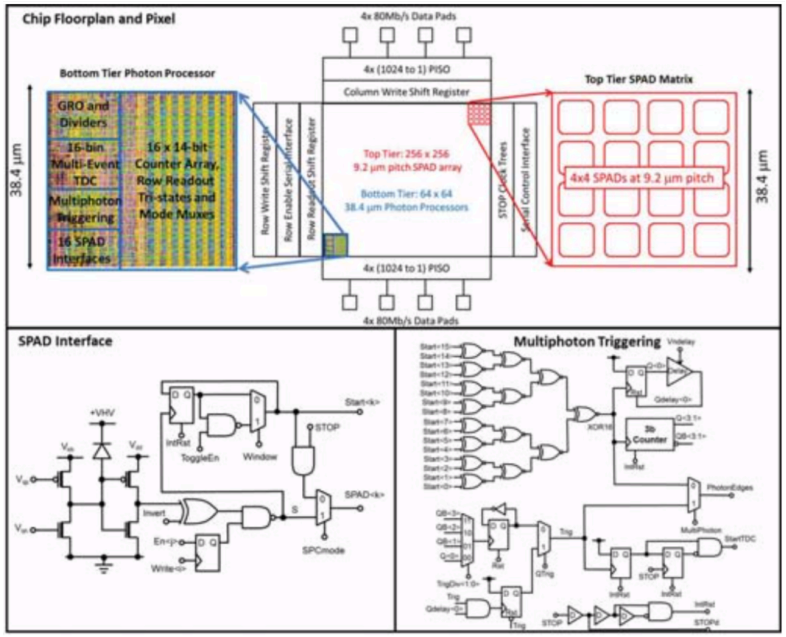
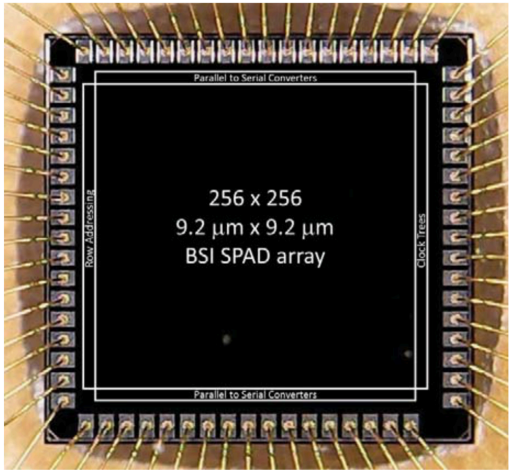


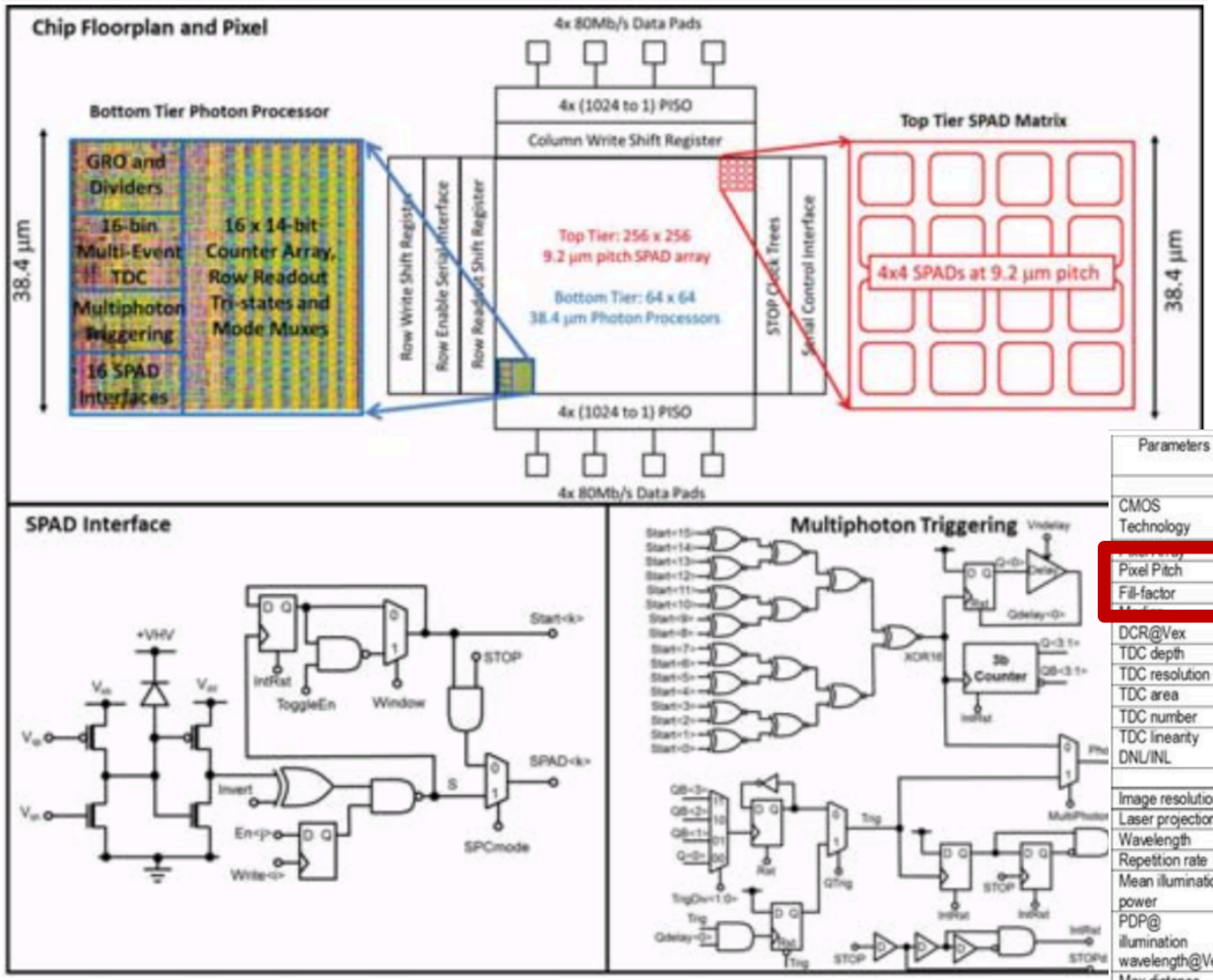
Figure 5.7.5: In-pixel histogramming mode: (a),(b) two-step timing schemes for LIDAR; (c) distance sweep over 1.6m; (d) histogram bin uniformity over full array; (e) 3 images from a 30fps movie taken at 50m.



Parameters	Units	This Work	[3]	[4]	[5]	[1]
Sensor						
CMOS Technology	-	**40nm/90nm**	180nm	45nm/65nm	150nm	180nm
Pixel Array	-	**256x256/64x64**	252x144	16x8	64x64	16x1/32x1
Pixel Pitch	µm	**9.2/38.4**	28.5	19.8	60	21
Fill-factor	%	**51**	28	31.3/50.6	26.5	70
Median DCR@Vex	cps	**20@1.5V**	195 @5V	5.3k@2.5V	6.8k@3V	2.65k@NA
TDC depth	bits	**14/4**	12	14	16/15	12
TDC resolution	ps	**35/560**	48.8	60-320	250-20000	208
TDC area	µm²	**130/150**	4200	550	NA	NA
TDC number	-	**4096**	1728	1	4096	64
TDC linearity DNL/INL	LSB	**+0.05/-0.05 +0.1/-0.08**	+0.6/-0.48 +0.89/-1.67	+0.8/-0.7 +3.4/-0.8	+1.2/-1 +4.8/-3.2	+0.15/-0.17 +0.32/-0.56
LIDAR Measurement						
Image resolution	-	**64x64**	252x144	256x256	64x64	202x96
Laser projection	-	**Flash**	Flash	Scanning	Flash	Scanning
Wavelength	nm	**671**	637	532	470	870
Repetition rate	MHz	**1.9**	40	1	NA	0.133
Mean illumination power	mW	**1.8**	2	6	NA	21
PDP@ illumination wavelength@Vex	%	**23@3V**	33.7@5V	21@2.5V	20@3V	NA
Max distance	m	**50**	50	150-430	367-5862	128
Imaging range	m	**50**	0.7	4.5	NA	100
FOV	deg	**1.2x1.2**	40x20	NA	NA	
Accuracy	m(%)	**0.17(0.34)**	0.088(0.17)	0.07(0.3)	1.5(0.37)	11(0.11)
Background light	-	**1klux**	dark	NA	100M/pix/s	70 klux
Target reflectivity	-	**white**	white	white	NA	9%
Power consumption	mW	**77.6**	2540	NA	93.5	530



Si Single-photon Avalanche Detectors

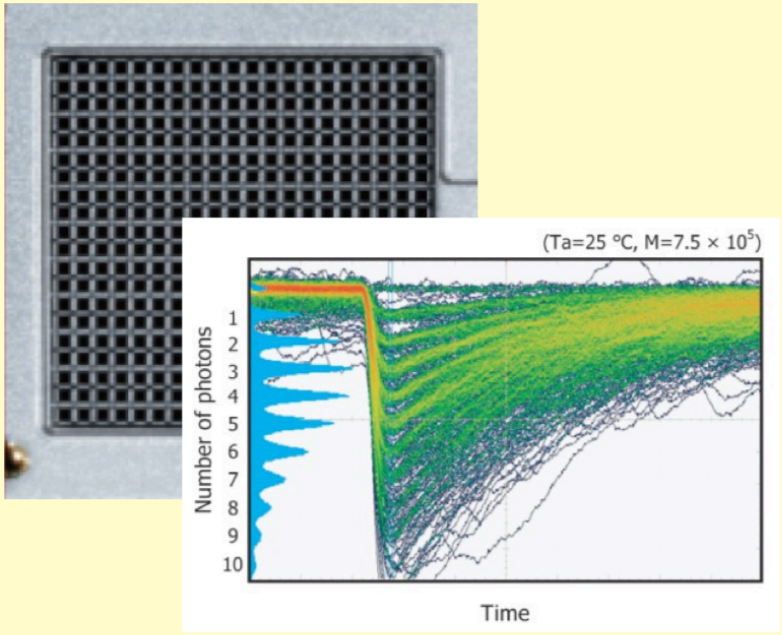


mini-SiPM (16 SPADs)

Parameters	Units	This Work	[3]	[4]	[5]	[1]
			Sensor			
CMOS Technology	-	**40nm/90nm**	180nm	45nm/65nm	150nm	180nm
			252x144	16x8	64x64	16x1/32x1
Pixel Pitch	µm	**9.2/38.4**	28.5	19.8	60	21
Fill-factor	%	**51**	28	31.3/50.6	26.5	70
			95 @5V	5.3k@2.5V	6.8k@3V	2.65k@NA
DCR@Vex						
TDC depth	bits	**14/4**	12	14	16/15	12
TDC resolution	ps	**35/560**	48.8	60-320	250-20000	208
TDC area	µm²	**130/150**	4200	550	NA	NA
TDC number	-	**4096**	1728	1	4096	64
TDC linearity	LSB	**+0.05/-0.05**	+0.6/-0.48	+0.8/-0.7	+1.2/-1	+0.15/-0.17
DNL/INL		**+0.1/-0.08**	+0.89/-1.67	+3.4/-0.8	+4.8/-3.2	+0.32/-0.56
			LIDAR Measurement			
Image resolution	-	**64x64**	252x144	256x256	64x64	202x96
Laser projection	-	**Flash**	Flash	Scanning	Flash	Scanning
Wavelength	nm	**671**	637	532	470	870
Repetition rate	MHz	**1.9**	40	1	NA	0.133
Mean illumination power	mW	**1.8**	2	6	NA	21
PDP@ illumination wavelength@Vex	%	**23@3V**	33.7@5V	21@2.5V	20@3V	NA
Max distance	m	**50**	50	150-430	367-5862	128
Imaging range	m	**50**	0.7	4.5	NA	100
FOV	deg.	**1.2x1.2**	40x20	NA	NA	
Accuracy	m(%)	**0.17(0.34)**	0.088(0.17)	0.07(0.3)	1.5(0.37)	11(0.11)
Background light	-	**1klux**	dark	NA	100M/pix/s	70 klux
Target reflectivity	-	**white**	white	white	NA	9%
Power consumption	mW	**77.6**	2540	NA	93.5	530

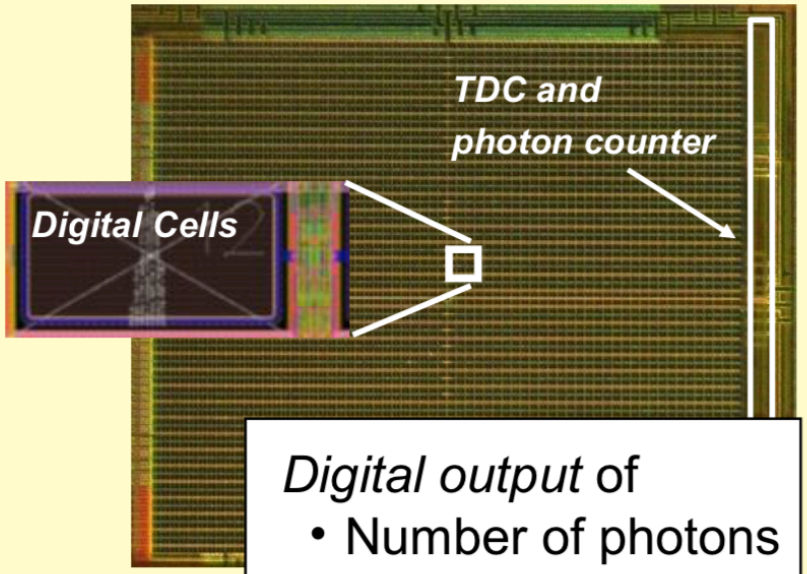
SPAD-based single-photon detectors

Analog SiPM



- Cells connected to common readout
- Analog sum of charge pulses
- Analog output signal

Digital SiPM



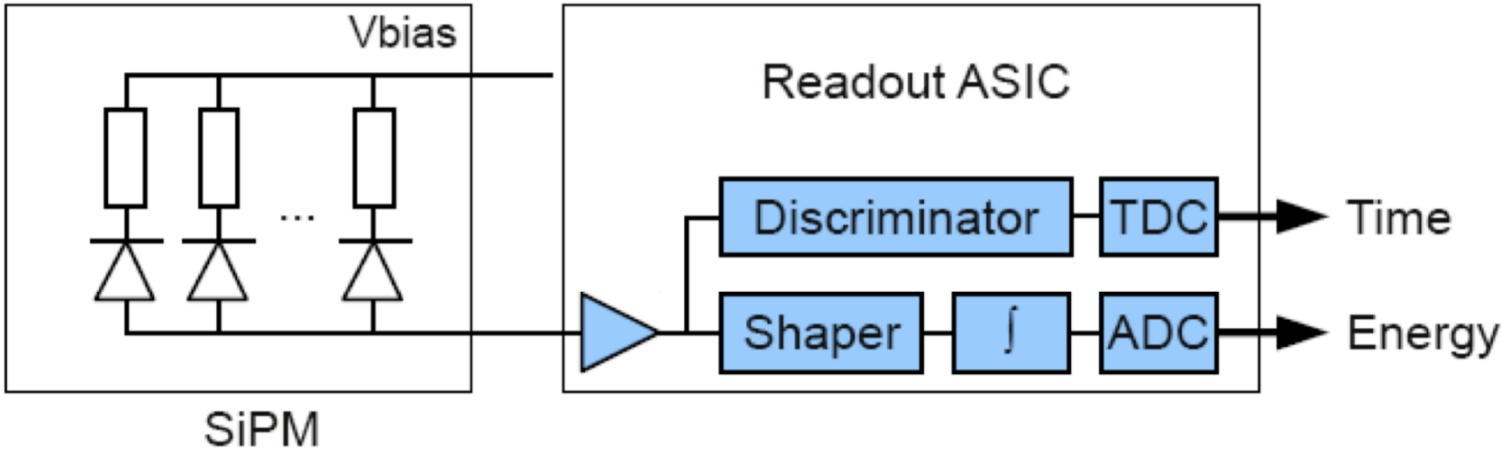
Digital output of
- Number of photons
- Time-stamp

- Each diode is a digital switch
- Digital sum of detected photons
- Digital data output

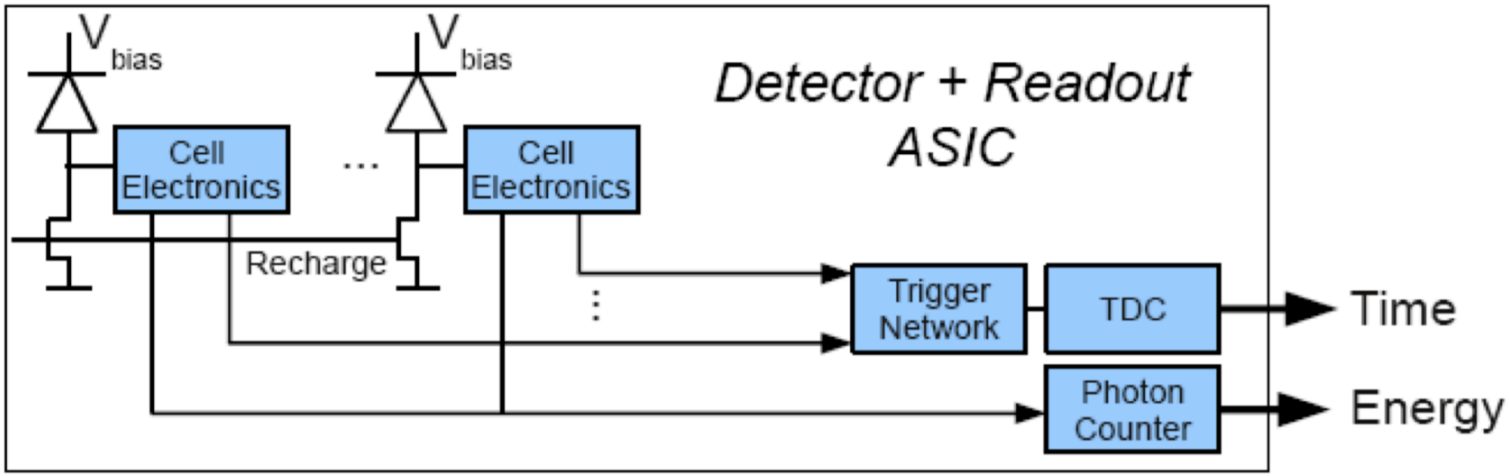
Thomas Frach (PHILIPS)

Analog vs. Digital SiPM

Analog Silicon Photomultiplier Detector



Digital Silicon Photomultiplier Detector



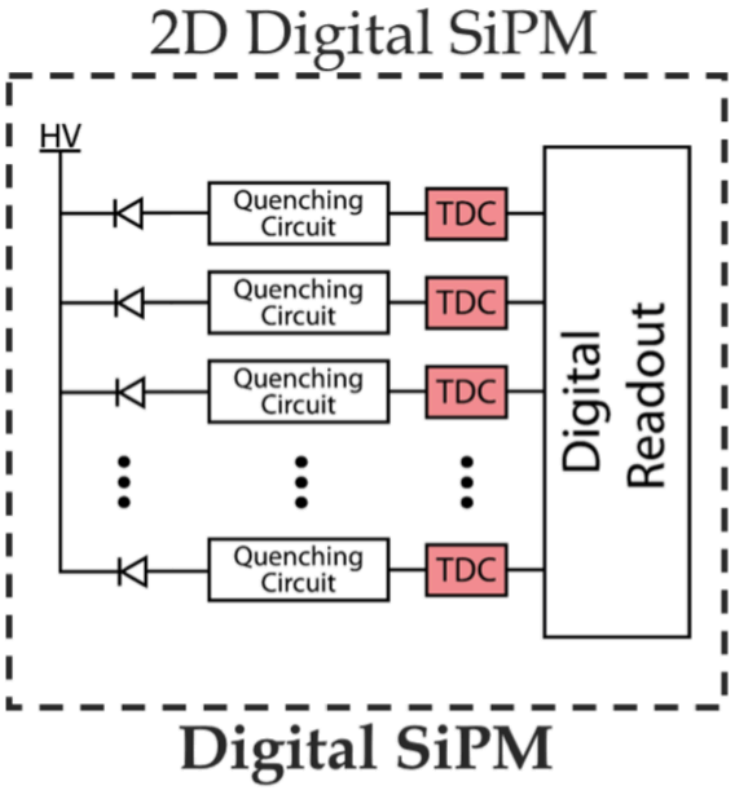
courtesy: York Hämisch

2D vs 3D Digital SiPM

Benefits of Digital SiPM for TOF-PET

Advantages
- 1 TDC per SPAD
- Uniform SPTR per pixel
- SPAD to SPAD skew correction

Cons of 2D implementation
- Low fill factor
- Same process for SPAD and CMOS
- No room for digital signal processing

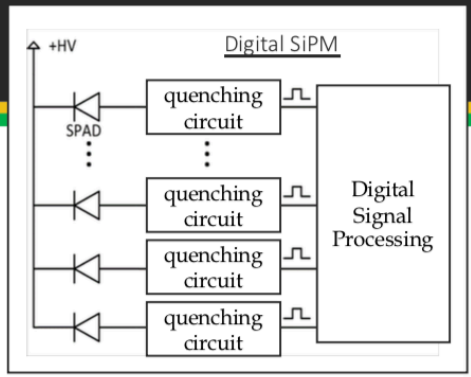


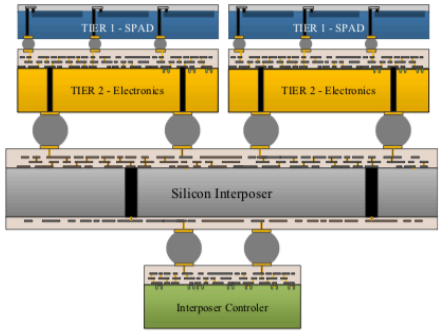
courtesy: J-F Pratte

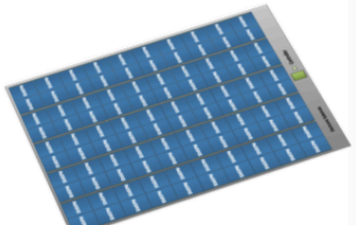
3D Digital SiPM

3D digital SiPM concept

- Digital SiPM to take advantage of the SPAD's digital nature
- 3D integration enables
  - Independent optimization of detector layer and readout electronics
  - One-to-one coupling minimizes digitization power, allows afterpulsing mitigation, enabling/disabling cells
  - One-to-one coupling between the SPAD and the Quenching circuit with uniform routing
  - One-to-one coupling provides greater immunity to process, voltage and temperature variations → picoseconds timing
  - Time-to-digital converter per pixel
- Promising new photodetectors
  - for fast timing applications: 10 ps time-of-flight PET or sub-ns calorimeters
  - for low background large scale experiments : in-situ digital processing







courtesy: Serge Charlebois

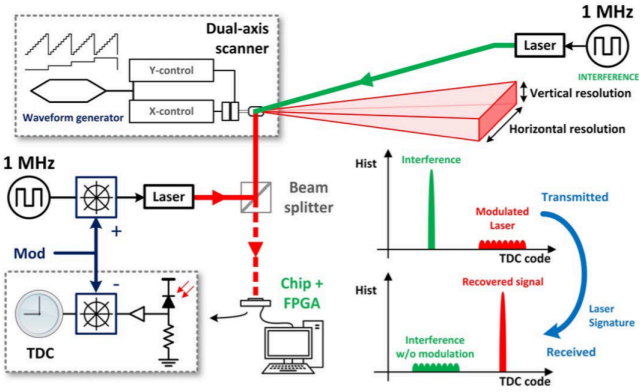
Advanced 3D Integration

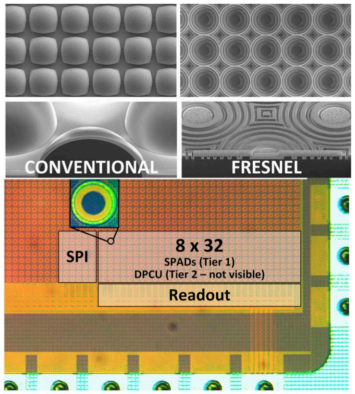
ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.9

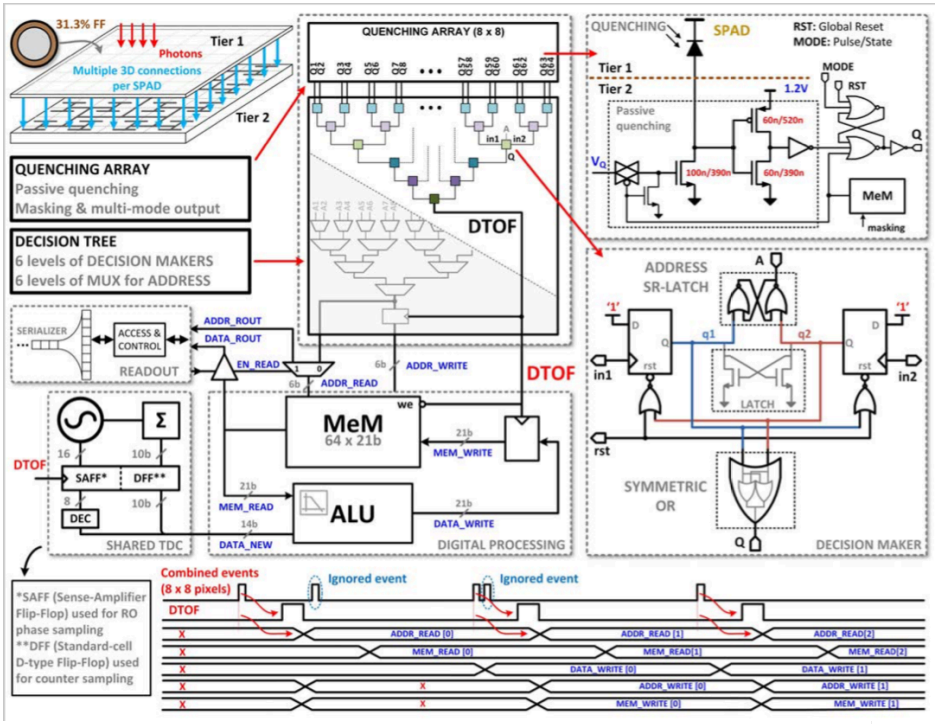
5.9 A 256×256 45/65nm 3D-Stacked SPAD-Based Direct TOF Image Sensor for LiDAR Applications with Optical Polar Modulation for up to 18.6dB Interference Suppression

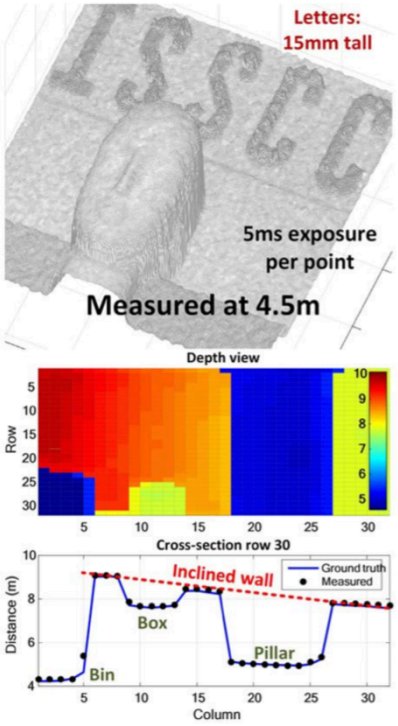
Augusto Ronchini Ximenes[1], Preethi Padmanabhan[2], Myung-Jae Lee[2], Yuichiro Yamashita[3], D. N. Yaung[3], Edoardo Charbon[1,2]

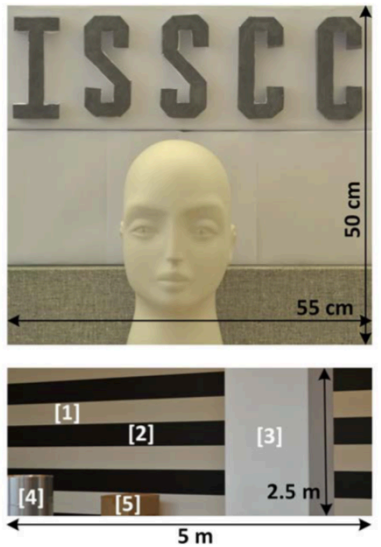
[1]Delft University of Technology, Delft, The Netherlands
[2]EPFL, Neuchatel, Switzerland; [3]TSMC, Hsinchu, Taiwan









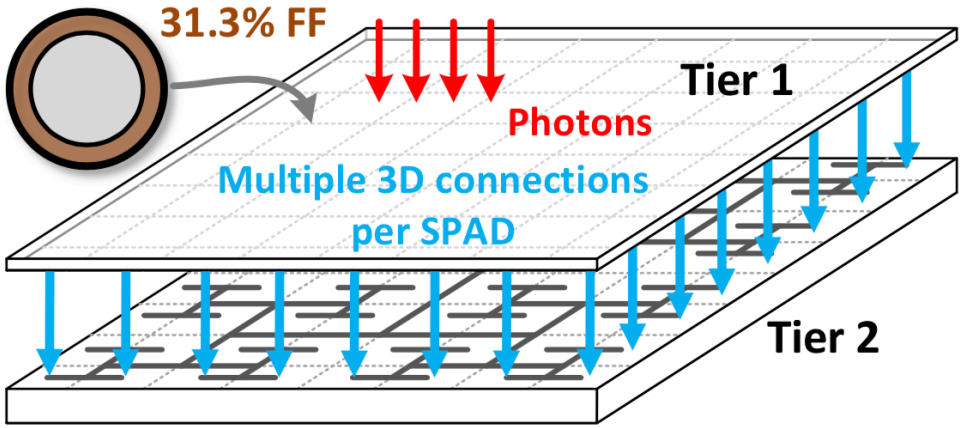


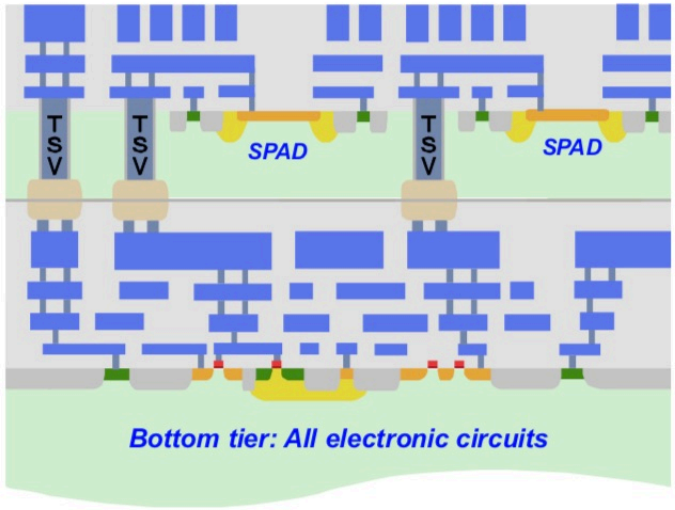
Different target reflectivities

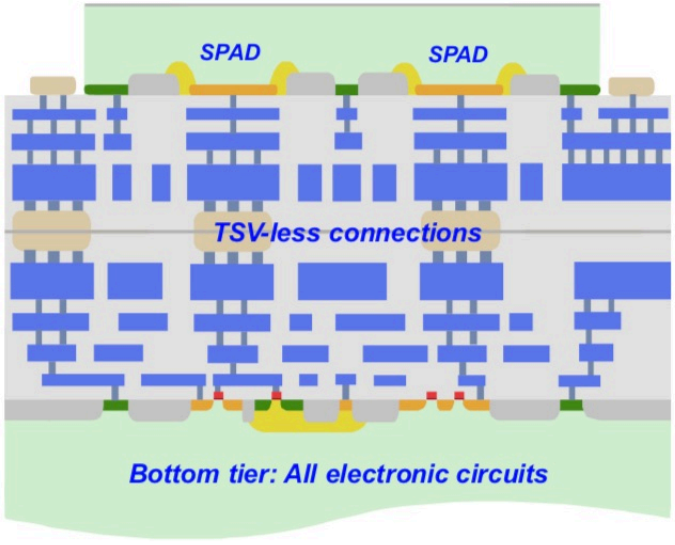
[1] – White wall – 50%
[2] – Black wall – 8%
[3] – White pillar – 60%
[4] – Aluminum bin – 54%
[5] – Cardboard box – 21%

3D Integration + Backside Illumination

BSI + 3D-Stacking







- Tier 1: SPADs + microlenses
- Tier 2: quenching, recharge, TDCs, multi-core, memories, communication unit, I/O

Edoardo Charbon, TechnoWeek2018

E. Charbon, C. Bruschini, M-J Lee, ICECS2018

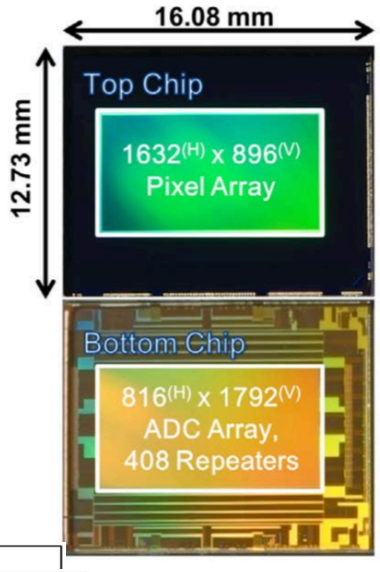
Advanced 3D Integration w/ BSI

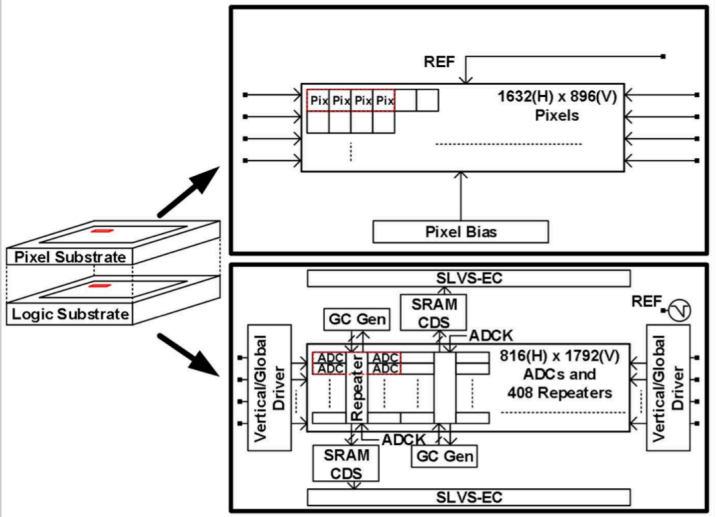
ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

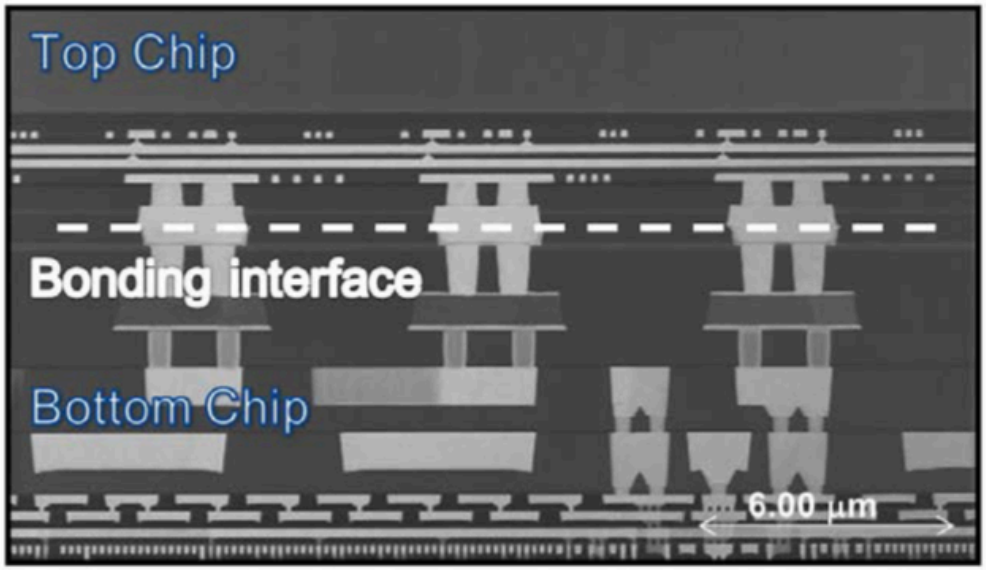
Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[1], Teruo Hirayama[1]

[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony Semiconductor Manufacturing, Kumamoto, Japan
[3]Sony LSI Design, Fukuoka, Japan





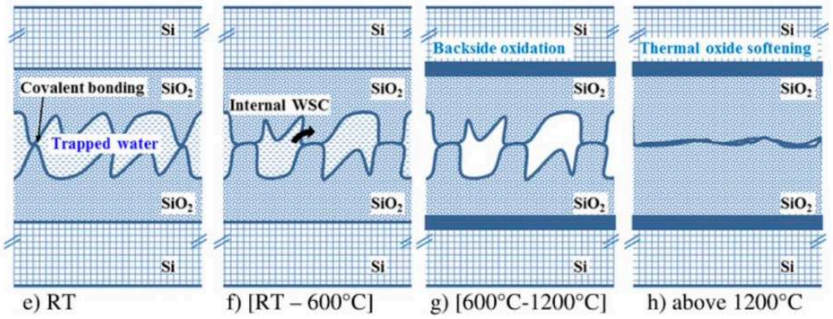
Item	Data	
Process	CIS wafer: 90nm 1 Poly 4 Metal Layer	
	Logic wafer: 65nm 1 Poly 7 Metal Layer	
Supply Voltage	2.9 [V] / 1.1 [V]	
Num. of pixels	$1632^{(H)}$ x $896^{(V)}$	
Pixel size	6.9 [µm] x 6.9 [µm]	
Output interface	16ch x 4.752 [Gbps/ch] SLVS-EC	
Max frame rate	660 [fps]	
Saturation signal	16.6k [e-]	
Sensitivity	61,500 [e-/lx· s] (green pixel, 3200K light with IR cut filter)	
PLS	-75 [dB]	
Conversion gain	60 [µV/e-]	
Comparator operation current	7.74 [nA]	111 [nA]
Comparator current (time average @660[fps])	1.67 [nA]	23.9 [nA]
Power consumption	654 [mW]	746 [mW]
Rms random noise @Analog Gain 0[dB]	8.77 [e^-_{rms}]	5.15 [e^-_{rms}]
Dynamic range	65.7 [dB]	70.2 [dB]
ADC resolution	14 [bit]	

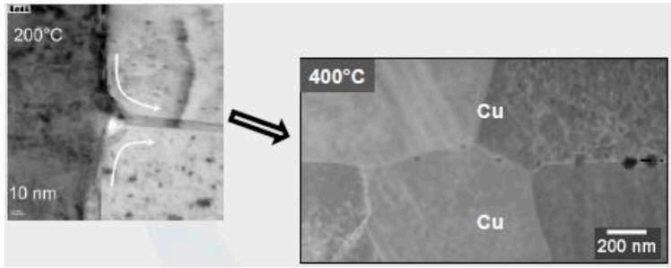


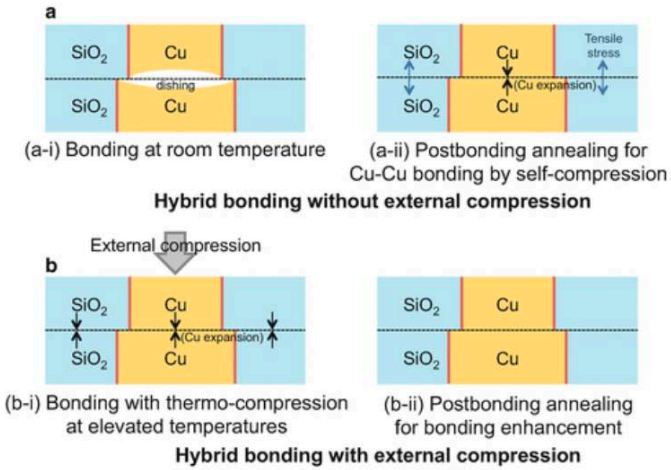
Wafer-to-wafer bonding techniques

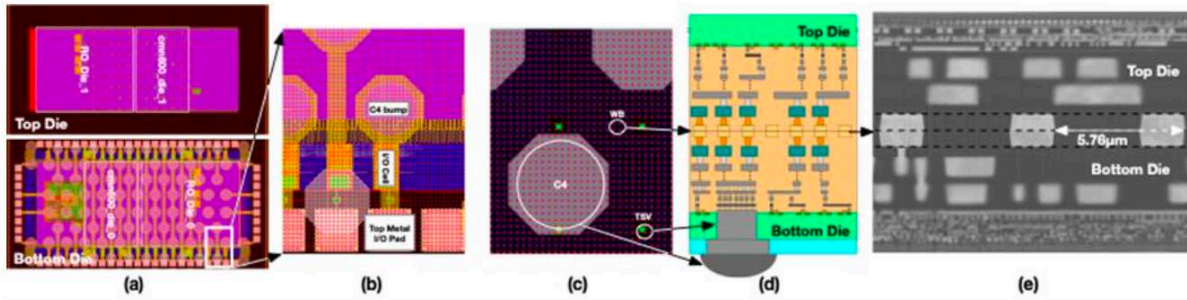
- **SiO_2-SiO_2 bonding: the most efficient**
  - Si-Si bonding not useful for 3D integration
- **Metal-Metal bonding**
  - Cu-Cu is widely used (Ti-Ti also works)
- **Hybrid Cu-SiO_2 bonding** => replace TSV
  - Used for W2W and D2W bonding

Fournel, 2015





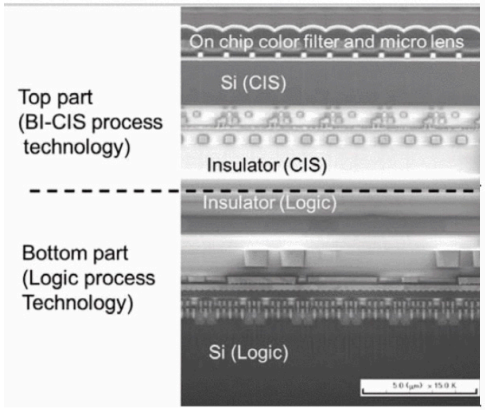




ECFA Detector R&D Roadmap Symposium of Task Force 7 Electronics and On-detector Processing, Christophe Wyon

Wafer-to-wafer bonding techniques

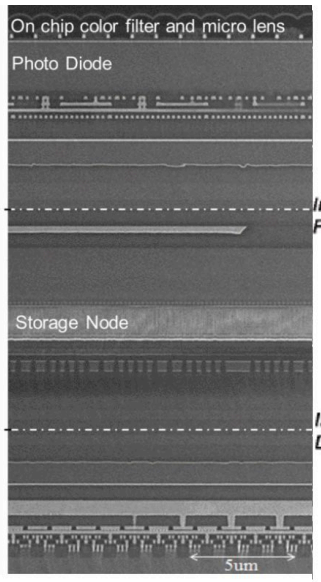
Sukegawa, 2013



Top part (BI-CIS process technology)

Bottom part (Logic process Technology)

Haruta, 2017

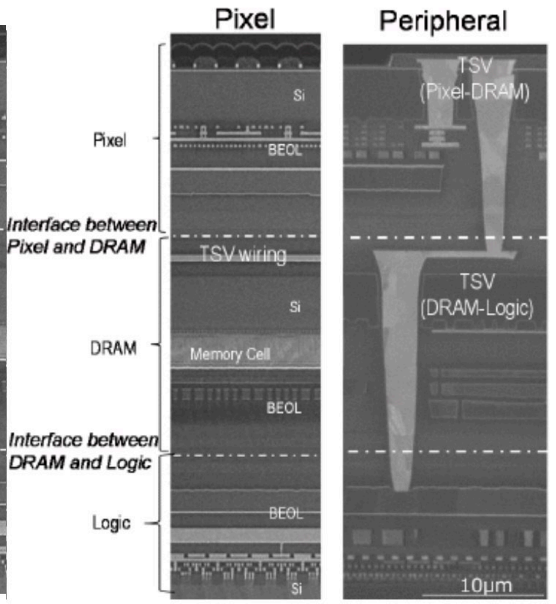


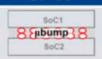
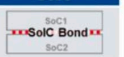
Top part (BI-CIS process technology)

Middle part (DRAM process technology)

Bottom part (Logic process technology)

Kagawa, 2019

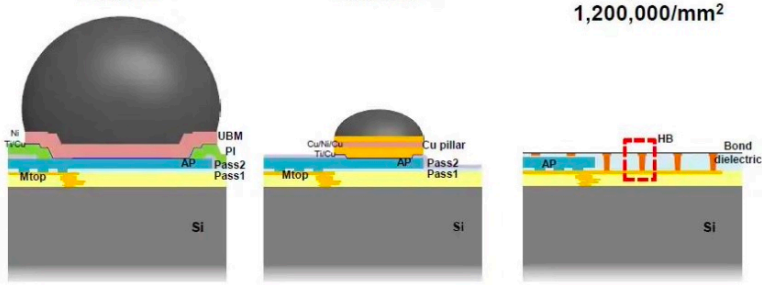


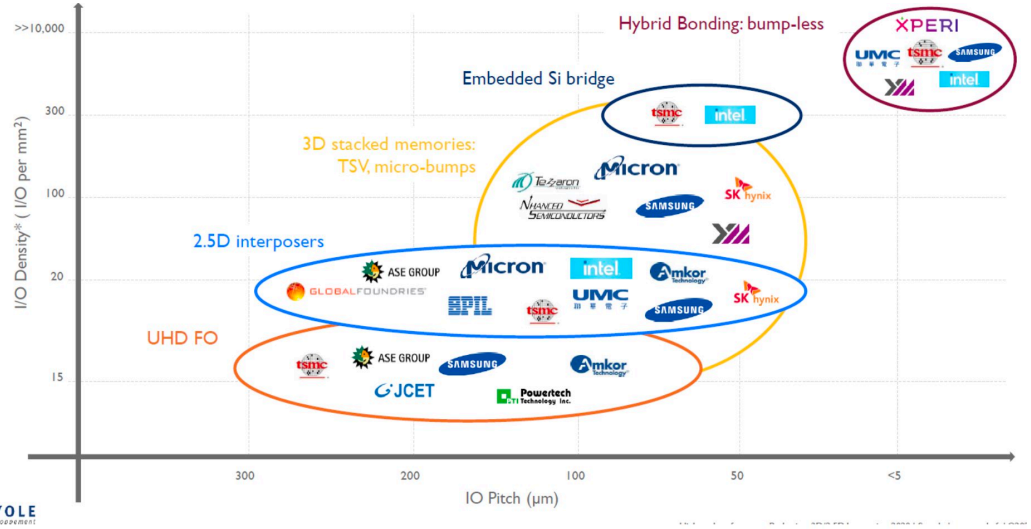
Technology	2.5D	3D-IC	SoIC
Structure cross-section			
Interconnect	μbump + BEOL	μbump	SoIC bond
Bump Density	1.0X	1.0X	16.0X
Speed	0.01X	1.0X	11.9X
Bandwidth Density	0.01X	1.0X	191.0X
Power Efficiency (Energy/bit)	22.9X	1.0X	0.05X

TSMC

C4 (Flip-Chip) → μ-bump (3DIC) → Bump-less (SoIC)

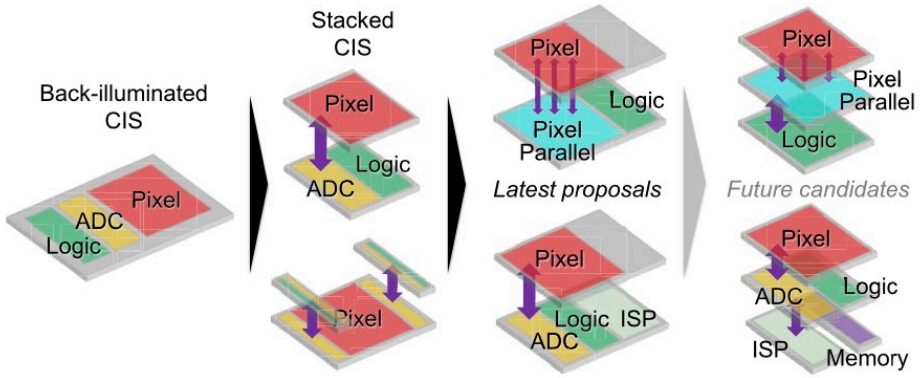
~120/mm² → ~ 800/mm² → 12,000 → 1,200,000/mm²



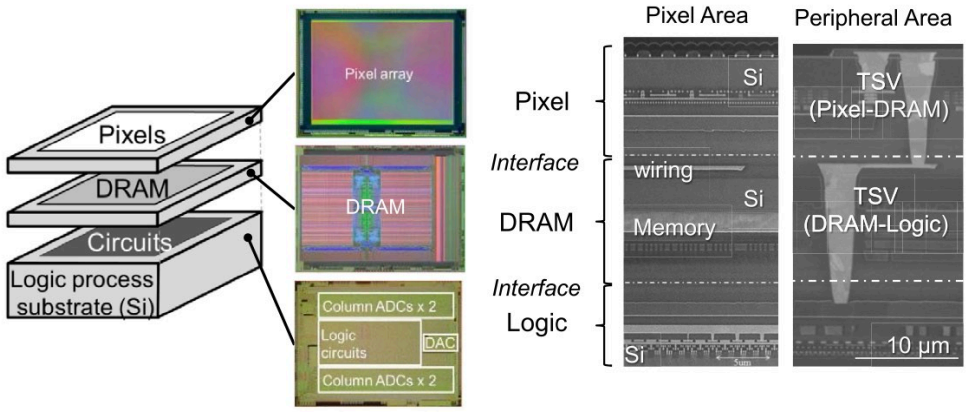


Outlook for CMOS APS Imagers

- Innovation on image sensor integration technologies mostly driven by the need of higher frame rates and higher pixel resolutions
- Enabled by the use of stacked device structures employing optimised sensor process technologies and advanced CMOS nodes
- Notable recent achievements featuring "pixel-parallel stacked circuitry" and UDSM CMOS circuits with more intelligence on board of the processing units
- ✦ Pixel-pitch Cu–Cu connections, wafer-on-wafer (WoW) bonding or Chip-on-wafer (CoW) when readout circuitry is smaller than the optics,...



Y. Oike, "Evolution of Image Sensor Architectures With Stacked Device Technologies," in IEEE Transactions on Electron Devices, 2021



Y. Kagawa et al., "Novel stacked CMOS image sensor with advanced Cu2 Cu hybrid bonding," in IEDM Tech. Dig., Dec. 2016

(left) A. Jouve et al., "1µm Pitch direct hybrid bonding with <300nm wafer-to-wafer overlay accuracy", 2017 IEEE S3S Conf

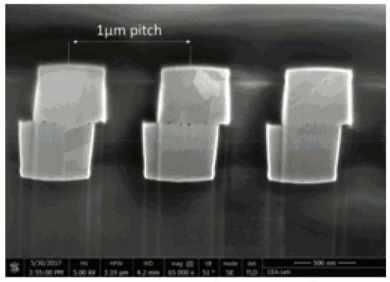
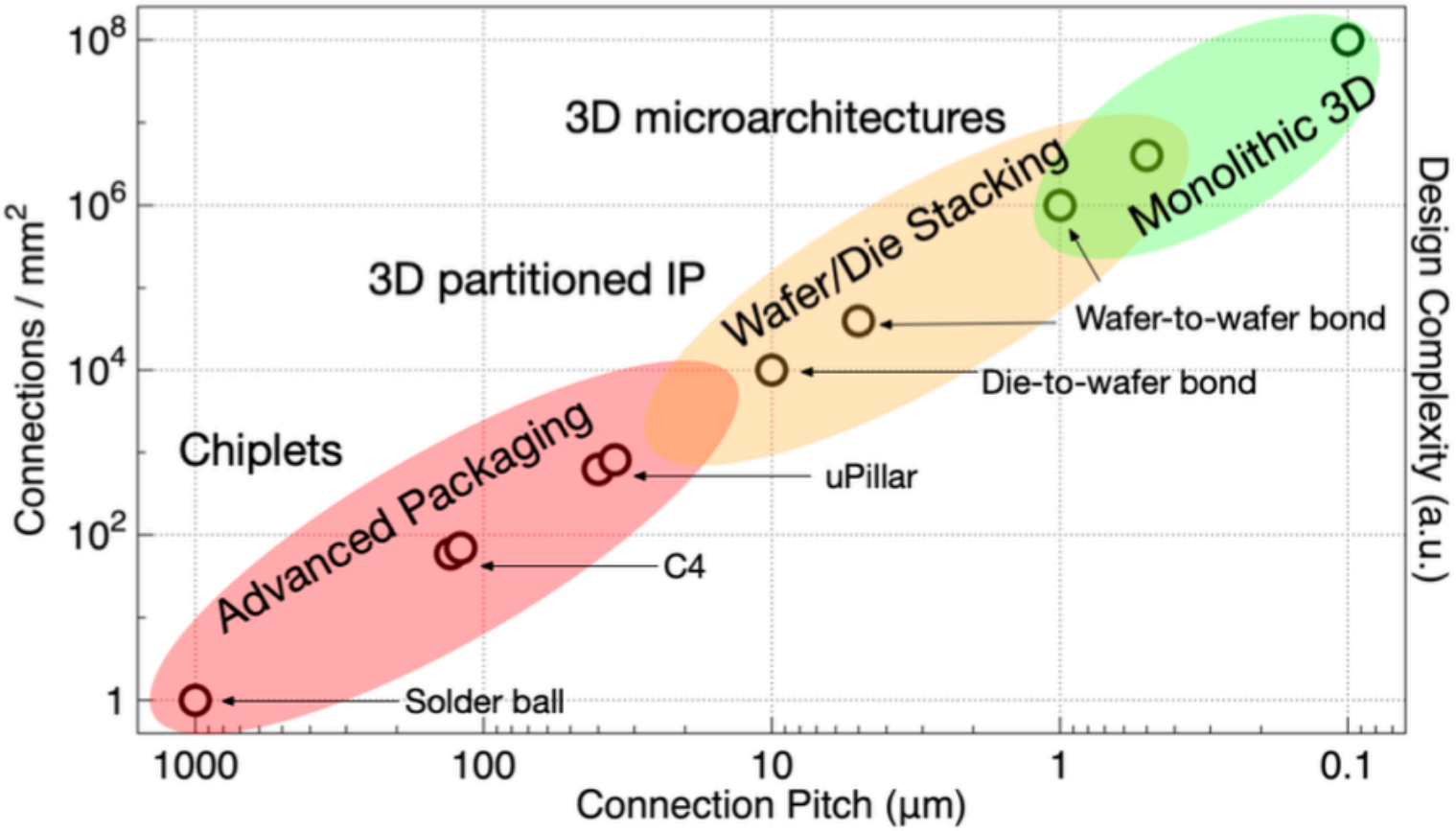


Figure 5: FIB-SEM X-section of 1µm pitch copper pads after 400°C-2h annealing.

3D Integration Roadmap



ECFA Detector R&D Roadmap Symposium of Task Force 7 Electronics and On-detector Processing, Christophe Wyon

On the definition of “Monolithic CMOS”

ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[1], Teruo Hirayama[1]

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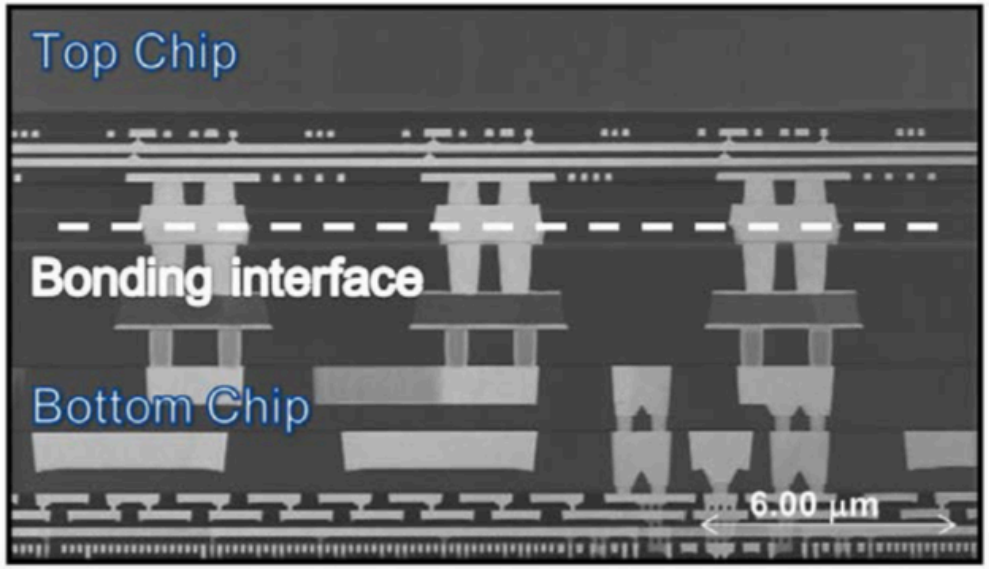


Item	Data	
Process	CIS wafer: 90nm 1 Poly 4 Metal Layer	
	Logic wafer: 65nm 1 Poly 7 Metal Layer	
Supply Voltage	2.8 [V] / 1.1 [V]	
Num. of pixels	1632(H) x 896(V)	
Max frame rate	660 [fps]	
Saturation signal	16.6k [e-]	
PLS	-75 [dB]	
Conversion gain	60 [µV/e-]	
Power consumption	654 [mW]	746 [mW]
Dynamic range	65.7 [dB]	70.2 [dB]
ADC resolution	14 [bit]	

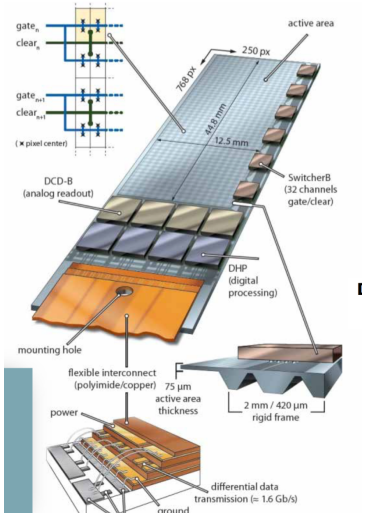
Disclaimer for the next slides:

The availability of advanced wafer-to-wafer bonding techniques inevitably leads to some ambiguity on the definition of the terms “hybrid” and “monolithic”

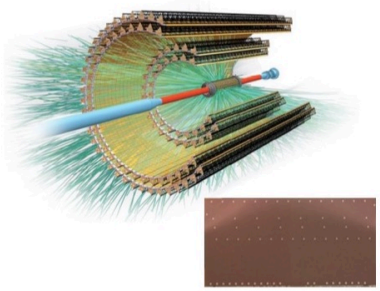
Monolithic Active Pixel Sensors

- **Sensor and Readout Electronics share the same wafer,** as opposed to hybrid pixel sensors, which use two chips that need to be interconnected
- Enabling technology for low material budget and/or very low power space applications, frontier detectors for particle physics
- Embedded electronics, less components and connectors: Lower cost and increased reliability on assembly and production of detectors:
  - no need for costly fine-pitched flip-chip assembly
  - small pixel pitches: O(10-30 μm) and low [capacitance] power: O(10-100 mW/cm^2)
  - less (failing) connectors and lower material budget
  - cost reduction for large productions (use of a commercial CMOS foundry): increased die-per-wafer and reduced cost per device

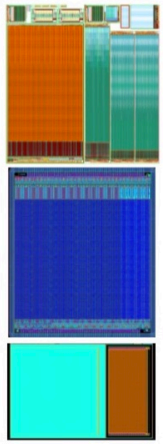
MAPS: The Evolution of the Species



ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system

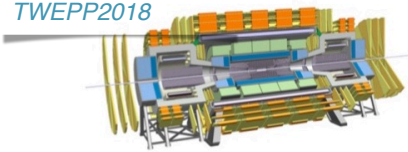


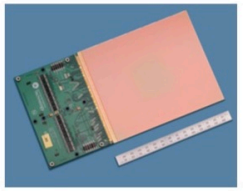
ALPIDE in ALICE
First MAPS with sparse readout
similar to hybrid sensors
Chip-to-chip communication
for data aggregation



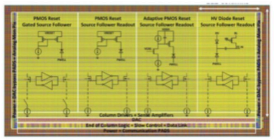
ATLAS CMOS
Depleted radiation hard
MAPS with:
Sparse readout
Chip-to-chip
communication
Serial power
...

Partially adapted from: W. Snoeys, TWEPP2018



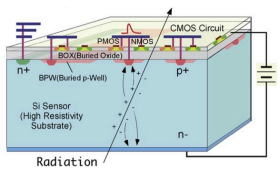


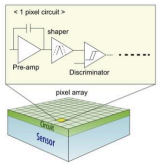
FCC, CLIC, ...
Large stitched fast
radiation hard MAPS
with:
Sparse readout
Chip-to-chip
communication
Serial power

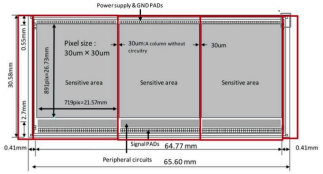


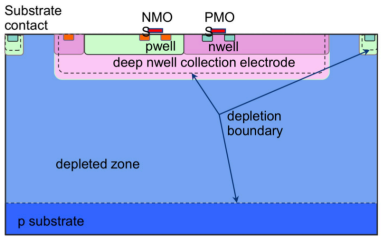
TJ-Monopix: 20 x 10 mm

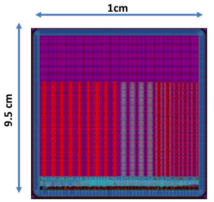
MALTA: 20 x 20 mm



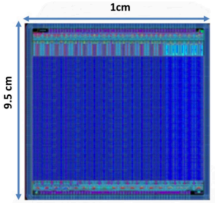




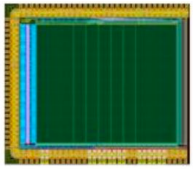




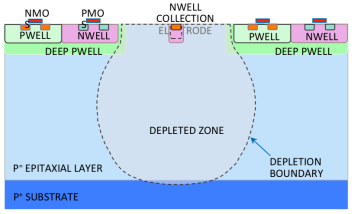
LF-CPIX (Demonstrator)



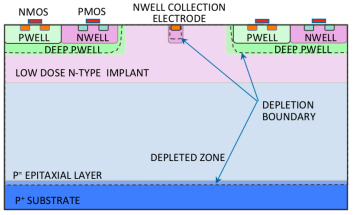
LF-Monopix (monolithic FE-I4)



JadePix2 (IHEP)
3 × 3.3 mm²



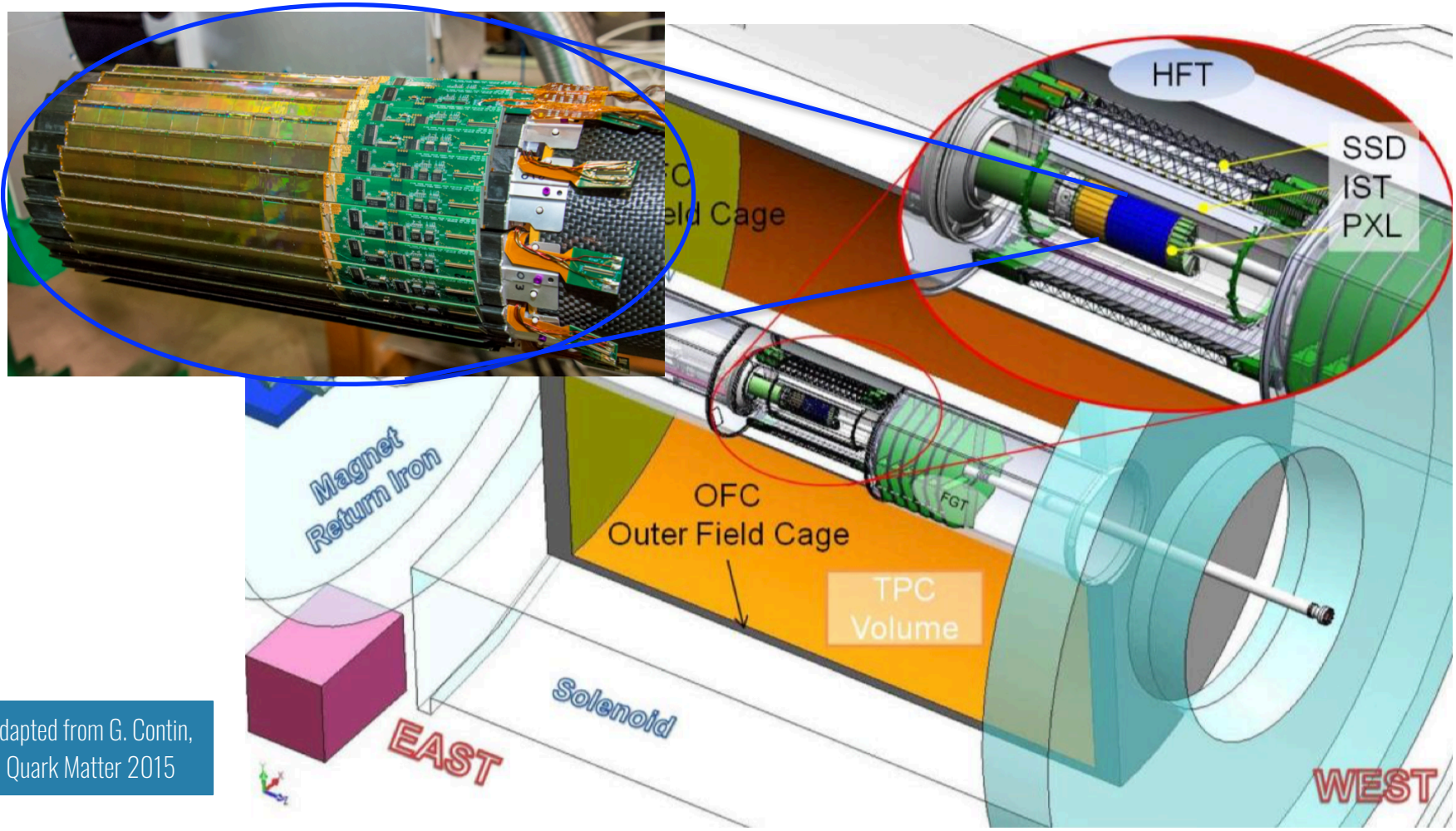
Standard: no full depletion



Modified: full depletion, better radiation tolerance

STAR HFT at the Relativistic Heavy Ion Collider (RHIC)

First MAPS based vertex tracker at a collider experiment!

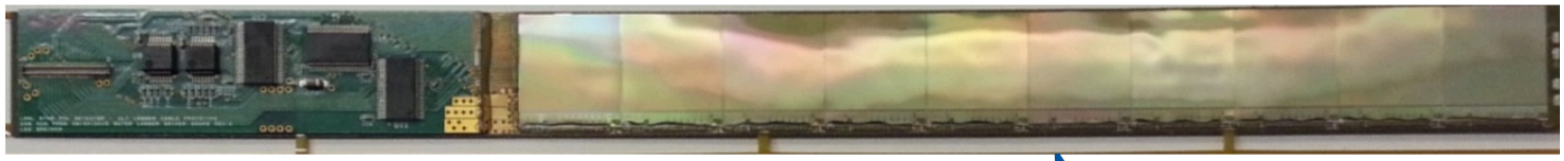


adapted from G. Contin, Quark Matter 2015

MIMOSA28 in STAR Heavy Flavour Tracker

Basic Detector Element

Ladder with 10 MAPS sensors (~ 2×2 cm each)



DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm rms (20 μm envelope)
Material budget first layer	X/X_0 = 0.39% (Al cond. cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

4 ladders / sector
5 sectors / half
10 sectors total

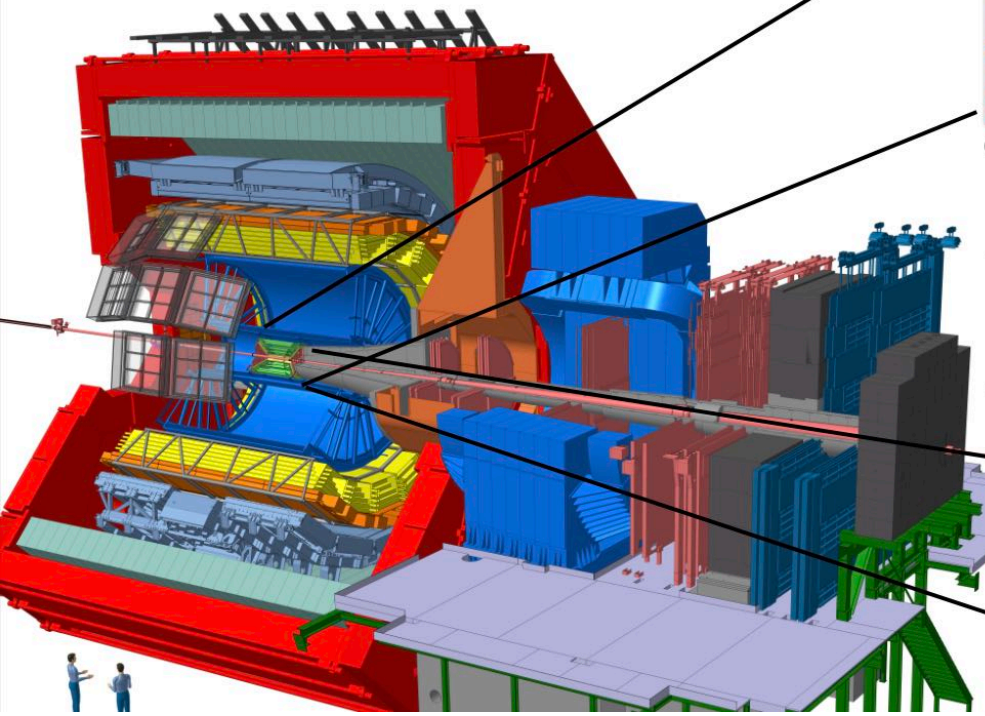
carbon fiber sector tubes
(~ 200 μm thick)

adapted from P. Riedler, CPAD 2018

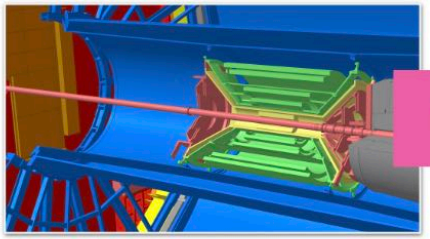
CMOS sensors for ALICE ITS2+MFT

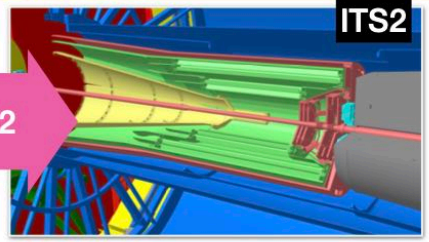
ALICE LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)

courtesy: M. Mager



Inner Tracking System





LS2

6 layers:
2 hybrid silicon pixel
2 silicon drift
2 silicon strip

Inner-most layer:
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425\ \mu m^2$

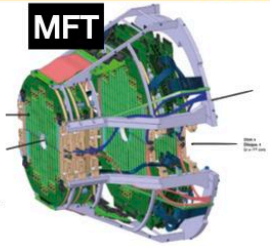
rate capability: 1 kHz

7 layers:
all MAPS
10 m^2, 24k chips, 12.5 Giga-Pixels

Inner-most layer:
radial distance: 23 mm
material: $X/X_0 = 0.35\%$
pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

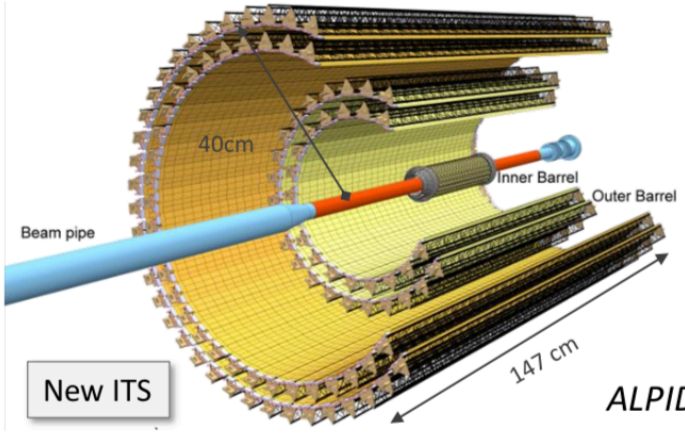
Muon Forward Tracker



new detector

5 discs, double sided:
based on same technology as ITS2

ALPIDE Chip - applications beyond ALICE



Closer to IP: 39mm ➡ 22mm

Thinner: ~1.14% ➡ ~ 0.3% (for inner layers)

Smaller pixels: 50μm x 425μm ➡ 27μm x 29μm

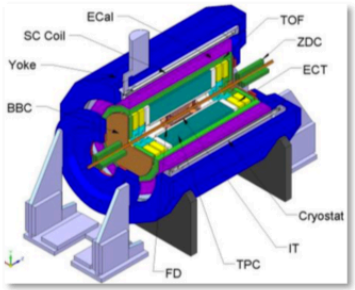
Increase granularity (x 10^3): 20 chan/cm^3 ➡ 2k pixel/cm^3

10 m^2 active silicon area: 12.5 G-pixels, $\sigma \approx 5\mu m$

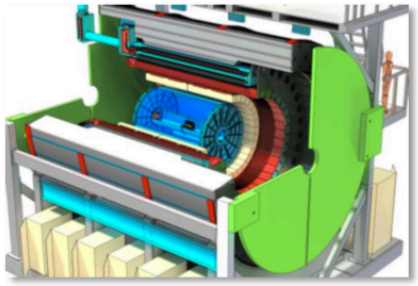
$1.5 \leq \eta \leq 1.5$

*ALPIDE (**ALICE Pixel Detector**) - Developed for the ALICE upgrade (ITS and MFT) will be used (or it is proposed) for several other HEP detectors and non HEP applications*

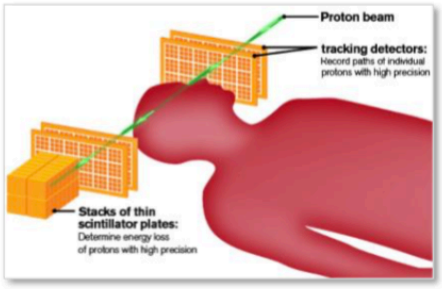
NICA MPD (@JINR)



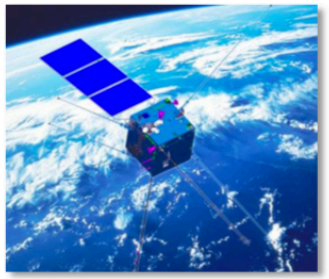
sPHENIX (BNL)



proton CT (tracking)



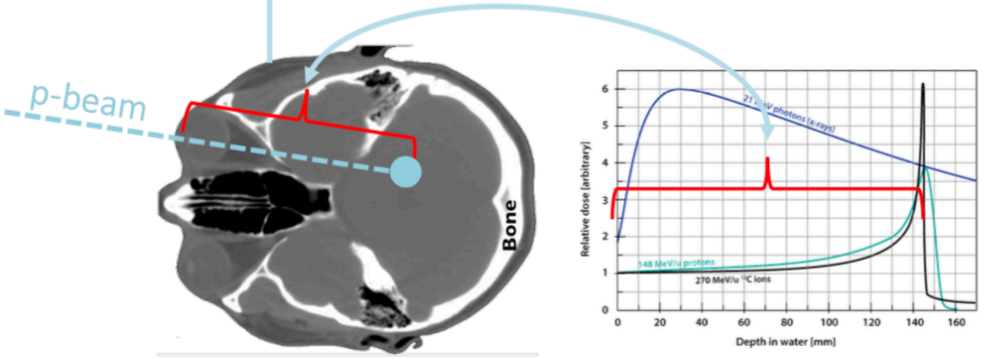
CSES – HEPD2 ...

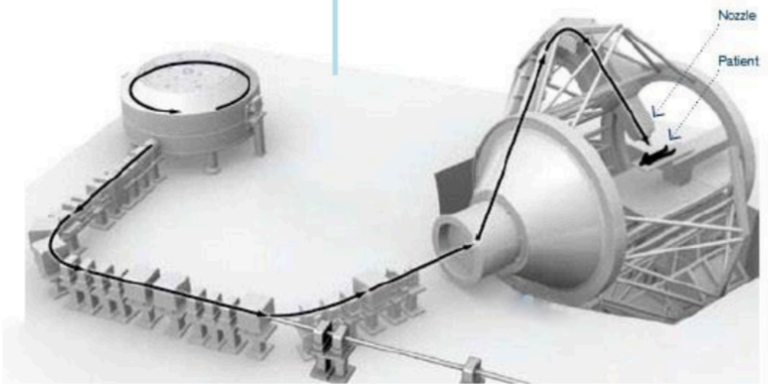


L. Musa – EIROforum, Topical Workshop, CERN, May 2018

MAPS for Medical Applications

Aiming the Bragg peak requires fine tuning of the proton energy to account for the tissue densities they have to traverse to reach the tumor.





Poor tissue density resolution from X-Rays CT

Fine energy tuning better than 0.5%

X-ray 3D CT cannot distinguish tissue densities with the required precision: proton therapy limit today (bigger systematic error, up to 5%). But protons actually can (and with much less dose, ≈ 1.5 mGy vs. 10-100 mGy).

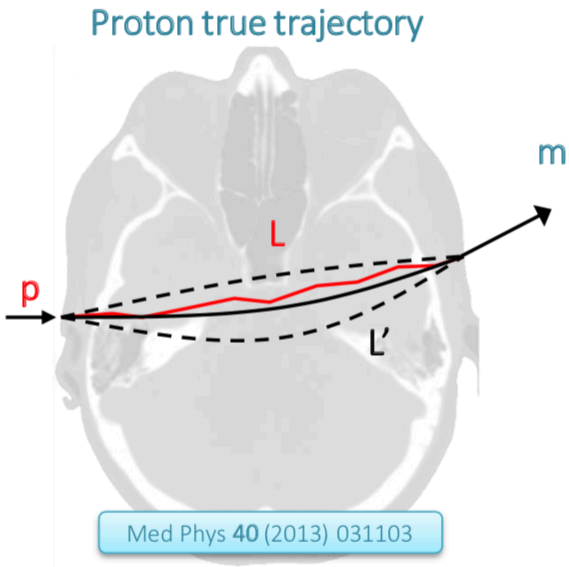
NIM B **268** (2010) 3295–3305 | Eur. Phys. J. Plus (2011) **126**: 78

Phys. Med. Biol. **56** (2011) 2407–2421

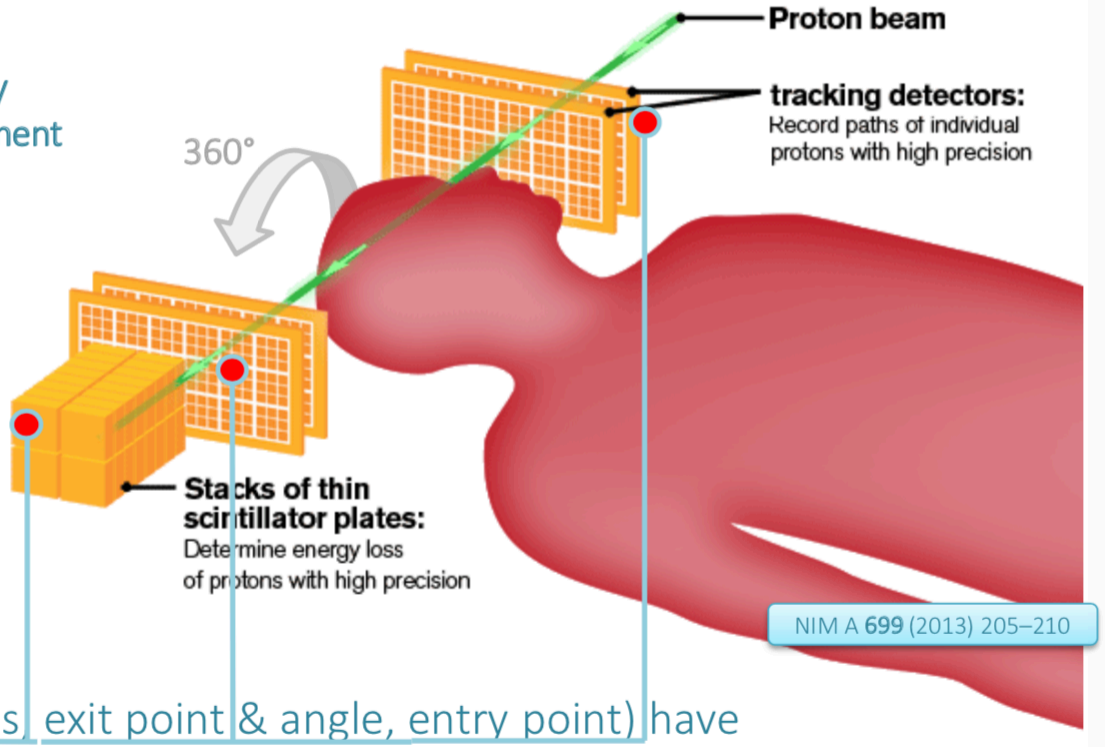
courtesy slide from Piero Giubilato: ERC iMPACT

MAPS for Medical Applications

The pCT works on the same principle as a "standard" x-rays CT: recording particles passing through the target from different angles to reconstruct a 3D image. Main difference is that, while photons are simply absorbed, protons also scatters.



Entry and exit points + angle
Most Likely Path calculation

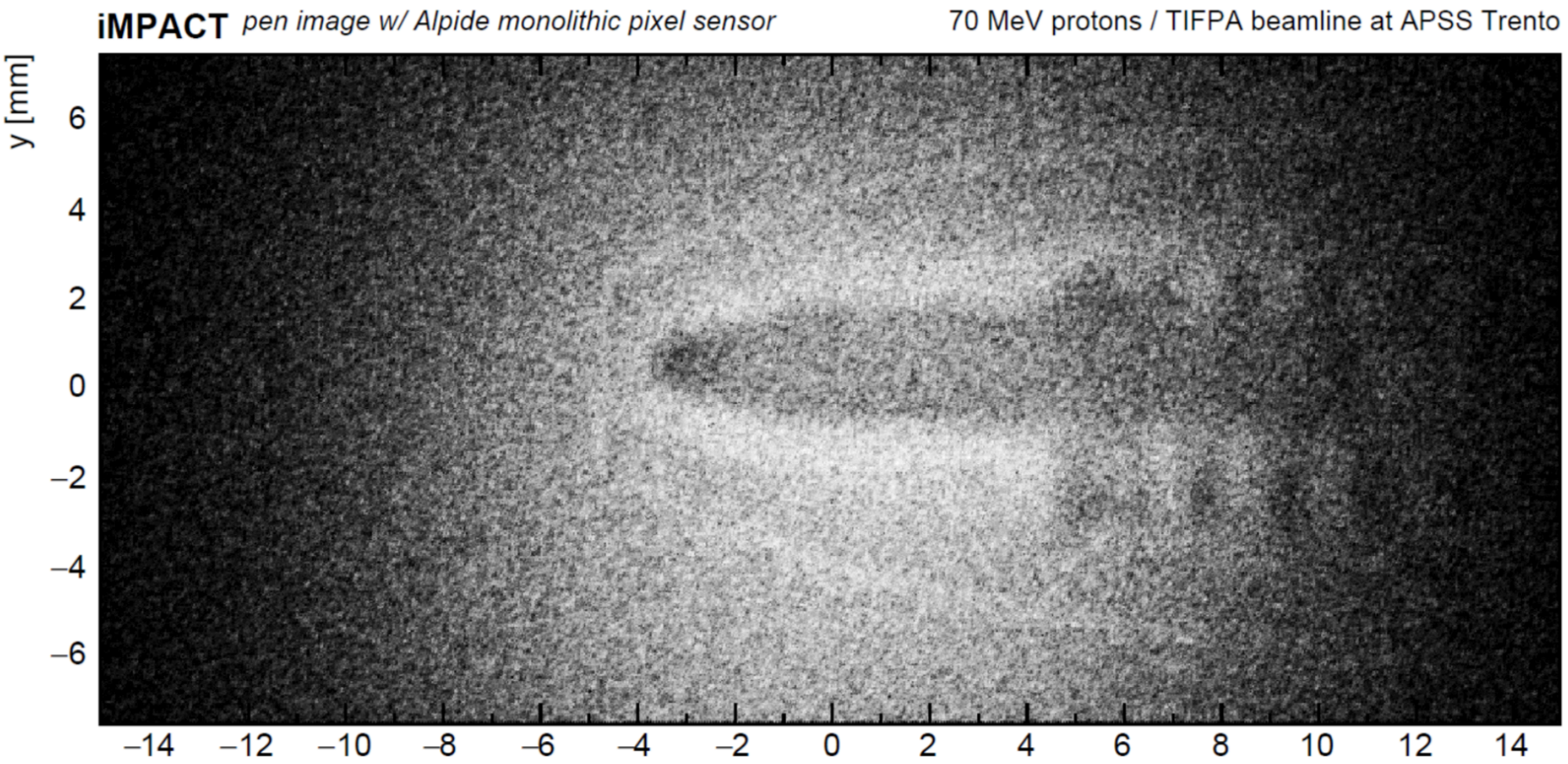


At least 10^9 proton tracks (energy loss, exit point & angle, entry point) have to be recorded to provide a detailed enough image. This leads to long exposure time (10s minutes) with current state of the art: limited to R&D only.

courtesy slide from Piero Giubilato: ERC iMPACT

ALPIDE first “proton” light

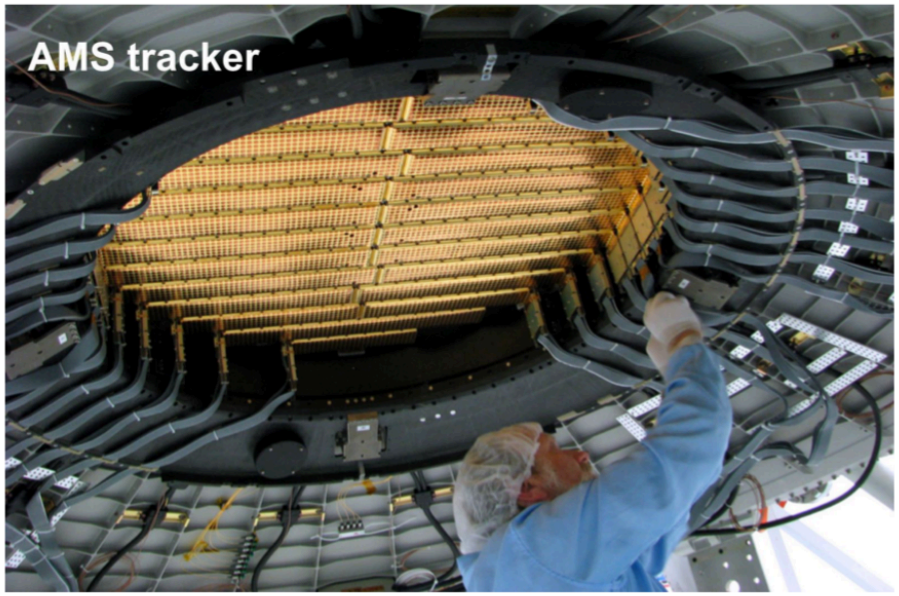
ALPIDE used to take a demonstrative proton radiography of a pen: metal, different plastic densities, air distinguishable.



courtesy slide from Piero Giubilato: ERC iMPACT

Monolithic APS in Space

Low power, reliability & small pixels ($< 50\ \mu$m)

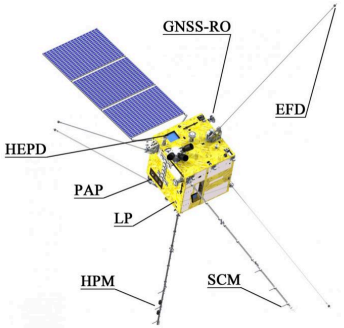


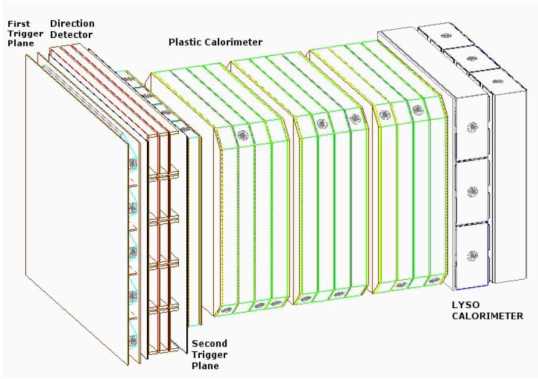
- ↪ Not much room for heavy magnets in space experiments!
  - ◇ Extra-small pixels to achieve the target tracks resolution
  - ◇ No much room for power supplies also: ultra low power definitely a must!
  - ◇ Extreme reliability in harsh operational conditions

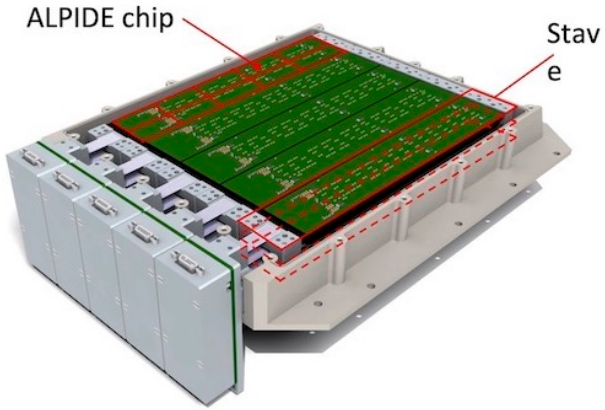
⋆ **Monolithic CMOS pixel sensors are a good choice to meet these goals!**

ALPIDE chip for space applications

- direction detector DD ("tracker") of the High Energy Particle Detector (HEPD-02) will be onboard of the China Seismo-Electromagnetic CSES-02 satellite (launch scheduled to 2022)
- 5 triple-stacked-stave turrets, stave mounts 10 ALPIDE (50μm)
- Low-power strategy: control line instead of high speed data link for readout and regional clock-gating at system level
- The HEPD-02 silicon tracker will become the **first use case of MAPS technology in space instruments**!

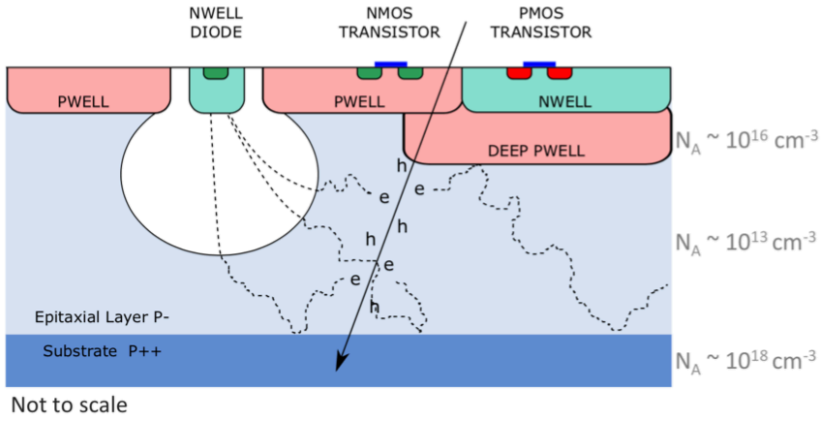


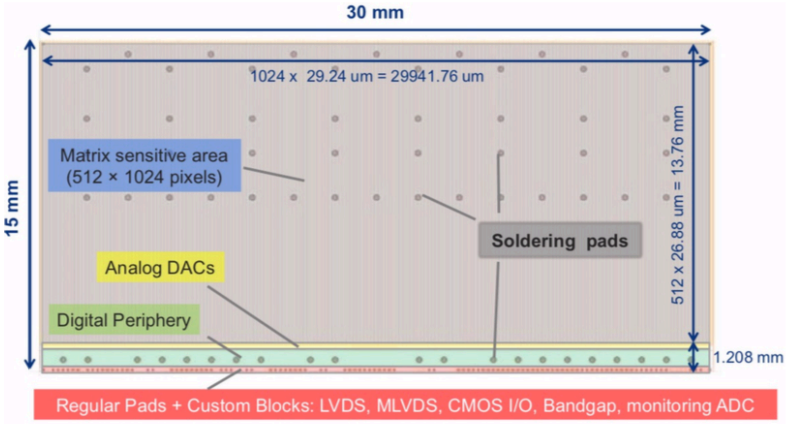




P Zuccon, iWoRiD2021

The ALPIDE (ALICE Pixel Detector) Sensor

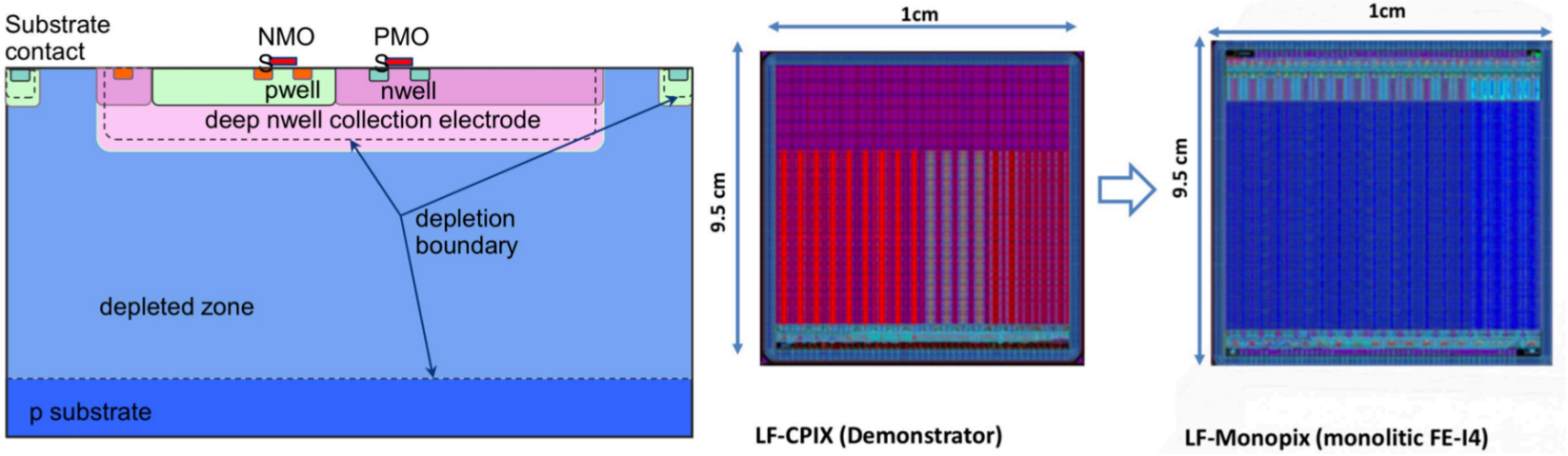




- 180nm TJ CMOS imaging sensor process
- System-grade large scale monolithic sensors with sparse readout
- charge collection by diffusion only - slow signals, unfit for O(ns) timing; sensitive to bulk damage due to collection time
- reverse bias increases depletion volume, sensor is not fully depleted

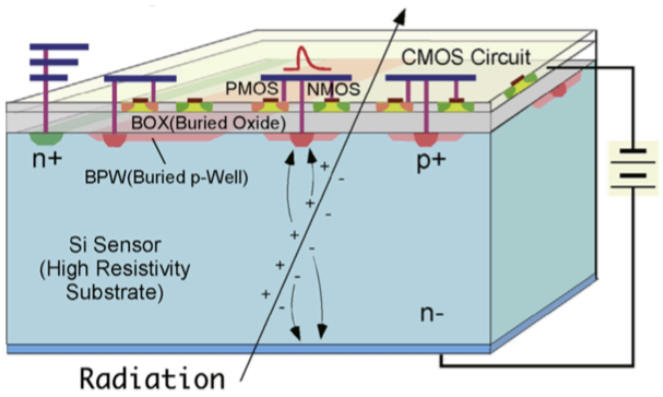
☑ Best in class in terms of system readiness!

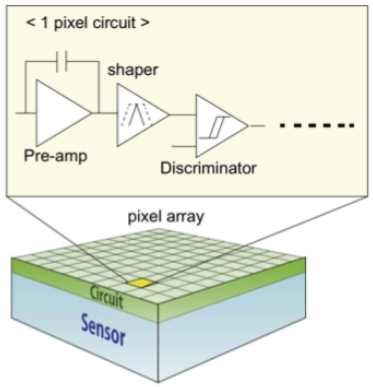
Depleted MAPS, large CE (HV-CMOS)

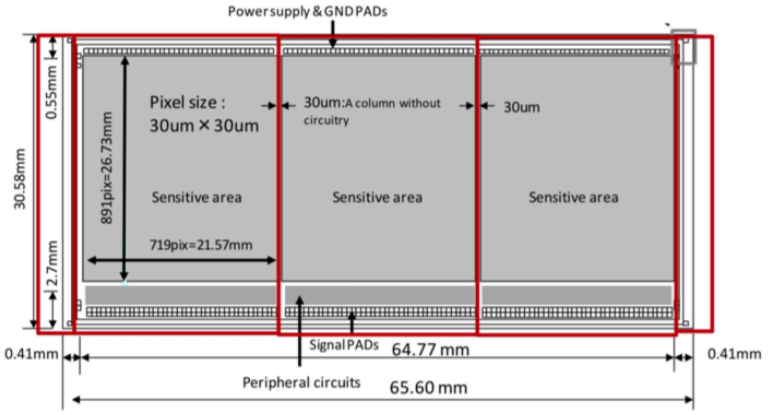


- e.g. ATLASpix, LF-Monopix, Coolpix, LF2
- Charge is collected by drift - faster signals!
- Uniform electric field and very good radiation tolerance (1E15 n_{eq}/cm^2)
- readout circuitry inside the collection electrode degrades input capacitance and hence SNR
- large CE: analog power, sensitivity to coupling of signals
- Initially proposed for ALTAS outer pixel layer Phase 2

Silicon on Insulator (e.g. PIXOR, SOPHIAS)





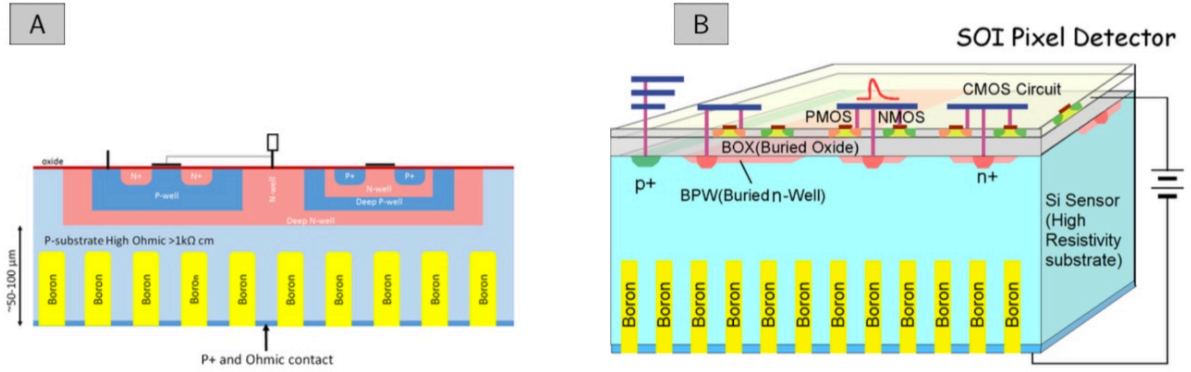


- buried oxide separates silicon layer (front-end circuit) and sensor on high resistivity substrate
- BOX is fairly thick and this increases the sensitivity to the damage caused by ionizing radiation
- high radiation tolerance, large depletion volume
- back-gate effect (causes shift on FET V_{th}) solved with Buried P-Well (BPW), but pixel capacitance increases
- SOI wafers cost, single vendor, wafer capability for volume?

MAPS for neutron detection

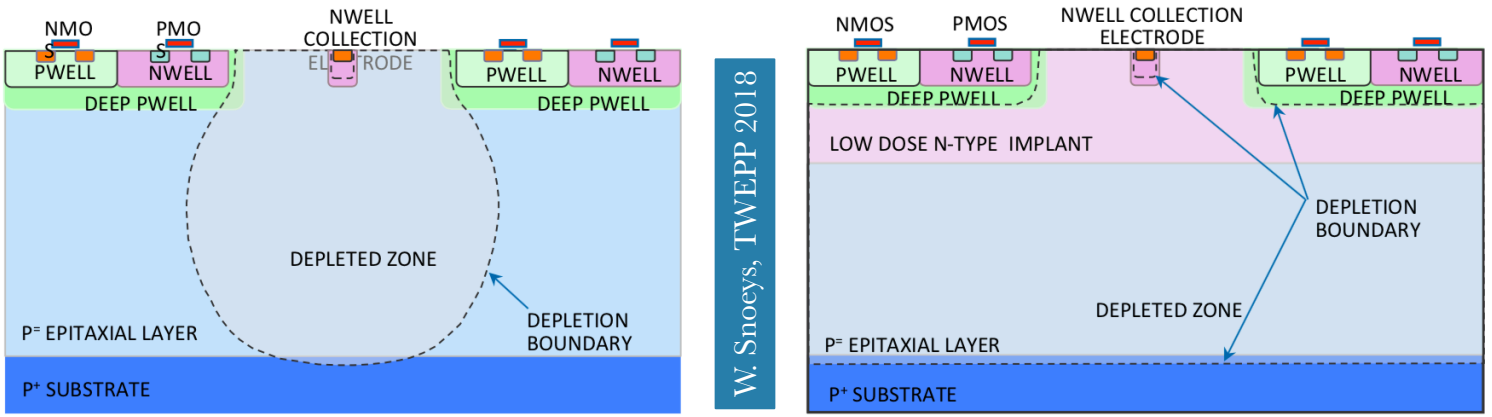
- Neutron imaging provides information on materials and structures otherwise opaque to X-rays (metal and mechanical structure analysis, automotive and aviation safety-sensitive diagnosis)
- Particularly important for the study of archaeological samples, non-destructive tests with high spatial resolution and low neutron fluxes (avoids material activation)
- Silicon is not sensitive to neutrons, but one could use a conversion material (e.g. lithium fluoride or enriched Boron) and then use a silicon sensor as detector
- use of 3D geometries to increase the probability of detecting reaction products
- Ongoing activity using MAPS on a HR-substrate (A) and SOI technology (B)

Roberto Mendicino, INFN Trento



a monolithic 3D detector would be a turning point for the field of neutron imaging

Fully-Depleted MAPS with small CE



Standard: no full depletion

Modified: full depletion, better radiation tolerance

- TJ180nm Investigator Sensor (ALICE) test chip, above 97% eff; 134 pixel sub-matrices of different designs (electrode size, PWELL spacing)
- use of a n-type layer to improve depletion under deep PWELL → better radiation tolerance (Investigator irradiated up to 1E15 n_{eq}/cm^2 and 1 Mrad in several steps) and charge collection by drift
- small collection electrode: low capacitance, low power, better isolation electrode/circuit
- depletion depth limited to the epi-layer (about 25 μm)
- Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers: TJ MALTA (2018) 20 x 22 mm^2 and TJ MonoPix (2018) 20 x 10 mm^2

Depleted MAPS for Future Detectors

	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm^2]	0.4	10	<0.3	100-200	2000	200-20000

Heinz Pernegger

- **Hit rate and radiation hardness for Frontier Detectors could require improvements of ~2 orders of magnitude in respect to the state-of-the-art technology**

- Charge collection by drift: faster signals, better radiation hardness
- New architectures for higher event rate capability
- Advanced integration and interconnect technology for large sensor area and lightweight modules

Opportunities for fully-depleted CMOS sensors

- cost reduction for large productions (use of a commercial CMOS line)
- embedded electronics, less components and connectors: increased system reliability with simpler system design, production and assembly all contribute to cost saving
- enabling technology for low material budget and/or very low power space applications, frontier detectors for particle physics

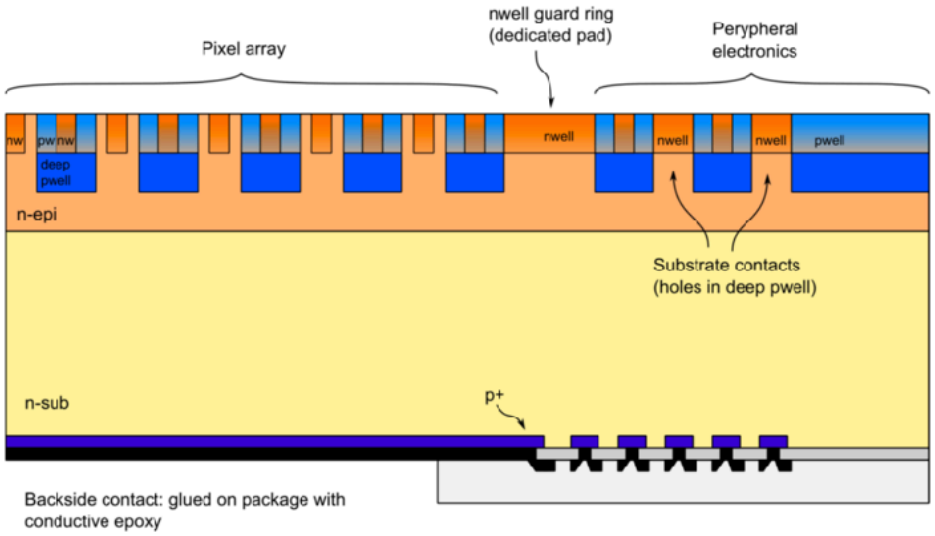
	Scalable to large area architecture	Extra low-power mode	Fully depleted sensor (sensitivity)	Fully depleted sensor (speed)
High Energy Physics	Scale economy in large detectors	Reduced material budget (no cooling)	dE/dx capability (equival. to Si-strips)	Cost-effective timing layers, pile-up reduction
Space applications	Reliability for space-born large detectors	High spatial resolution space-born detectors		
X-ray and UV Imaging	Reduced dead area in imaging panels		Broad spectrum imaging (0.5 eV to 10 keV)	Counting mode possible
Medical imaging and tracking	Self-supporting sensors to avoid scattering			Accurate timing for PET, particle tracking matching

ARCADIA DMAPS R&D at INFN

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

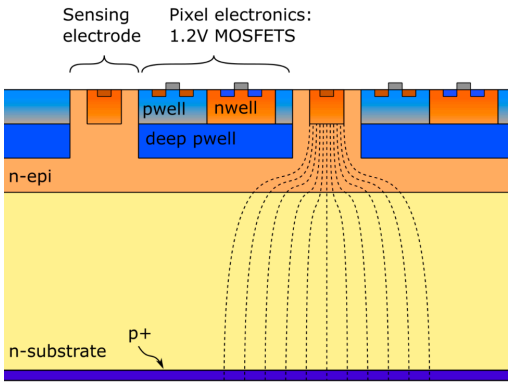
Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

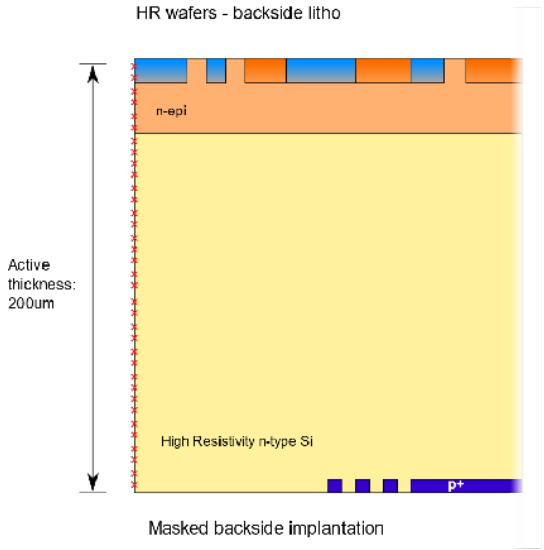
- Active sensor thickness in the range 50 µm to 500 µm;
- Operation in full depletion with fast charge collection by drift, small collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(**10 mW/cm²**));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: LF11is 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry

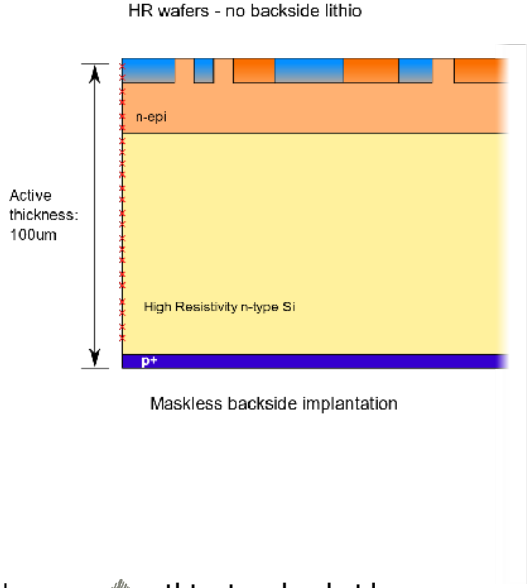


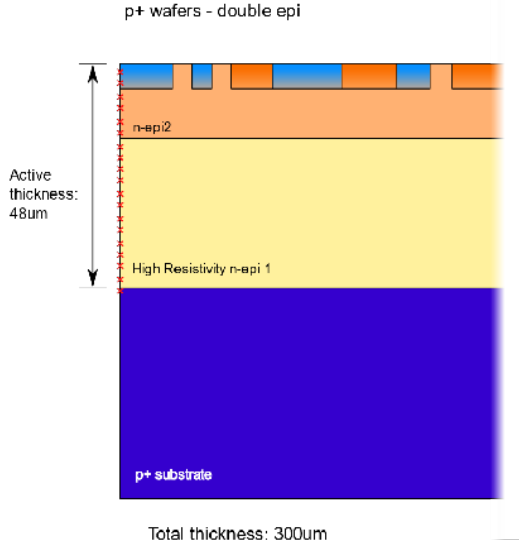
Sensor Concepts and post-processing

- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top









- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition
- thinning, backside p+ implantation and laser annealing
- thinning down to 100 or 300μm total thickness

Full-chip FD-MAPS: ARCADIA MD3

Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

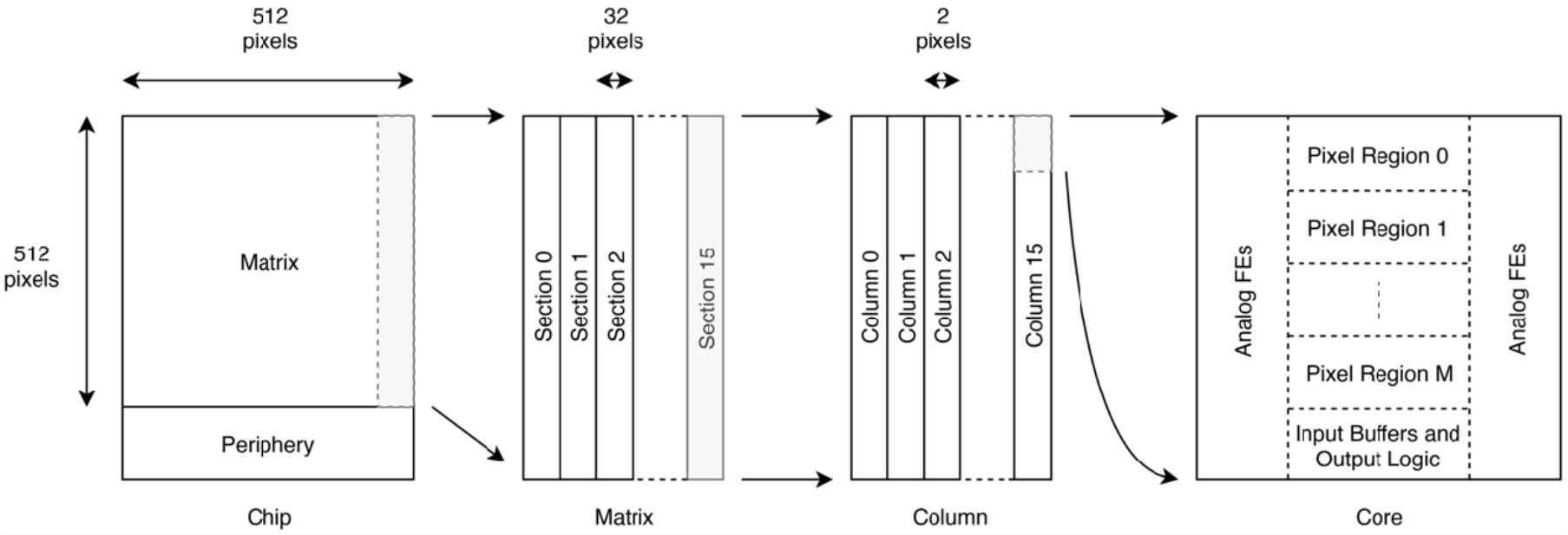
Periphery

SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe

Stacked Power and Signal pads

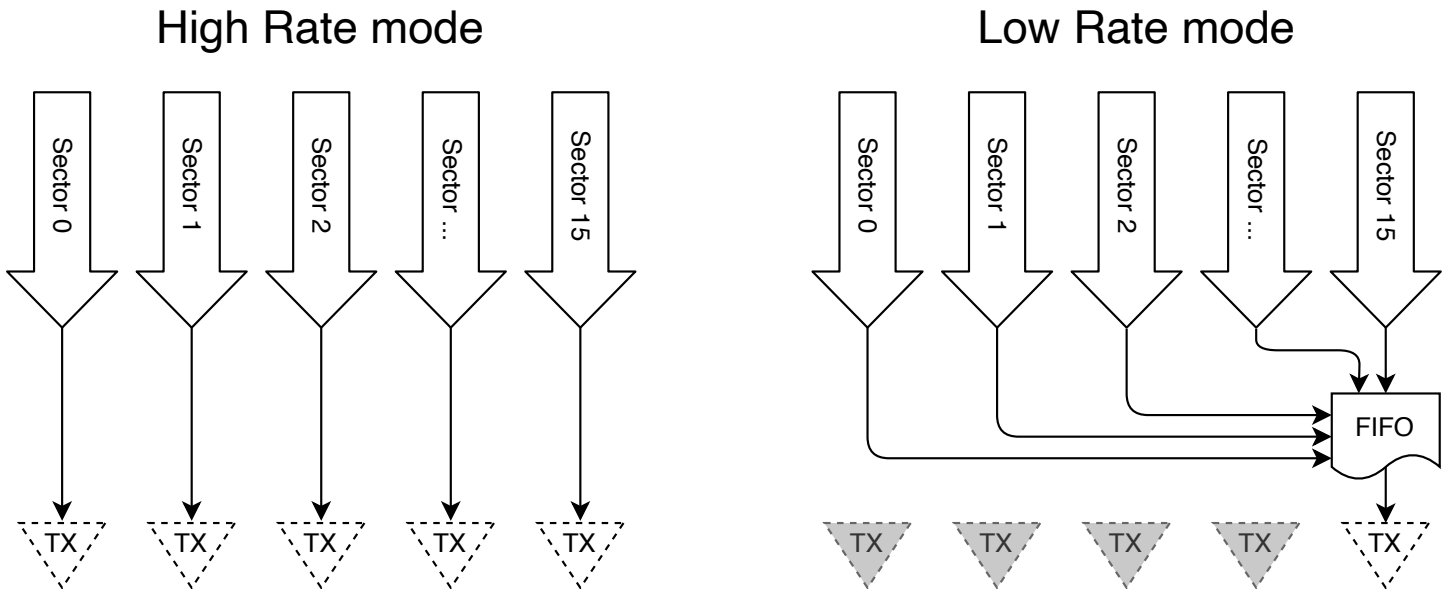
Full-chip FD-MAPS: ARCADIA MD3



- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm^2 silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- High-rate operation (16 Tx): 17-30 mW/cm^2 depending on transceiver driving strength
- Low-power operation (1 Tx): **10 mW/cm^2**

ARCADIA MD3 data flow modes

- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.



* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

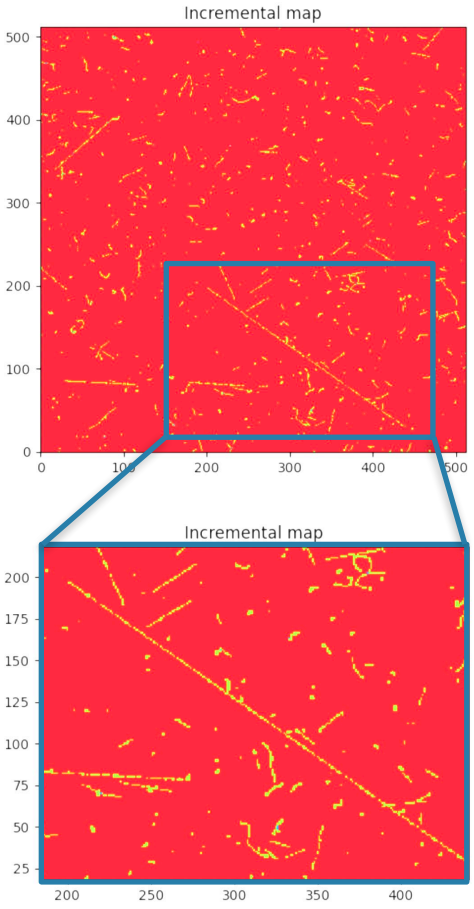
ARCADIA MD3: charged particles

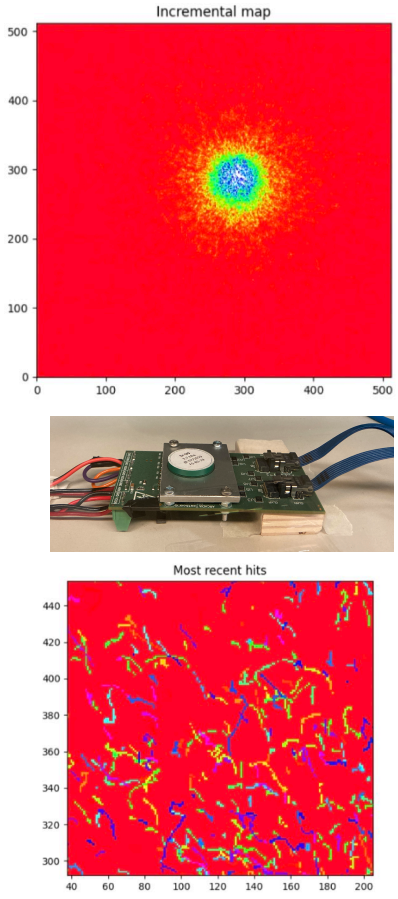
Cosmic rays (tilted sensor)

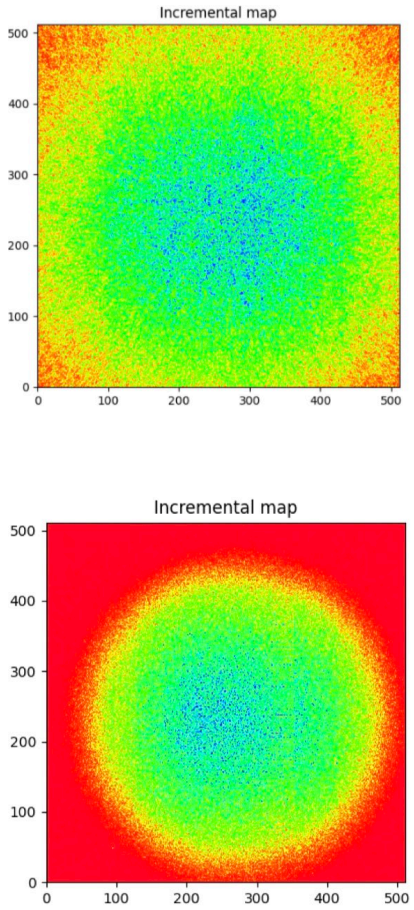
^{90}Sr (collimated 1mm)

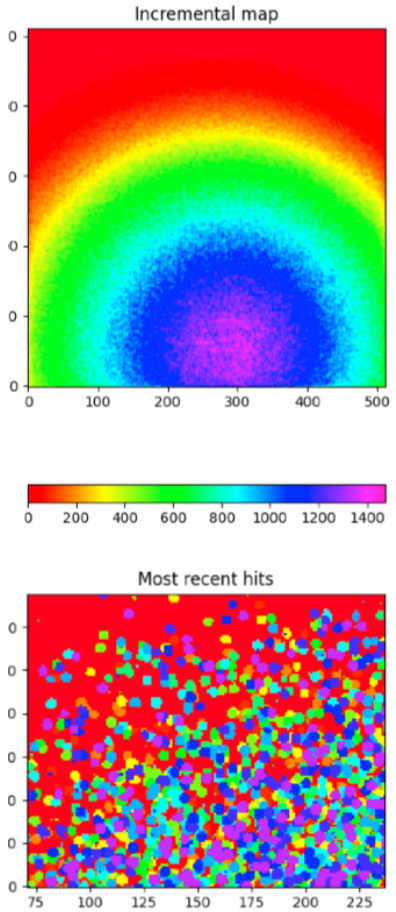
^{90}Sr (uncollimated)

^{241}Am

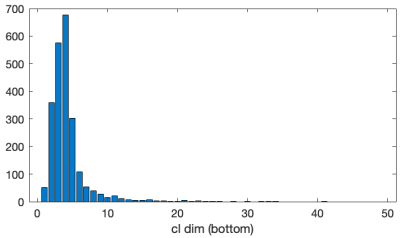


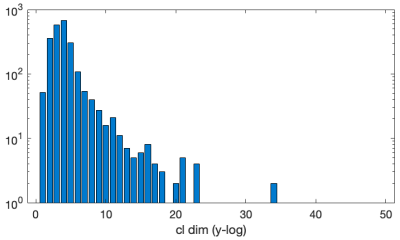


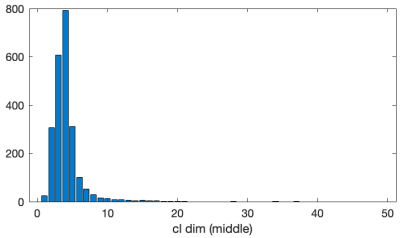


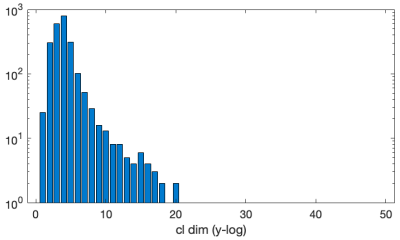


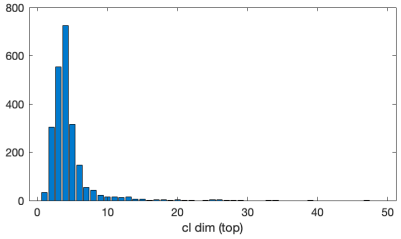
MD3 cosmic data: setup and cluster size

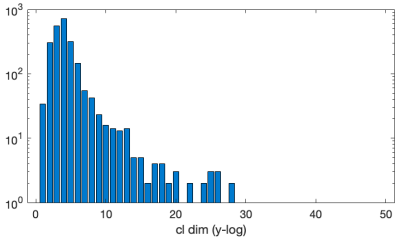


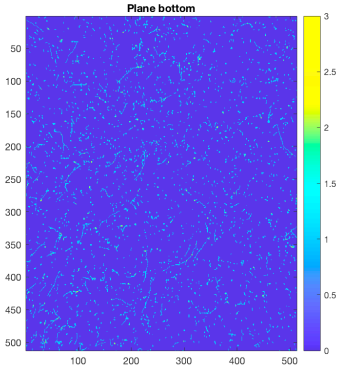


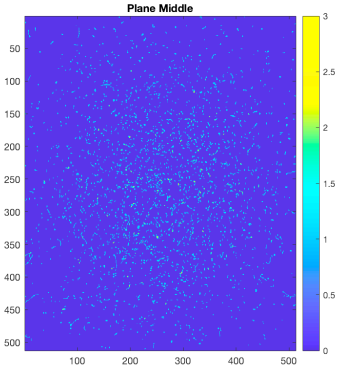


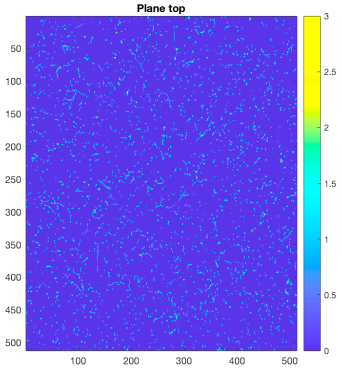




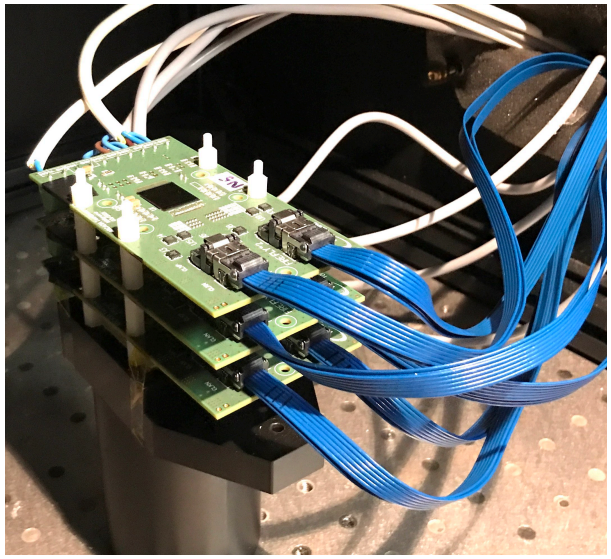








- Cosmic ray data taking: 1 week
- 3-plane MD3 installed on a black box, neither temperature control nor parameter optimisation (pixel discriminator V_{th} still to be equalised at double-column level).
- Threshold 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels



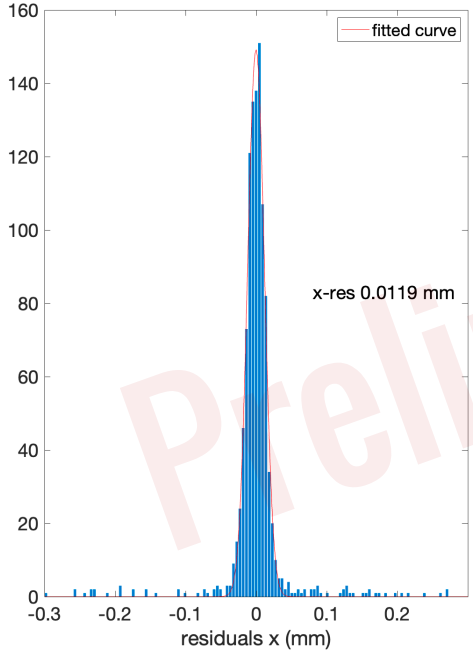
MD3 cosmic data: x-y residuals

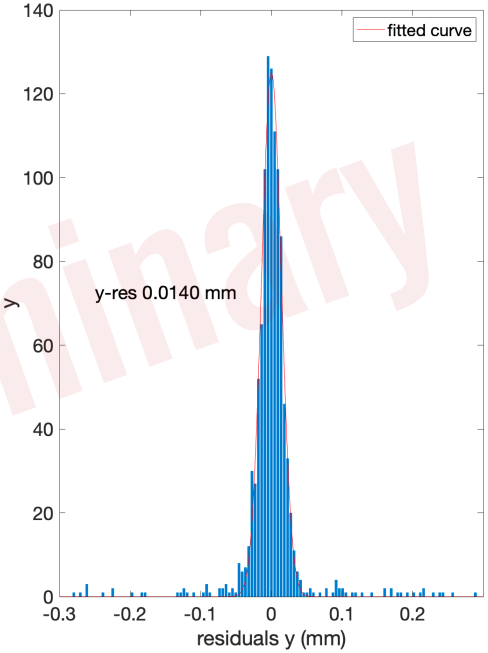
Preliminary data without mechanical alignment (3-plane setup without external references), ignoring multiple scattering:

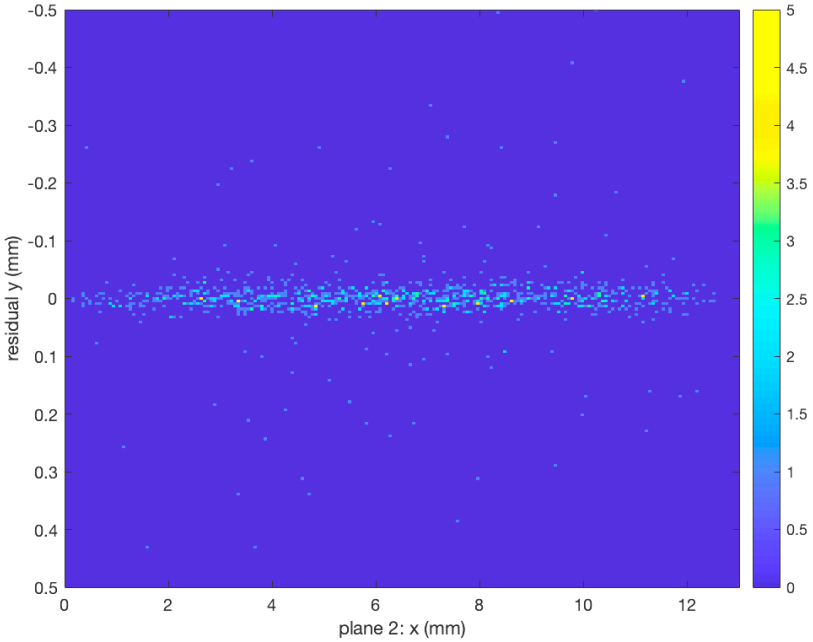
Selection criteria:

- 1 cluster per plane
- dt <= 10 clock cycles
- Cluster dimension <=4 in all planes

Selected ~46% of the synchronised events







FD Monolithic Active Microstrips

- Design and Production of continuous and “pixelised” strips, range 10 - 100µm pitch
- Proof-of-concept: CMOS monolithic strip block and readout electronics (active sensor area is 12800 × 3200 µm^2)

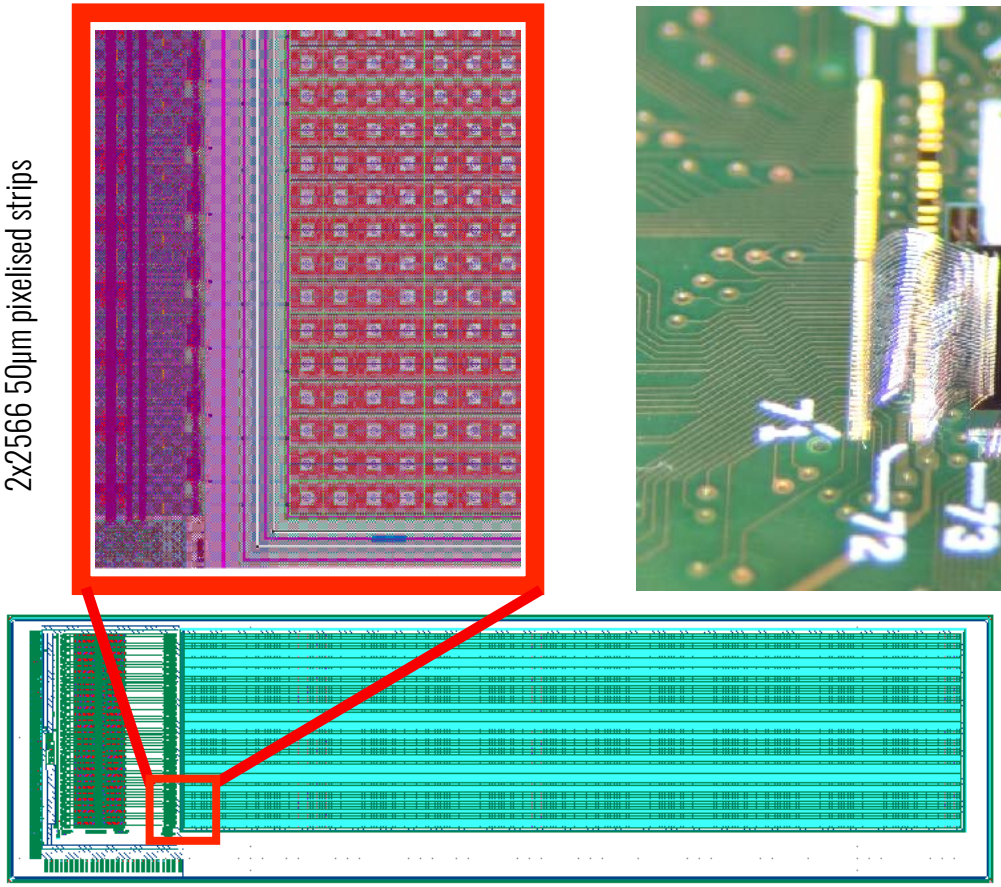
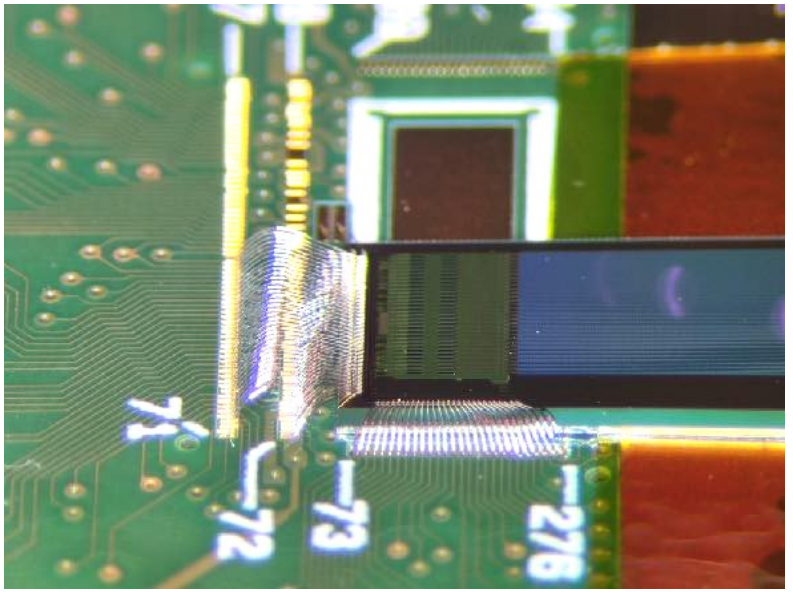


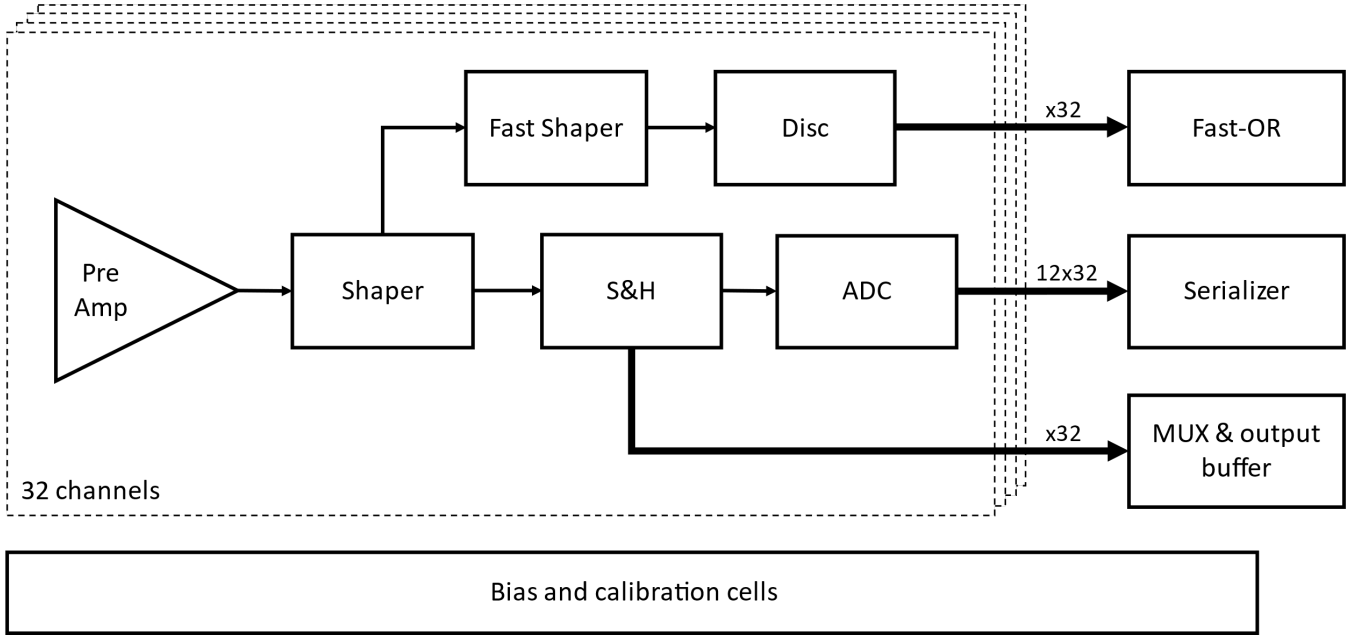
Figure: CAD Layout of 32-block of 2x2566 50µm pixelised strips



Fully Depleted Monolithic Active Microstrip Sensors: TCAD Simulation Study of an Innovative Design Concept. Sensors 2021, 21, 1990. https://doi.org/10.3390/s21061990

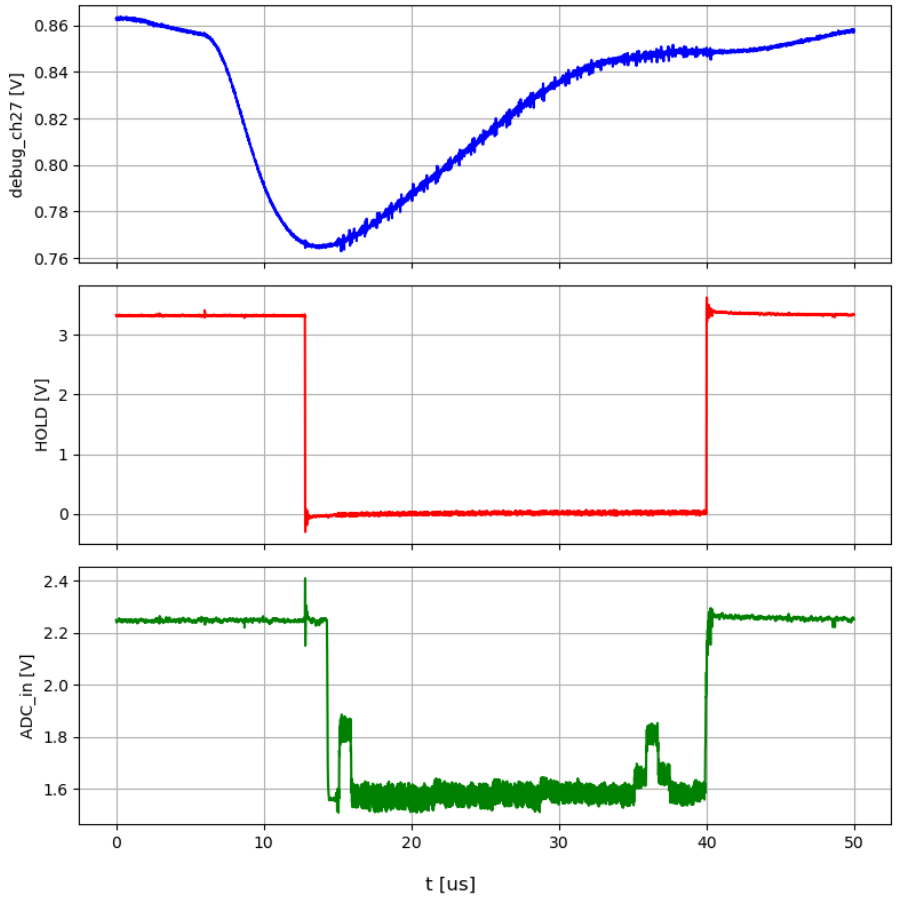
Readout: 32-channel architecture

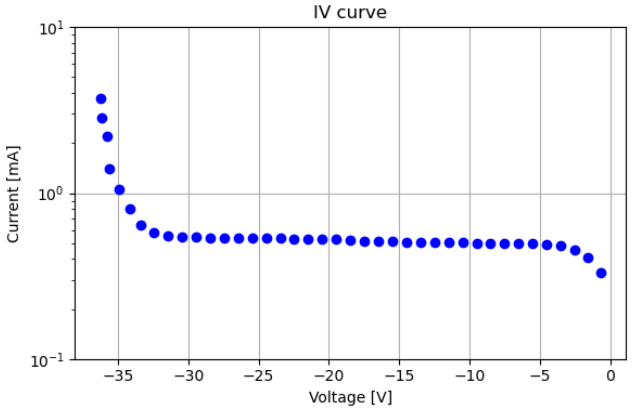
- preAmp: CSA + TP injection circuit
- Slow Shaper branch for charge measurement with externally controlled S&H circuit
- Analogue readout: MUX-differential output buffer
- Digital readout: Wilkinson ADC and serialiser
- Trigger output: Fast Shaper branch providing a fast-OR output



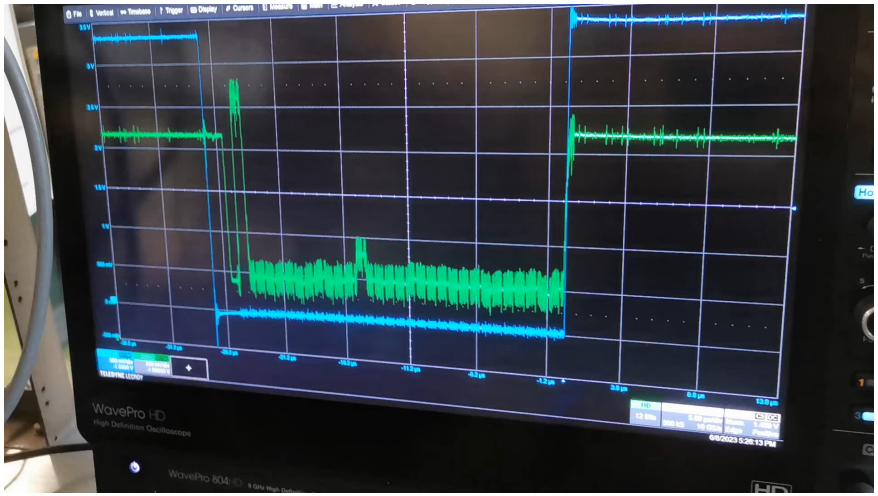
FD Monolithic Active Microstrips

First tests with ^{90}Sr



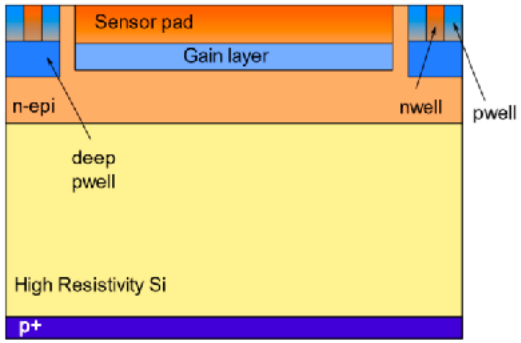


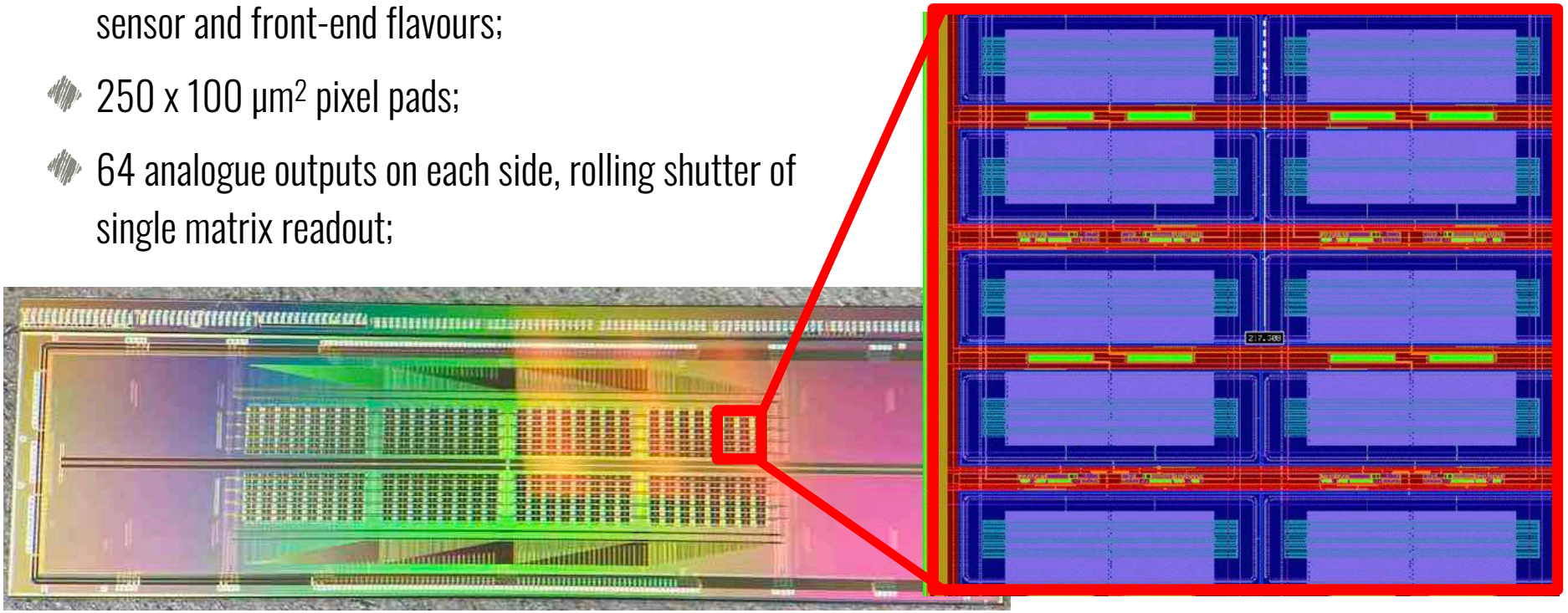
- ASTRA FastOR signal provides trigger to the FPGA
- FPGA sends HOLD signal and then start readout of analogue MUX



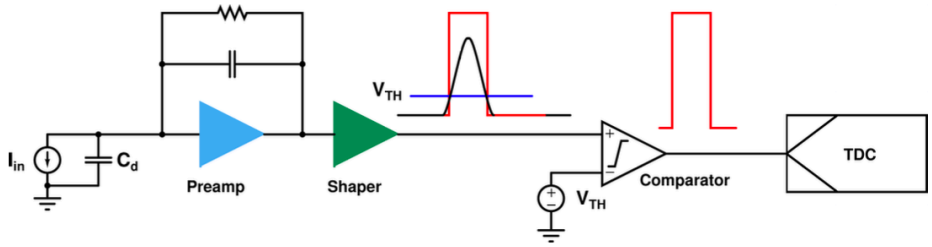
ARCADIA Sensor: R&D for fast timing

- partial lot of HR and p+ wafer splits implement an extra gain layer added to the sensor;
- first small-scale demonstrator 4 x 16 mm^2;
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- 250 x 100 μm^2 pixel pads;
- 64 analogue outputs on each side, rolling shutter of single matrix readout;



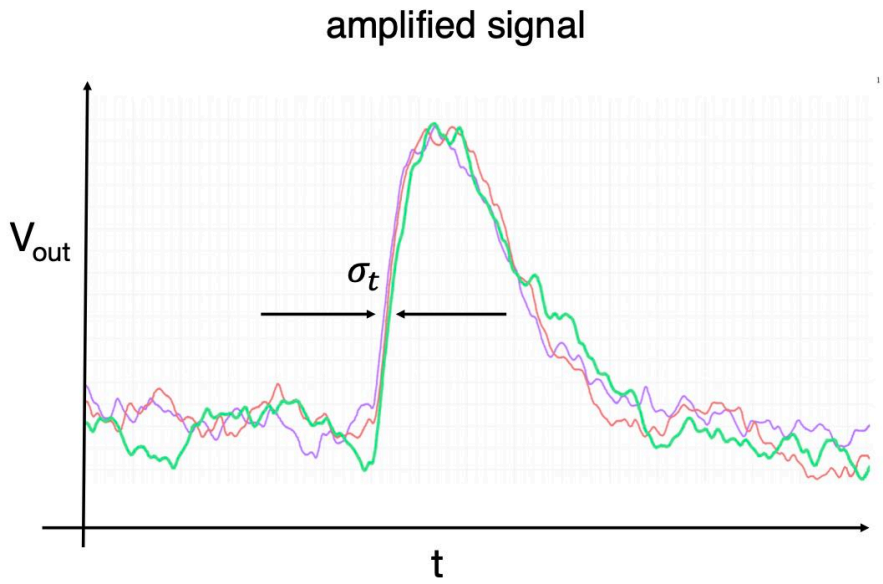


Resolution of a Si timing detector



$$\sigma_t^2 = \sigma_{timewalk}^2 + \sigma_{Landau}^2 + \sigma_{TDC}^2 + \sigma_{Jitter}^2$$

- **Time Walk**: minimised by using Constant Fraction Discriminator (CFD) for time reference
- **Landau** noise: Landau fluctuations of the charge deposited during the FEE integration time); reduced for thinner sensors (50, 35 μm)
- **TDC**: quantisation error of the time-to-digital converter (bin/√12)
- **Jitter**: reduced by increasing SNR with gain.

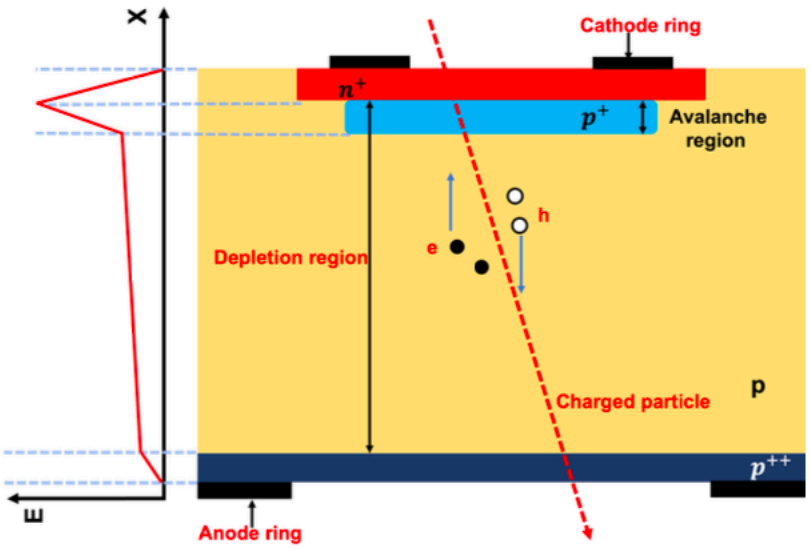


$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{t_{rise}}{Signal/Noise} \cong \frac{ENC}{I_{Ind}}$$

- Low Equivalent Noise Charge (**ENC**) with a low noise amplifier
  - For a given power and bandwidth: **ENC α C_d**
- Larger I_{Ind} possible with a gain layer

courtesy: T. Kugathasan

Low Gain Avalanche Detector (LGAD)



- Silicon detectors with charge multiplication
- Gain layer provides a high-field region
- Radiation hard (10^{15} neq/cm^2)
- Low Noise (low shot noise)

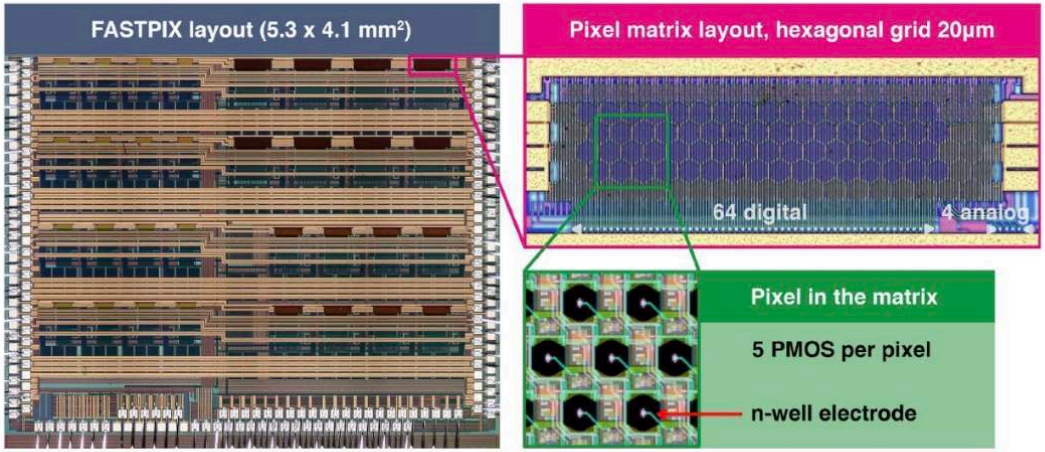
- Improved SNR: 5-10 times better than current PIN detectors
- Good timing resolution:
  $\sigma_t = 30$ ps $\rightarrow$ 50 µm thick LGADs (1.3×1.3 mm^2)
- No-gain region $\sim$ 30-80 µm
  A. Bisht et. el., Characterization of Novel trench-isolated LGADs for 4D tracking
  $\rightarrow$ No-gain region $\sim$ 3 µm

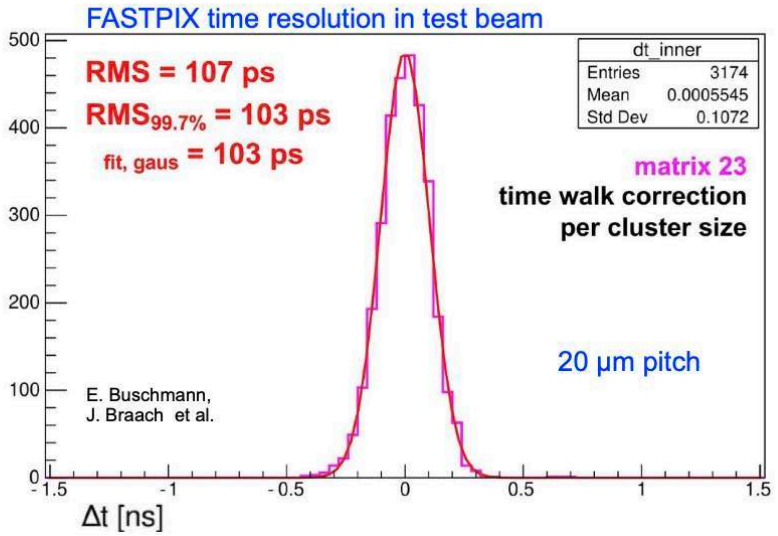
courtesy: Ashish Bisht (FBK)

FastPIX (180nm)

exploring the intrinsic limits of 180 nm

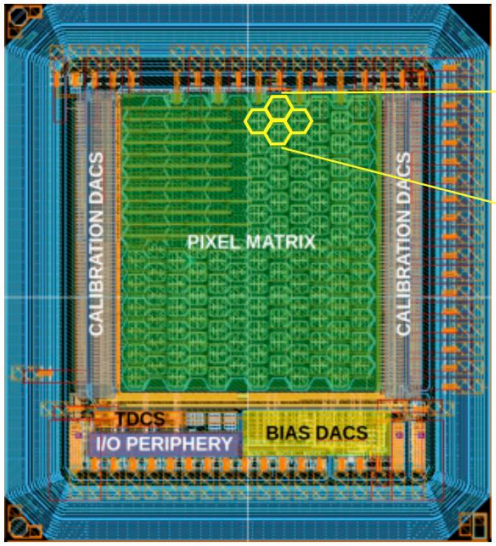
- Small (8.66 to 20 µm) hexagonal pixels with optimised process for fast charge collection
- Time resolution: ~100 ps achieved in test beam at >99% efficiency
- Position resolution: ~1 µm for 8.7 µm pitch
- So far, "only" a technology demonstrator

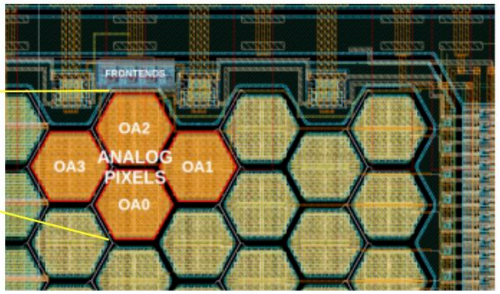




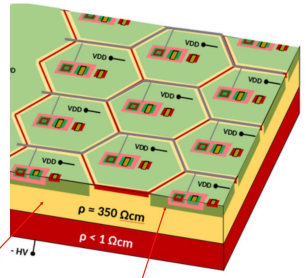
D. Dannheim, BTTB 2023

SiGe HBT sensors for picosecond-level timing



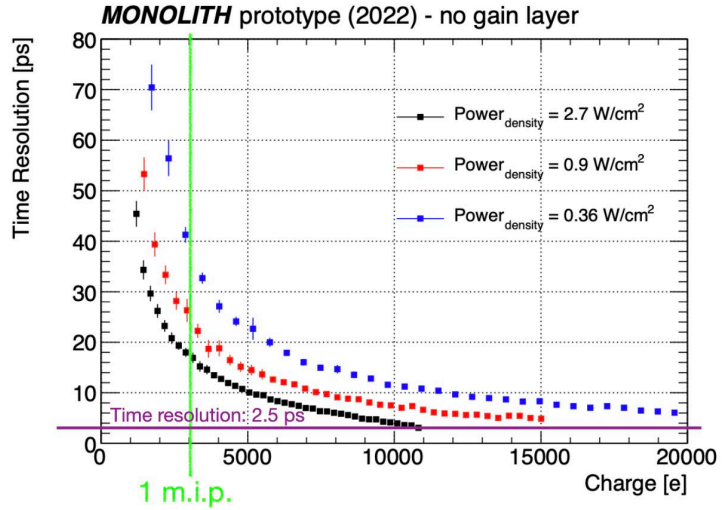


100 µm pitch
Hexagonal grid
65 µm



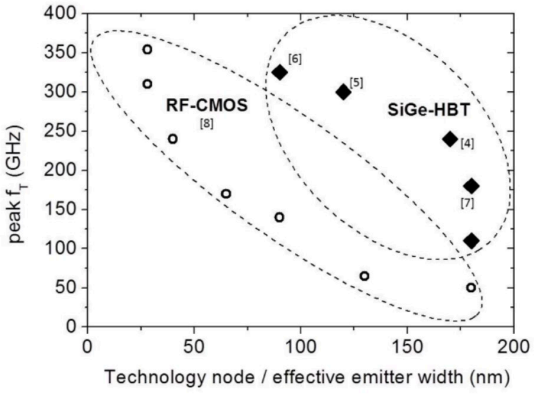
1. heavily P-doped substrate. Negative High Voltage
2. High resistivity epitaxial layer as active volume (50 µm thick)
3. Electronics inside the n-well (collection electrode). Nwell potential kept at positive low voltage (vdd).

courtesy: T. Kugathasan



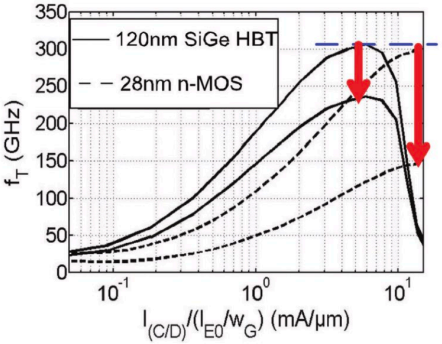
IHP SG13G2 130 nm process featuring SiGe HBT

Peak transition frequency vs. technology node



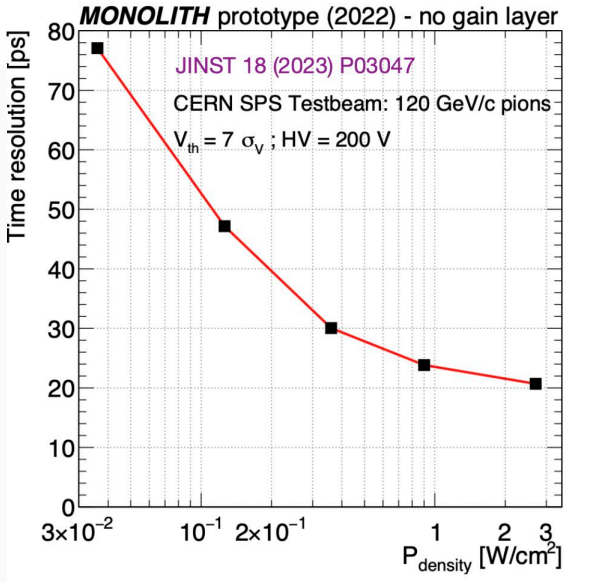
A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

Peak transition frequency vs. current density



Robustness to parasitic

M. Schröter, U. Pfeiffer and R. Jain, Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications.



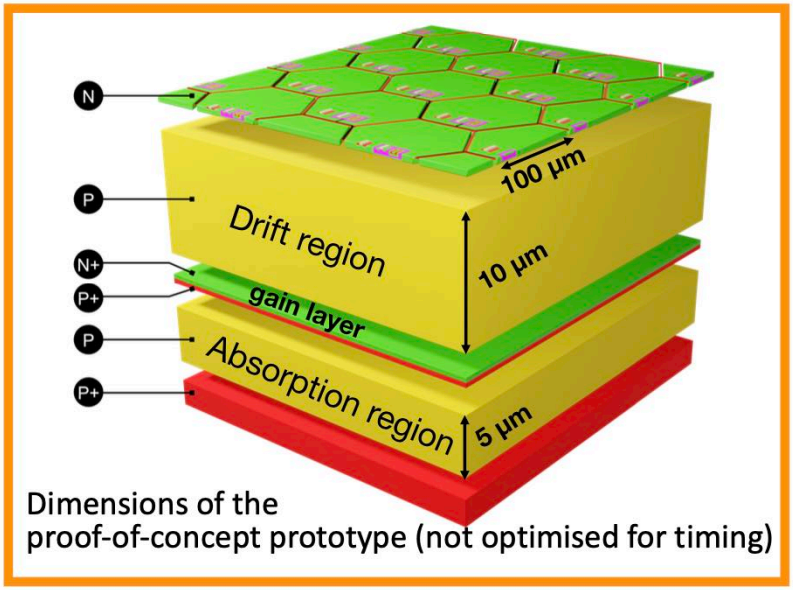
PicoAD Sensor Concept

PicoAD: Large collection electrode, SiGE (Heterojunction Bipolar Transistor) HBT **with gain layer**

Multi-Junction Picosecond-Avalanche Detector©
with continuous and deep gain layer:

- De-correlation from implant size/geometry
  → **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  → **reduced charge-collection noise**
  (enhance timing resolution)

gain 60–70 for a MIP



Dimensions of the
proof-of-concept prototype (not optimised for timing)

The PicoAD© sensor works. Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps : 13 ps** at center and **25 ps** at pixel edge
  (although sensor not yet optimized for timing)

courtesy: T. Kugathasan

Novel trends

"Nuclear powered vacuum cleaners will probably be a reality within 10 years."

Alex Lewyt - 1955

Novel trends

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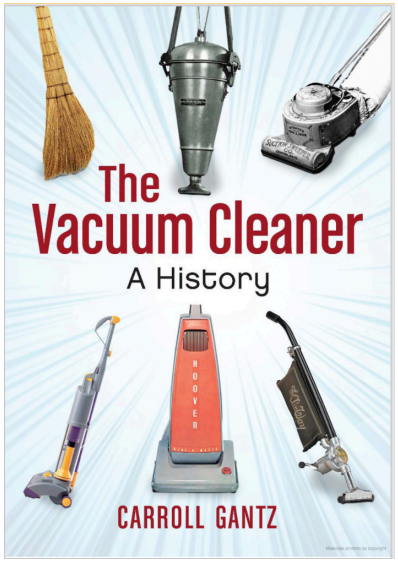

quoted in the same year as
"the worst prediction of all time"
by the New York Times

Novel trends

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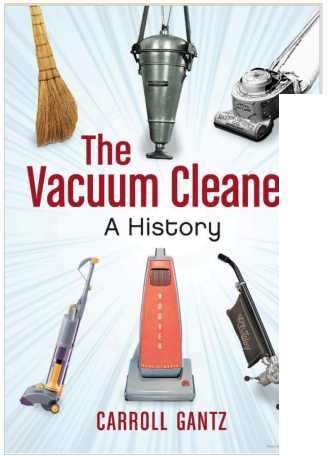

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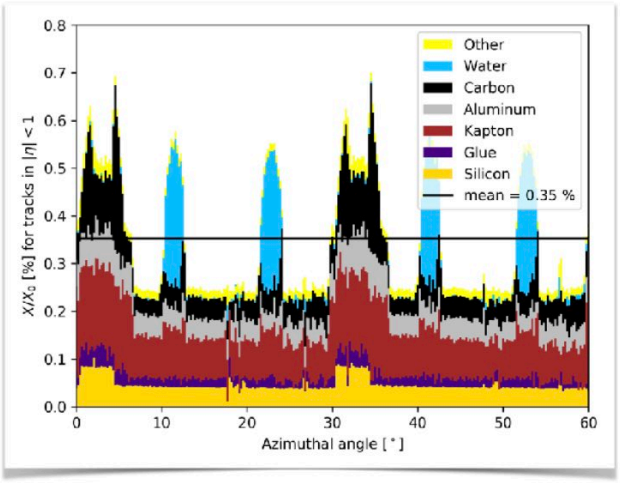
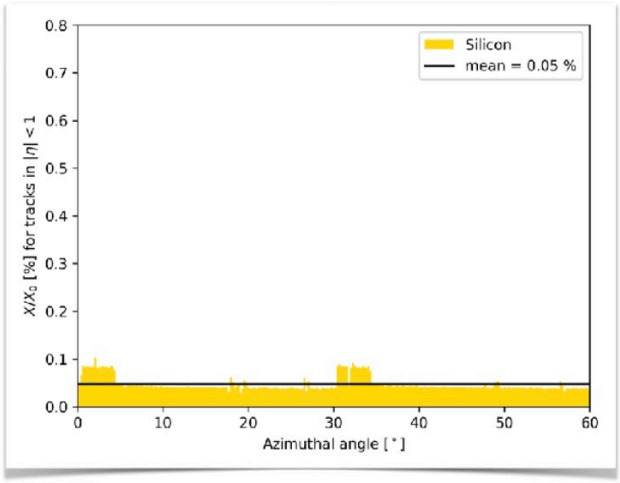
Predicting the future, or even the next decade, of silicon detectors could give you hilarious material for the XLI Edition of this School…

Trending up: go "green"





courtesy slide from Magnus Mager

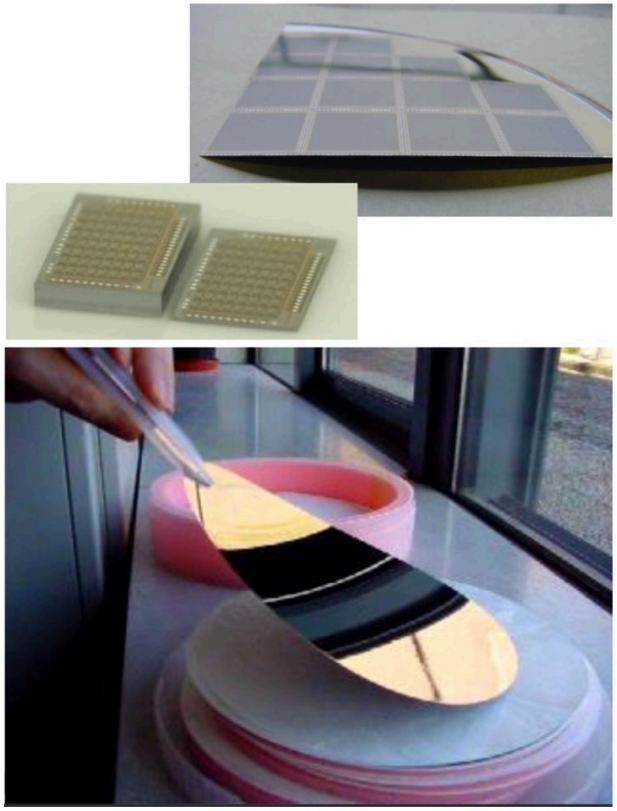
- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/cooling
- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm²
- Removal of the circuit board (power+data)
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

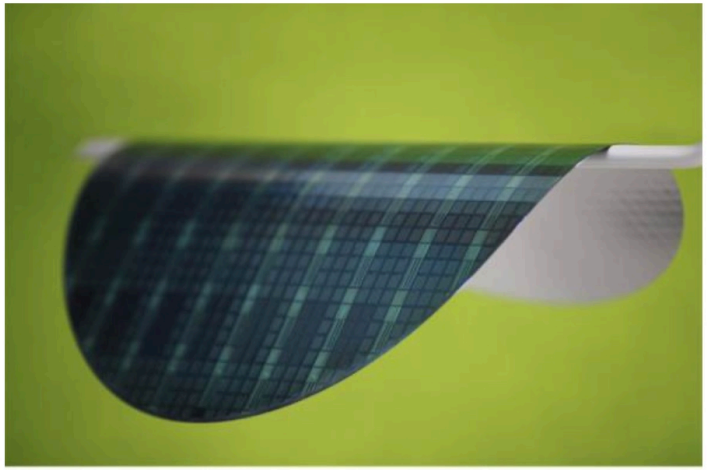
* Power requirement needs to be lowered to O(20mW/cm²)

Trending up: go thinner

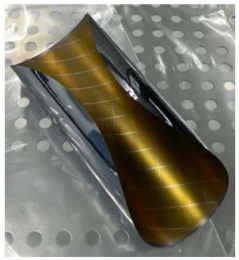
- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

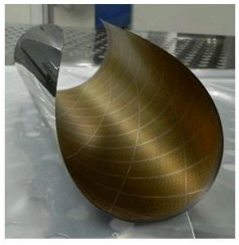
P. De Moor (IMEC)

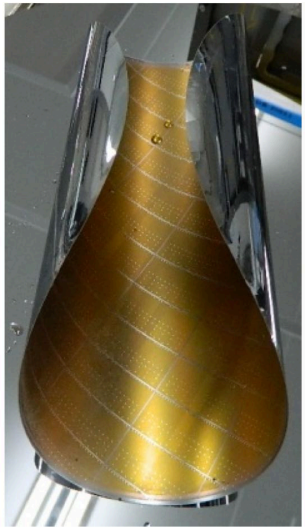




50 µm thin 300 mm Silicon Interposer Wafer with Cu-RDL metallisation. Source: Fraunhofer IZM







* **Wafer-scale ultra-thin (< 20 µm) stitched MAPS could bend into a cylindrical mechanically stable self-supporting shape:**

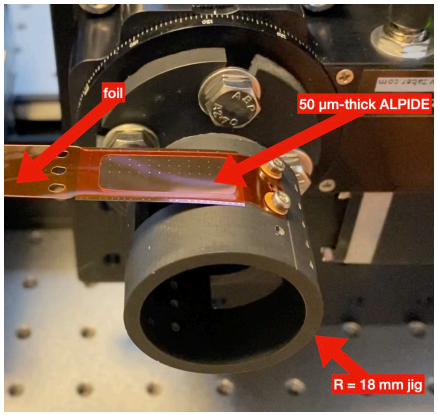
☑ purely Si based collider detector for tracking and PID with a VERTEX with an unprecedented low material budget of < 0.05 % X_0 per layer

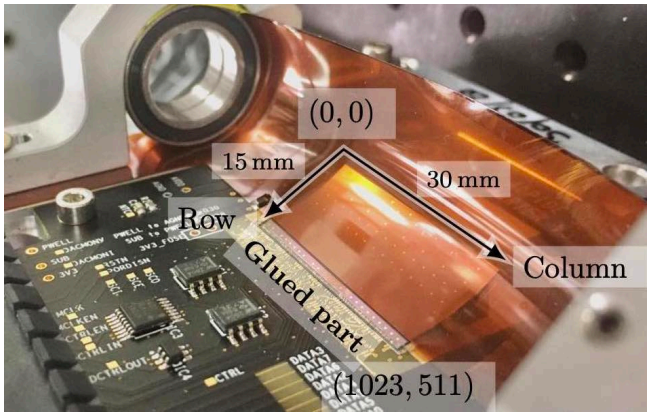
Wafer Thinning, applied to MAPS

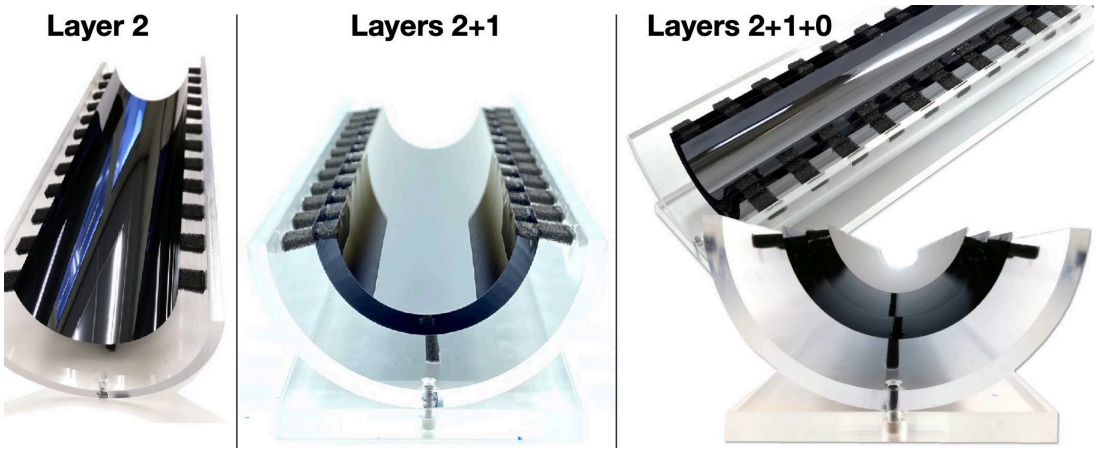
or… µITS3, i.e. 6 ALPIDEs at ITS3 radii

ALICE ITS3 working group demonstrated the bending, operation and performance of thinned MAPS, using 1.5 cm × 3 cm ALPIDE chips, and system studies towards the integration of wafer-scale sensors

- bent to radii of about 2cm without any signs of mechanical or electrical damage
- characterisation using a 5.4 GeV electron beam, detection efficiencies above 99.9 % at typical operating conditions
- 3-layer integration successful using 50 µm dummy Silicon



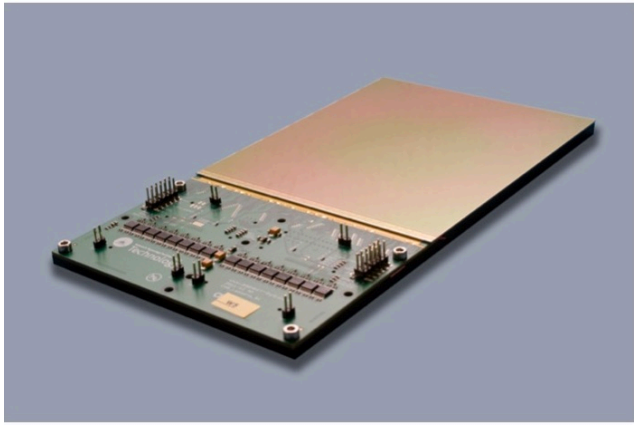


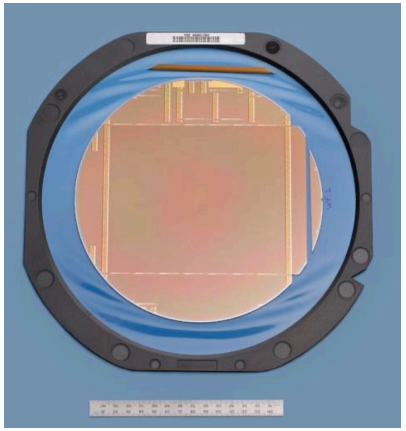


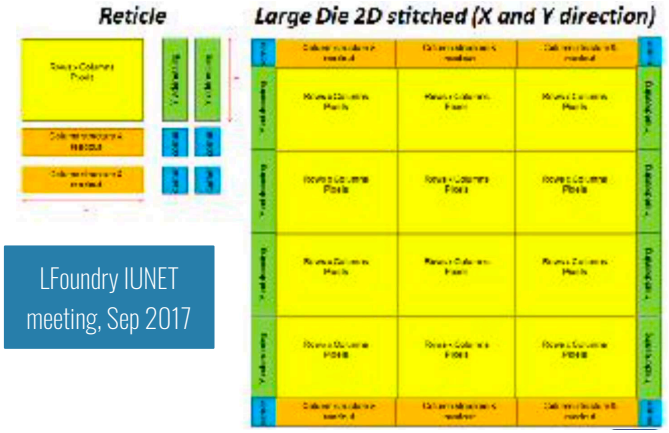
Magnus Mager CEPC2021

arxiv:2105.13000 "First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors"

Trending up: Bigger, Stitched Silicon







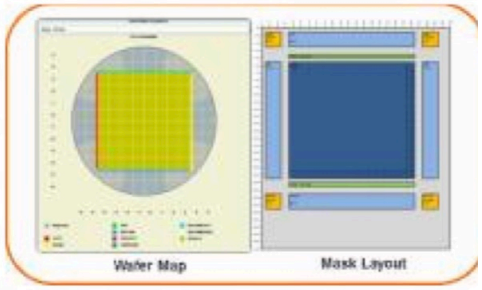
LFoundry IUNET meeting, Sep 2017

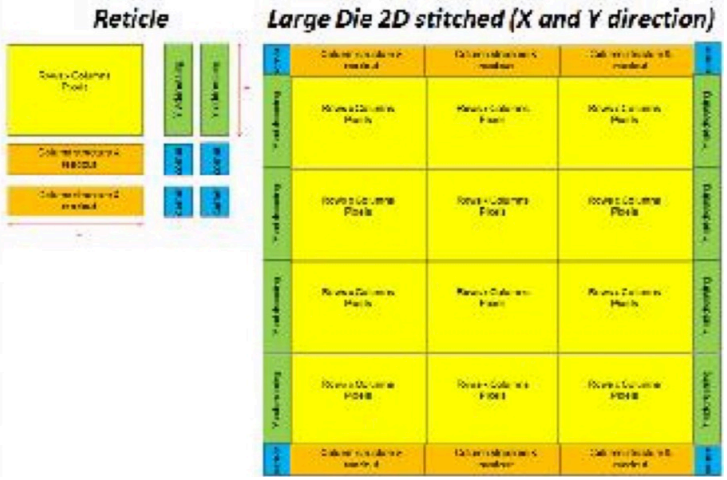
- (left) **Example of a wafer-scale imaging sensor chip for X-Ray applications developed at RAL (UK)**
- **139 x 120 mm CIS, Towerjazz 180nm on 200 mm (8'') wafers, 1 sensor per wafer**

- 2D Stitching paves the way for all-silicon CMOS monolithic APS as active interposers: substrate handles signal, power and data interconnects, enabling the development of ultra-low material budget trackers;
- particularly interesting assuming 12" wafers, very low power (no water cooling) and no mechanical support for an only-silicon inner tracker in future HEP colliders. Different considerations may apply for an outer Si-tracker…

2D Stitching

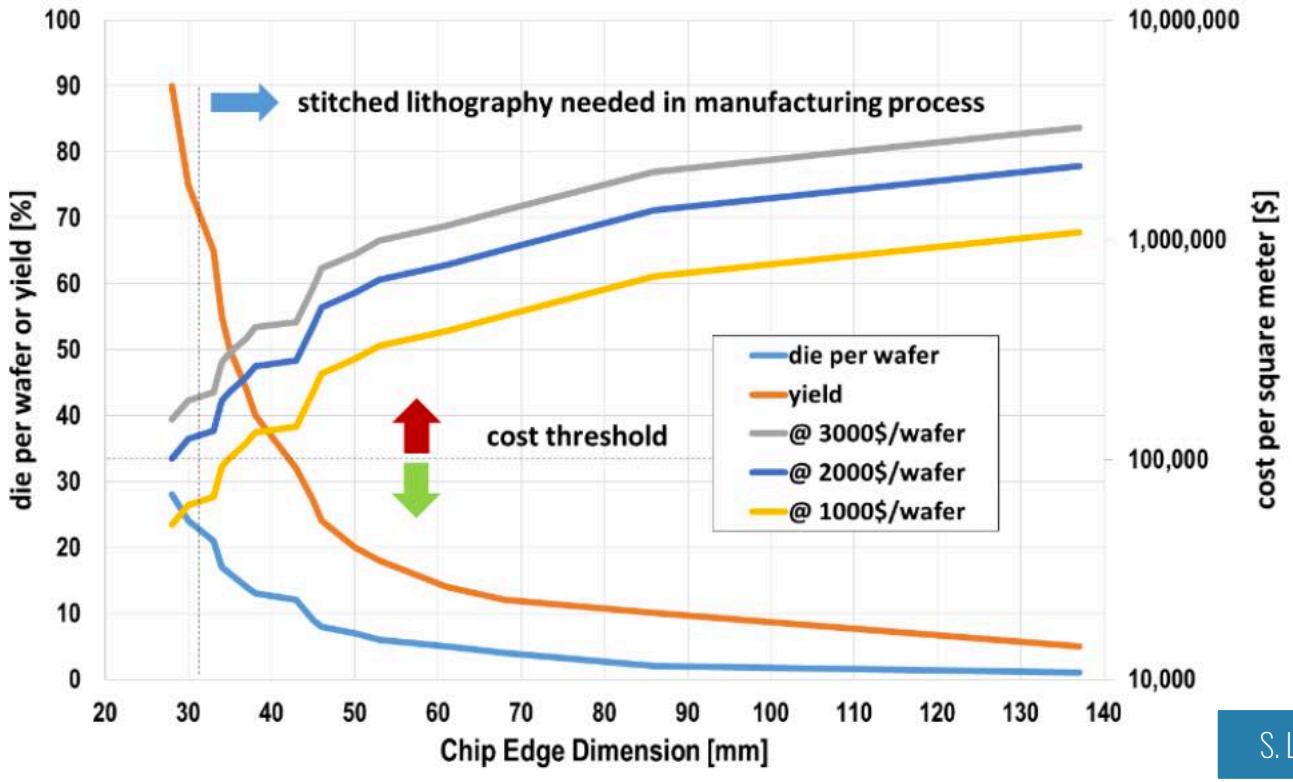
- Need for image sensor sensors with larger size than the field of a semiconductor lithography equipment is not new
- However the challenge is the need of customized solutions for the wide field of different applications i.e.
  - 1D Stitching in low complexity (non CMOS) optical sensors (PDs) for large panels and thus interaction with final assembly concepts
  - 2D Stitching within wafer with high complex circuitry and thus challenge of device/layout optimization on stitching borders





LFoundry presentation at IUNET meeting, Sep 2017

Cost and Yield considerations (my favourite slide on)



S. Lauxtermann, PIXEL2018

Cost of $100,000/m² tracking area is achievable with the following assumptions

- **> 75% Yield**
- **No stitching**
- **Wafer cost <$2,000 (only achievable using high volume CMOS manufacturing)**

Summary and Outlook

- Advanced integration technologies introduced by the imaging industry is driving the development of frontier detectors for science: TSV, fine-pitched bump bonding, wafer-wafer bonding
- 3D integration of sensor and readout tiers using TSV and/or BSI (for photon detection) are pushing the limits of highly segmented high-gain silicon detectors for time-of-flight measurements with excellent timing and spatial resolution
- The development of very low-power monolithic fully-depleted sensors using standard CMOS lines and foundries is an enabling technology for future colliders, both for future low material budget silicon trackers and for timing layers, space and medical applications

> CMOS Sensors seem to have created a "class by itself, and anything in a class by itself is likely to go a long way." (Arthur H. Snell)

Thank you for listening!

CMOS sensors and readout for experimental physics: challenges, opportunities and future trends

Giornate di Studio sui Rivelatori

Cogne

June 26th - 30th, 2023

Istituto Nazionale di Fisica Nucleare

Manuel Rolo (INFN)