Falaphel

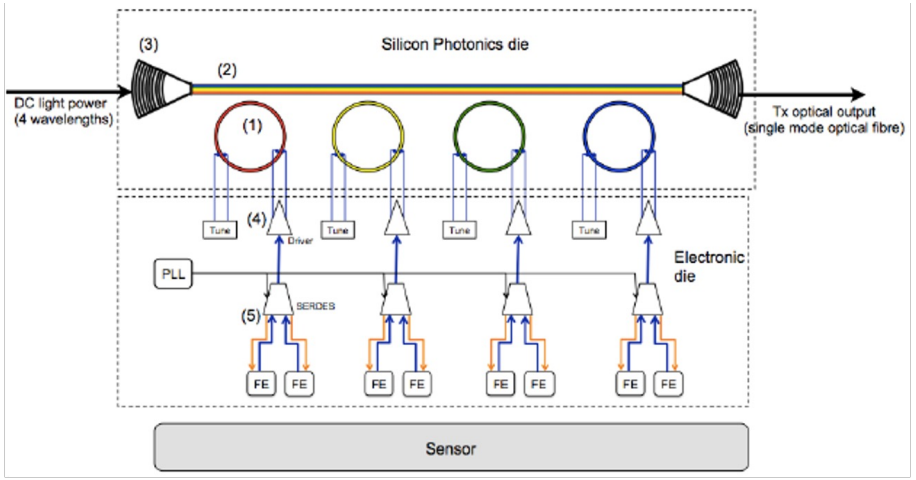
Preventivi 2024

Fabrizio Palla

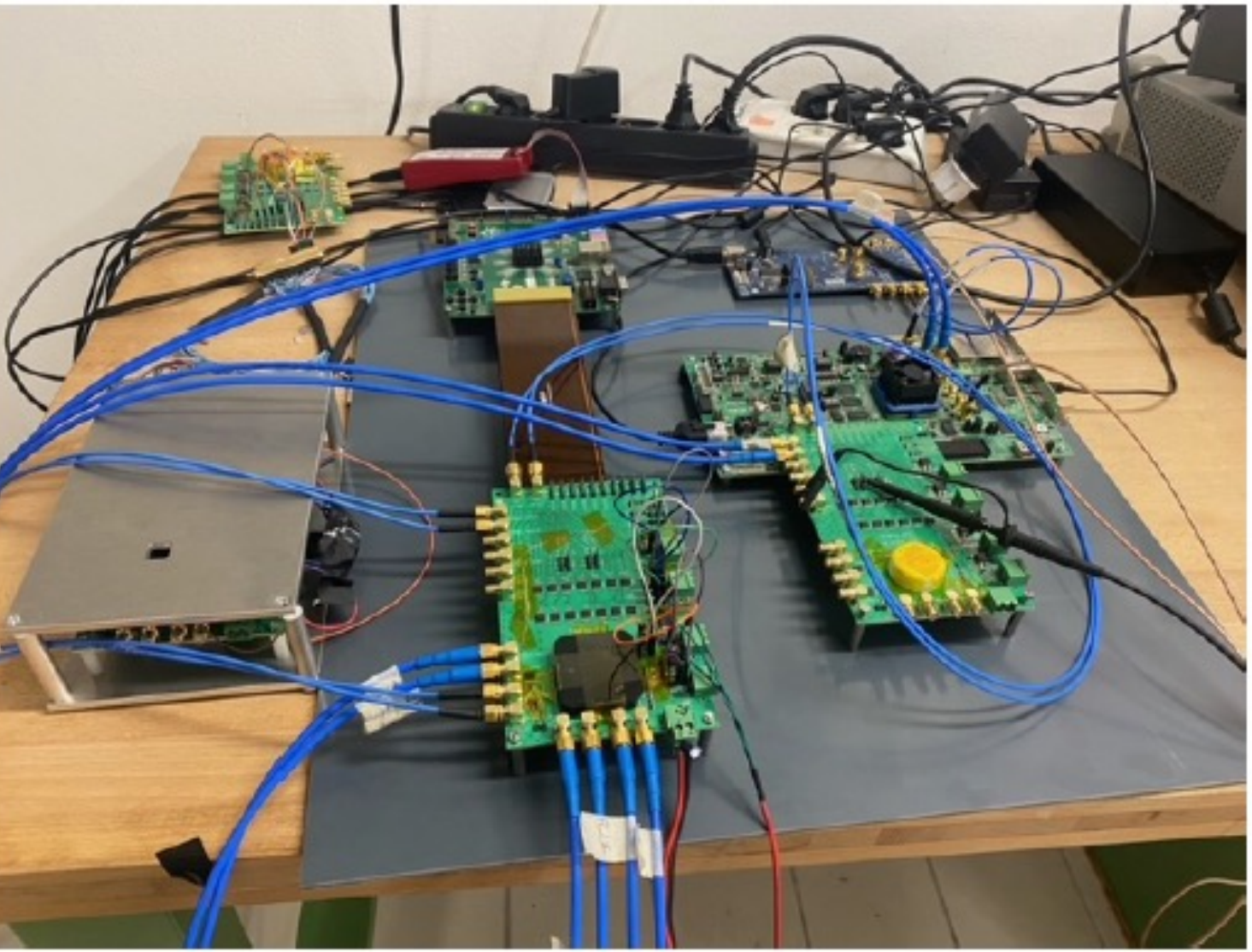
6 luglio 2023

Attività 2023 → 2024

- FALAPHEL finisce nel 2023 … ma ancora sottomisisoni, testare i chip e fare il dimostratore
  - **Analog Front-End (Pavia)**
    - Test FLASH ADC in corso
    - TOT based da sottomettere
  - **Serializzatore (Pisa)**
    - CML irraggiamenti in corso (TID, SEU)
    - CML DDR sottomesso
    - Disegno CMOS in corso – da sottomettere
  - **Driver (Pisa)**
    - CML da irraggiare
    - CMOS da progettare
  - **Chip fotonico (Pisa)**
    - Risultati irraggiamenti fatti a Padova
    - Progettazione chip finale
  - **Bonding PIC+EIC (Pisa)**
    - da definire – possibili sinergie con IGNITE
  - **Caratterizzazioni TID e SEE (Padova e Pisa)**



SER_V1 (Test and Characterization)



Test Setup ready for SEU test at LNL

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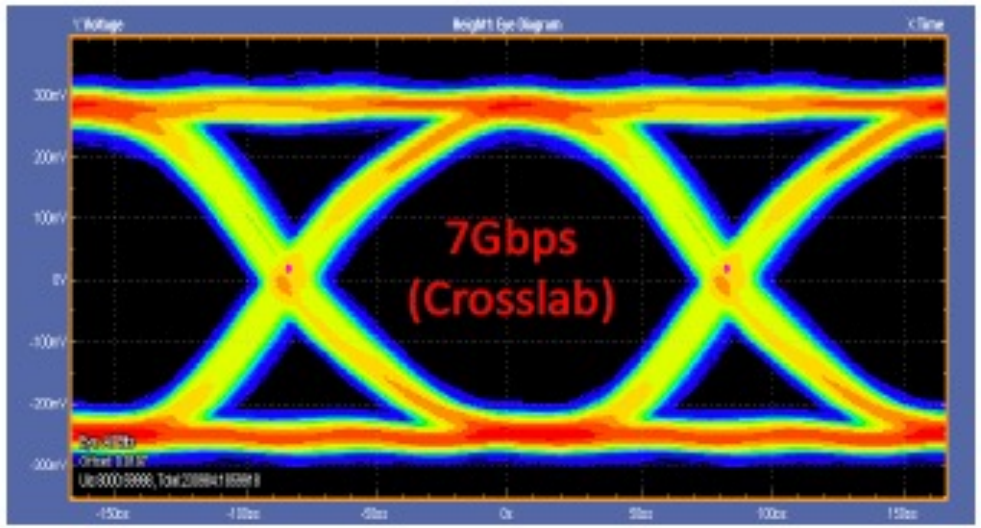
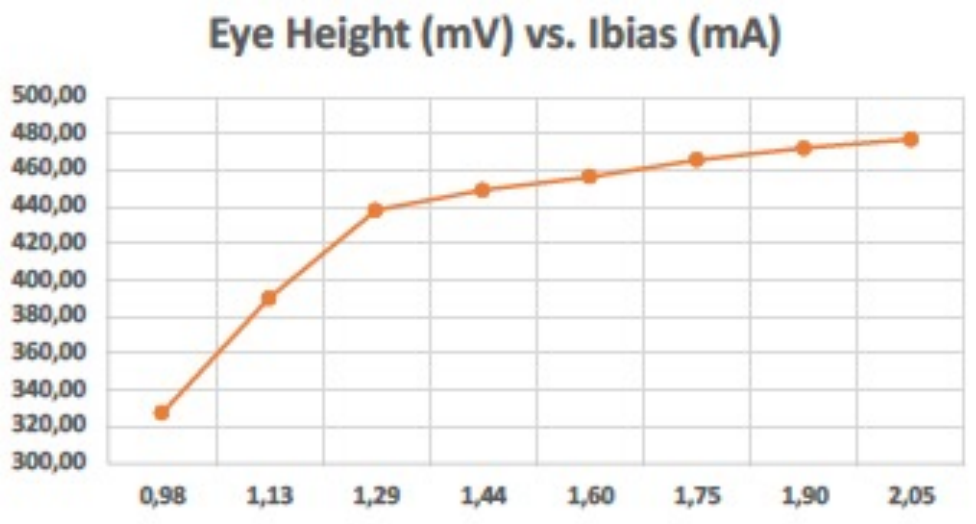


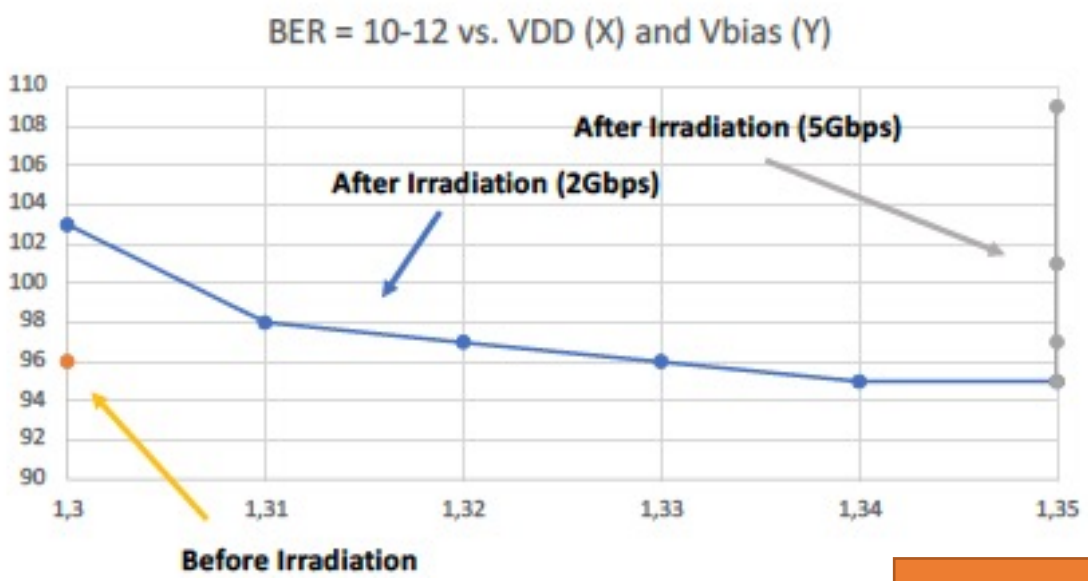


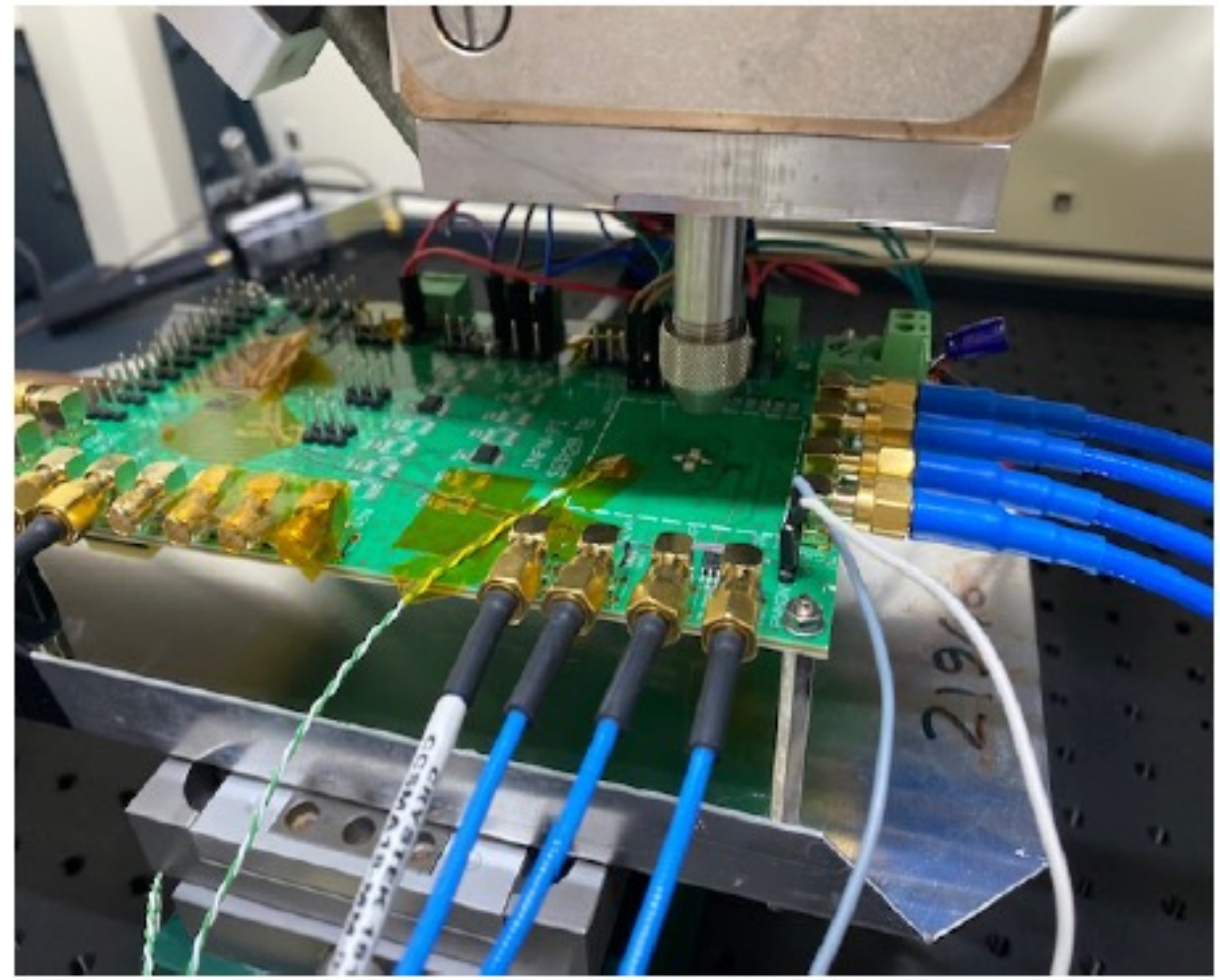
G. Magazzù/ M. Minuti/ P. Prosperi/ F. Morsani

SER_V1 (Test and Characterization)

TID Test @ INFN-Pisa

- **Dose Rate = 3.1 Mrad/h**
  - **V = 40KV**
  - **I = 40mA**
- **TID = 1.25Grad (17 days!)**
- **BER measured during and after irradiation**
  - **Data Rate = 2-5Gbps**
  - **Acquisition Time = 500s => BER = 10^{-12} (different Vbias and Vdd values)**
- **Small increase of BER (expected) recovered by bias adjustment**





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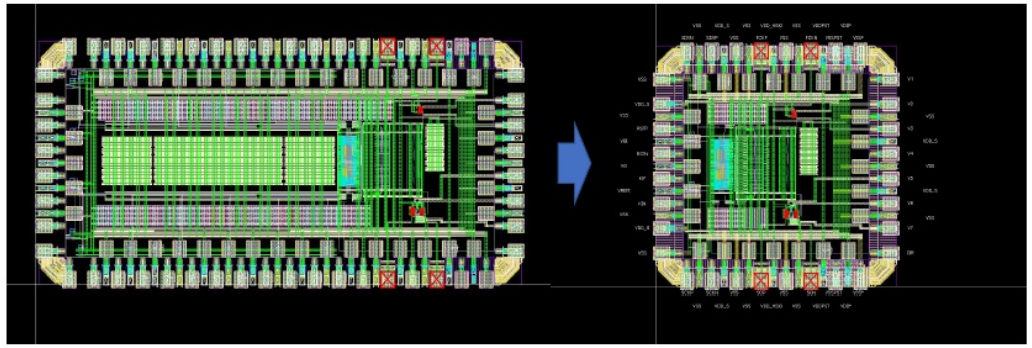
Ser_V2 e Ser_V3 (CMOS)

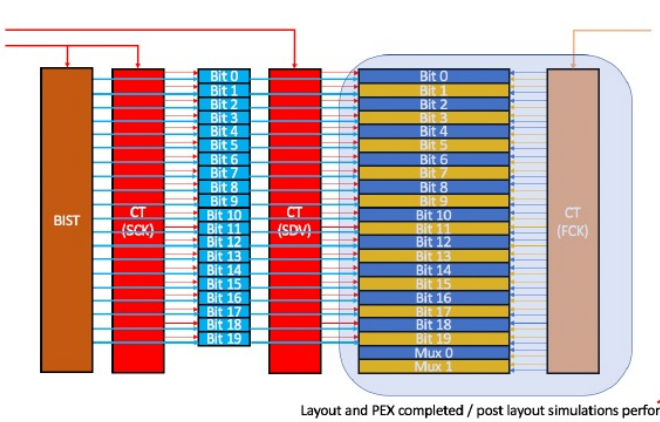
SER_V1 to SER_V2



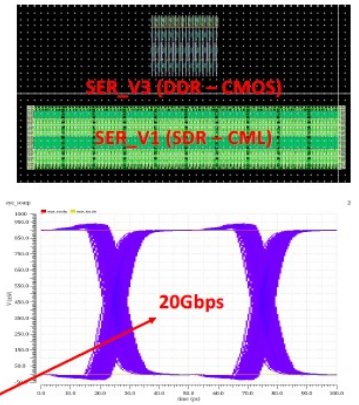
SER_V1 (SDR – CML)

SER_V2 (DDR – CML)

SER28_V3 (CMOS)



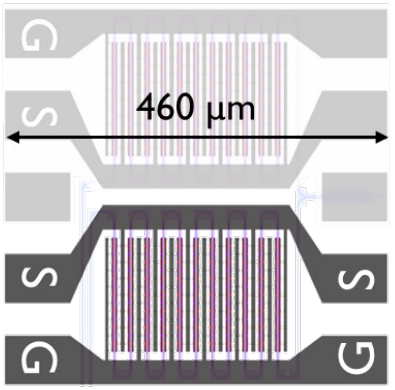
Layout and PEX completed / post layout simulations performed

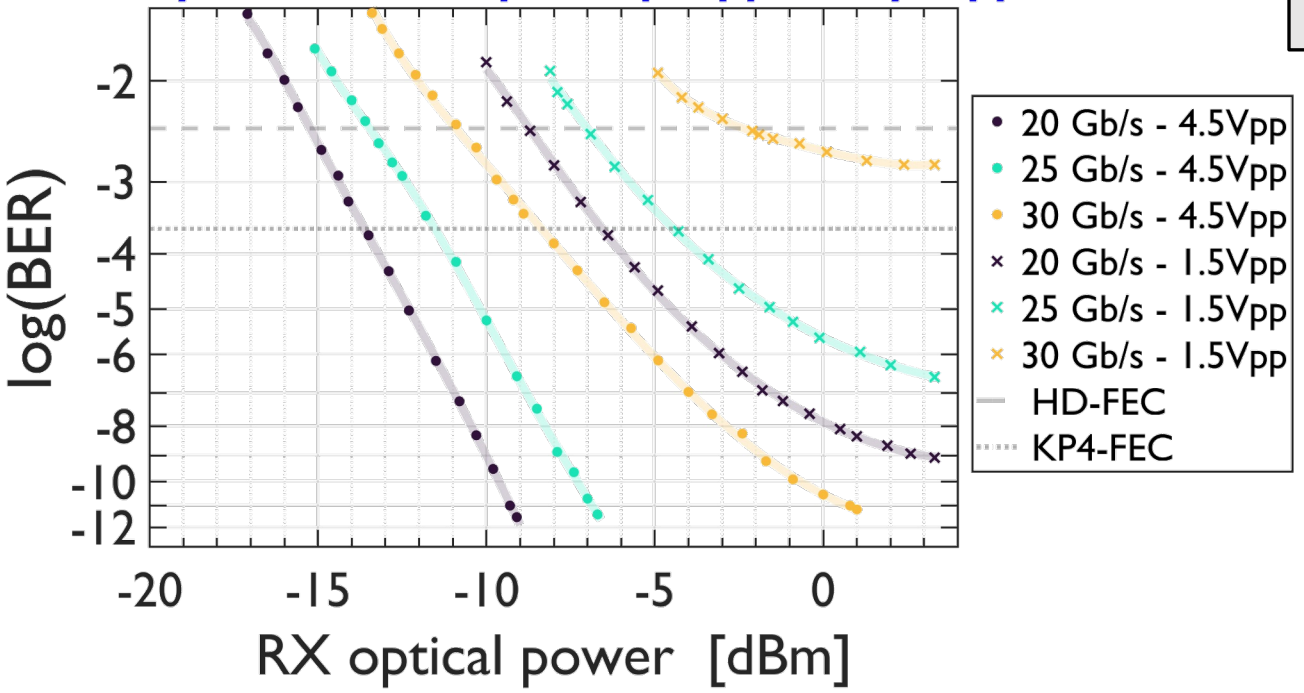


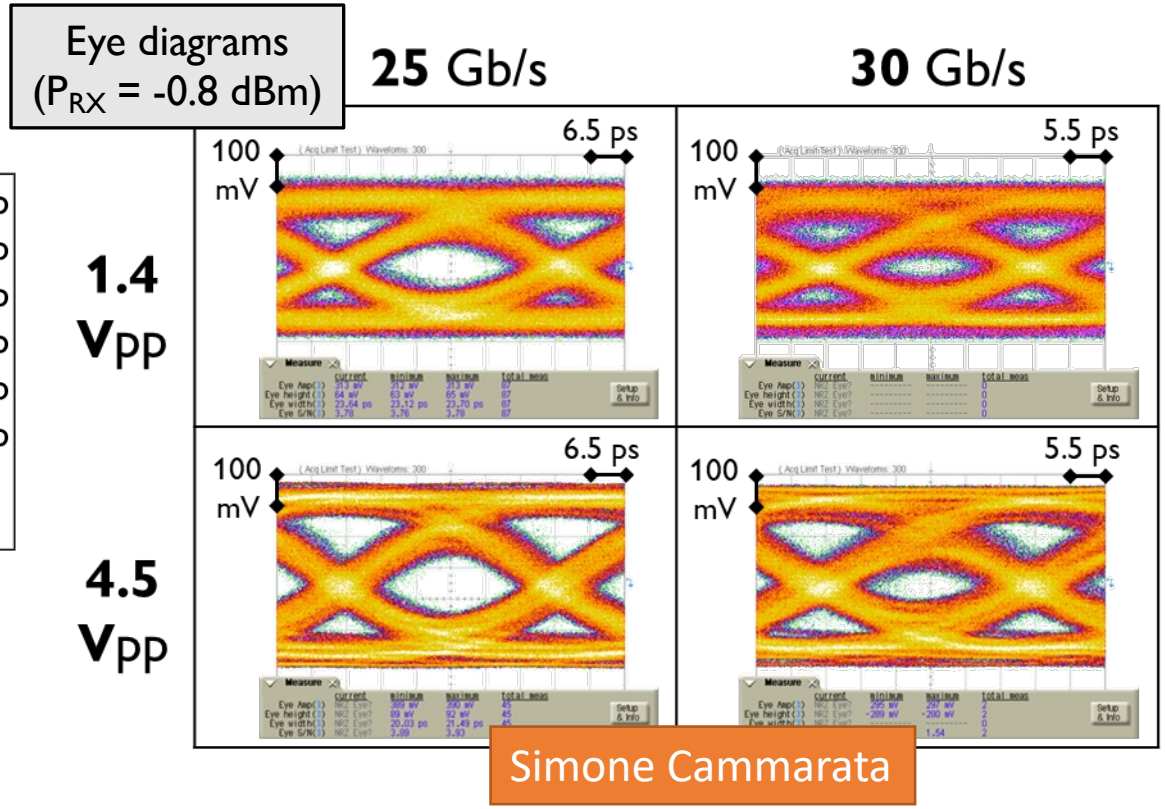
G. Magazzù/P. Prosperi

PICv1 FMZM1 Large-Signal Results (2/2)

- Folded MZM tested with different driving voltages in quadrature:
  - 4.5 Vpp (**4 V** bias)
  - 1.4 Vpp (**4 V** bias), “CMOS-compliant” level
- Driving voltage-induced power penalty ~ 7 dB at KP4-FEC limit





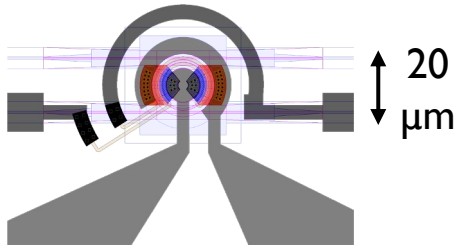


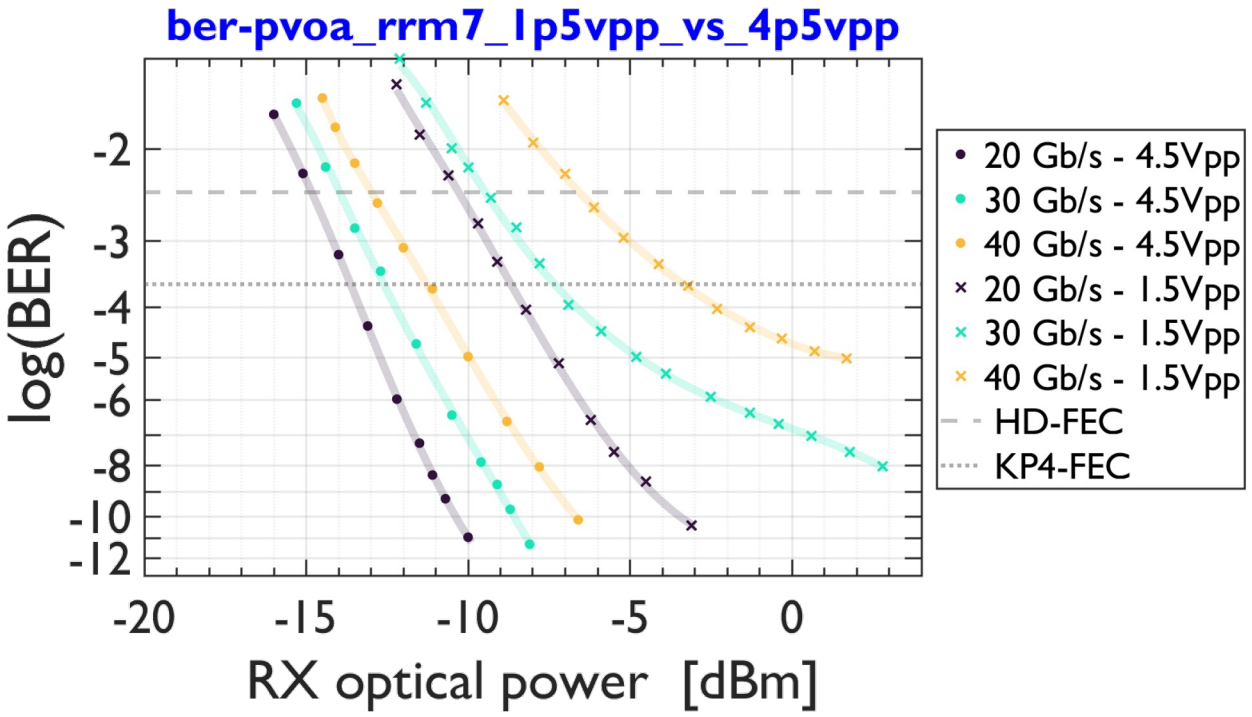
Simone Cammarata

PICv1 RM7 Large-Signal Results (2/2)

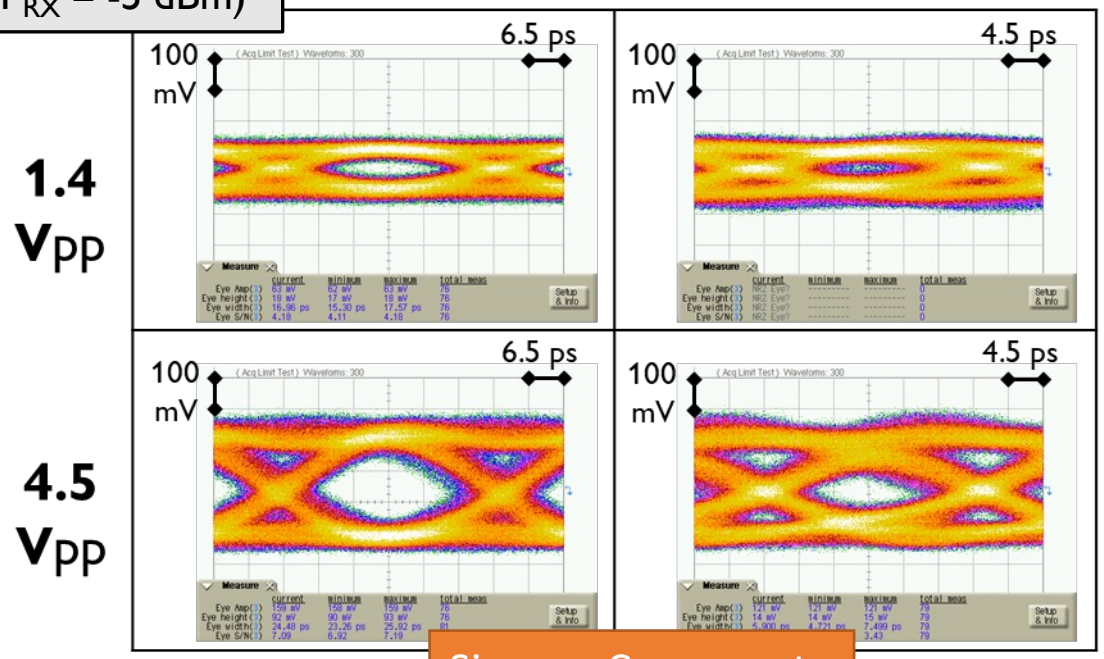
- Add-drop 7.5 µm-radius RM tested with different driving voltages:
  - 4.5 Vpp (**3 V** bias)
  - 1.4 Vpp (**0 V** bias), CMOS-compliant level
- Driving voltage-induced power penalty ~ 5 dB at KP4-FEC limit

FWHM	~ 790 pm
Q	~ 2000
Modulation **depth**	~ 15 dB
Modulation **efficiency**	~ 25 pm/V





Eye diagrams (P_{RX} = -5 dBm)



Simone Cammarata

Pending richiesta estensione

- Alcune sottomissioni di chip elettronici dovremmo farle tra la fine del 2023 e inizio 2024.

- Il chip fotonico finale dovrà esser sottomesso nel Q4 2024.

- Cercheremo di impegnare quello che è possibile in estate, nel caso chiederemo un’estensione

Relazione con i DRD ECFA

- Abbiamo sottomesso la nostra disponibilità alla partecipazione del DRD7 WP7.1.a sui link fotonici
  - Non c’è ancora un documento in cui specifichiamo le nostre “deliverables”
- Secondo quanto richiesto dalla GE
  - Tutti i chip prodotti in FALAPHEL possono essere considerati come materiale di “consumo”

Personale

Cognome	Nome	Status	Percentuale	Sinergie
Cammarata	Simone	Ass. Ricerca	25%	IGNITE
Ciarpi	Gabriele	RTDA UniPi	25%	
Magazzù	Guido	I Tecnologo	10%	CMS
Messineo	Alberto	Prof. Associato	5%	CMS
Palla	Fabrizio	Dir. Ricerca	5%	IGNITE/CMS
Verdini	Piero Giorgio	I Ricercatore	5%	CMS

Supporto in sezione

- Alte tecnologie (µbond)
- Supporto progettista meccanico e officina per piccole lavorazioni (<~5%)