FALAPHEL SER28
Project Status

Guido Magazzù

June 27th, 2023

FALAPHEL SER28 Devices

- SER28_V1 (submitted in May 2022)
  - Single Data Rate (SDR) + Common Mode Logic (CML)
  - BIST + Parallel LVDS Input Port
  - Target Data Rate = 10Gbps
  - Validated up to 7Gbps - Failures at higher data rates under investigations (test setup issues?)
  - TID Test (INFN-Pisa) => Recoverable effects on BER
  - SEU Test (LNL) => June 29th/30th
- SER28_V2 (submitted in April 2023)
  - Double Data Rate (DDR) + Common Mode Logic (CML)
  - BIST, No Parallel Input Port
  - Target Data Rate = 20Gbps
- SER28_V3 (submission Q4-2023 or Q1-2024)
  - Double Data Rate (DDR) + CMOS
  - BIST, No Parallel Input Port
  - Target Data Rate = 25Gbps

SER_V1 (Test and Characterization)

FPGA MODE (Boards T1 & T2)

Test	Eye Characterization	Serializer Test
Setup 1 (1-2 Gbps)	K Mode => 1,2 Gbps	K,1P,4P Modes => 2Gbps PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => 2,3,4,5 Gbps	K,1P,4P Modes => 5Gbps PRBS Mode => ?
Setup 3 (5-10 Gbps)		

Test	Eye Characterization	Serializer Test
Setup 1 (1-2 Gbps)	K Mode => 1,2 Gbps	K,1P,4P Modes => 2Gbps PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => 2,3,4,5 Gbps	K,1P,4P Modes => 5Gbps PRBS Mode => ?
Setup 3 (5-10 Gbps)	K Mode => 5,6 Gbps	K,1P,4P Modes => ? PRBS Mode => ?

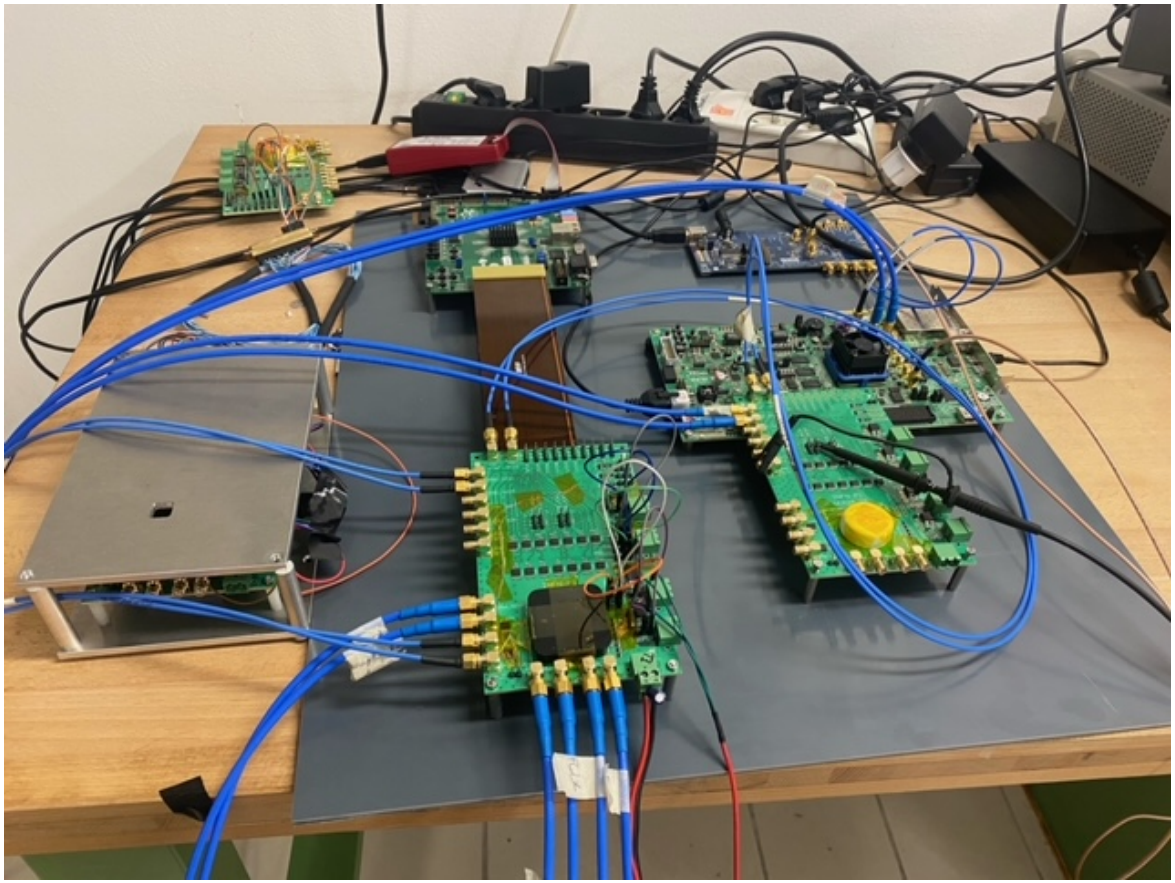
BIST Mode (Boards B1 & B2)

Test	Eye Characterization	Serializer Test
Setup 1 (1-2 Gbps)	K Mode => 1,2 Gbps	BIST Test => OK BIST Mode => OK
Setup 2 (2-5 Gbps)	K Mode => 2,3,4,5 Gbps	BIST Test => OK BIST Mode => OK
Setup 3 (5-10 Gbps)	K Mode => 5,6 Gbps	BIST Test => ? BIST Mode => ?

Test	Eye Characterization	Serializer Test
Setup 1 (1-2 Gbps)	K Mode => ?	BIST Test => ? BIST Mode => ?
Setup 2 (2-5 Gbps)	K Mode => ?	BIST Test => ? BIST Mode => ?
Setup 3 (5-10 Gbps)	K Mode => ?	BIST Test => ? BIST Mode => ?

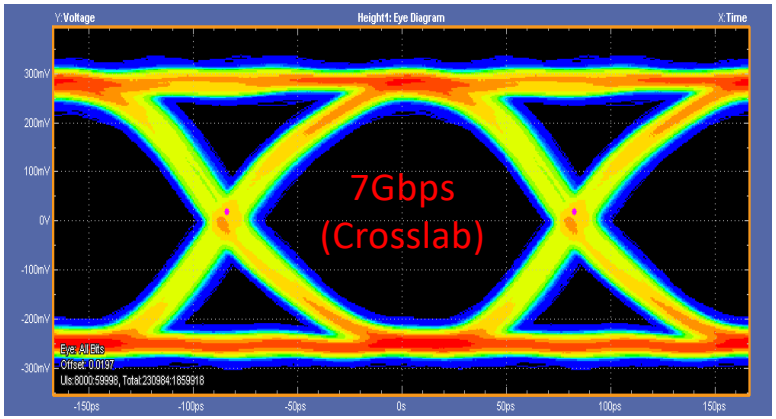
4 Test Boards initially assembled – DUT replaced in T1 and B2 (June 2023)

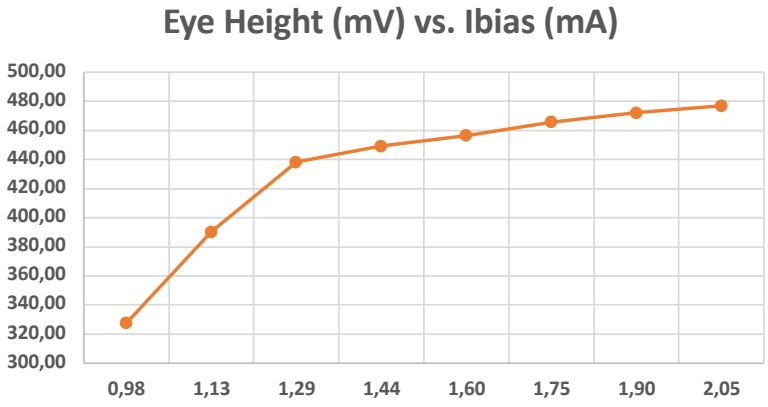
SER_V1 (Test and Characterization)



Test Setup ready for SEU test at LNL

Test Setup ready for SEU test at LNL

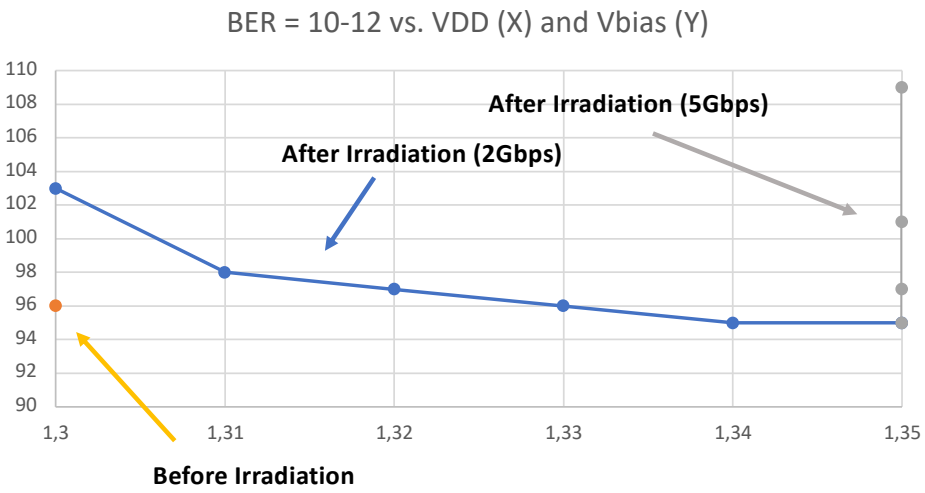


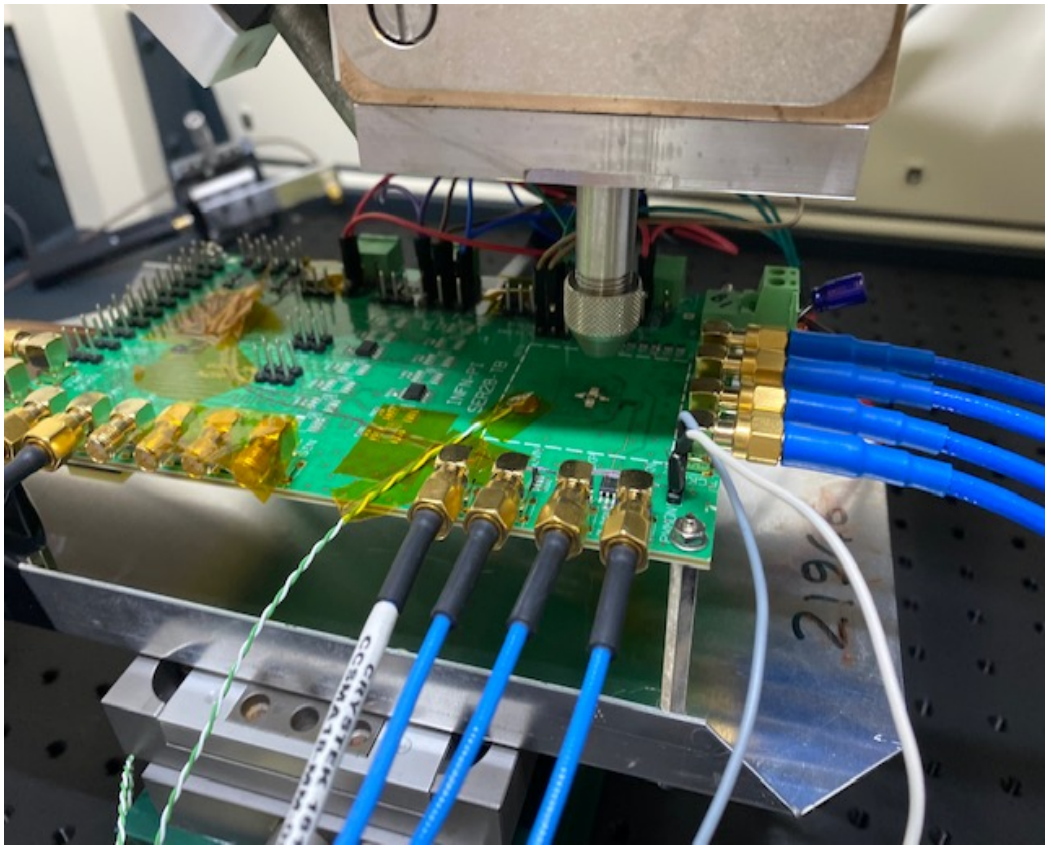


SER_V1 (Test and Characterization)

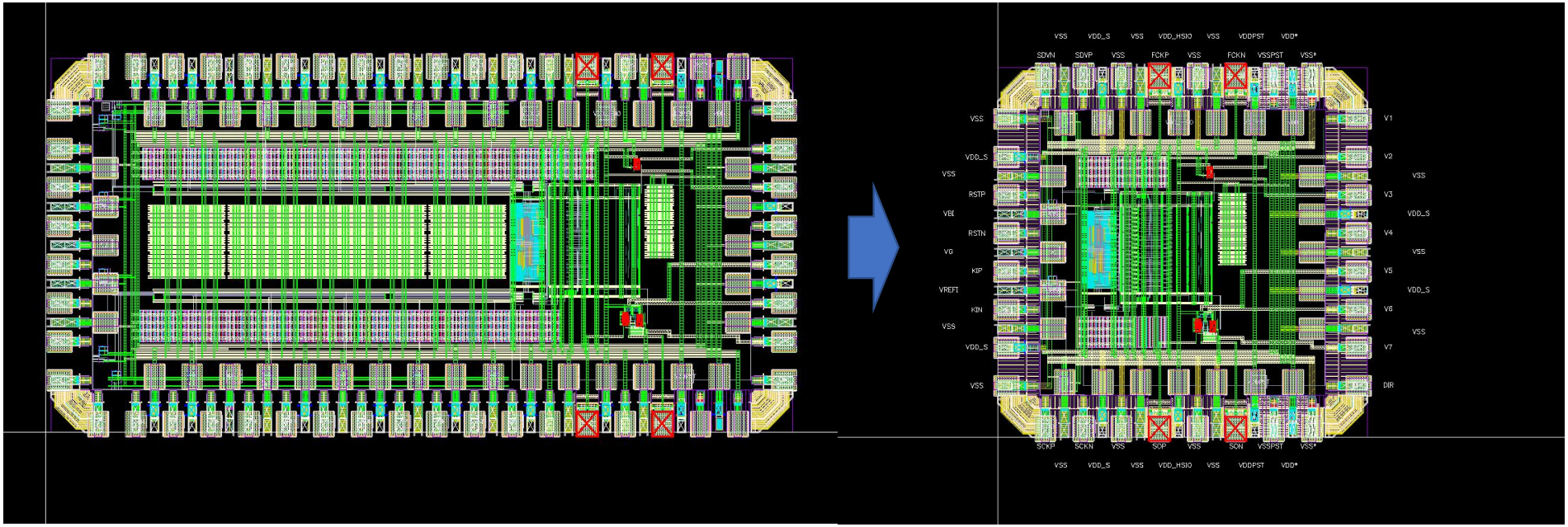
TID Test @ INFN-Pisa

- **Dose Rate = 3.1 Mrad/h**
  - **V = 40KV**
  - **I = 40mA**
- **TID = 1.25Grad (17 days!)**
- **BER measured during and after irradiation**
  - **Data Rate = 2-5Gbps**
  - **Acquisition Time = 500s => BER = 10^{-12} (different Vbias and Vdd values)**
- **Small increase of BER (expected) recovered by bias adjustment**





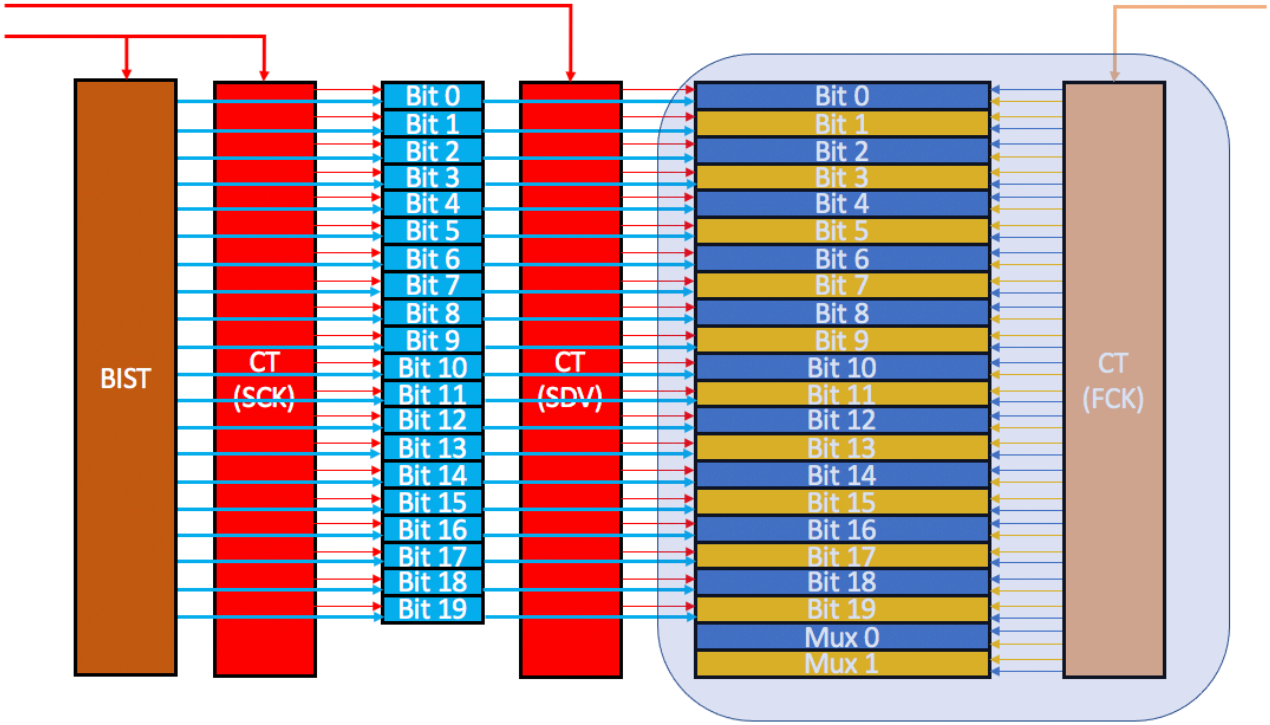
SER_V1 to SER_V2

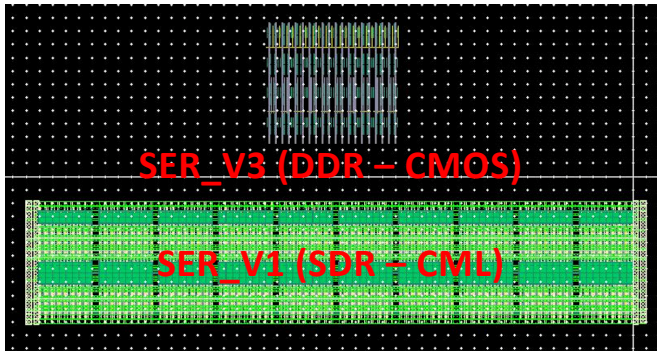


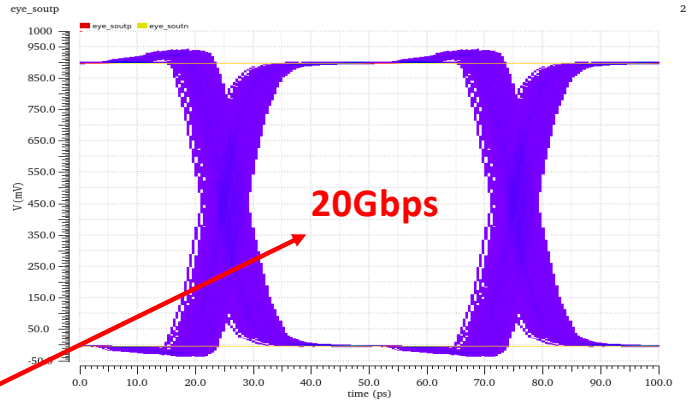
SER_V1 (SDR – CML)

SER_V2 (DDR – CML)

SER28_V3 (CMOS)







Layout and PEX completed / post layout simulations performed