Front-end design in 28 nm CMOS

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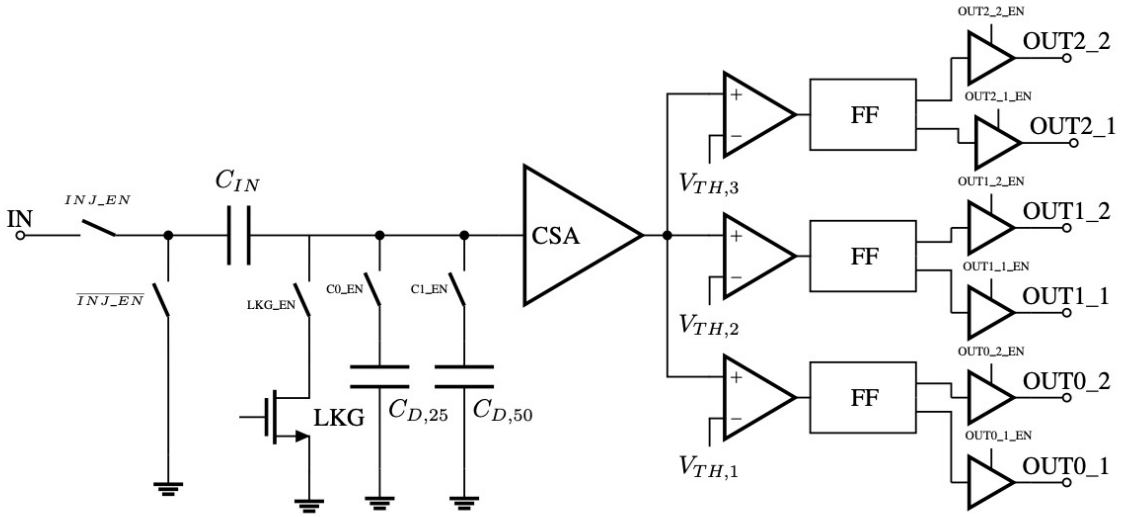
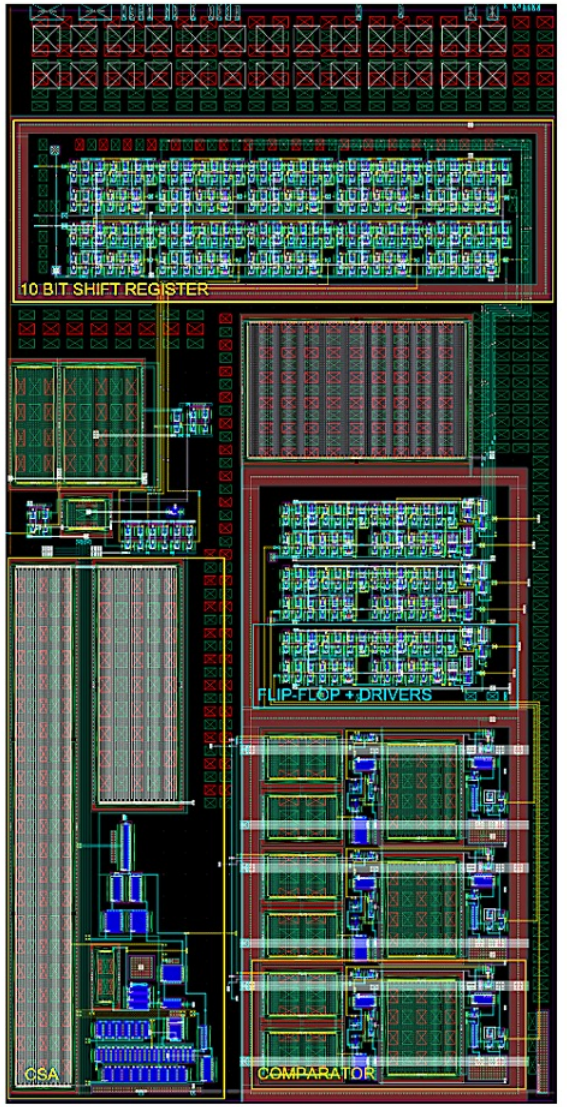
Flash ADC based front-end

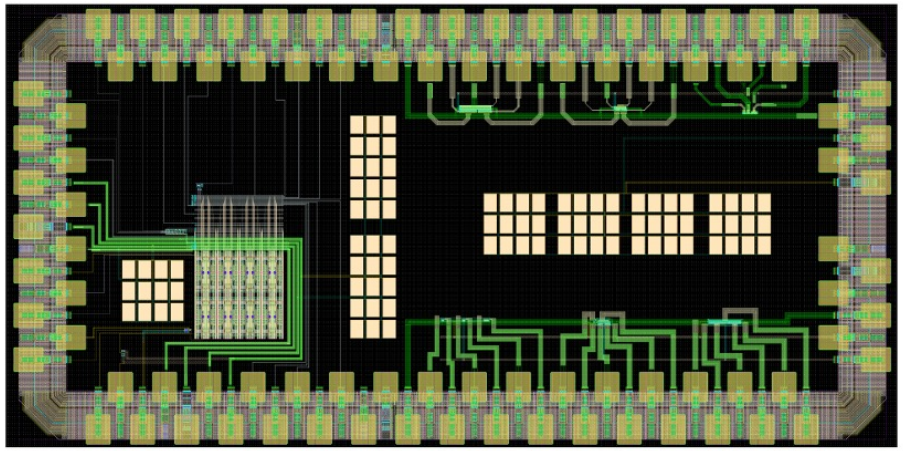


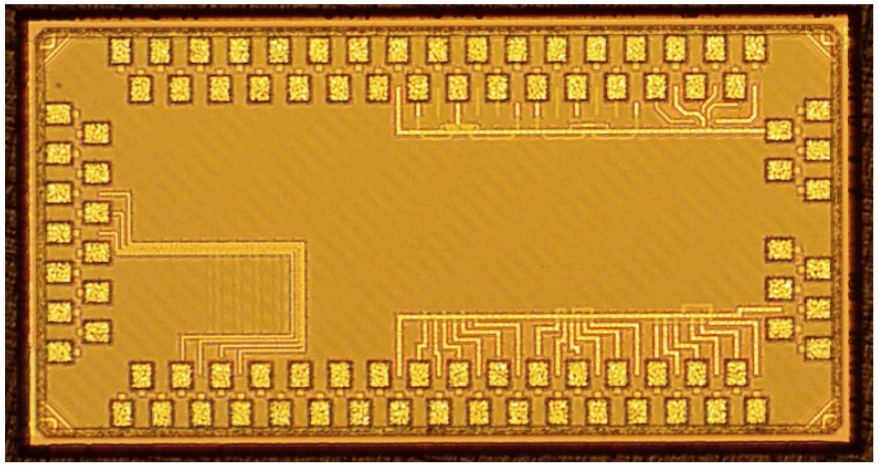
- Preamp (**regulated cascode**) two independent feedbacks
- Ancillary blocks for **detector emulation**



- **AC coupled, auto-zeroed comparators**, operated with 40 MHz clock, implementing a **2-bit flash ADC.** The design is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V
- Elementary cell size: 25 x 50 μm^2 (analog+digital)
- Minimum **in-time threshold**: 600 e-

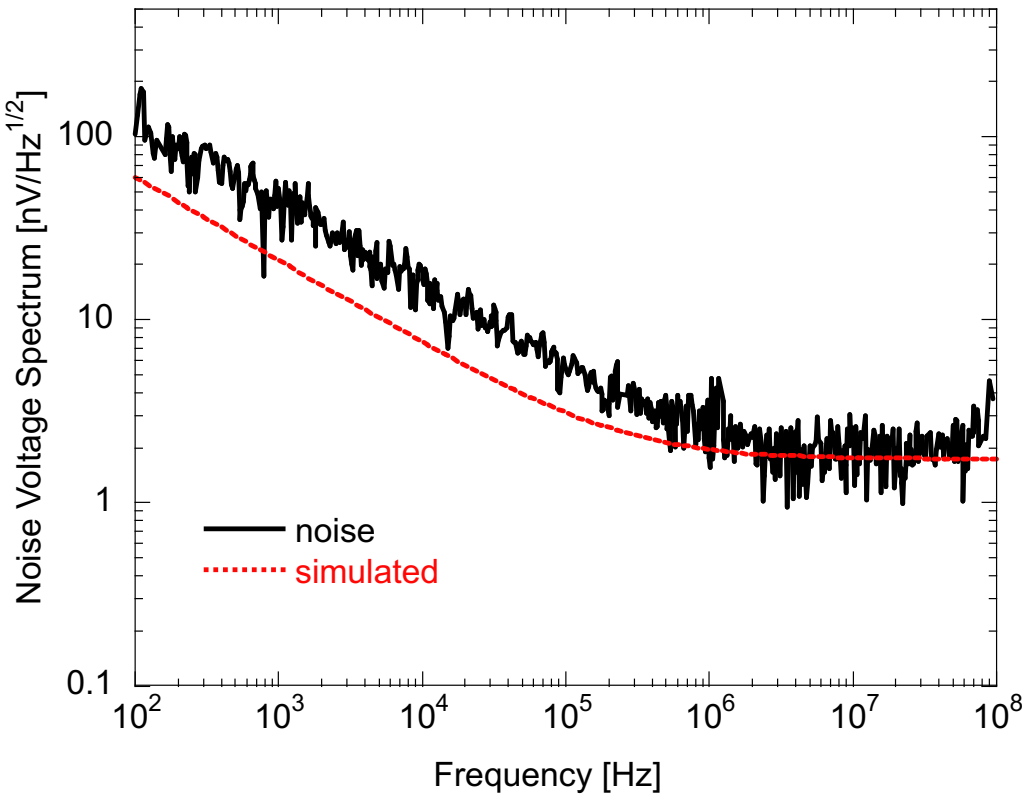
Flash ADC based front-end

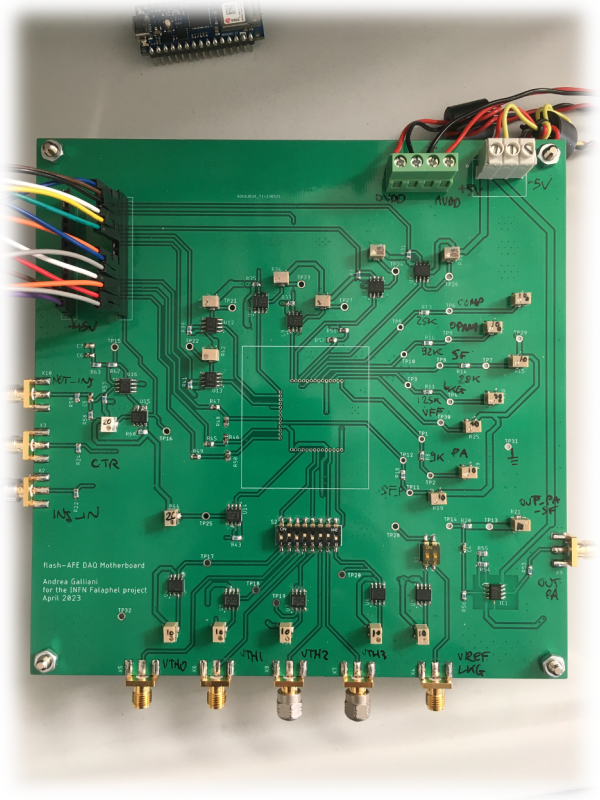


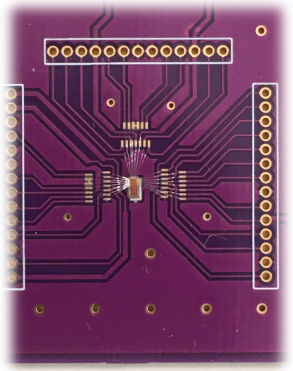


- **Prototype chip including a 4x8 readout matrix** has been submitted in a mini@sic run in October 2022
- Simple digital configuration and readout (shift registers)
- Prototype chip includes **standalone NMOS and PMOS** transistors for static and noise characterization

Prototype testing







- **Static** and **noise** characterization of single devices on going
- Received the first mezzanine with **wire-bonded chip** last Friday. Two more mezzanines now in Milano for wire bonding (thanks to Fabrizio Sabatini & Alberto Stabile)
- Debugging of **the test board** and **DAQ system** on going

ToT-based front-end

- **A front-end architecture (optimized for very low threshold)** is being investigated, based on **Time-over-Threshold (ToT)** → preamp + DC coupled comparator + **5/6-bits** threshold tuning DAC
- To be submitted in a mini@sic run in ~~October 2023~~ **January 2024**
- Development of **DAQ system** and **testing activity in 2024**