HASPIDE WP2

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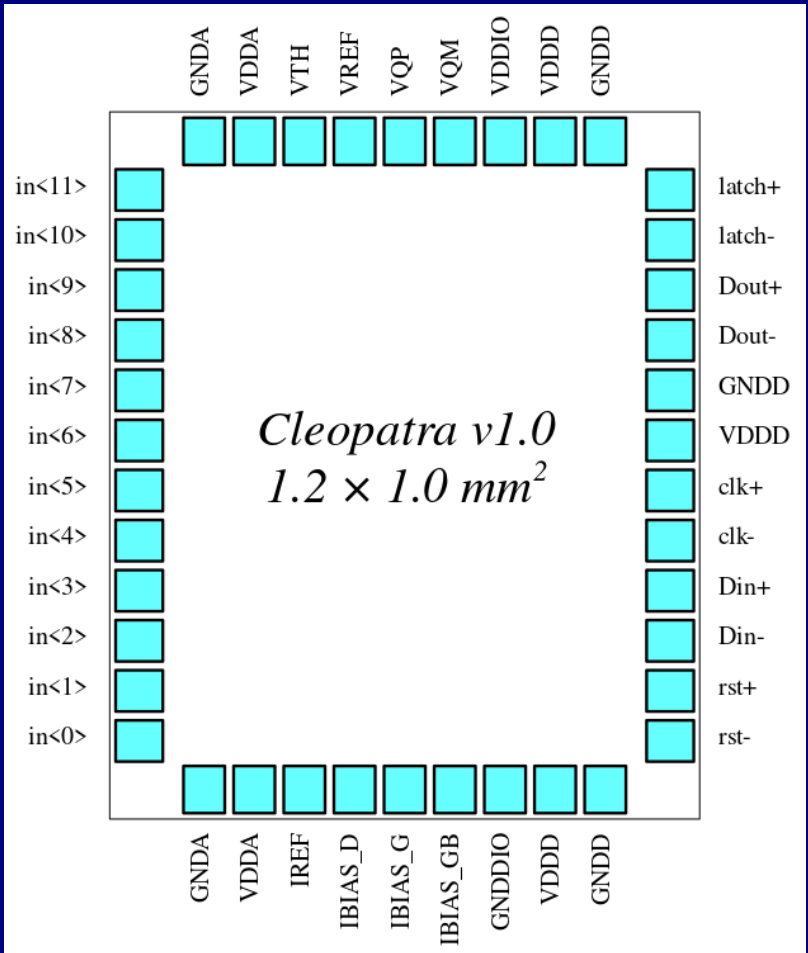
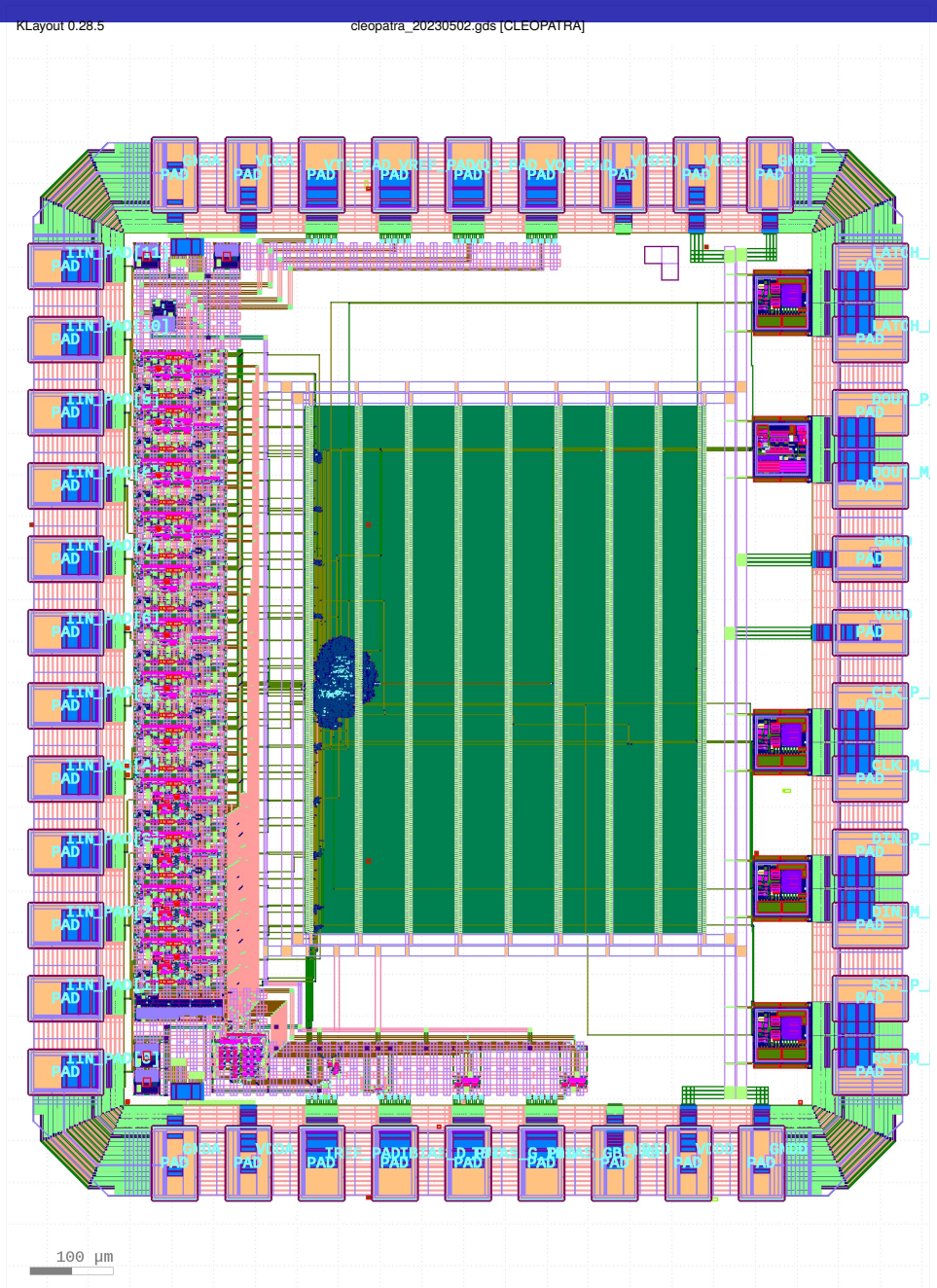
Cleopatra v1.0

Test ASIC pinout



- Technology : CMOS 28 nm
- 12 channels recycling integrator
- Simple serial interface
- Submitted on April 26^{th} 2023
- Expected back on August 2023
- Board design ongoing

cleopatra1 - layout



- Layout submitted to IMEC on May 2, 2023
- PAD ring designed using the rad-hard library provided by CERN

cleopatra1 - waived DRC error

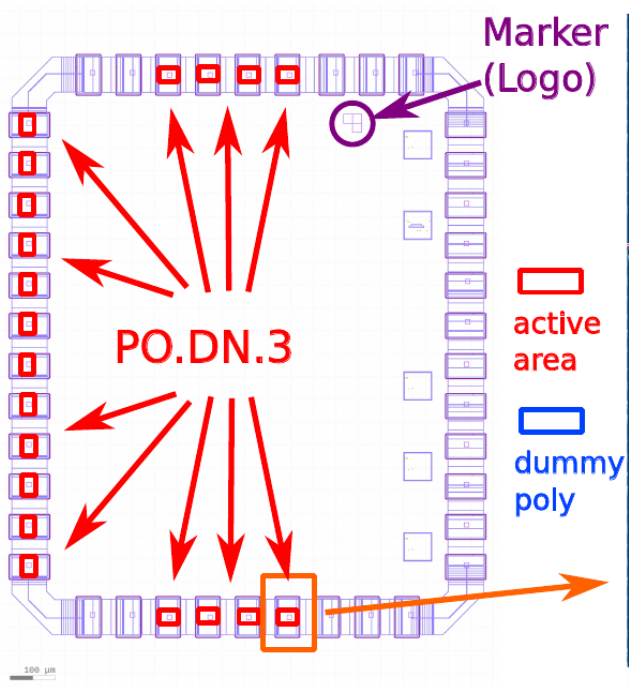
Security C – TSMC Secret

- Device name: **INFN_Cleopatra**
- Violated rule: **PO.DN.3**

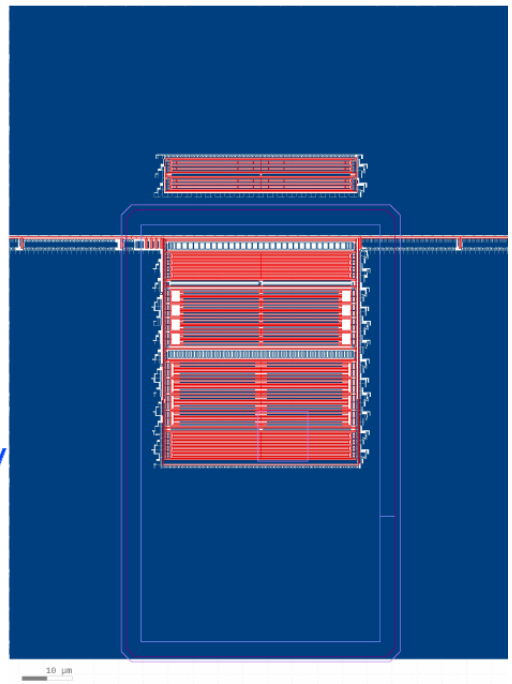
Failed coordinates: left: (67.325, 167.325) to (67.325, 1147.325); bottom: (367.325, 67.325) to (637.325, 67.325); top: (367.325, 1247.325) to (637.325, 1147.325) - 20 violations in total.

- **Customer comment: Radiation-hard pads have large diodes and we cannot draw poly over active area.**

Whole chip

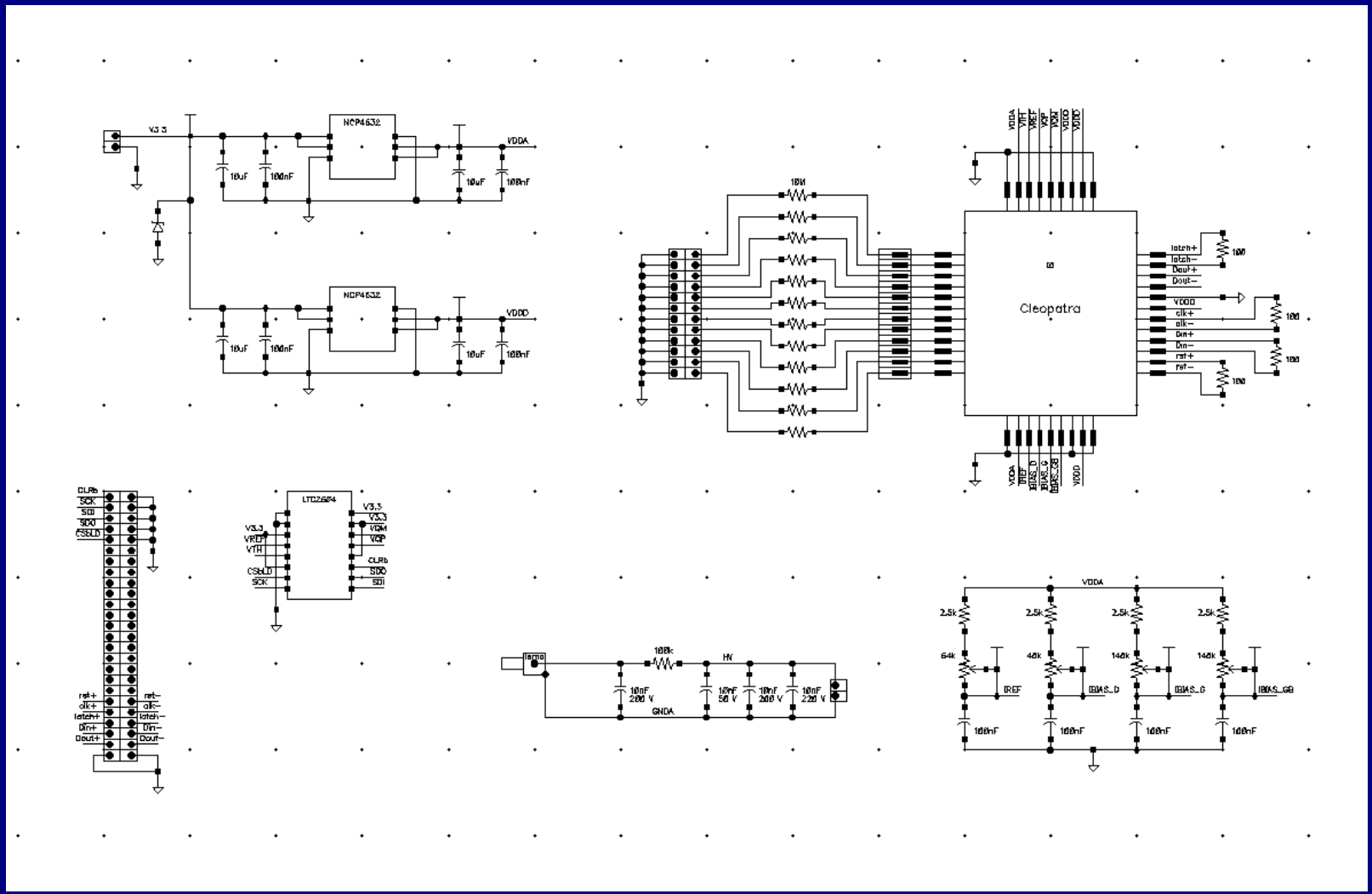


Enlarge image (shows why violate)

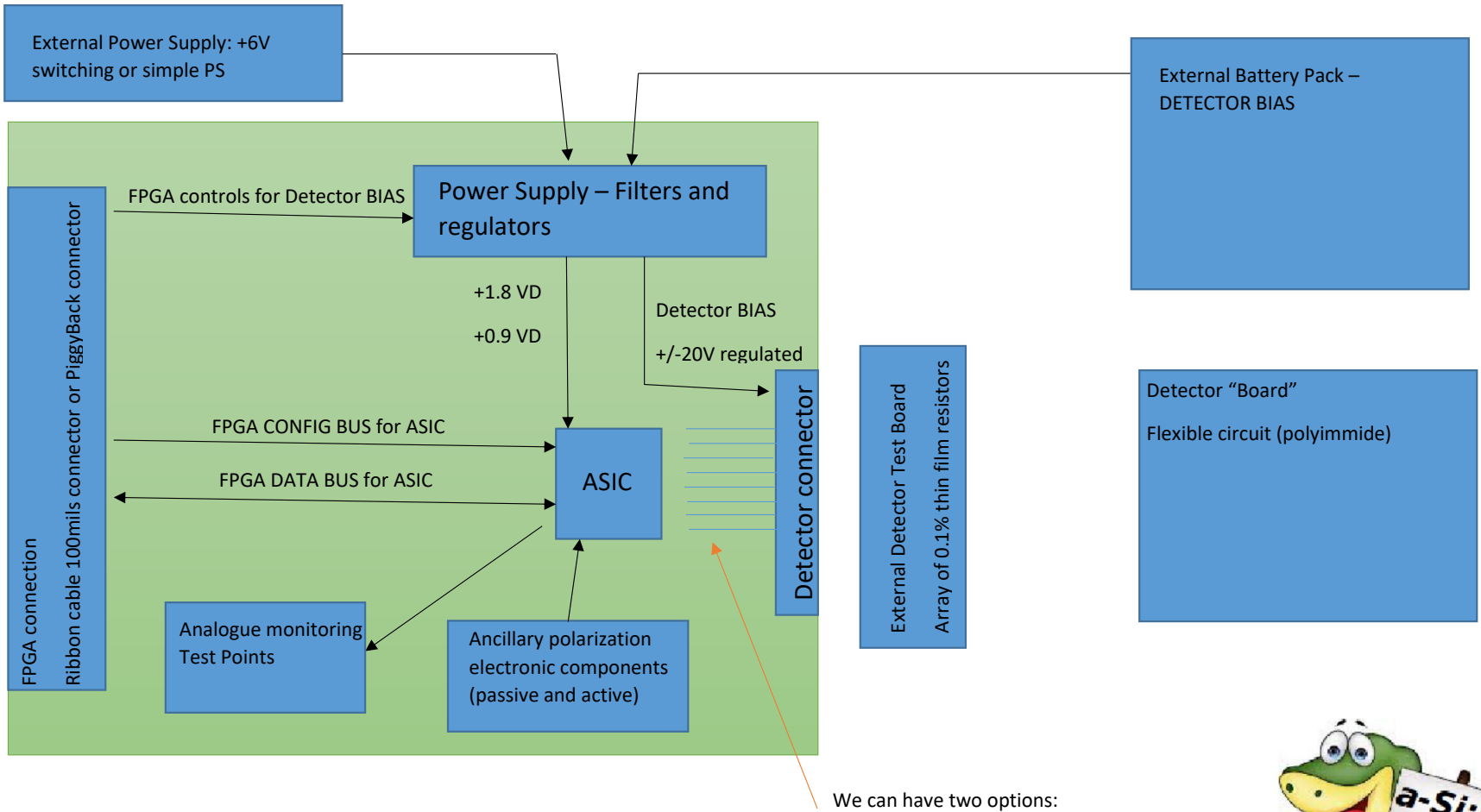


Poly density is (7.7 to 8) % instead of 10 %.

Test board schematic (α *release*)



Test board - requirements from UoW



We can have two options:

1. ASIC can be bonded to the PCB; Fan-out to the detector's connector is achieved by standard PCB routing with a standard PCB-to-Cable connector (ZIF, FPC, standard header etc etc)

2. ASIC is bonded to the detector to minimize input impedance (bonding issues on aSi:H sensor must be solved).

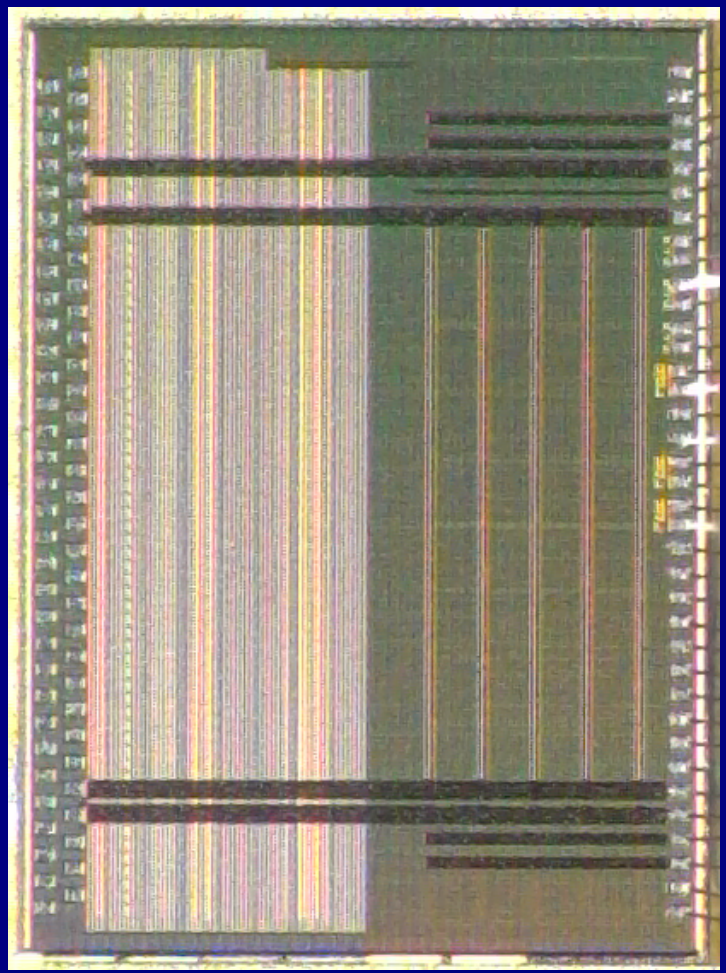
Cleopatra v2.0

- Based on v1.0, 32 or 64 channels
- 32 channels
  - Estimated size : 1.5×2 mm^2
  - Possible package : QFN64 9×9 mm^2 €163/pkg
- 64 channels
  - Estimated size : 2.8×2 mm^2
  - Possible package : CERQUAD FP 128, 11.6×11.6 mm^2, €194/pkg
- Submission in 2Q2024

cleopatra2 - estimated cost

- for MPW: must ask IMEC
- for miniASIC: 8229 € / 1 mm^2 (min area) + 788 € / 0.1 mm^2 (additional area) + VAT
  - 3 mm^2: $\approx$ 30 k€
  - 5.6 mm^2: $\approx$ 55 k€

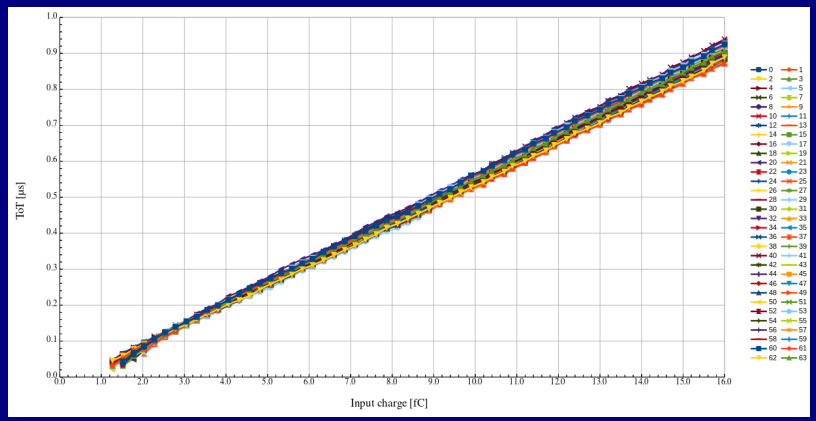
Chip for single particle detection



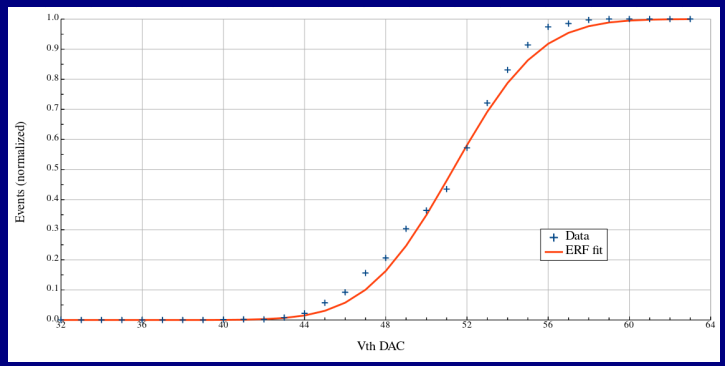
- Designed for the PANDA MVD
- 64 channels ASIC for strip readout
- Detector capacitance 2÷17 pF
- ToA and ToT measurement
- Input charge up to 50 fC
- Reference clock 160 MHz
- Die size 3.24 $\times$ 4.41 mm^2
- Time resolution (rms) 1.8 ns
- CMOS UMC 0.11 μm technology

Test results

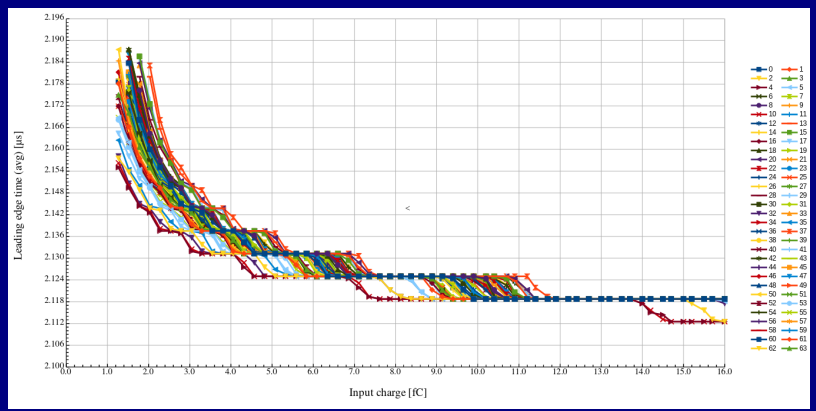
Linearity after calibration (Gain 60ns/fC)



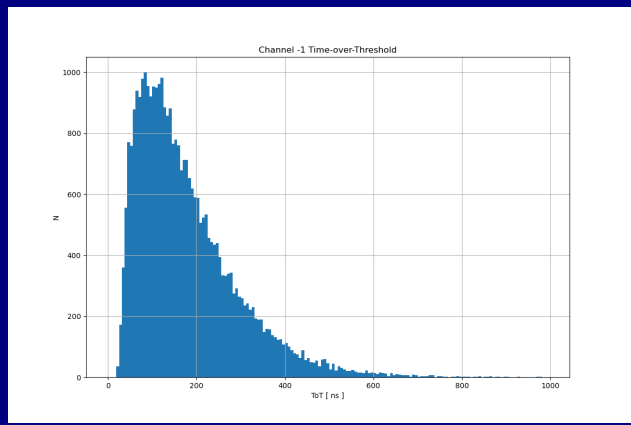
Noise (without sensor) ≈300 e^-



Time resolution (before ToT correction)



ToT distribution connected to a strip sensor and exposed to a Sr^{90} source



Beam test scheduled for August 2023 at Cosy

Costs for 2024 (and 2023?)

- in 2023: 1 Assegno di Ricerca "junior" – Milano
- in 2024:
  - fabrication of the second prototype: depends on area
  - test board for the second prototype: 2 k€
  - travel ?