



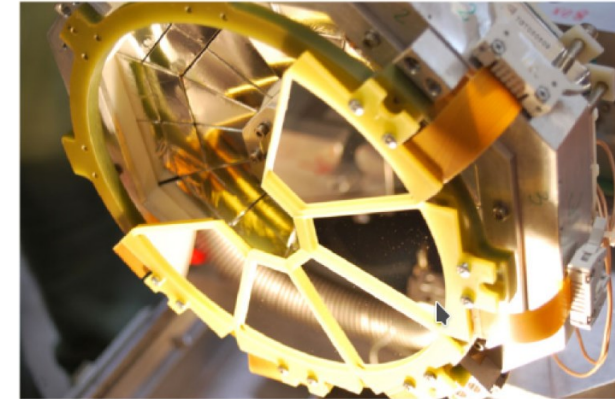
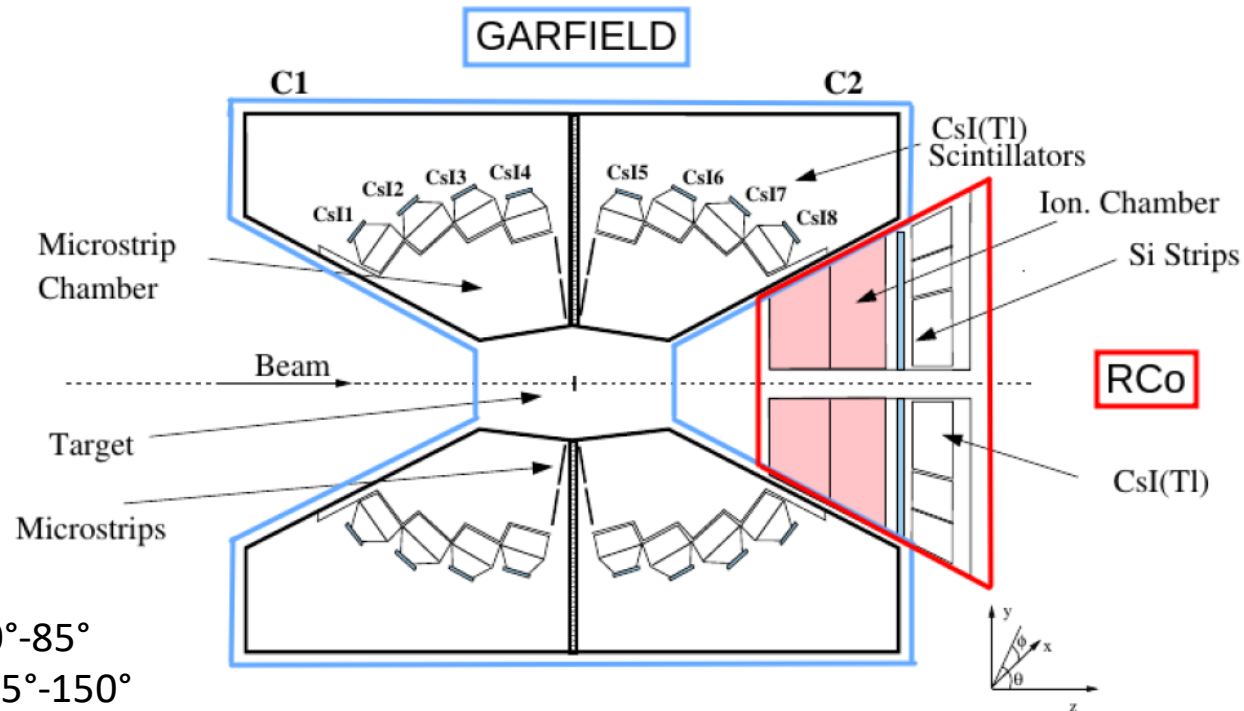
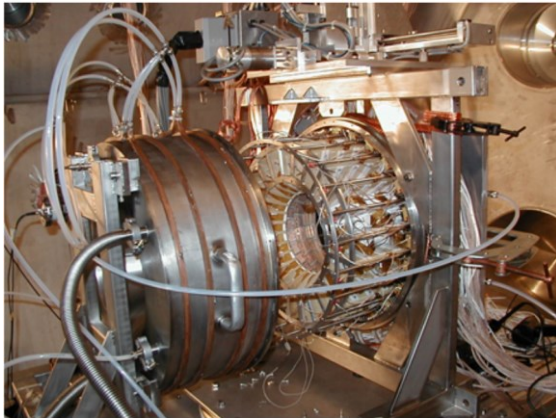
# The GARFIELD upgrade

Lucia Baldesi  
University of Florence

2023 LNL User Community  
Meeting



# The GARFIELD setup



## Ring Counter

- Angular range  $\theta=5^\circ-17^\circ$
- Three active layers
  - Ionization chamber
  - Silicon detectors
  - CsI(Tl) crystals

## GARFIELD

- Two chambers
  - forward chamber  $\theta=30^\circ-85^\circ$
  - backward chamber  $\theta=95^\circ-150^\circ$
- Two active layers
  - Drift chamber
  - CsI(Tl) crystals

# GARFIELD upgrades

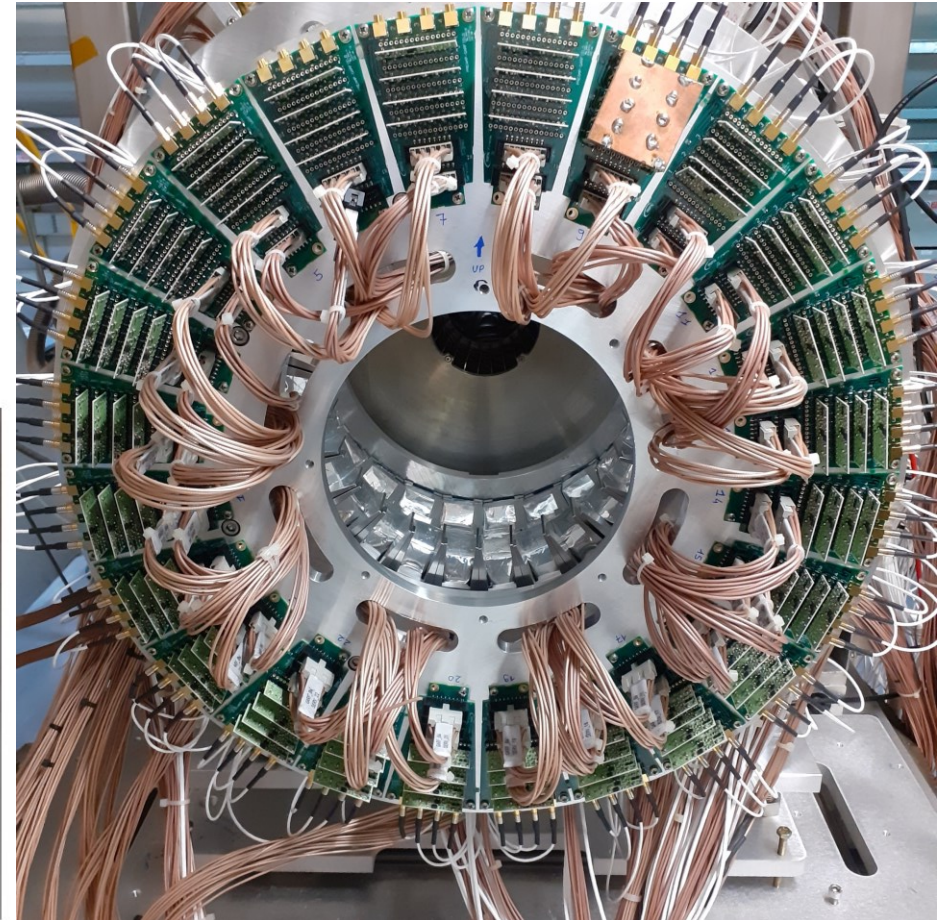
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- Mechanics upgrade
- Electronics upgrade
  - new FEE boards
  - reorganization of the external electronics
- DAQ upgrade

# Mechanics upgrade

## The new backward array

- Motivations:
  - Only ions with  $Z \leq 3$  have been detected beyond  $90^\circ$  in lab with typical kinetic energies very low
  - The CsI(Tl) crystals were old and needed an intervention of maintenance.
- Characteristics of the new backward array
  - Reuse of the old 84 crystals after the intervention of maintenance + 12 new crystals (96 needed to complete the array)
  - Ease of assembling and handling of the structure
    - removed the gas chamber
    - the mechanical unit is now a sector
    - each sector can be removed independently





# Electronics upgrade

## The new FEE boards

- The readout electronics of GARFIELD+RCo is now fully digital and each detector is read by a dedicated front-end channel

- Old FEE boards

- One channel
- 12-bit, 125 MHz ADC
- DSP

- ❖ GARFIELD forward micro
- ❖ GARFIELD backward
- ❖ RCo Ionization Chamber



- New FEE boards

- Two independent channels
- **14-bit**, 125 MHz ADC
- DSP
- **FPGA**

- ❖ GARFIELD forward CsI(Tl)
- ❖ RCo Silicon detectors
- ❖ RCo CsI(Tl)



# Electronics upgrade

## The new FEE boards

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### The FPGA features:

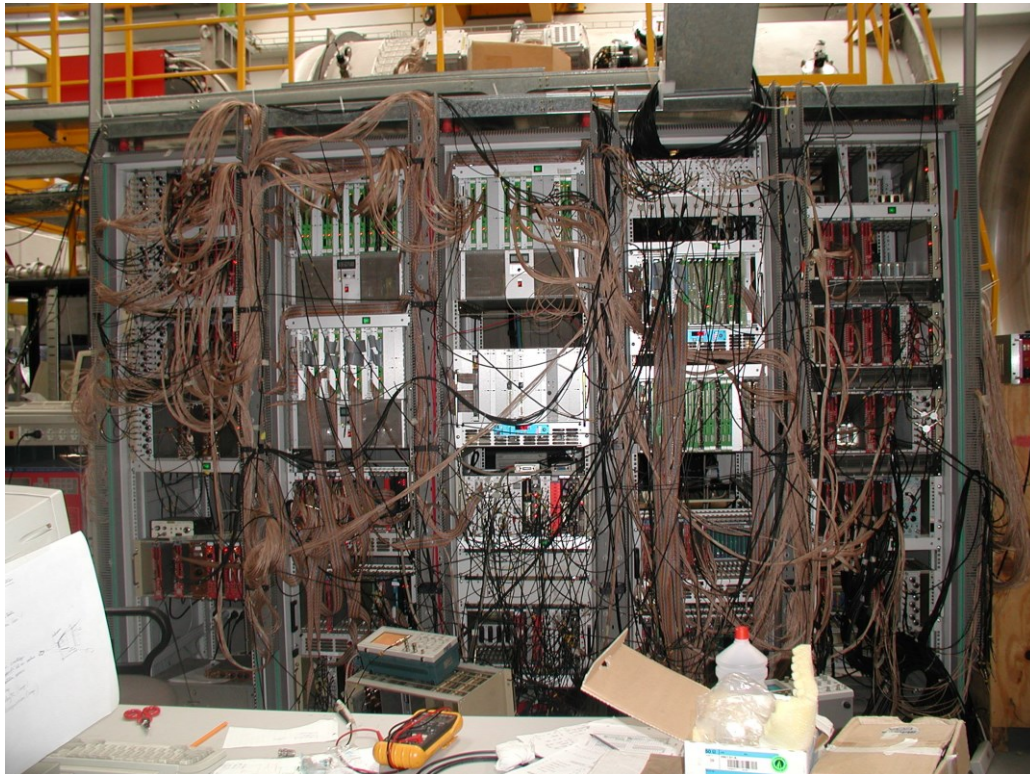
- Speed up the data processing
  - reduction of dead time
- Internal trigger system
  - old: analog comparator with a programmable threshold.
  - new: fast bipolar shaper followed by a zero-crossing detector
- Algorithm for the extraction of the current maximum from the charge signal (Rco silicon detectors)
  - real-time interpolation of the sampled charge signal
  - differentiation and sampling of the interpolated charge signal
  - reduction of throughput data
  - PSA with the current maximum

# Electronics upgrade

reorganization of the external electronics

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- Before



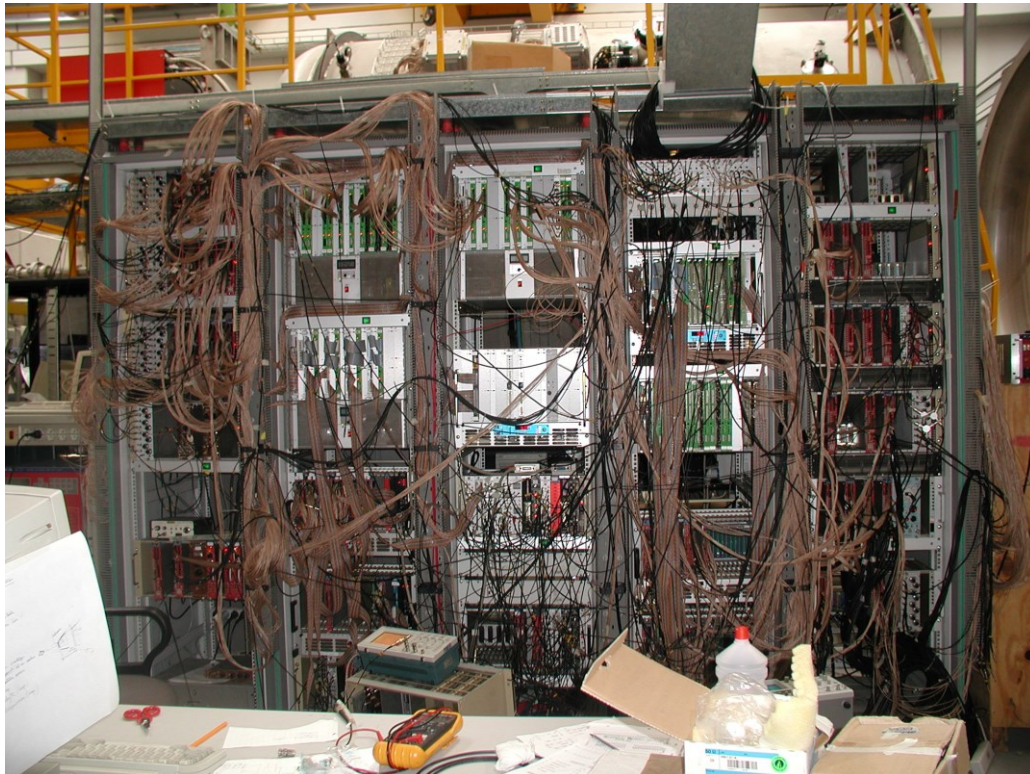


# Electronics upgrade

reorganization of the external electronics

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- Before



- After



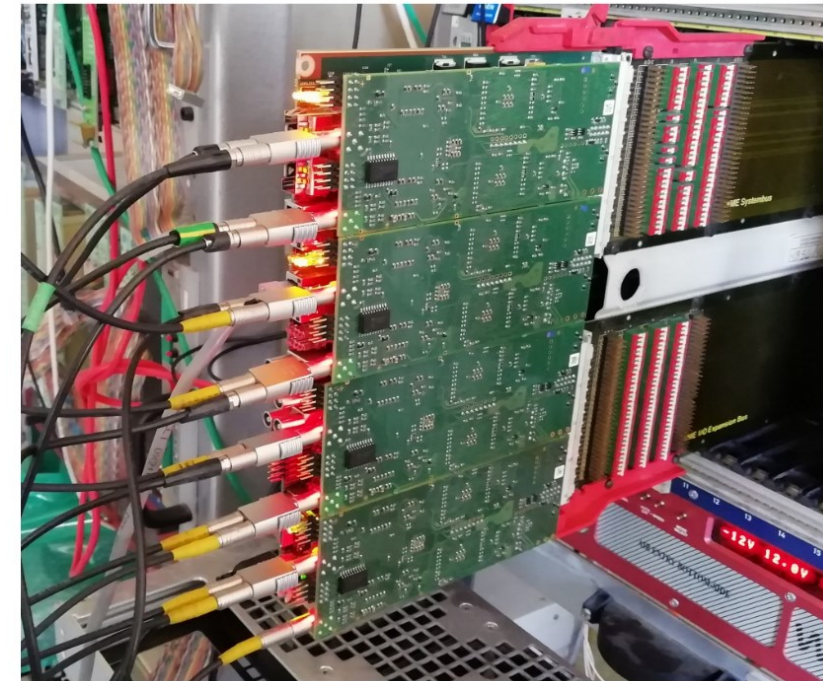


# DAQ upgrade

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The acquisition system is being upgraded

- Motivations
  - obsolete components of the custom data readout bus (FAIR) of present mother-boards
- The new DAQ
  - hardware development in collaboration with the electronics service of Padova starting from the acquisition board (GCU) of the Juno experiment
  - GCU modified to be compatible with GARFIELD
  - FPGA firmware developed in Florence by Ottanelli e Scarigella
  - the software is being developed
  - FAIR bus replaced with Ethernet
- Up to now
  - 12 prototypes (delays due to supply problems)
  - 2 prototypes successfully tested during the Helica experiment at AN2000



# Conclusions

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- Mechanics upgrade → **completed**
- Electronics upgrade
  - new FEE boards → **completed**
  - reorganization of the external electronics → **almost completed**
- DAQ upgrade → **planned for 2025**

Next experiment  
in 2024

Thanks to the User Service LNL (P. Cocconi, D. Rosso, A. Cogo, A. Gambalonga, V. Volpe), Padova technicians (M. Caldogno), Electronics Service of Padova (R. Isocrate, D. Corti)



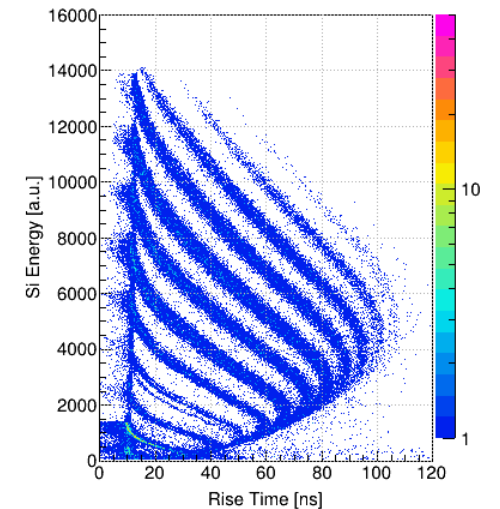
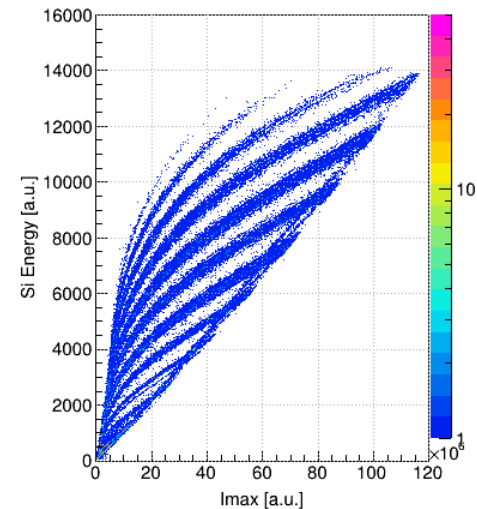
Thanks for your attention

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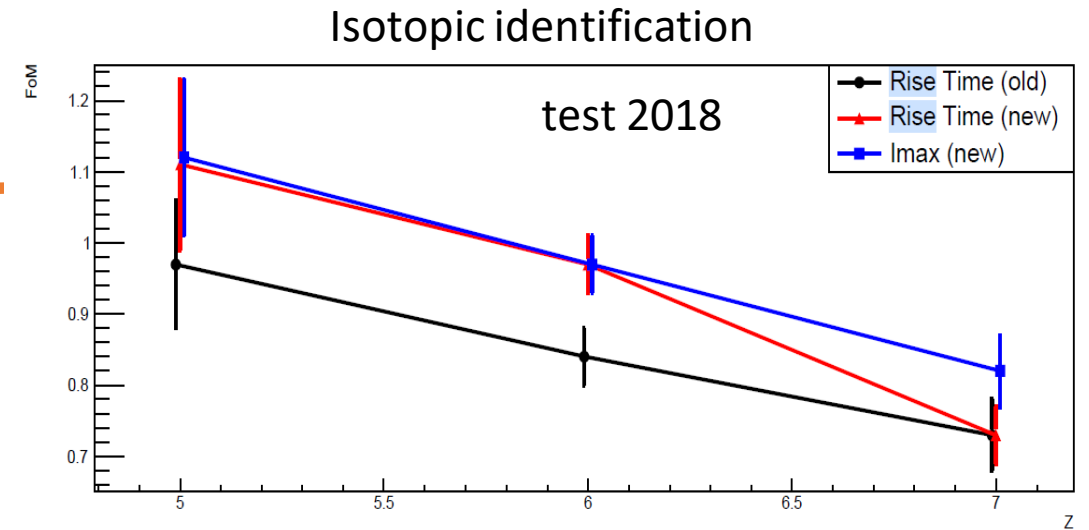
# Pulse Shape Analysis

- The PSA methods allow to identify the fragments fully stopped in a single detector by plotting the correlation of the energy with a shape dependent parameter
  - Charge rise time
  - Current maximum
- The FAZIA collaboration has tested two PSA methods showing that the  $I_{\max}$  PSA has better performances in terms of isotopic identification
- Up to now the RCo apparatus could exploit only  $Q_{\text{rise}}$  PSA
- With the new FEE boards
  - Better performances thanks to the higher precision of the ADC (14 bit)
  - $I_{\max}$  PSA can be exploited thanks to algorithm for current maximum extraction implemented in the FPGA



# PSA: comparison of different methods

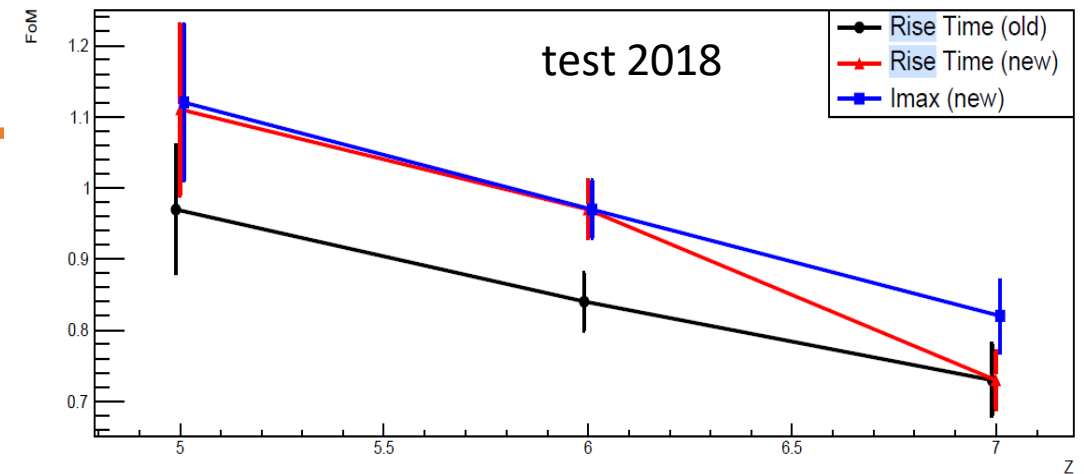
$$FoM = \frac{|C_1 - C_2|}{2.35 (\sigma_1 - \sigma_2)}$$



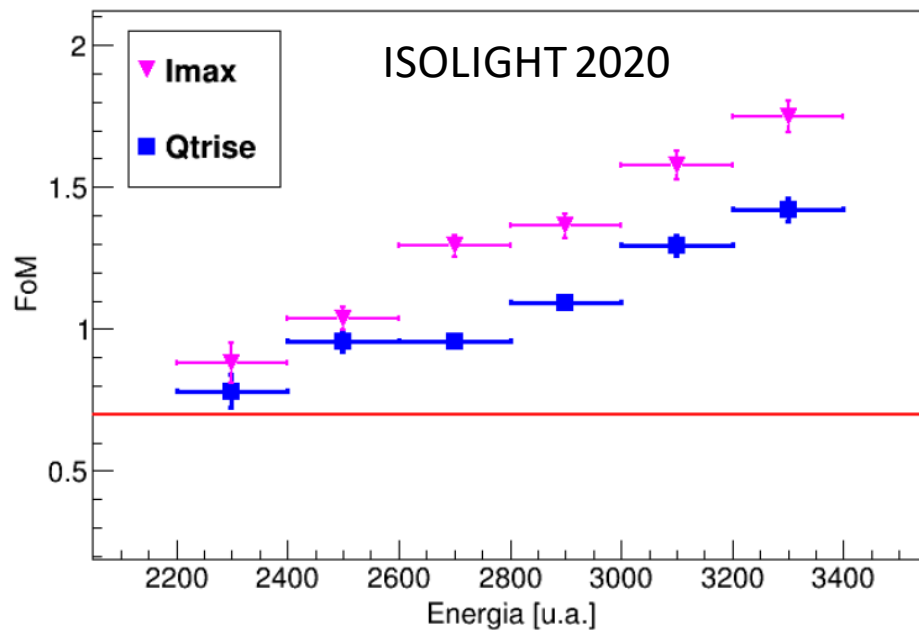
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Isotopic identification



Elemental identification

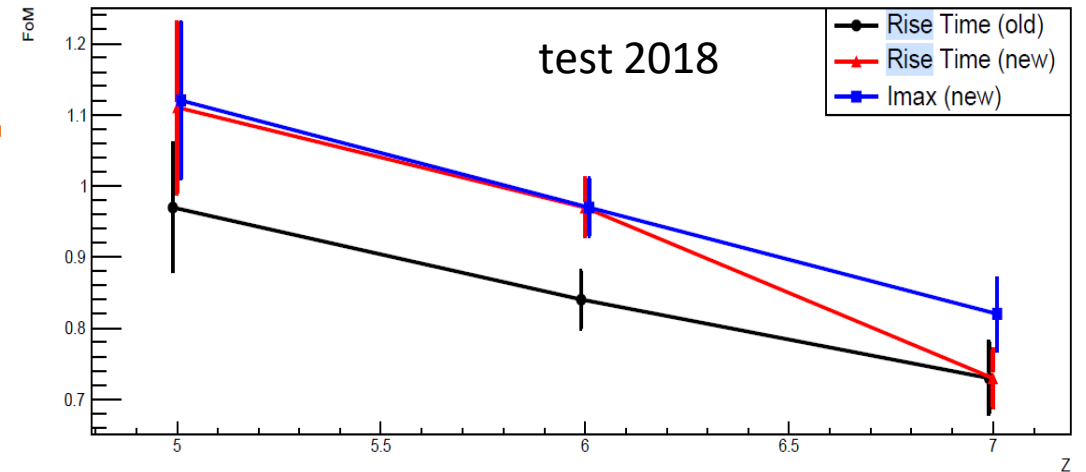




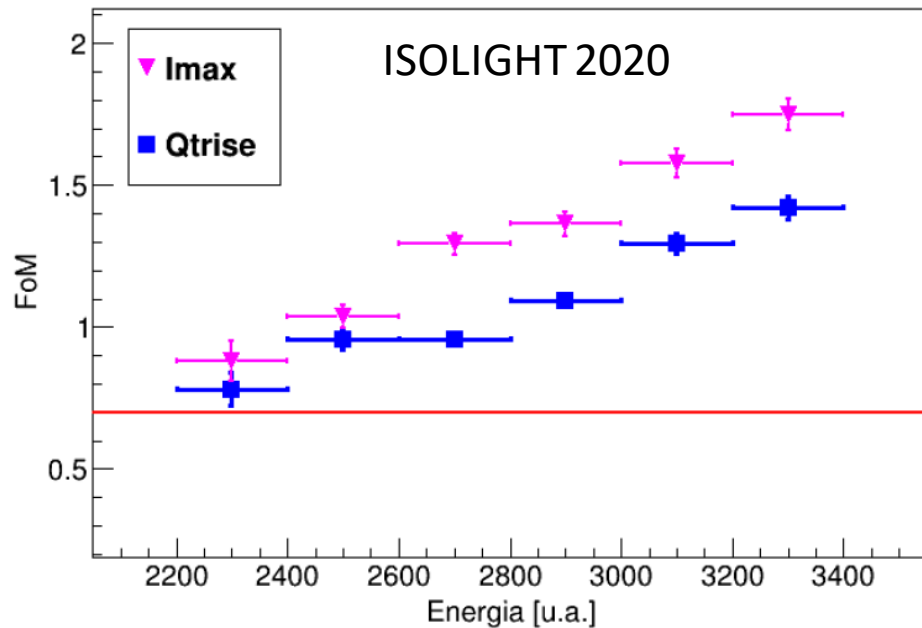
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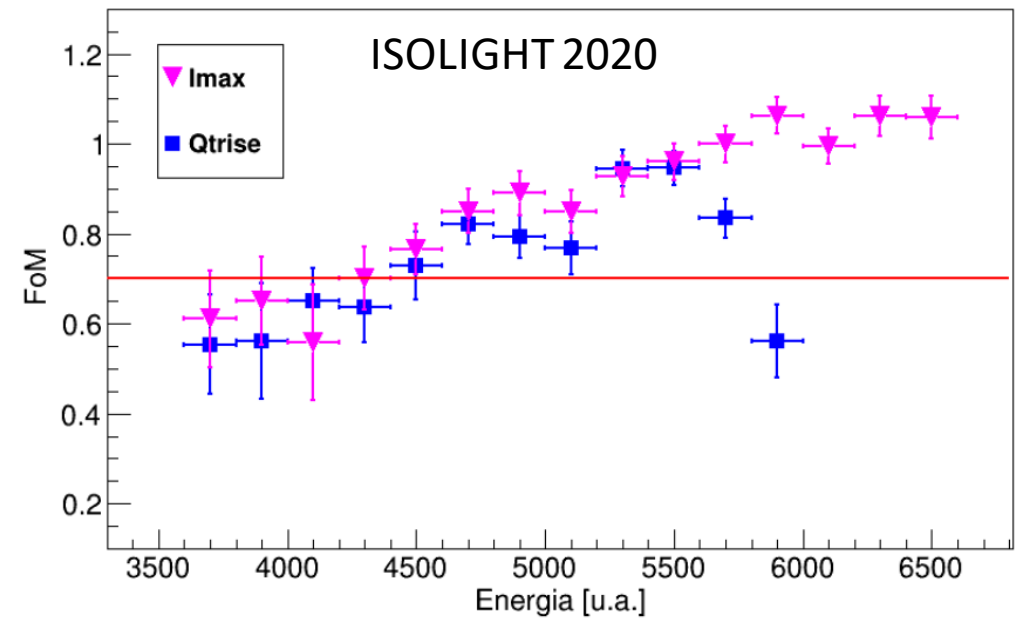
Isotopic identification



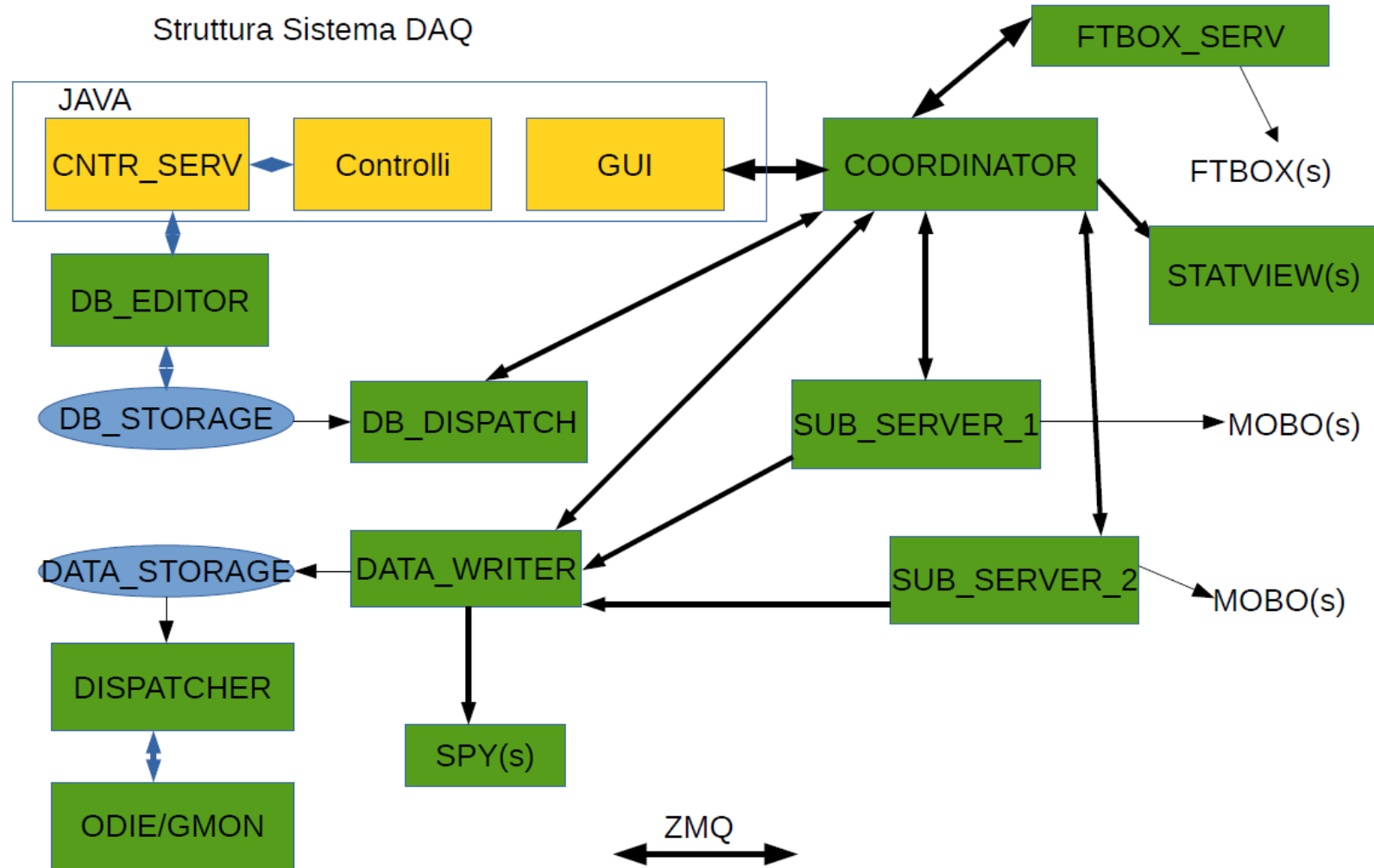
Elemental identification



Isotopic identification



# ACQ Garfield - SOFTWARE



Etc...