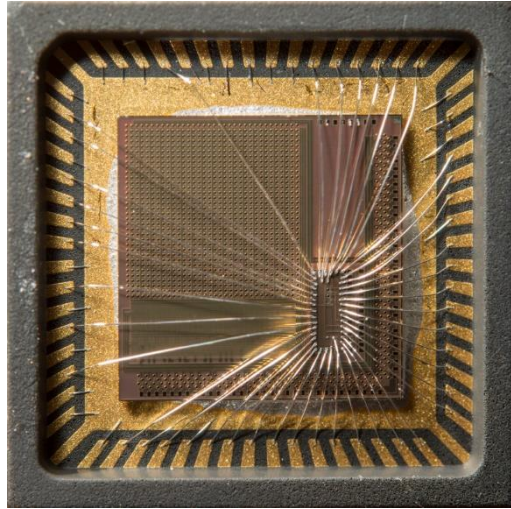# Microelectronics at Fermilab

Davide Braga on behalf of Microelectronics Division

26 July 2023
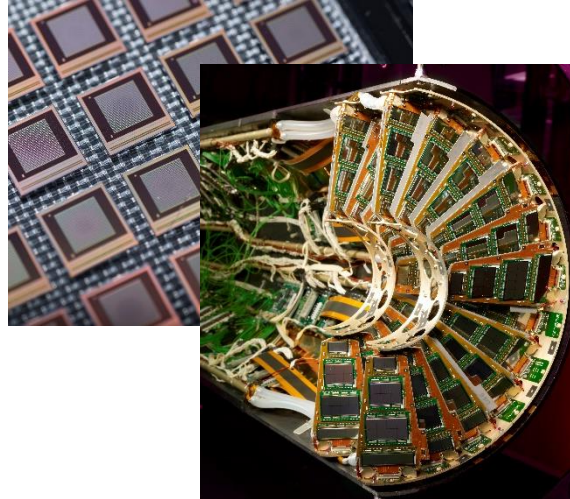
Fermilab Integrated Circuits Design Capabilities and Mission

ACADEMIC RESEARCH

- **Support interdisciplinary research**
- **Enables new scientific discovery and foundational engineering**
- **Novel solutions**
- **Mission: new knowledge and education of students**

NATIONAL LABS: ADVANCED SCIENTIFIC INSTRUMENTATION

- **Support scientific experiments operating in extreme environments**
- **Mid-size scaling for large experiments**
- **Mission: robust performance over several decades**

INDUSTRY – PRODUCT DRIVEN

- **Support consumer electronics**
- **Mature designs**
- **Mission: incremental product driven design**

Technology readiness level

🛠 **Fermilab**

Growth of Integrated Circuit design over ~ 4 decades at Fermilab

- Highly specialized expertise in developing robust custom microelectronics with long-term reliability over decades

- Investigate novel solutions and ensure technology development to enable mid-volume prototyping

- Increased complexity: **2016**: 0.5B transistors in **~cm^2** -> **2021**: 2B transistors in **~mm^2** (shifting the burden from design to verification)

Since 1980's

Ionizing radiation
>1 Grad (1000x higher than outer space)
Extreme flux for single event effects
- Collider Experiments (FCC, HL LHC)

Since 2010's

Cryogenic electronics (77K – 100K)
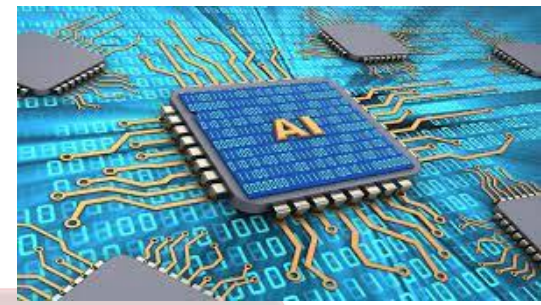- Neutrino experiments (DUNE), Dark matter experiments (Skipper CCDs)

Since 2019

Deep Cryogenic electronics (~ 4K)
- Dark matter experiments (Cryogenic detectors e.g. SNSPDs, TES etc.), Quantum Information Science

New 2022

Superconducting electronics (~100 mK)
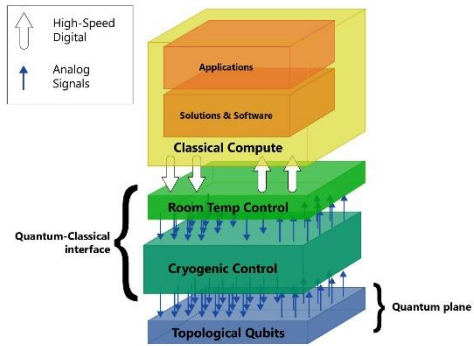- Quantum Information Science for HEP (TWPAs, JPAs for ADMX)

🎔 Fermilab

ASIC Design at Fermilab

ETD: Emerging Technology Directorate (HEP/ ASCR/DOD/NASA)

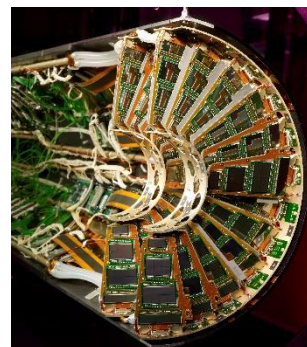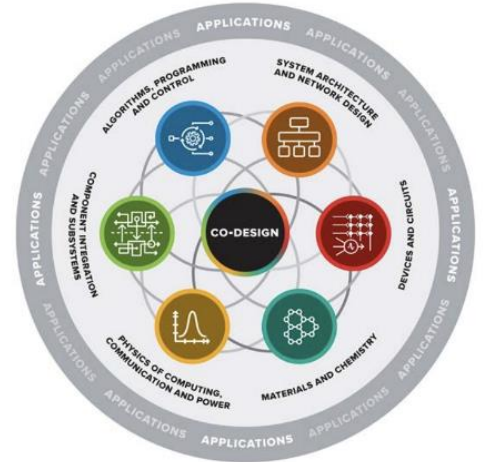CSAID: Computational Science and AI Directorate (HEP/ASCR)

Quantum ⟷ Artificial Intelligence

OPTT Technology Transfer

CMS/DUNE ⟷ Microelectronics Codesign

PPD: Particle Physics Directorate

PPD, ETD, CSAID, AD, etc. (HEP/BES/ASCR/NP/FES)

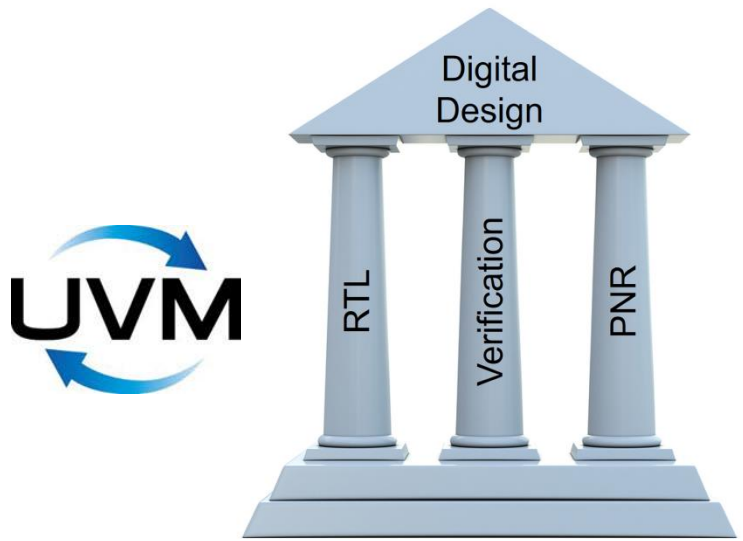High-Speed Digital
Analog Signals

🧲 Fermilab

Core competencies

Analog and Mixed Signal Design

Low noise, low-power front end circuits

High frequency (e.g. PLL, VCOs)

Sensor interface and codesign
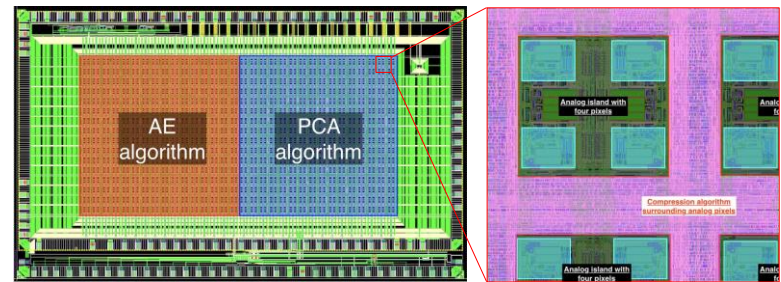
Digital Design and Verification

Design, placement and verification

RTL, Synthesis, P&R

Functional and formal verification

Testing, modeling and characterization

Robotic testing for mid-volume chip characterization (100K chips)

Cryogenic test stands (77K and 4K)

Development of extreme environment **technology models** for cryogenic and rad-hard chips

Automated 12" wafer prober

Radiation testing at Fermilab Irradiation Test Area
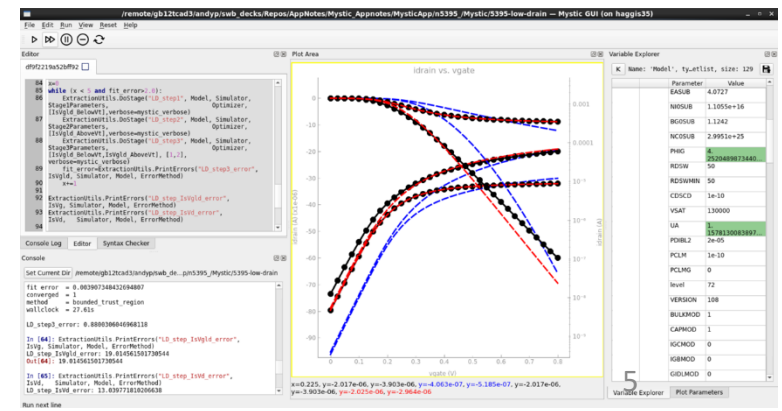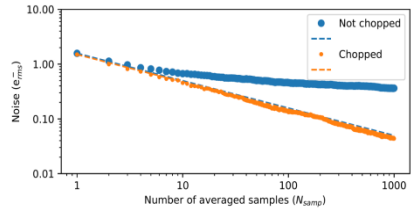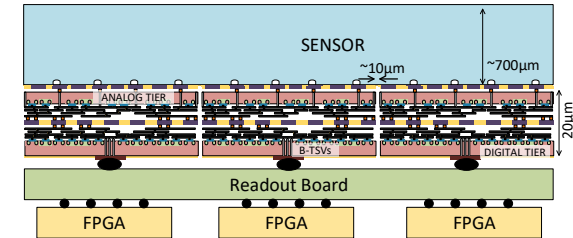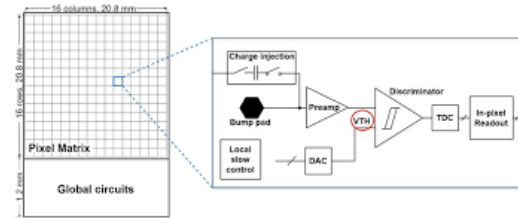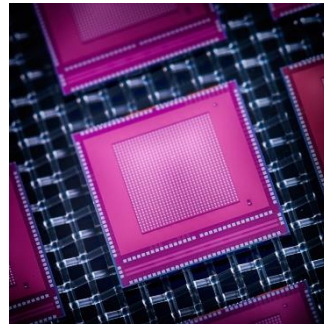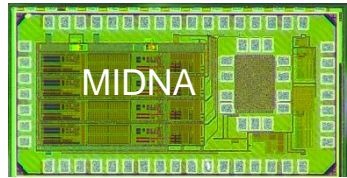
IMPACTFUL HARDWARE DEVELOPMENT

| Ultra-Low Noise Sensing (Dark matter detectors)	Ultra-High Frame rates (Xray detectors)	Picosecond timing (HL LHC detectors)	Operation in extreme radiation/ cryogenic (HL LHC/ DUNE)	Edgeless 3D ICs (HEP / BES light sources)

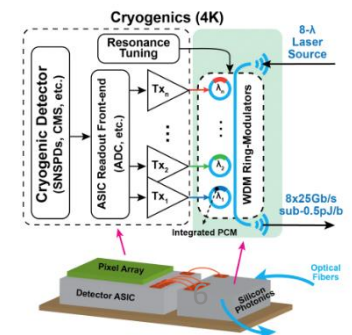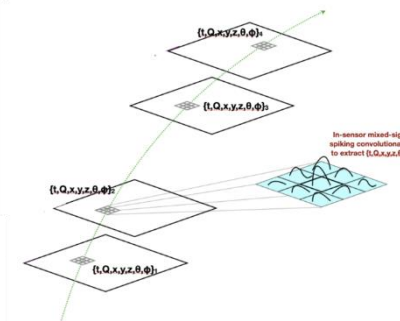| High speed cryogenic data converters (with Microsoft)	Quantum Support Chips	AI-on-chip (ultra-fast data processing)	AI-in-pixel (minimizing data movement)	High-speed Photonic links (low power communications)
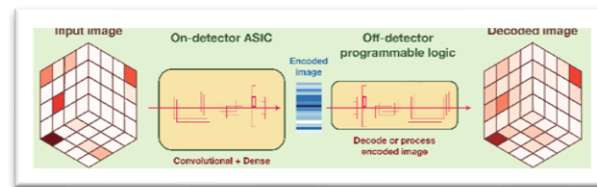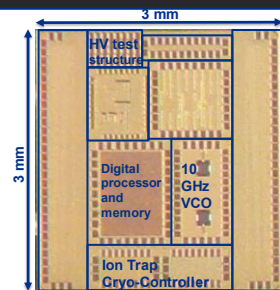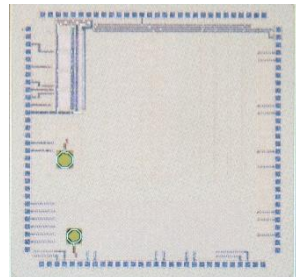
Fermilab: Integrated Circuits

Fast Timing

ETROC

- LGAD readout ASIC for CMS Endcap Timing Layer
- 16x16 pixel, full reticle chip in 65nm
- ETROC2: full size, full functionality prototype currently being tested
- Per-pixel TDC with self calibration scheme to compensate for process variation, temperature, and power supply voltage
- Sensor+ASIC time resolution of 40ps
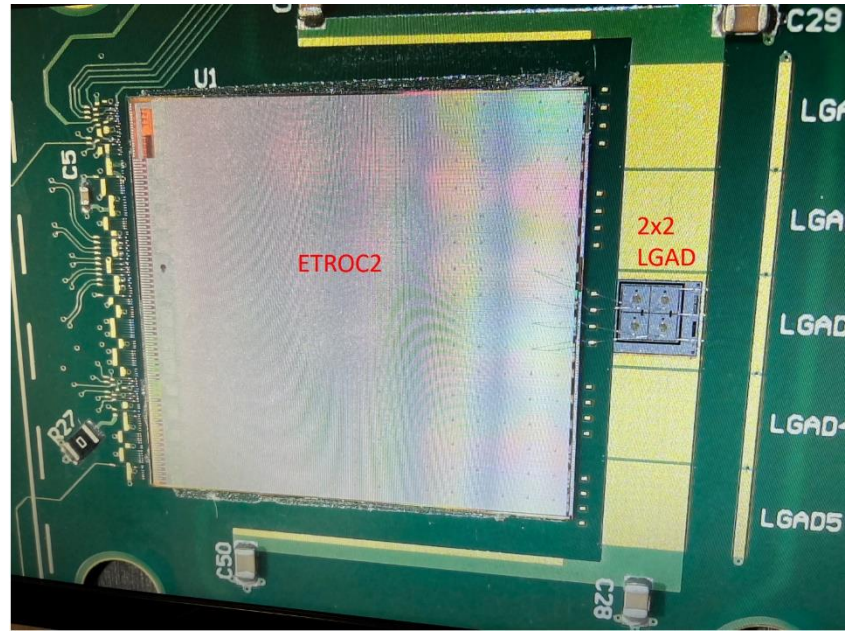
Constant Fraction Discriminator

- 65nm CMOS
- does not require offline corrections or calibrations
- Achieves 15ps for 20fC signal
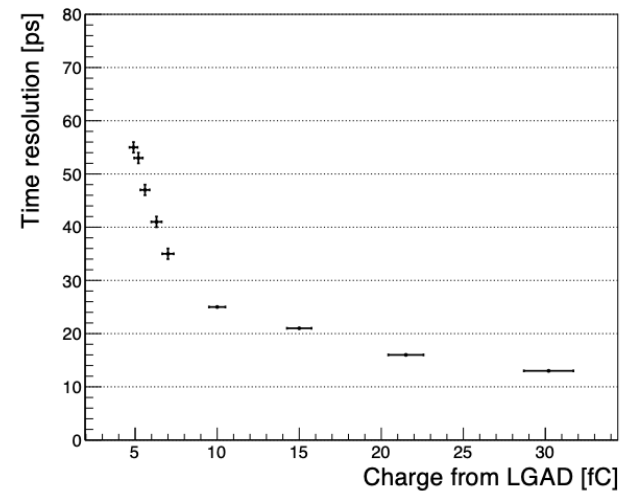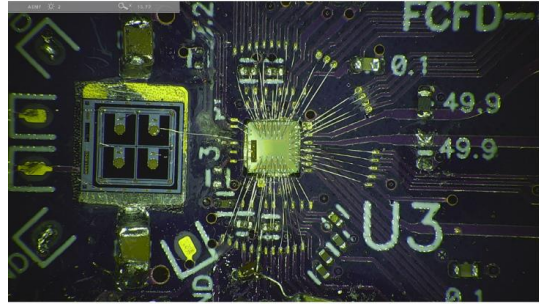
ASIC TDC

- Time-to-digital converter test structure for SNSPD readout
- Cryogenic operation (4K)
- 22nm CMOS
- Demonstrates better than 8ps timing resolution at 4K (300uW)

TDC block: 250x20µm

Quantum support chips

cryoCMOS for Quantum

cryoCMOS model and tool-kit development (4K)
cryoCMOS workshops (e.g. IceQubes, IEEE Quantum week)

EPFL **SYNOPSYS®** **GlobalFoundries™**
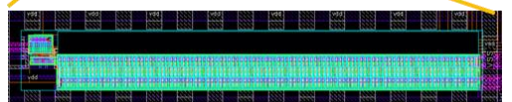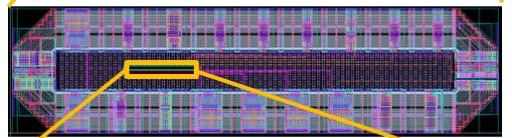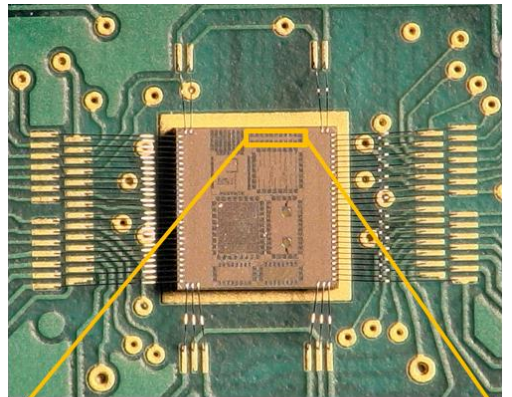
QUANTUM SENSING

Portable optical atomic clocks

(Joint DOE-DOD development)

MIT LINCOLN LABORATORY
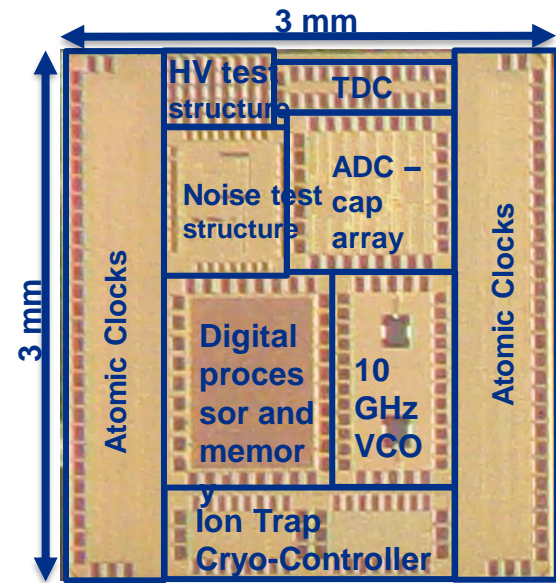
QUANTUM COMMUNICATION

SNSPD

Low Noise amplifier, Photon counting and picosecond timing

[space science applications, dark matter detection]

JPL **MIT** **GT**

QUANTUM COMPUTING

Utility scale QC

ADC: 12b, 10 GSPS, < 100mW, operating at 4K

Quantum Science Center

Cryoelectronics for Ion-Trap based QC

Co-design system for Spin-Liquid simulations

Multi-tier compact cryogenic system

Eliminating cryogenic isolators and circulators, combining superconducting electronics with cryoCMOS

Microsoft

OAK RIDGE National Laboratory

🔷 Fermilab

AI ASICs

AI chiplet: AI Autoencoder ECON

On-detector Edge Compute for Adaptive-Autonomous Real time data processing at the Large Hadron Collider

- Algorithm Co-design: Low power (2nJ/inference), Low latency (25ns), Radhard operation

- Adaptive programable interface for various detector geometries and evolving detector conditions

To our knowledge, the first AI ASIC in HEP (all of DOE??)

AI tools and design methodology

Open source tool and design methodology: **hls4ml,** backend compatible for ASICs, extending to eFPGAs, mixed signal and beyond CMOS (**CrossSim** – Sandia), **ESP**

Industry and community driven: A large community from a variety of applications. Industry adding Open-source to tool plug-in

SIEMENS

Energy Efficient Edge AI hardware

- Chiplet, on-chip-edge, in-pixel

- Types of NN: DNN-Digital CMOS, Digital SNN, Analog NN (SRAM, ReRAM, ECRAM)

## AI-driven integrated heterogenous systems

Beyond system-on-chip: Heterogenous Compute On-chip

- Electronic – Photonic Integration
- In-memory compute
- Incorporate Industry/ Open source IP: ARM/RISC cores
- Heterogenous Detector stack: Sensors, Neuromorphic Layer (Novel Materials), Mixed signal electronics, Photonics

Fermilab

Skipper CCD and CCD-in-CMOS readout

Skipper CCD readout: MIDNA

- State-of-the-art noise performance (~3e- noise performance)

- Cryogenic operation (100K)

- On-chip analog pile-up to reduce readout time

- 100x lower power, extremely small footprint, significantly reduced cost

- Excellent test performance
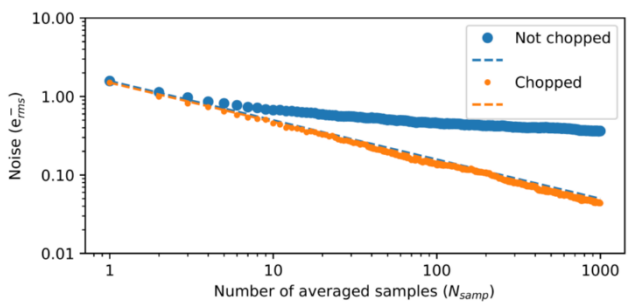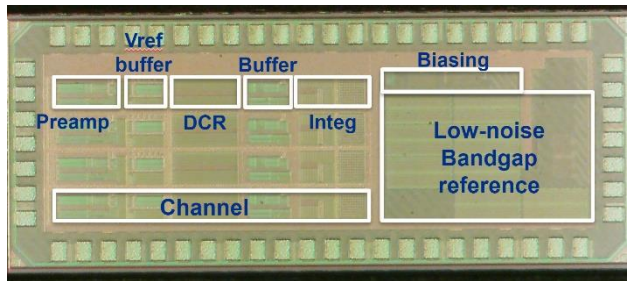
Skipper CCD-in-CMOS Sensor

- Collaboration with leading CMOS foundry (Tower Semiconductor) to develop Skipper-CCD in commercial CMOS process

- Prototyped ASIC has ~400 variations (pixel designs/process splits) to evaluate best design

- Testing underway, so far demonstrated detection, charge transfer, and skipping

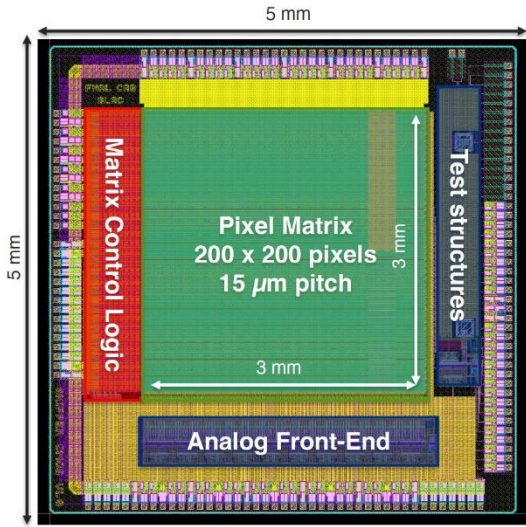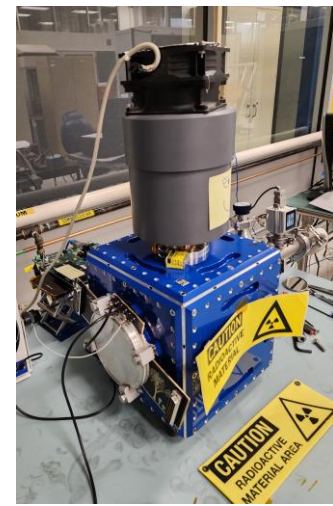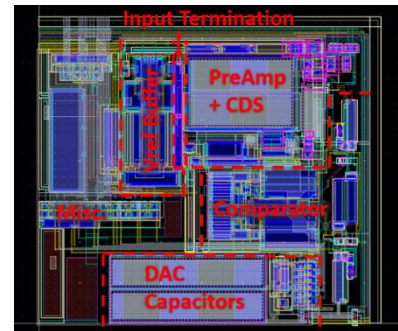- Full-reticle large area prototype to follow

Image sensor ASIC
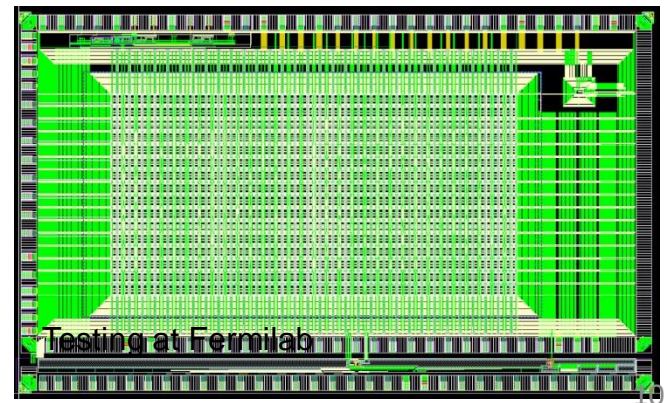

Highly-parallel readout ASIC for Skipper-on-CMOS

- Developed low-power in-pixel ADC for highly parallel readout (→ high frame rates)

- Per-pixel 10b ADC for massively parallel readout

- First two prototypes under test

- Full-reticle ASIC in 2023

10b, 100KSPS in-pixel ADC (~30x30μm)

SPROCKET ASIC: 64x32 pixels (09/22)
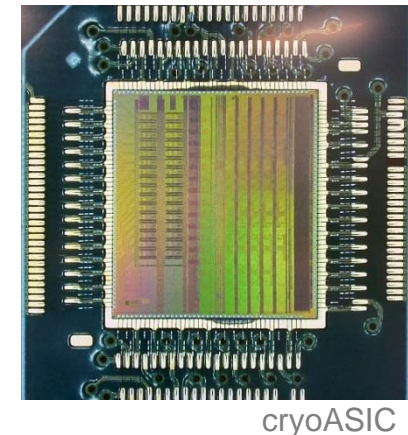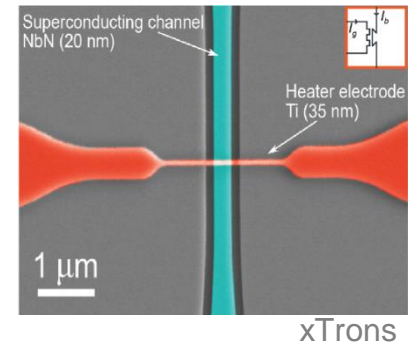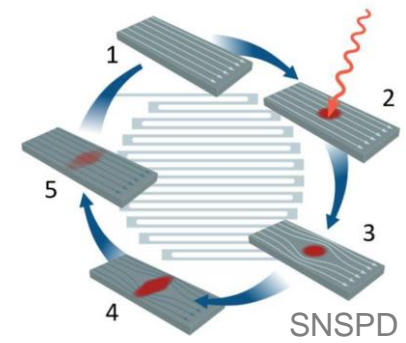

Testing at Fermilab

DOE Microelectronics Co-Design Research:
"Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes" (HYDRA)

SNSPD

Advancement of two complementary classes of cryogenic state-of-the-art single-photon and particle detectors:

- the **Skipper CCD-in-CMOS** silicon detector

- a **hybrid detector platform based on superconducting nanowires**

xTrons

Development and co-design of:

- advanced **fabrication and integration techniques**

- novel optimized **hybrid readout architectures**

- cryo-ASICs and cryotron-based superconducting electronics for **integrated sensing** and data reduction at source, through **feature extraction** and **edge computing**.


cryoASIC

 Fermilab   Argonne NATIONAL LABORATORY   SLAC NATIONAL ACCELERATOR LABORATORY   NIST   MIT   CALIFORNIA INSTITUTE OF TECHNOLOGY   JPL Jet Propulsion Laboratory California Institute of Technology   SYNOPSYS®

 Fermilab
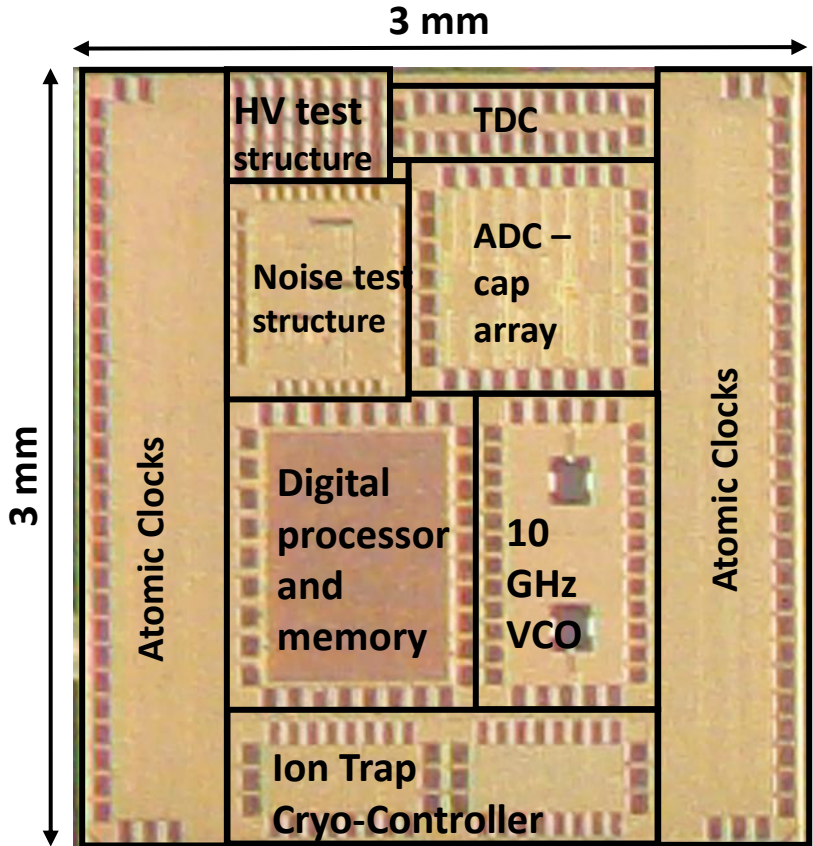
Cryogenic testing

- Custom ~4K close-cycle cryocooler (large area and # flanges)
- Cryogenic probe station in the planning

Chips received in Apr 2022

- 2 channels of Cryo DAC: 100 MSPS, 10V O/P swing
- 10 GHz VCO for on-chip PLL
- High voltage test structure for debugging
- Noise test structure
- Capacitive DAC test structure
- Digital processor and memories
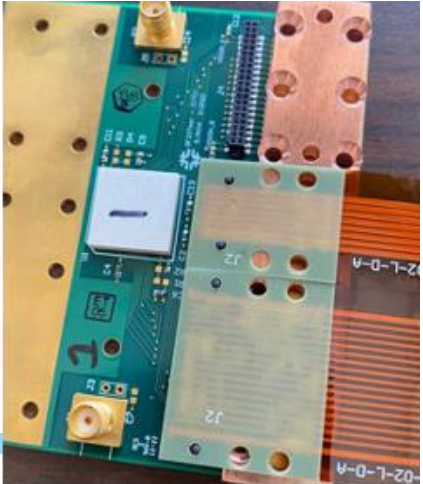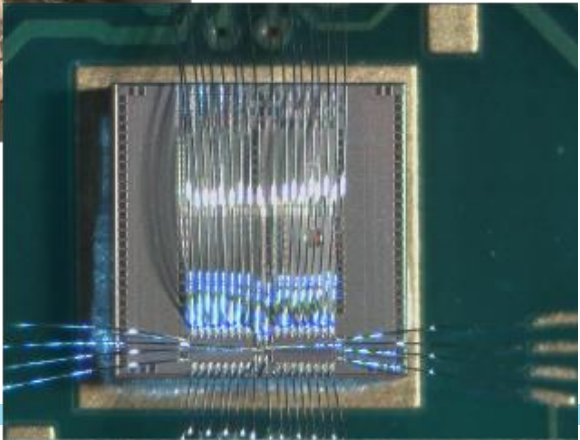
Overview of Fermilab's 22FDX Cryo-CMOS modeling activities

Fermilab is leading several activities for the cryogenic characterization of 22FDX transistors:

In House:
- Measurement and modeling of high voltage devices at 4K (BOXFET, LDMOS)

With EPFL:
- Measurements of transistors at 4K
- Development of simplified EKV model for analog design
- Low noise test structure measurements

With Synopsys:
- PDK-compatible BSIM-IMG for 4K

22FDX Navigation/Test Documentation
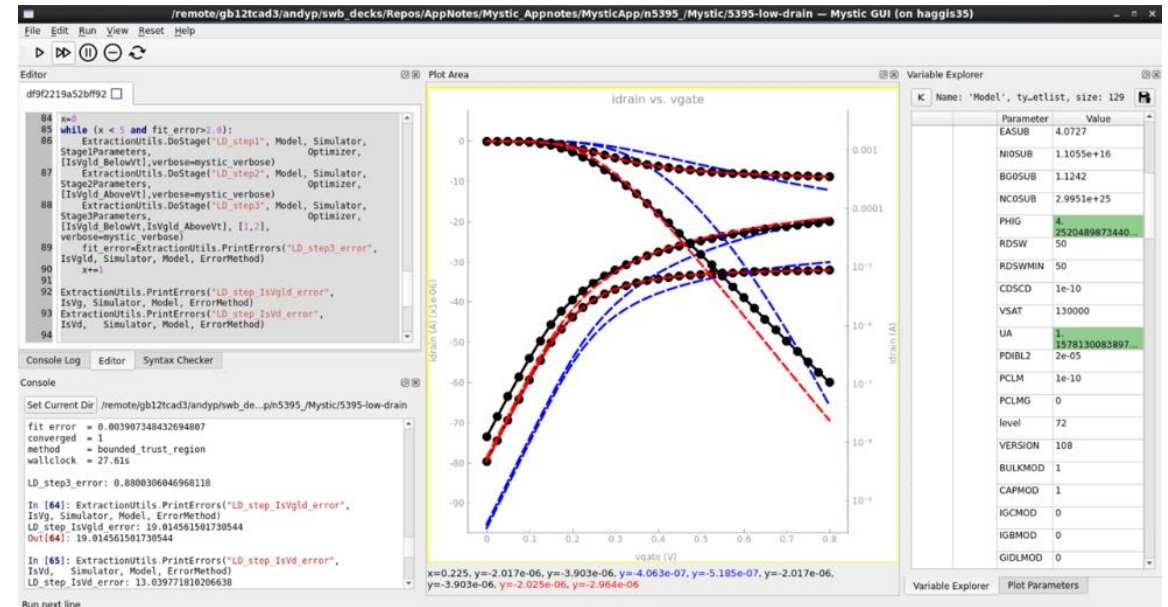
Basic FET Test Structures – Start slide 2
RF Test Structures – Start slide 26
MPWCS12

GLOBALFOUNDRIES

Fermilab is working with **Synopsys** to develop PDK-compatible isothermal models at 4K with **Mystic** (advanced **compact model** parameter extraction tool for **SPICE** models)

- Currently working on thin and thick oxide cmos
- HV devices next
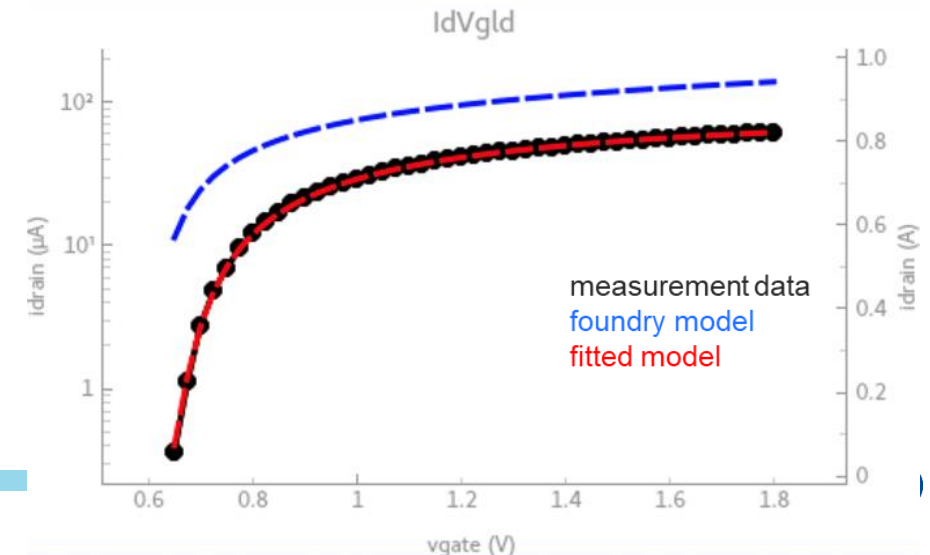
Cryo-CMOS Modeling – before extraction

Tranfer Characteristics PDK Simulated


Gm Low Drain PDK Simulated


Low Drain PDK Simulated
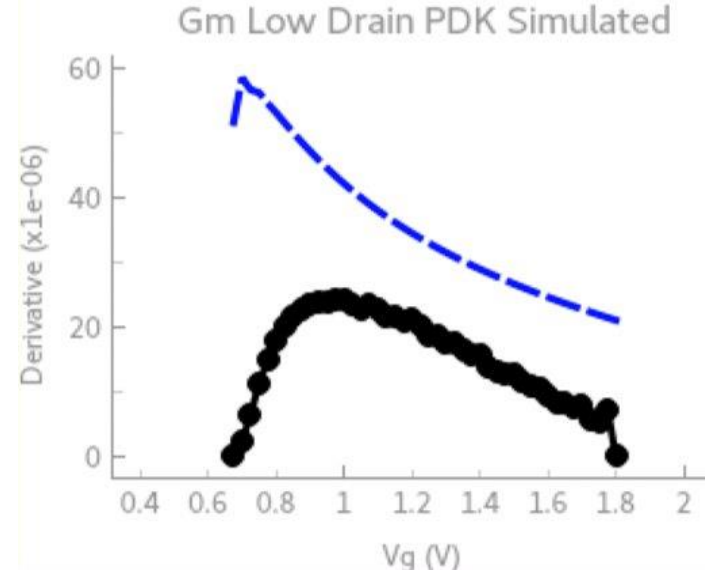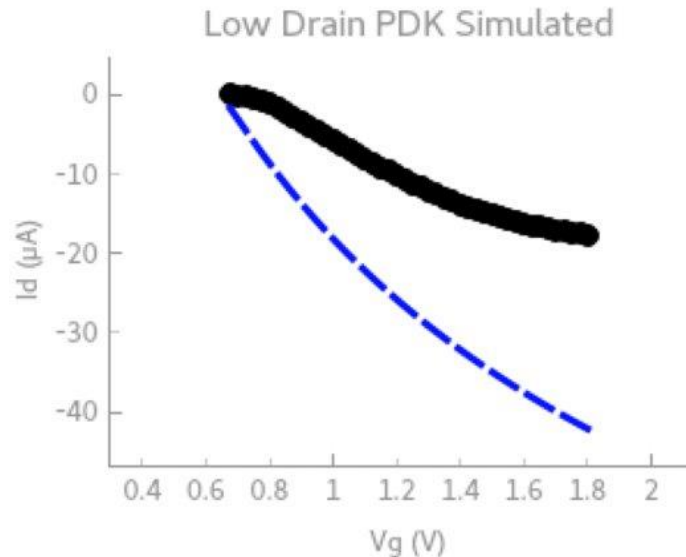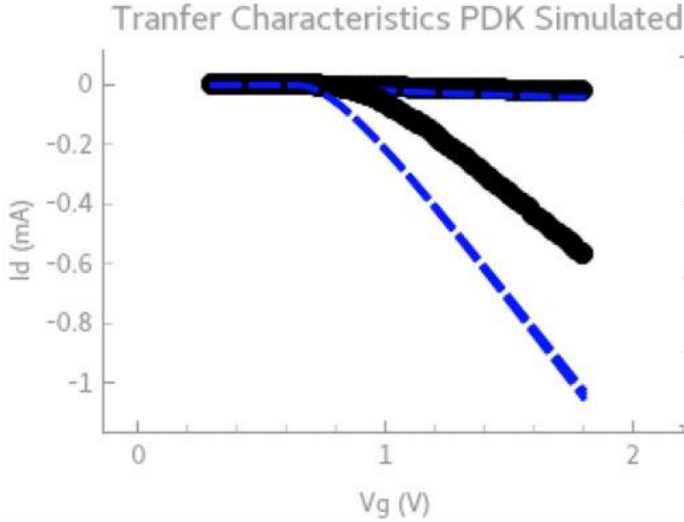
Original Process Design Kit Simulated data
vs Data at 3.8K

Black is our measurement data, the blue is the
Process Design Kit simulated data from Global
Foundries

- PDK models are numerically robust but not accurate at extremely low temperature (e.g. 40K)

- Significant discrepancy between measurement data and simulation data

Cryo-CMOS Modeling – after extraction
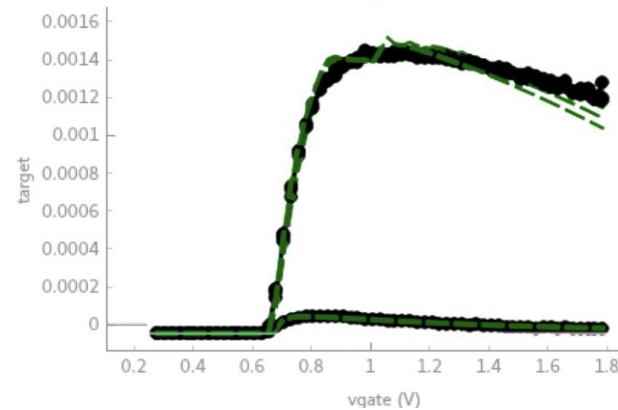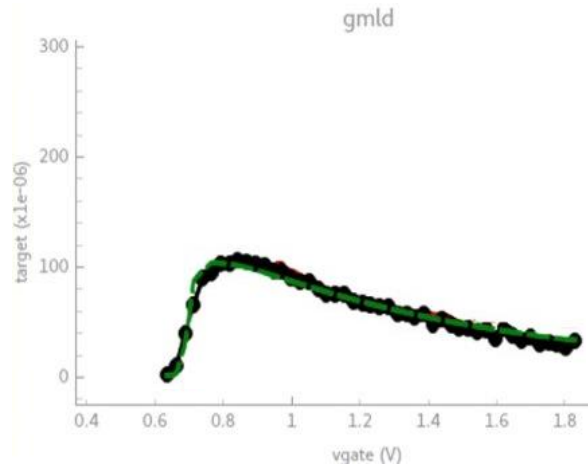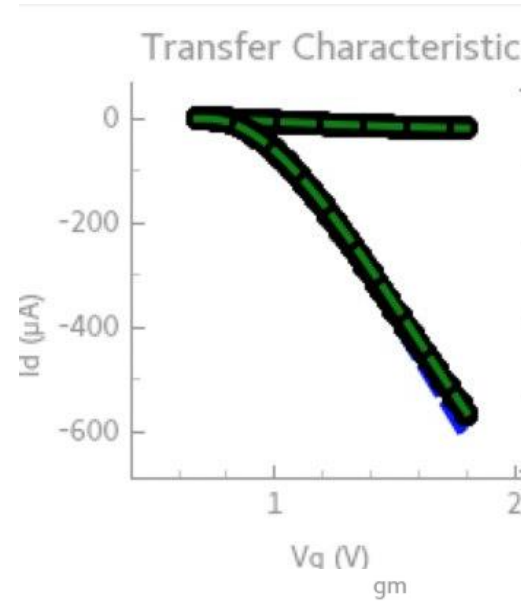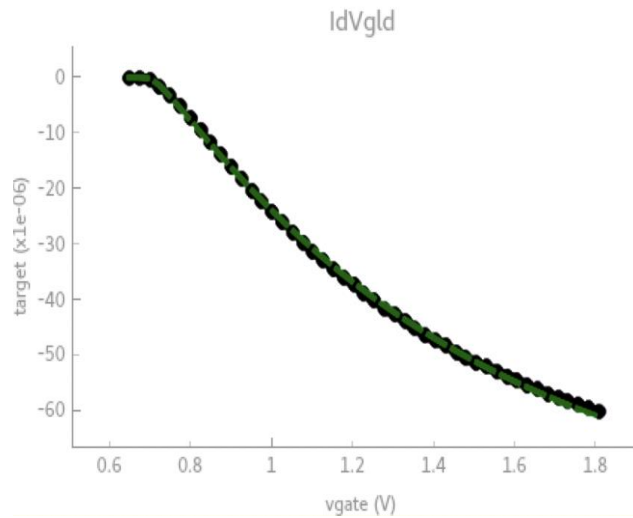
- PDK models are numerically robust but not accurate at extremely low temperature (e.g. 40K)

- Significant discrepancy between measurement data and simulation data

- Fitting so far progressing well

CMOS Sensors Vision

GOALS for a HEP community-driven CMOS sensor development

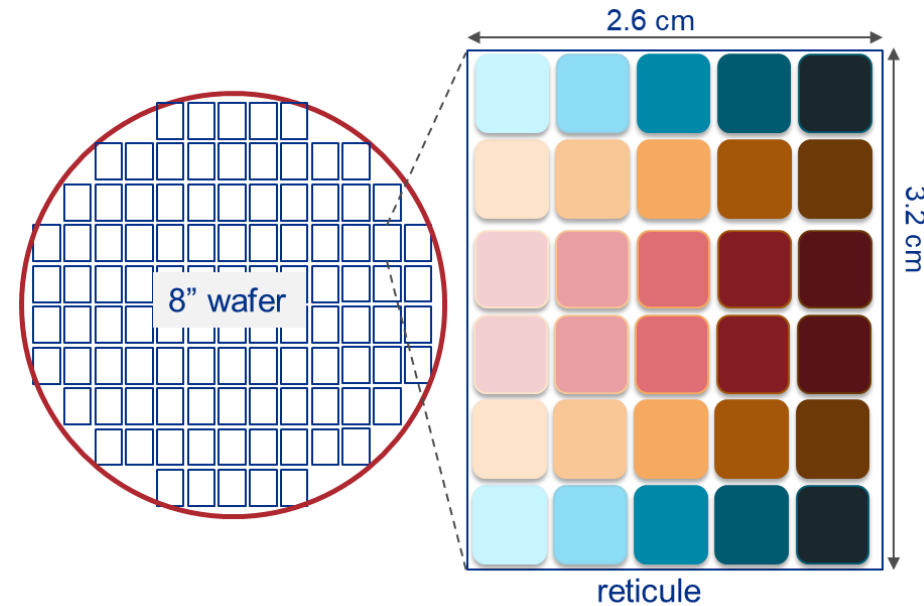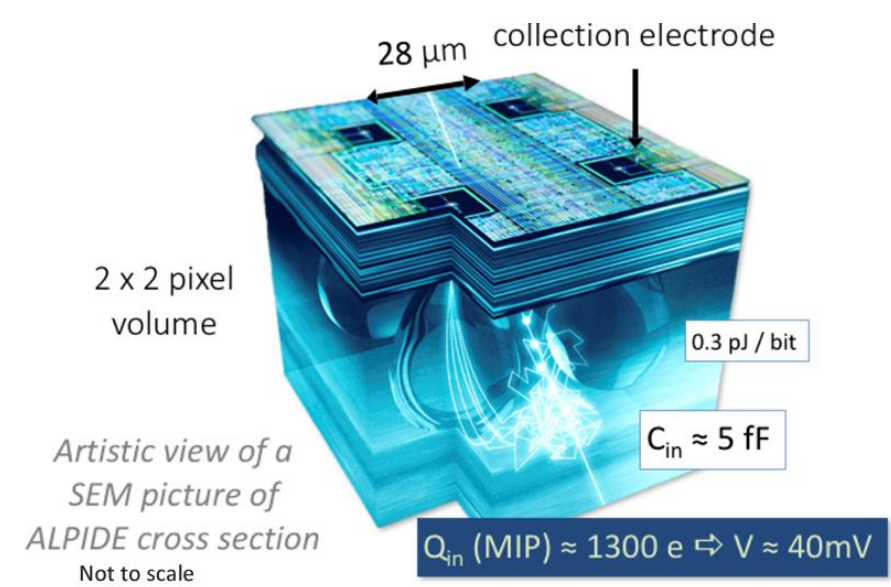- Enable US manufactured sensor capability for HEP experiments
- Optimize the process to enable various types of sensors ubiquitously used in HEP (MAPS, MAPS with timing, Digital SPADs, LGADs, CMOS LGADs)
- Co-design sensor and readout electronics

- Enable the broad adoption of the development across HEP community

PARTNER with SKYWATER TECHNOLOGIES

Strong academic support for device simulation and testing

Engineering run with various designs on a high resistivity wafer

High-throughput testing of sensors at Fermilab

28 μm collection electrode

2 x 2 pixel volume

0.3 pJ / bit

$C_{in} \approx 5$ fF

Artistic view of a SEM picture of ALPIDE cross section Not to scale

Q_{in} (MIP) ≈ 1300 e $\Rightarrow$ V ≈ 40mV

2.6 cm

3.2 cm

8" wafer

reticule

Fermilab

Silicon Photonics

- Goal: Integrated sensing - edge computing – communication

- Creating high bandwidth, low power interconnect for sensor networks

- Preliminary use case: Pixel detectors → 1M pixels generate > 1 Tbps data zero-suppressed data; with edge computing we can get to 30 – 100 Gbps

High bandwidth data transmission integrated with chips

Cryogenic data transmission (100K to 4K)

Rad-hard data transmission
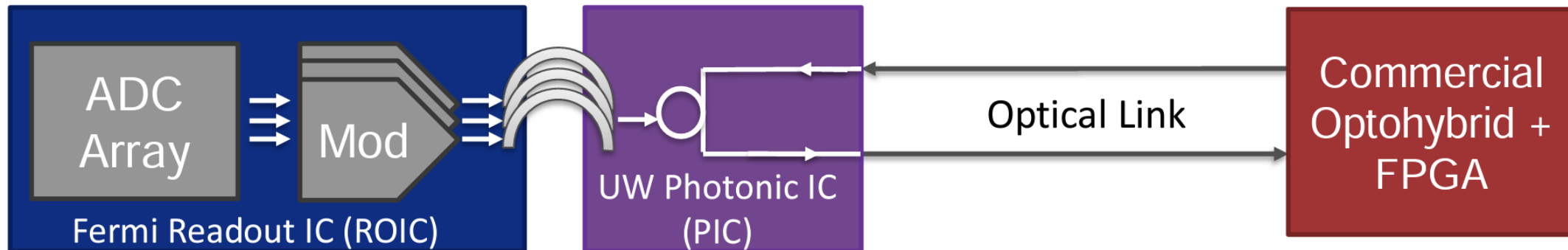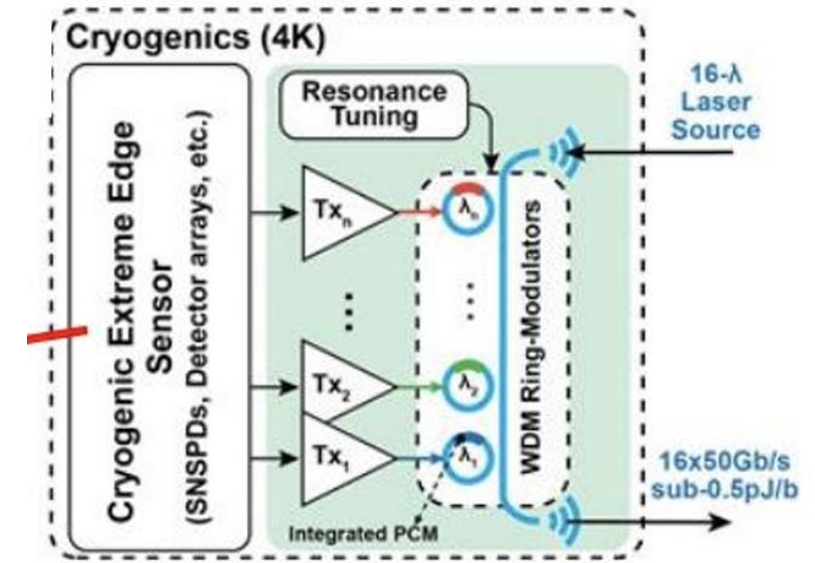
🔷 **Fermilab**

3D ICs – community driven for DOE applications

Fermilab started pursuing 3D integration in 2006

- Work with partners (university, national labs, industry) to create a 3D IC Consortium

- Create pathway for DOE applications

- Work with vendors to setup standards/processes for low-mid volume prototyping

‡ Fermilab
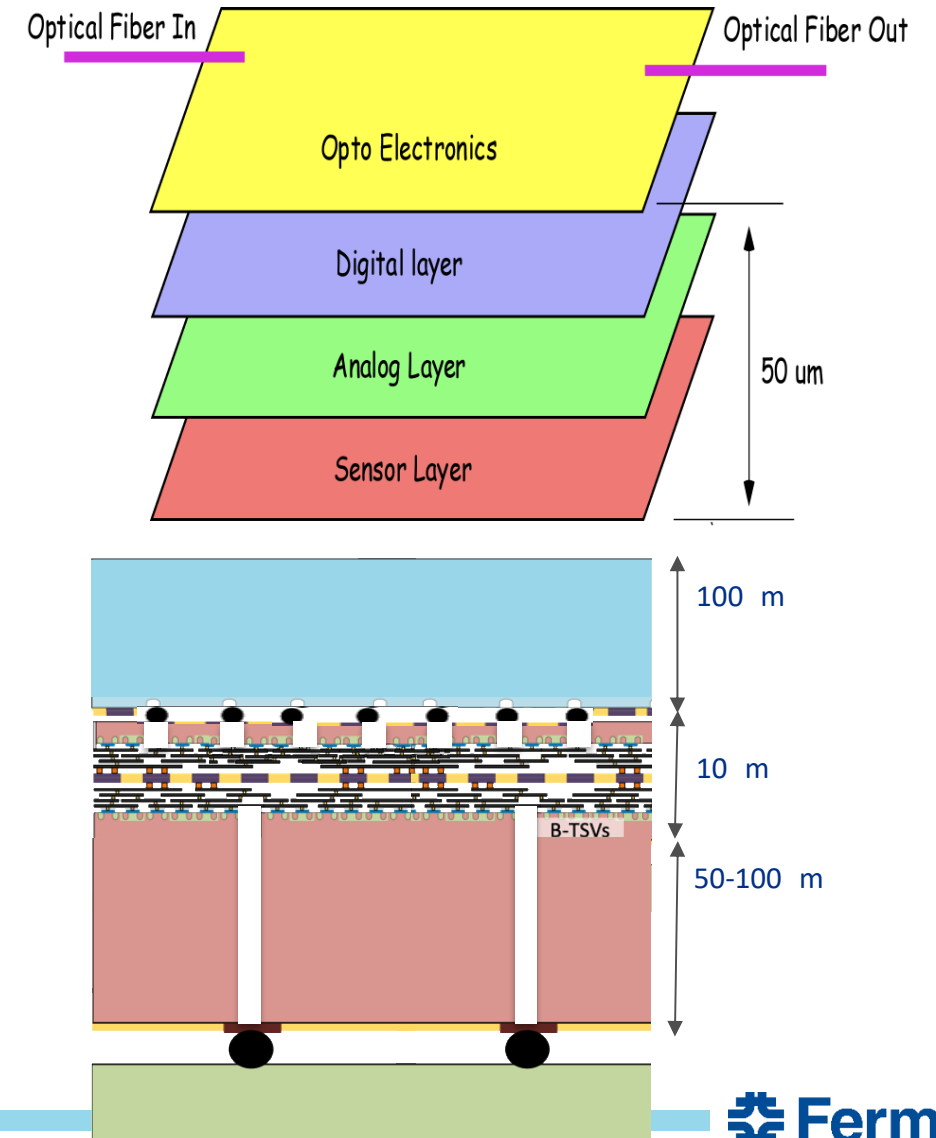
Why do we need AI/ML in Science?

~2024.

Rubin LSST

~ 20 TB / day
~ 100 PB total by
  DR11

DUNE

~ 30-60 PB / year (raw)
~ 114x4 TB / month (raw)
for Supernovae detection
(speed need for
followups)

~2026.

HL-LHC

~ order of magnitude more data
~ 650 PB / year

Slides courtesy of Ben Hawks
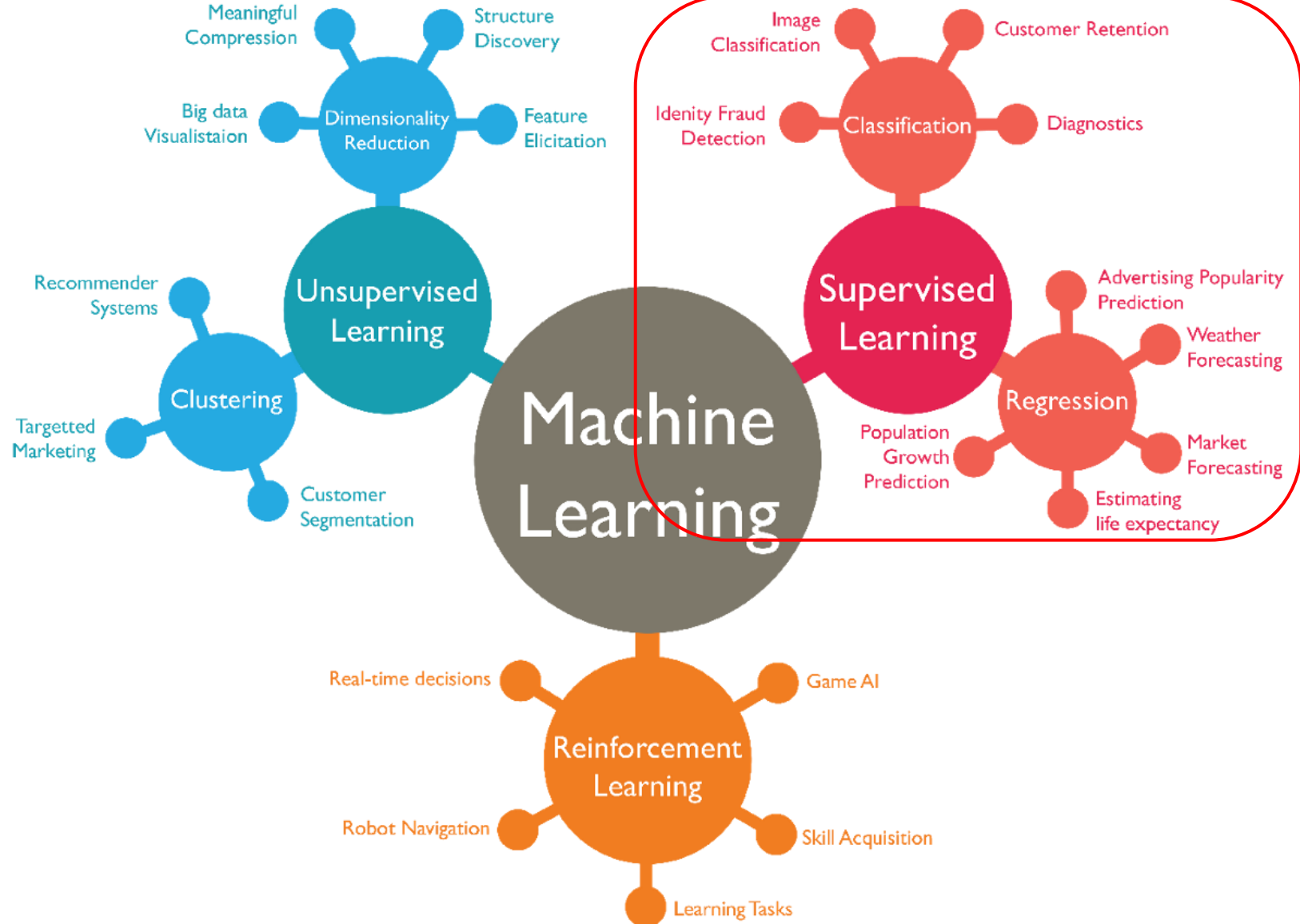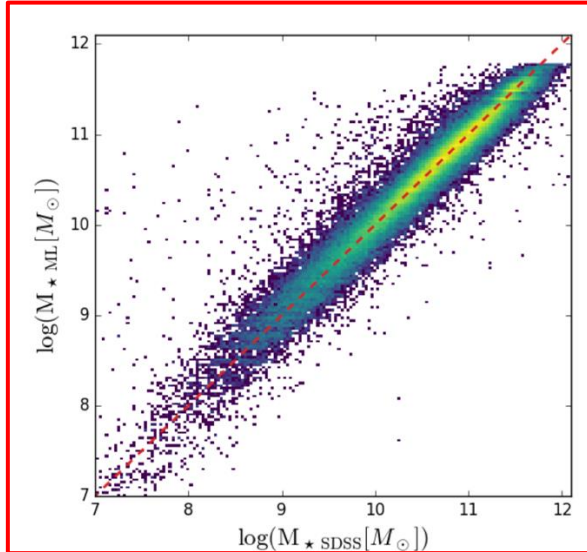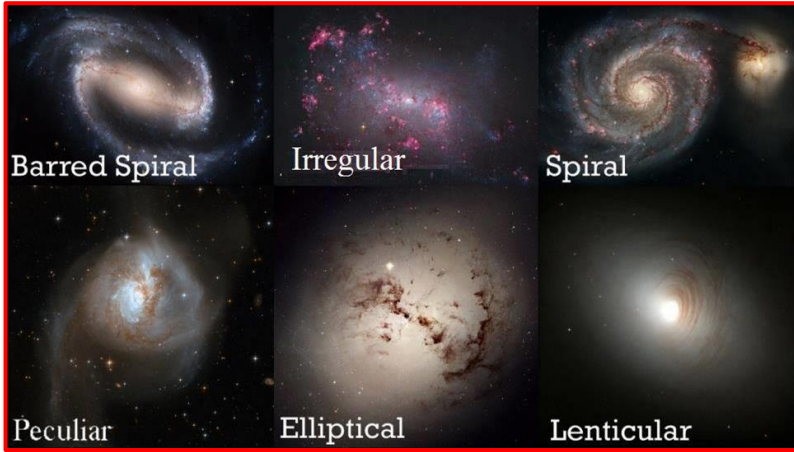(he/him/his)
AI Researcher @ Fermilab
Real Time Processing Systems - Data Intensive Systems
bhawks@fnal.gov
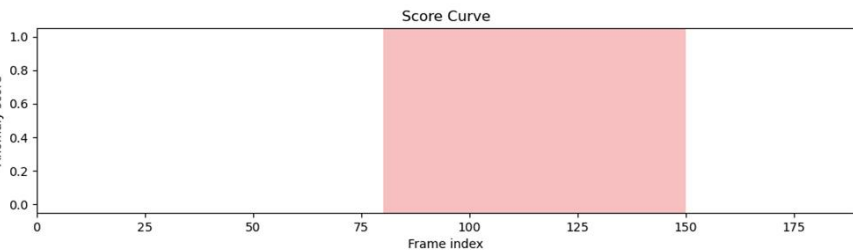@quantized_bits<@defcon.social>

Types of ML Tasks - Supervised Learning

Types of ML Tasks - Unsupervised Learning

Ground truth video | Predicted video | Prediction error

Score Curve

Le, VT., Kim, YG. Attention-based residual autoencoder for video anomaly detection. *Appl Intell* **53**, 3240–3254 (2023). https://doi.org/10.1007/s10489-022-03613-1
https://vt-le.github.io/astnet/
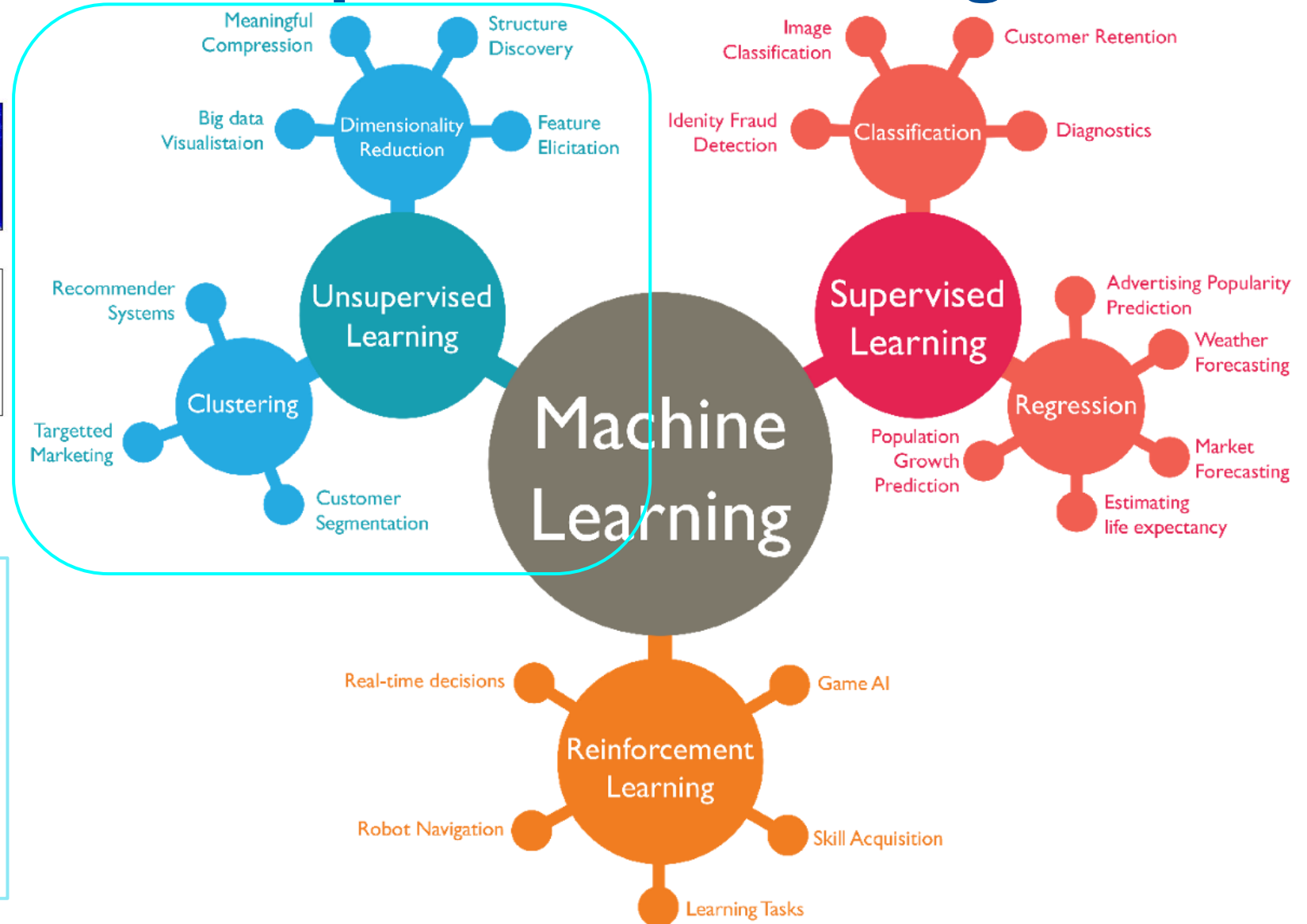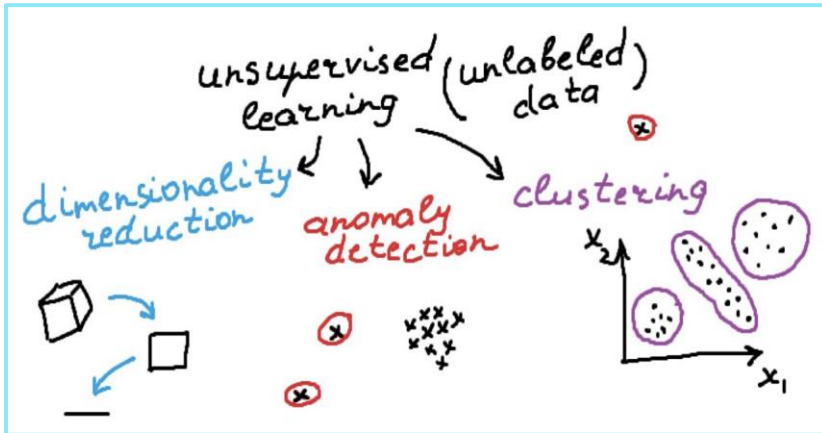
Design Methodology: Physics driven hardware co-design

- Algorithm development based on Physics data
- **hls4ml** simplifies the design of on-chip ML accelerators

  | hls4ml directives | << | HLS directives |

  C++ library of ML functionalities optimized for HLS

- TMR4sv_hls: Triple Modular Redundancy tool for System Verilog & HLS
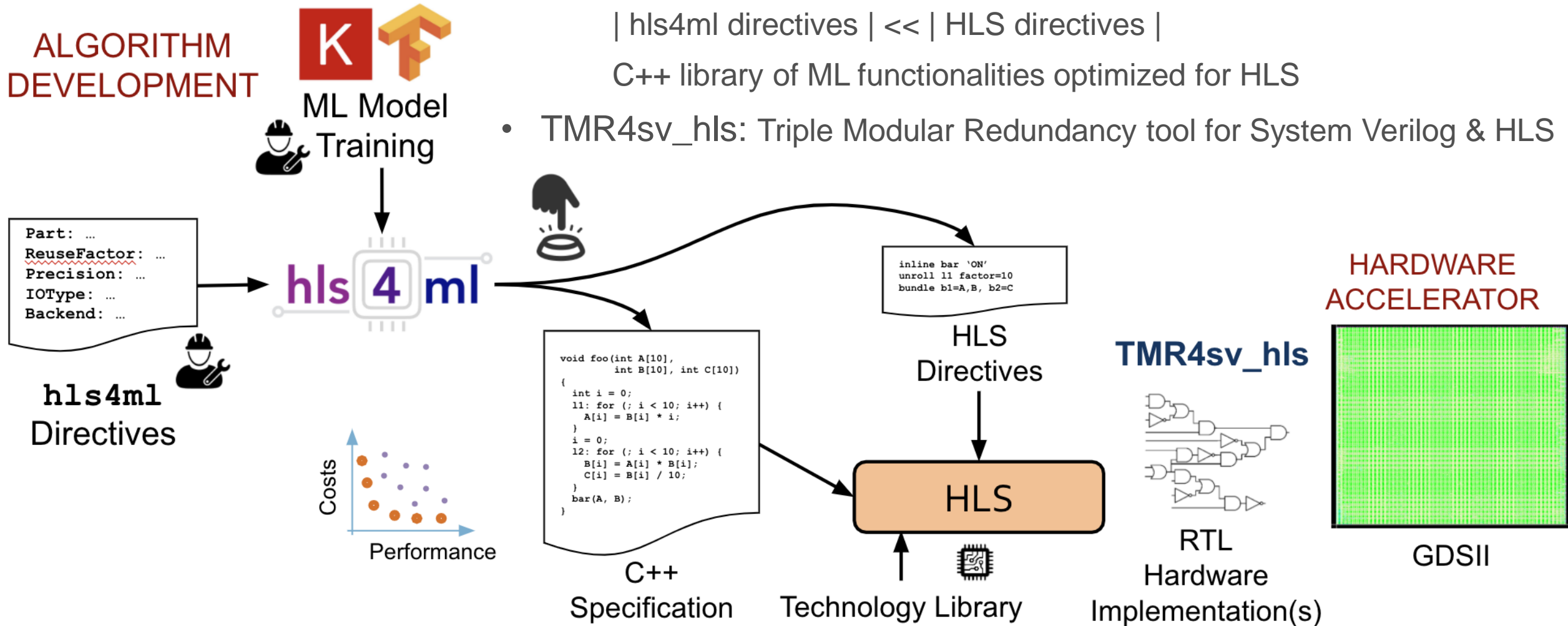
OPEN SOURCE TOOLS & EDGE AI

Model → Quantized model → hls4ml → HLS project → Hardware

- Develop **efficient edge ML** algorithms

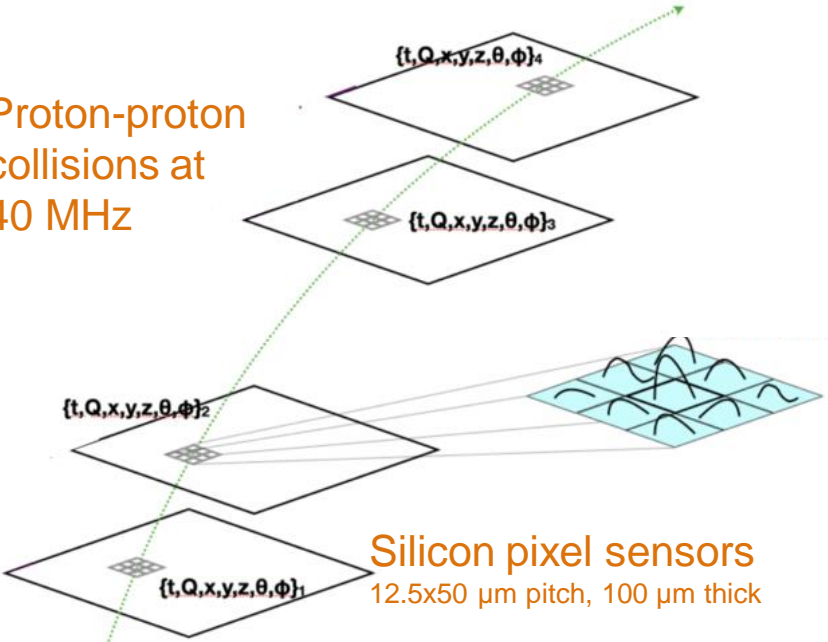 - Quantization and sparsity, optimization techniques

  - Physics-inspired and robust inverse algorithms

- Build user-driven, **open-source workflows** for algorithm-hardware codesign

  - Democratizing powerful edge ML for a broad range of scientific applications and industry

  - Workforce development, multi-disciplinary collaborations, and education/demos/tutorials
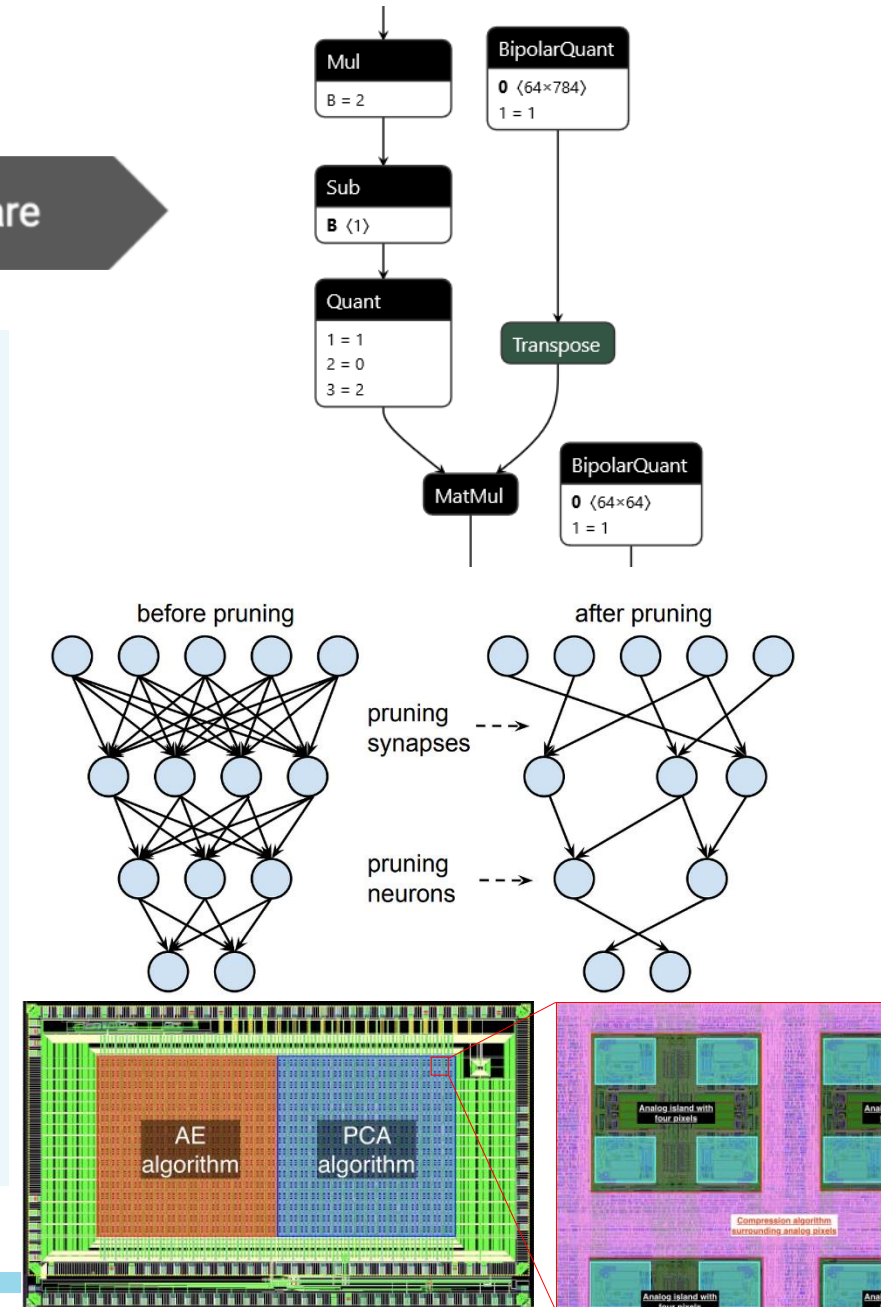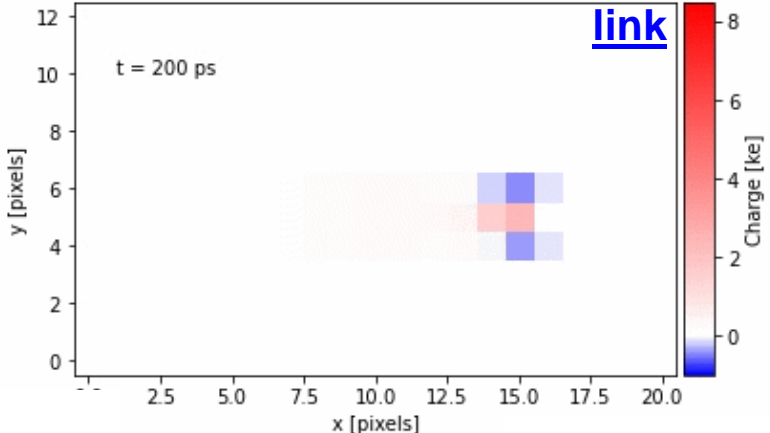
Real-time tracking for pixel detectors

Proton-proton collisions at 40 MHz

{t,Q,x,y,z,θ,φ}$_4$

{t,Q,x,y,z,θ,φ}$_3$

{t,Q,x,y,z,θ,φ}$_2$

{t,Q,x,y,z,θ,φ}$_1$

Silicon pixel sensors
12.5x50 μm pitch, 100 μm thick

Simulation
[link](#)

Cluster shapes and Pulse information for filtering out low p_T particles

- NN classifier identifies and saves clusters from tracks with $p_T > 2$ GeV

- ≥ 95% data reduction by saving only high p_T

- Low power implementation

Compact algorithms for data reduction through featurization

- **Predict** physics information $(x, y, θ, φ)$ and **meaningful error** (UQ) on particle position, angle

- Potential for reduction of track seeds → saves time & computing resources down the line

Technology development to enable on-sensor computing

- Ultra low power in-memory compute chips

- 3D integration for optimized data processing

- Leverage emerging technologies such as novel CMOS compatible memristors

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Scalable Quantum Control

System-on-Chip
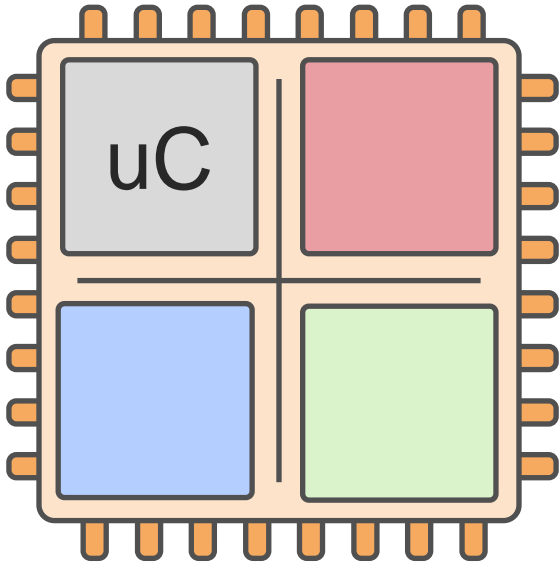
- **Platform for Scalable Quantum Control** = ESP + FlexLogix eFPGA
  - ML running on eFPGA/SoC in the cryostat for scalable quantum control
  - Methodology: hls4ml + Catapult HLS + Synplify + FlexCompiler
  - Architecture: eFPGA integration in SoC tile(s)
- **Quantum control applications**
  - Data acquisition, model training, model evaluation, hardware synthesis
    - State preparation (Control)
      - Workshop on Quantum Computing Software 2022
    - Readout, Error correction
  - Early emulation on FNAL QICK looking for collaborators for demonstration
- **CryoAI, 22nm**
  - Digital test chip to evaluate low power cryogenic performance of digital backend at lower core voltages
  - Design and integration of an ML Accelerator (AutoEncoder for Anomaly Detection – IoT MLPerf Tiny)
  - Chip & board fabricated – Ongoing testing
 - ESP simulation for future respin

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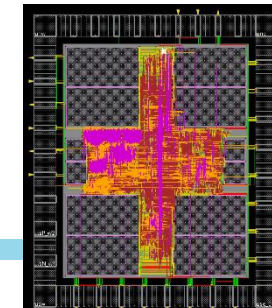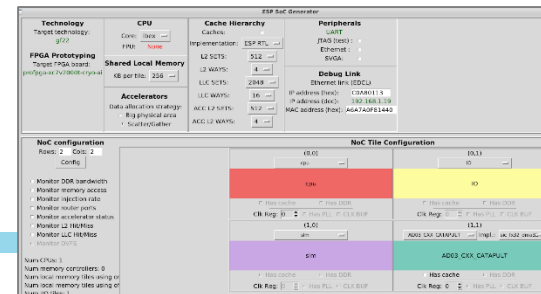
Reconfigurable Edge AI – Solve the HEP data challenge

- Collaboration with Columbia U. & Northwestern U.

- Edge AI: Combining two established open-source platforms (ESP and HLS4ML) into a new system-level design flow to build and program a System on chip

  In the modular tile-based architecture, we integrated a low-power 32-bit RISC-V microcontroller (Ibex), 200KB SRAM-based memory, and a neural-network accelerator for anomaly detection utilizing a network-on-chip.
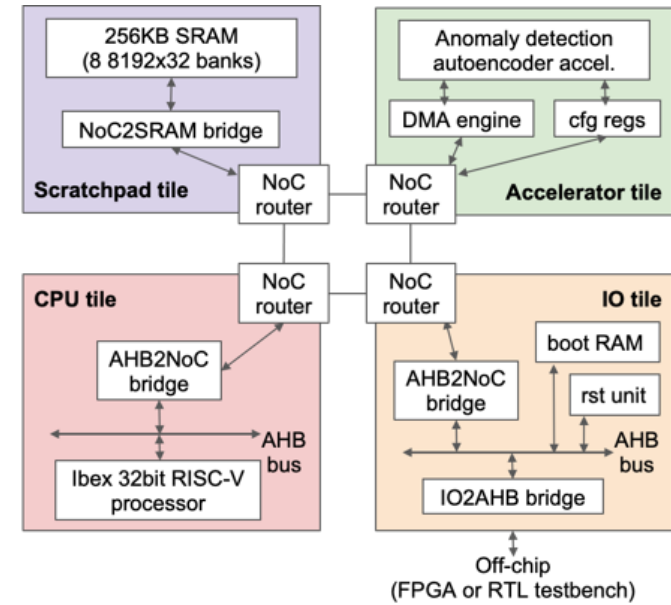
- Embedding FPGAs on detector: Radhard/ cryogenic eFPGA on-chip – with Flex Logix (22nm / 28nm). Establishing design flow and investigating extreme environment performance

Fermilab: Integrated Circuits
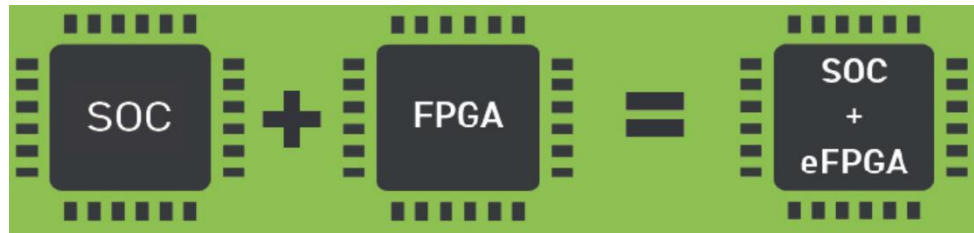
Thank You!

Many topics not covered in this presentation

If interested, please contact us

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