FAZIA electronics report

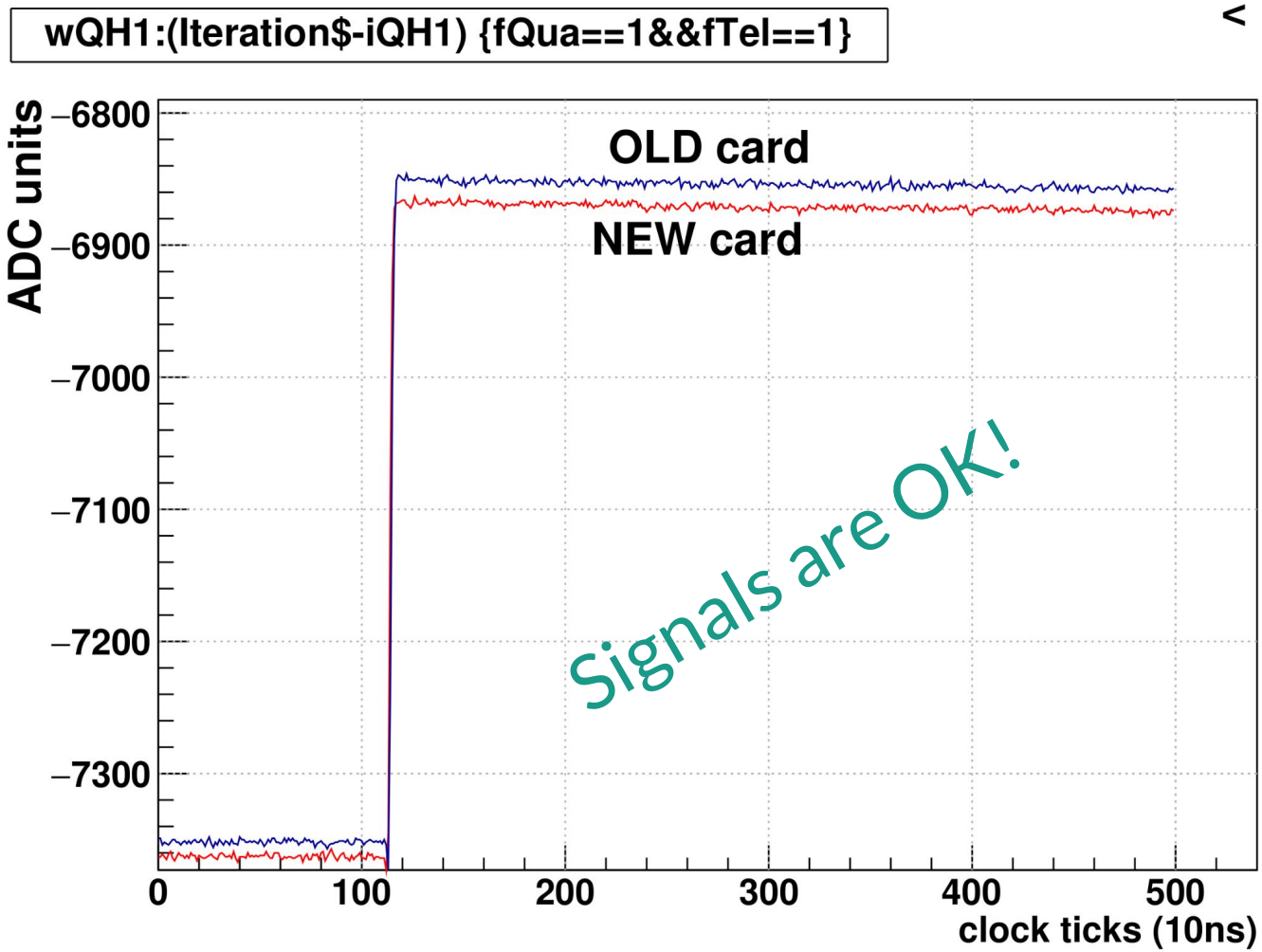
Simone Valdre', INFN - Sezione di Firenze

FAZIA days @ Villa Gioiello, 28/06/2023

Front-end electronics

Brief history

- FAZIA front-end electronics were developed and improved during the last ~12 years
  - versions 1 and 2 (v1 and v2) were prototypes
  - from v3 to v5.4 used in experiments
- Small differences in component schematics and PCB layout in order to solve problems
  - BUT same FPGA model used from v2 to v5.4!!!
- Today some components used in the reference design are obsolete
- In 2021 NOTICE company (in Korea) produced new FEEs
  - designed by Korean side of FAZIA collaboration
  - same design as v5.4 BUT new FPGA model (Kintex 7) and a CPLD added
  - we are still solving some firmware problems but the new cards are overall working!


wQH1:(Iteration$-iQH1) {fQua==1&&fTel==1}
ADC units
−6800
−6900
−7000
−7100
−7200
−7300
OLD card
NEW card
Signals are OK!
0
100
200
300
400
500
clock ticks (10ns)

Benefits of new boards

- Less PCB surface used
  - margin for designing a smaller FAZIA block!
- ~10% less power consumption and thermal dissipation
  - better in-vacuum operations
- Modern components
  - less expensive and easier to find on the market

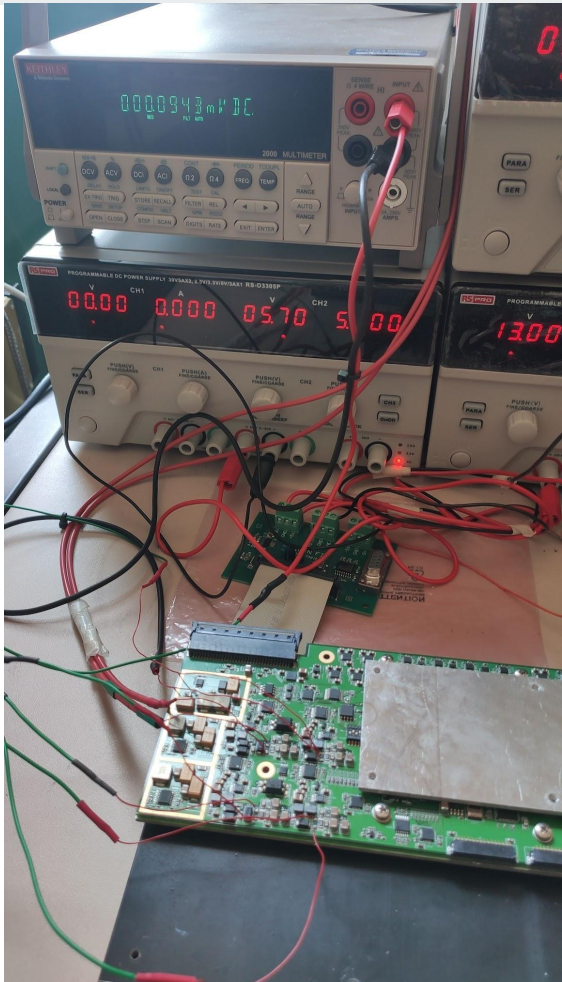
more details in the talk by MinJung Kweon (given yesterday)

FEE testing procedure

FEEs are very complex boards…
…testing after production or repair happens in two phases:

1. Test bench -> card is tested alone with TBC board
    a. Low voltages / High voltages (+leakage current measurement check)
    b. Pre-amp status
    c. ADC bit check

2. Mounted on the FAZIA block -> card is tested in real conditions
    a. SNR of all acquired waveforms
    b. Pulser check



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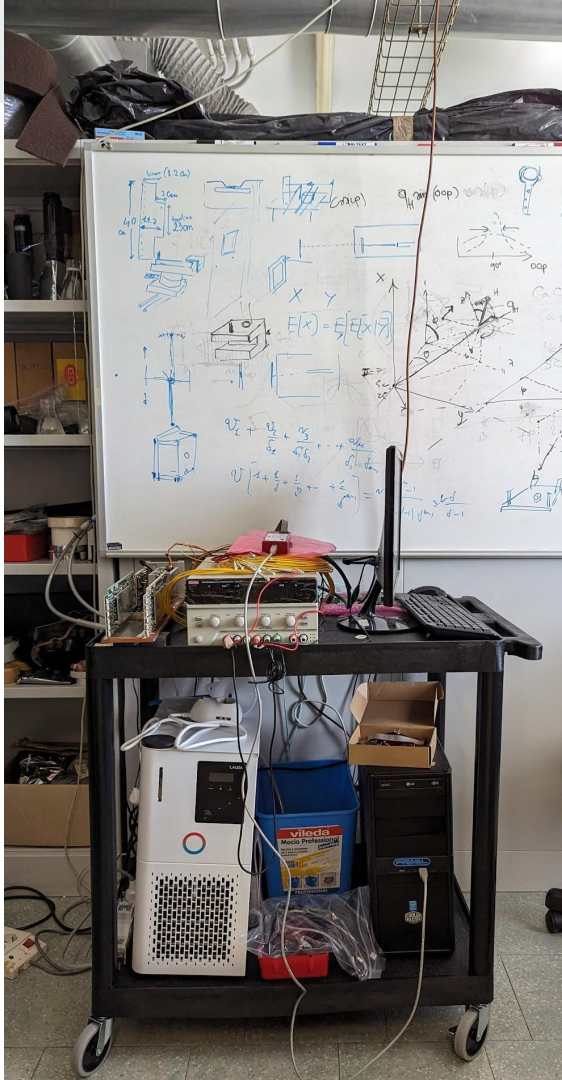

FEE testing procedure

- Maintenance was handled by IPN Orsay up to ~2018.
- We gradually built a bench at INFN - Firenze division in order to test and calibrate FEEs
  - Test software integrally rewritten
  - TBC boards re-engineered
  - Simplified HV calibration procedure

- In 2021 we started a collaboration with AGE Scientific company to repair FEEs
  - 24 front-end cards repaired (equivalent to 3 blocks)!

FEE v3 status

34 total card produced:

- 27 fully working
- 3 to be checked
- 1 with minor issues
- 3 fully broken
  (used for spare parts)

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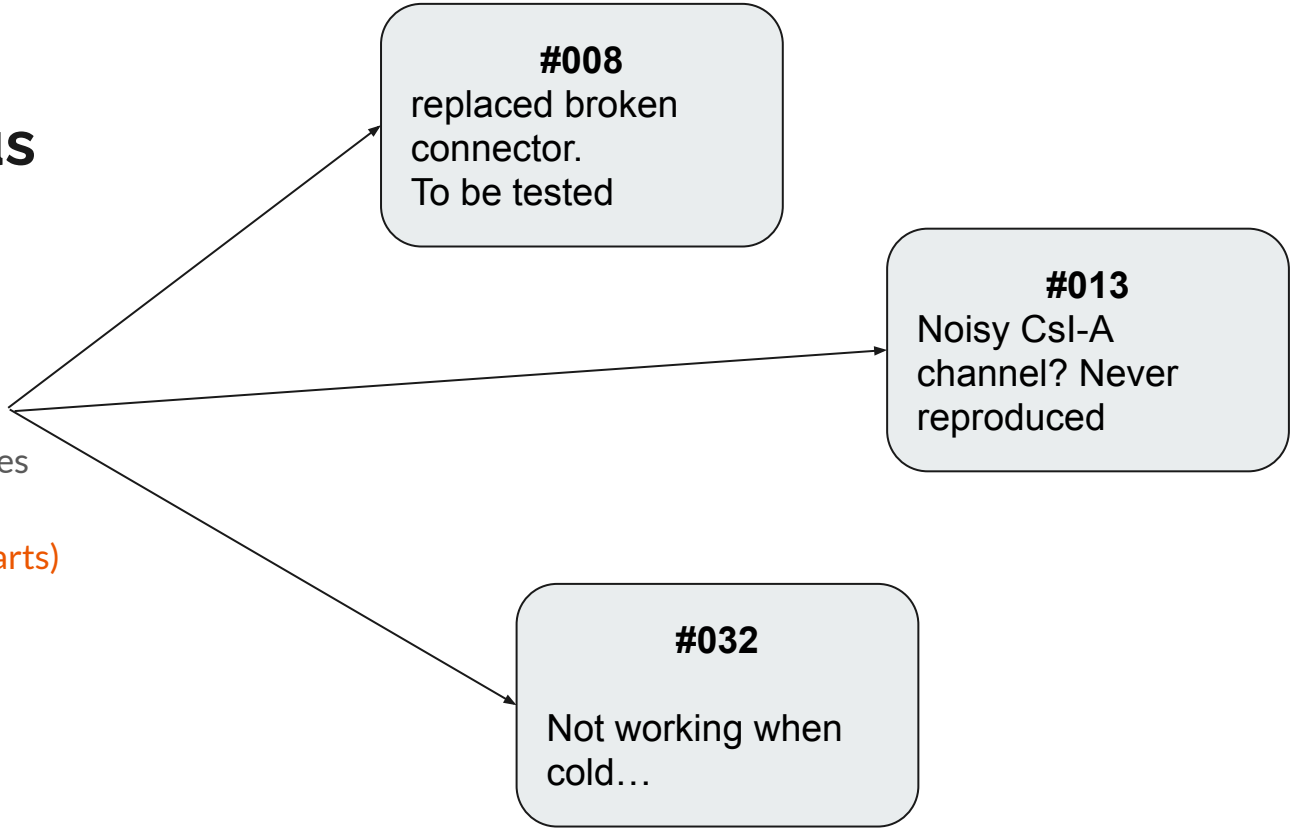

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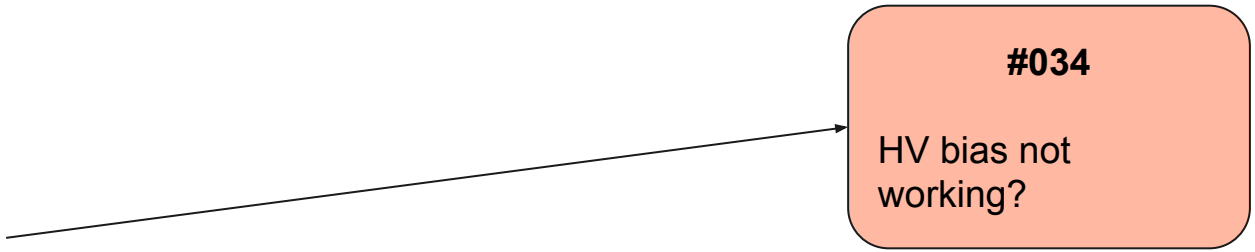

FEE v4/5 (ASCO) status

82 total card produced:

- 76 fully working
- 4 to be checked
- 2 with minor issues

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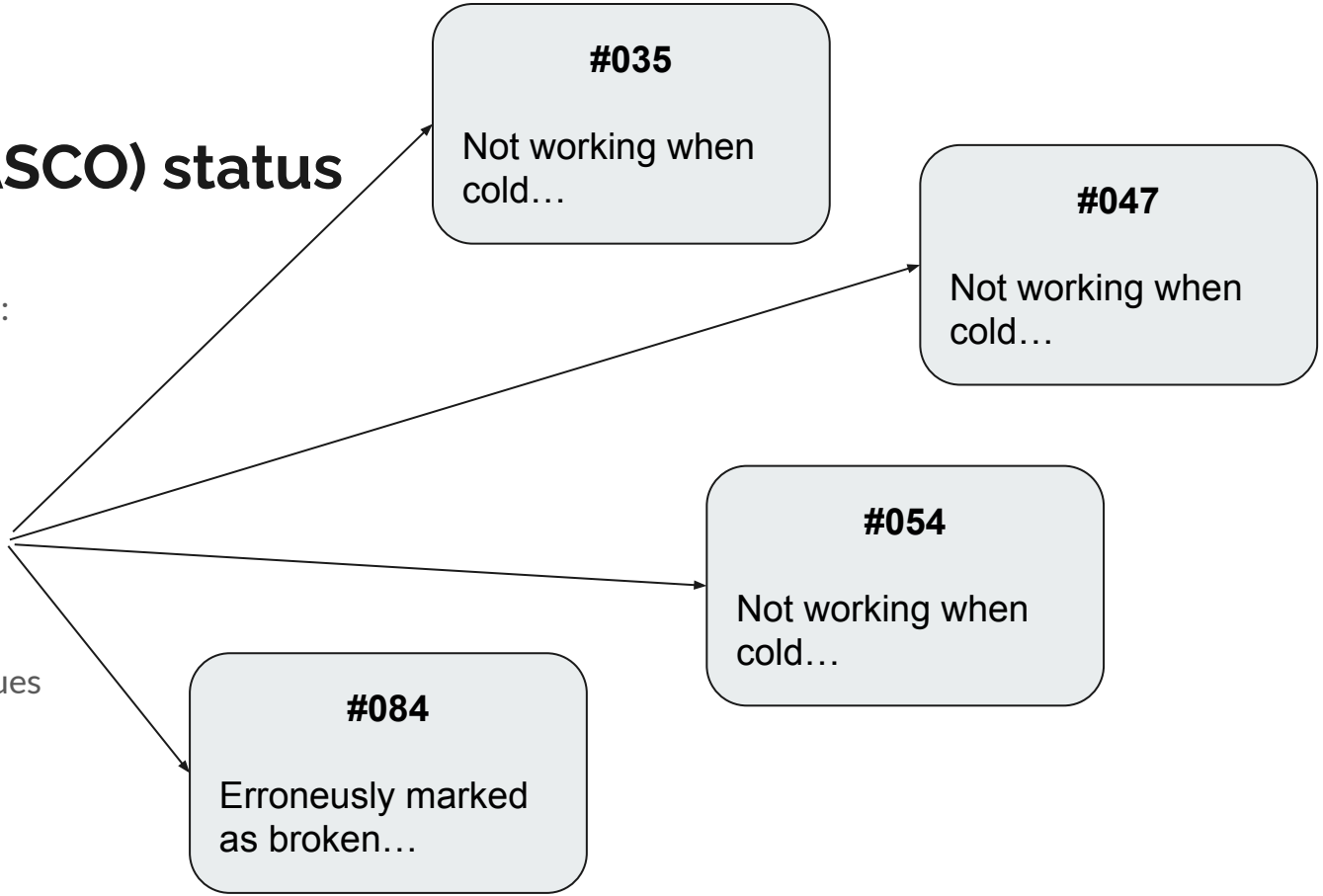

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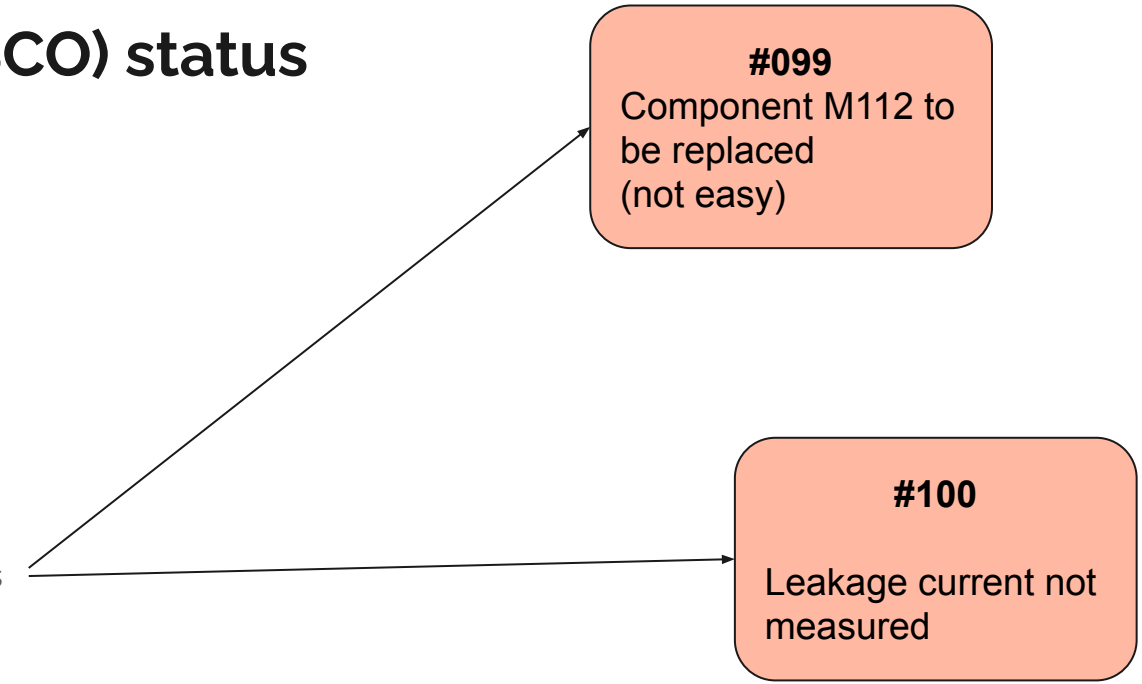

FEE v5 (ARTEL) status

30 total card produced:

- 23 fully working
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- 3 with minor issues
- 1 fully broken (probably not recoverable)

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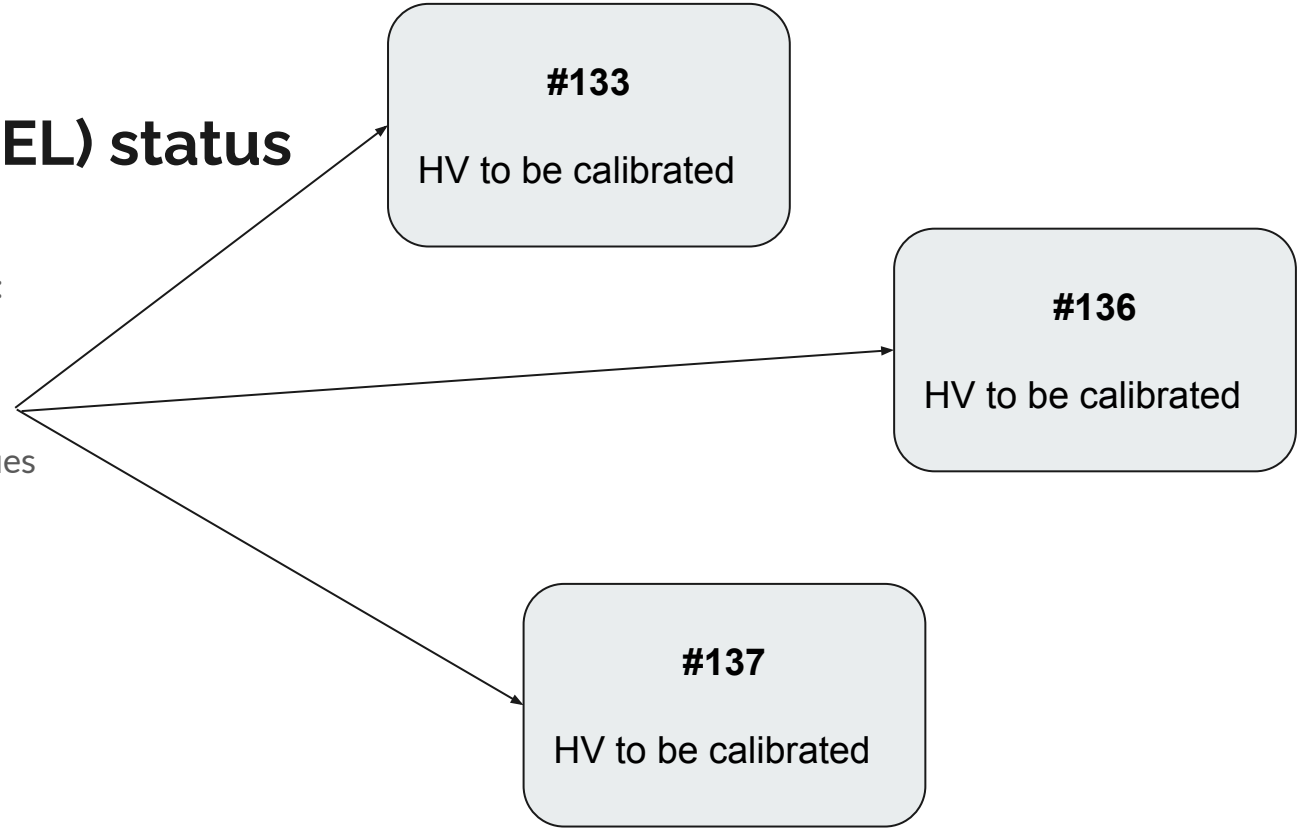

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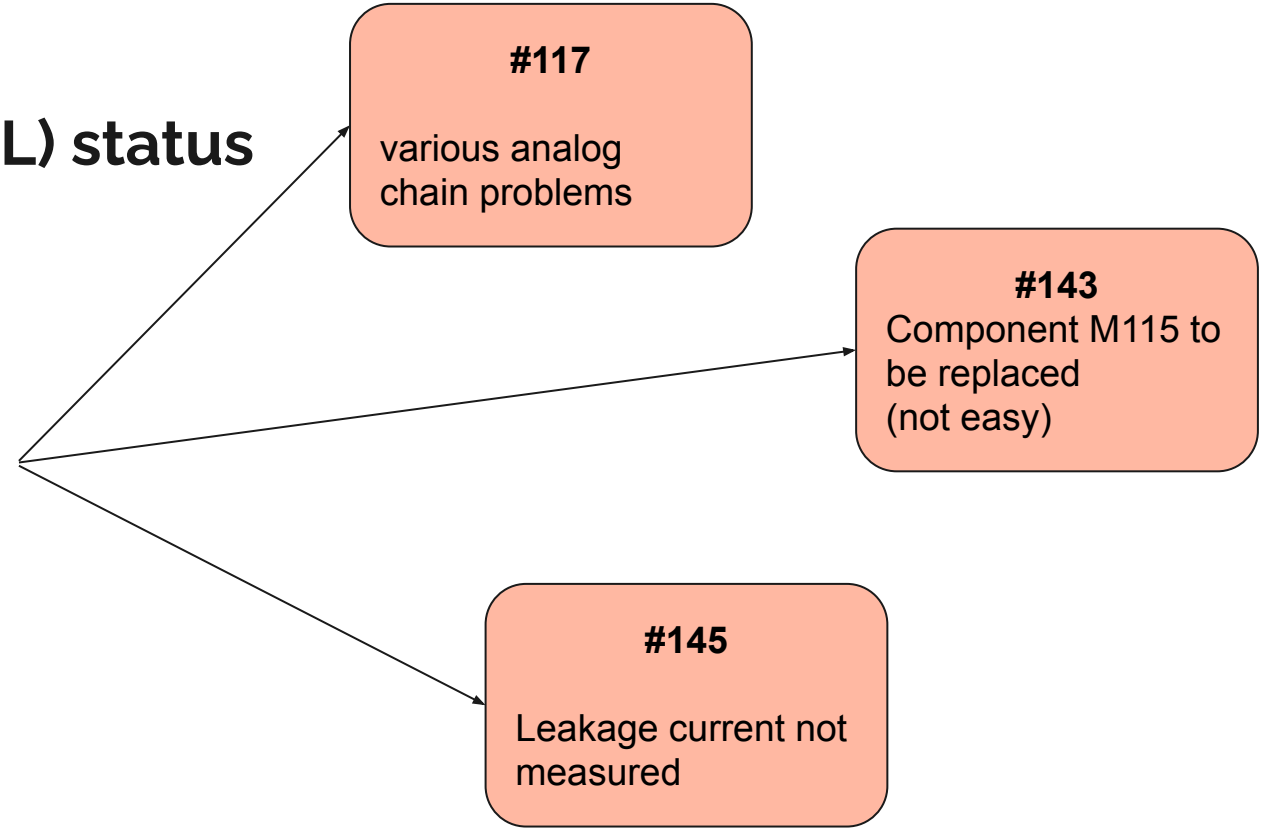
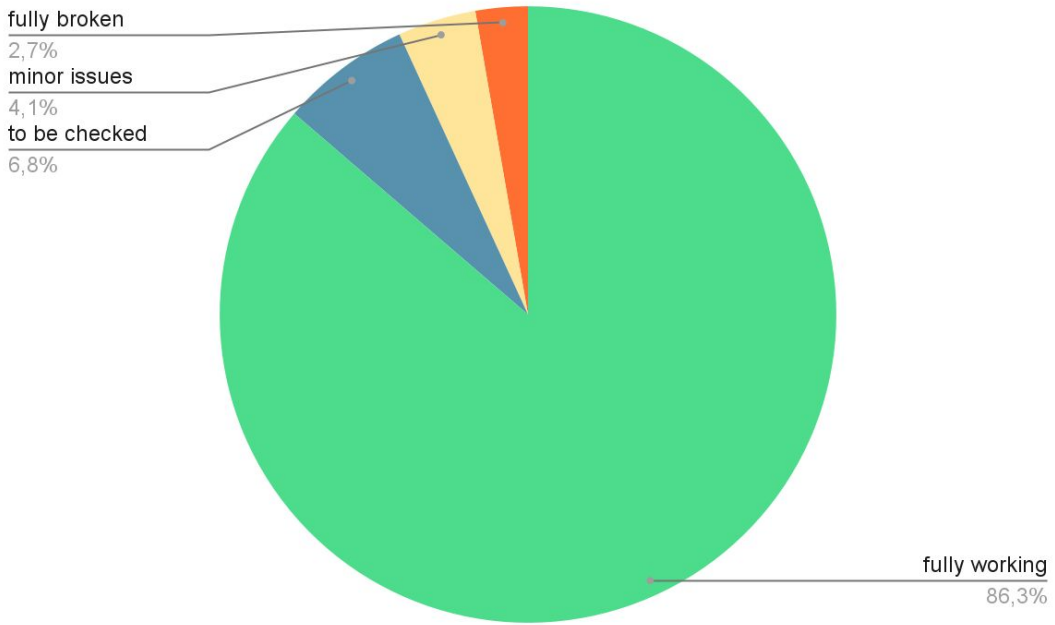


Full FEE summary

146 total cards produced:

- 126 fully working
- 10 to be checked
- 6 with minor issues
- 4 fully broken



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136 usable cards:

- 96 mounted at GANIL
- 11 as spare at GANIL
- 28 as spare at Firenze
- 1 as reference board at Korea University

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Up to 5 new blocks with spare FEEs available today

“Trittico” cards

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- Block card: data collection and clock synchronization
- Half bridge: high power voltage conversions (+48 V to +22 V and +5.5 V)
- Power supply: low power voltage conversions (+22 V to +13 V, -9 V, +5 V, -5 V)

- Historically maintained by Napoli division
- Now trying to sort them in Firenze

Block cards status

24 total card produced:

- 12 working and mounted @ GANIL
- 9 spare
- 3 with problems

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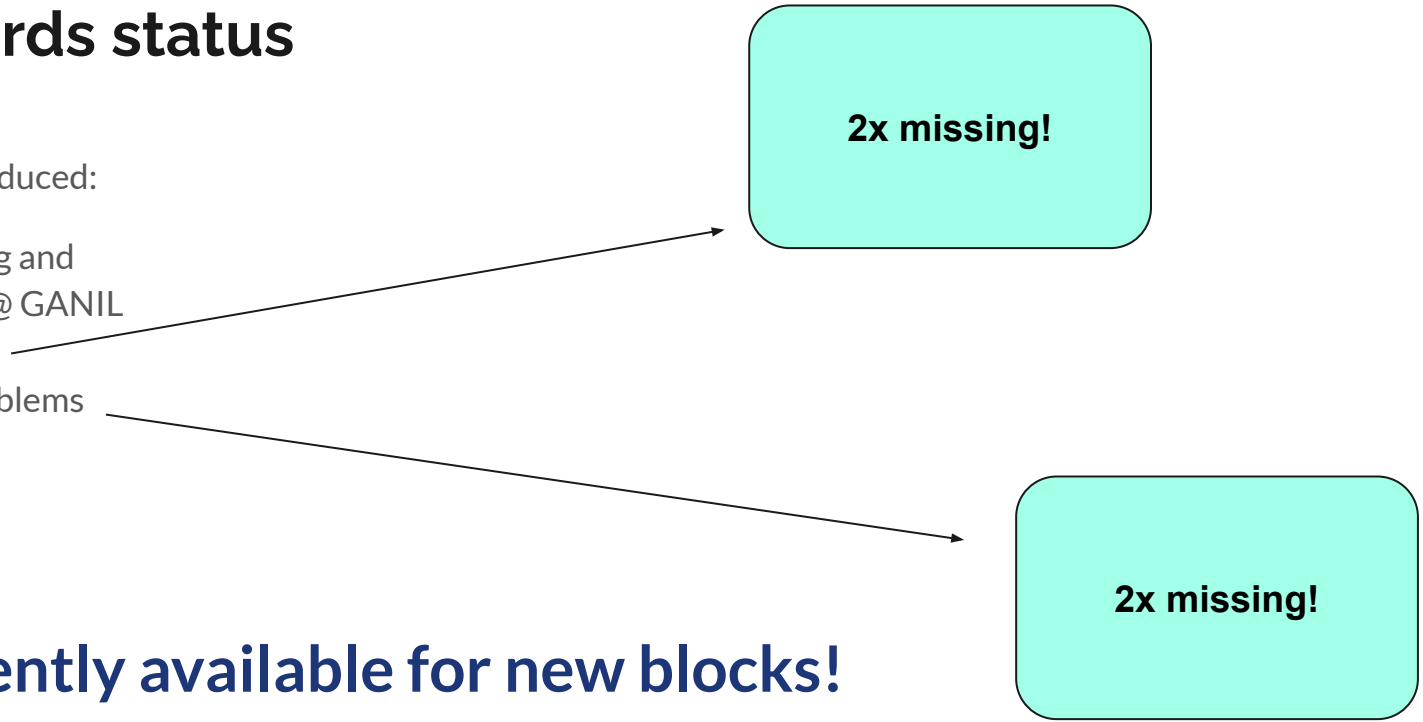

7 BC currently available for new blocks!

Half bridges status

21 total card produced:

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- 5 spare
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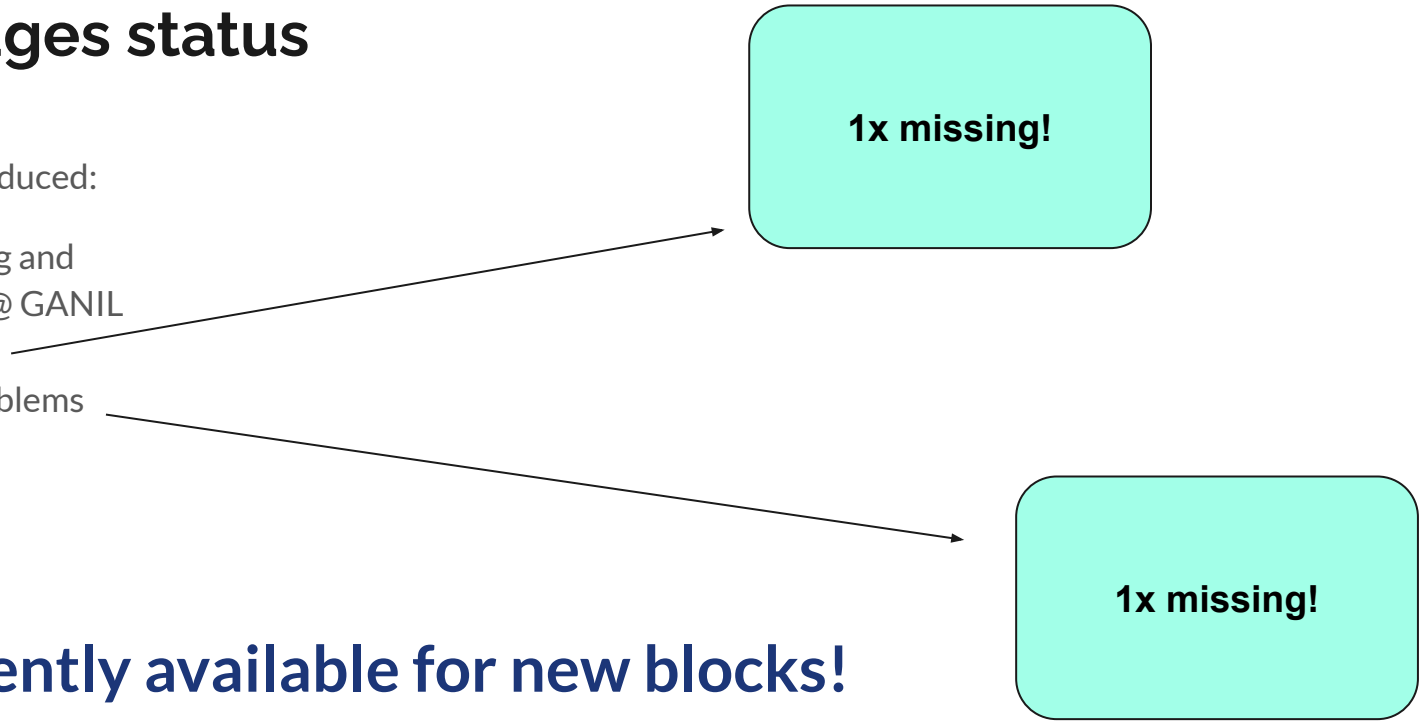

4 HB currently available for new blocks!

Half bridges status

21 total card produced:

- 12 working and mounted @ GANIL
- 5 spare
- 4 with problems

1x missing!

1x missing!

3 HB are currently under repair at AGE!

4 HB currently available for new blocks!

Power supplies status

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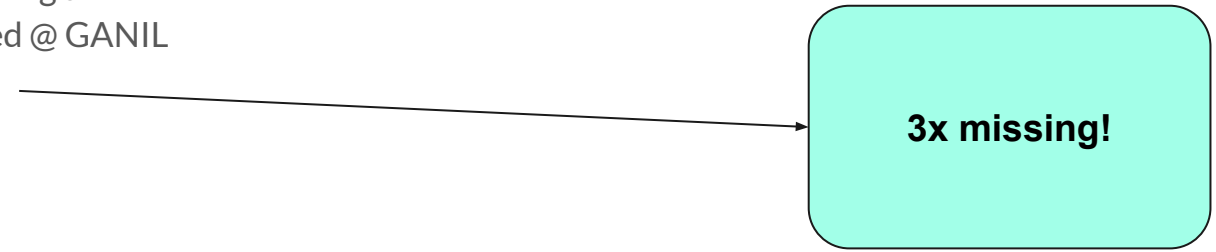

6 PS currently available for new blocks!

Missing cards must be found!

New trittico cards production

- Half bridge and power supply cards are easy to be produced (contacts already taken with AGE scientific)
- Block cards needs to be re-engineered since FPGA became obsolete!

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- Block card and RB communication must guarantee clock synchronization!
  - critical aspect in view of a new BC production!

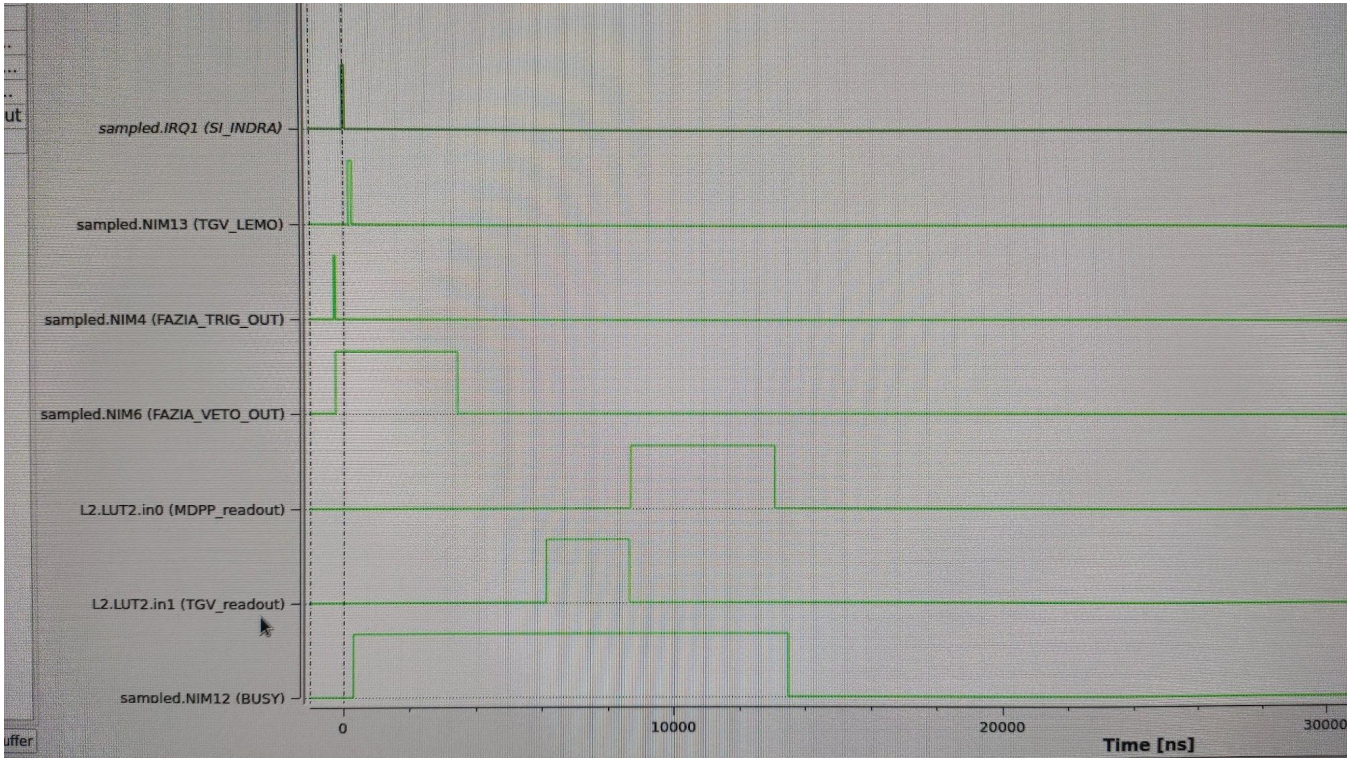
Regional Boards (and Test Cards)

Constantly updating firmware

- Regional board firmware can be easily updated in view of particular needs
- Lots of functionalities added in the last years:
  - Multi-IP data sending interface
  - Improved slow control state machine (multiple clients simultaneously allowed)
  - CENTRUM interface
  - Pt100 probe reading for temperature measurements

- Latest addition: trigger/veto signal synchronization with slow control registers

Test results @ GANIL (dec 2022)



TC and RB production

- 2x Test Card v1 (no more used)
- 2x Test Card v2: improved FPGA model
  - 1x sent to Korea University
- 2x Regional Board v1: increased transceivers number (up to 36 blocks!)
- 2x Regional Board v2: minor design improvements

- In view of a new production RB needs to be re-engineered since FPGA became obsolete!

- Regional board and BC communication must guarantee clock synchronization!
  - critical aspect in view of a new RB production!

Conclusions and perspectives

Short-term path (personal opinion)

Since (as INFN) we are in the period of the year when we ask for services, I think that we should really consider asking for help from Napoli Electronic Service (Alfonso Boiano) for 2024.

Alfonso could collaborate with MinJung, Jeonghyeok and Giyeong for a new production of Block Cards and/or Regional Board based on new FPGA models.

Critical point: new BC must be compatible with old RB and vice-versa

Open questions and conclusions

- A new run of FEE repairs could be done in 2023 or do we wait for more broken cards?
- Many efforts toward new FEEs (INHA, CENuM and Korea University)
- How many PS and HB do we need? We can easily produce them.
- We should start thinking to a new BC design considering FPGA obsolescence
- Do we have enough Regional Boards? We may design new ones together with new Block Cards!
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Thanks for your attention!