ASTRA:
Adaptable Silicon sTrip Read-out Asic

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ASTRA: Adaptable Silicon sTrip Read-out Asic

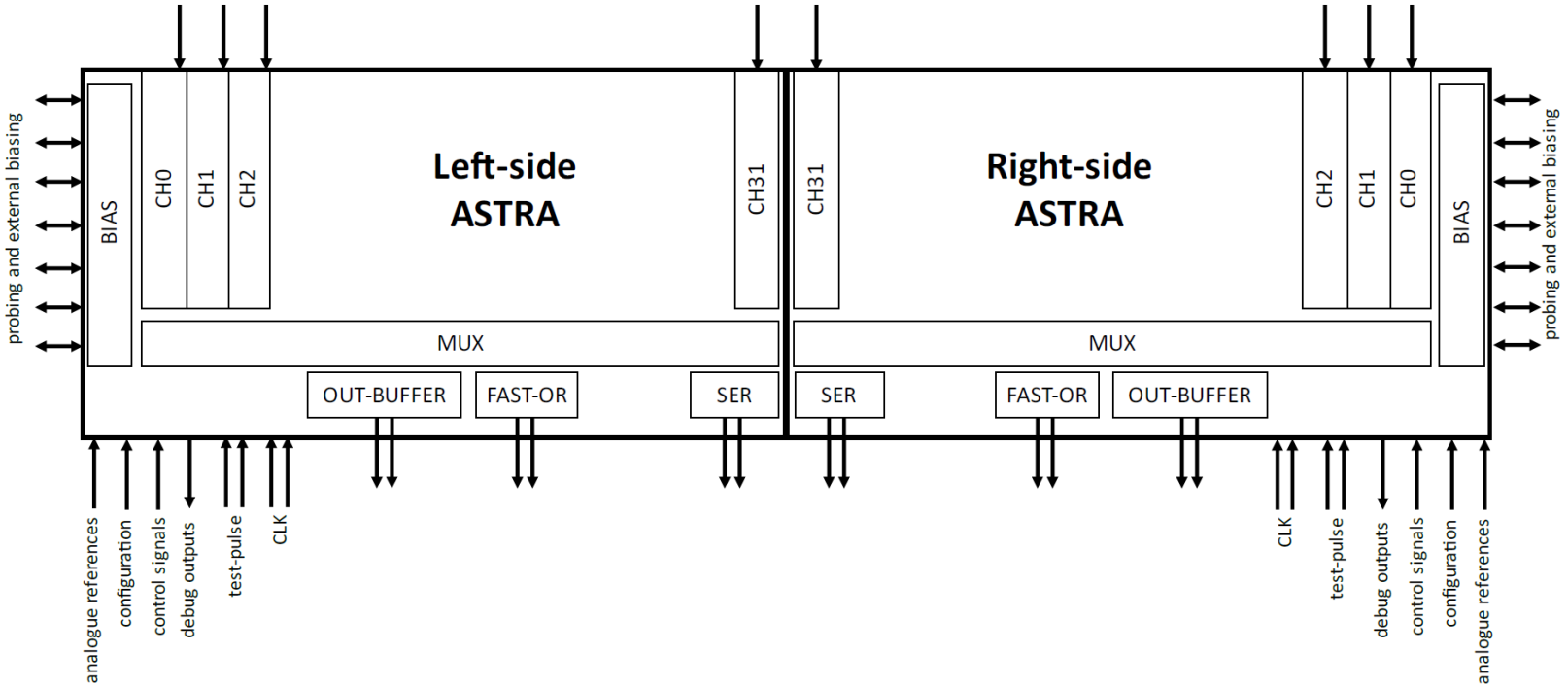
64-channel mixed-signal ASIC

- Designed to read-out micro-strip silicon detectors
  - Replace the commercial IDEAS IDE1140 ASIC

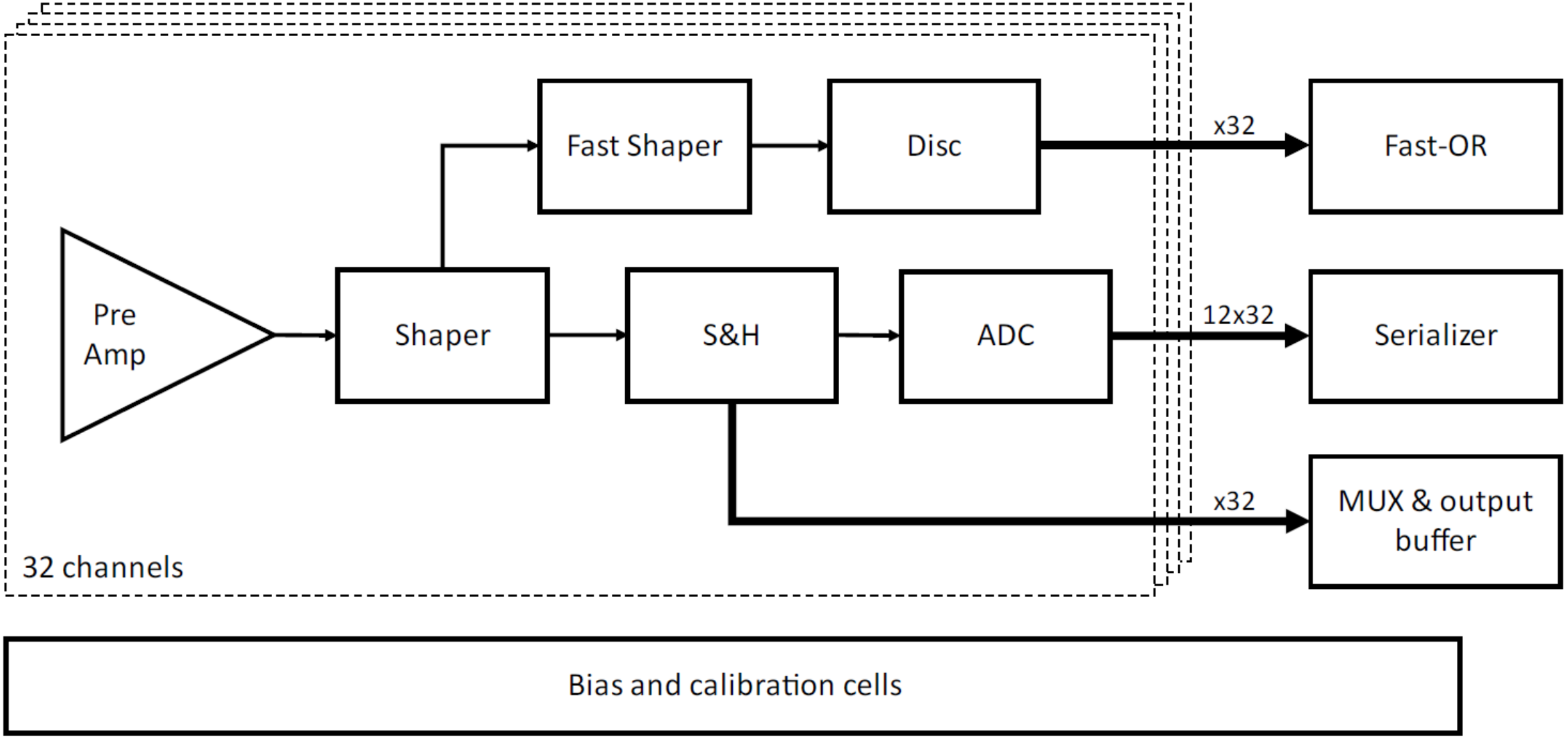
- Main Specs:
  - 64 channels
  - Same aspect ratio of the IDE1140
  - High Dynamic Range
  - Adjustable shaping time
  - Dual readout mode (analog and digital)
  - Auto-Trigger capability
  - Low Power consumption
  - Low Noise

ASTRA Architecture

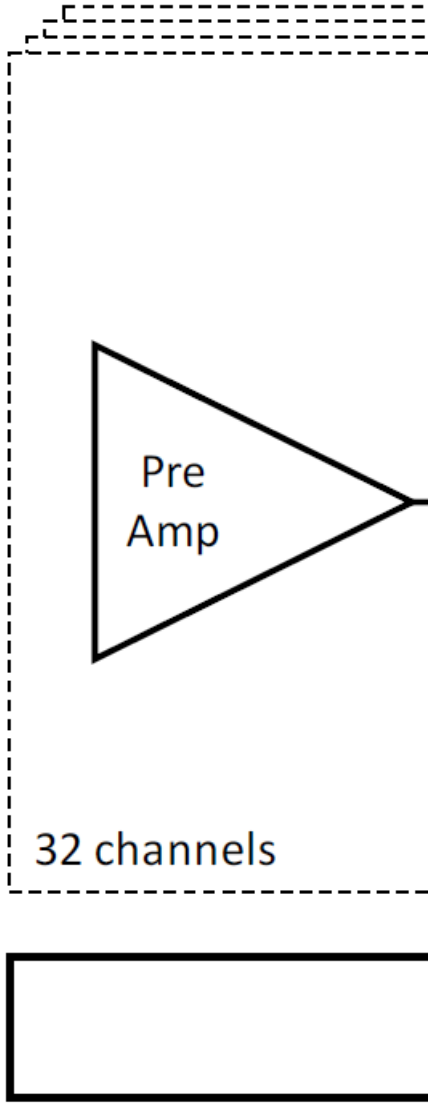
- Two identical mirrored blocks
  - 32 channels
  - Independent
    - Only share the power distribution
  - Analog and digital supply: 1.2 V
- Process: 110 nm
- Size: 8.0624 mm x 3.1 mm
  - Slightly wider than the IDE1140
    - 6.2 mm x 6.5 mm
  - Improved in version 2



One-Side Architecture

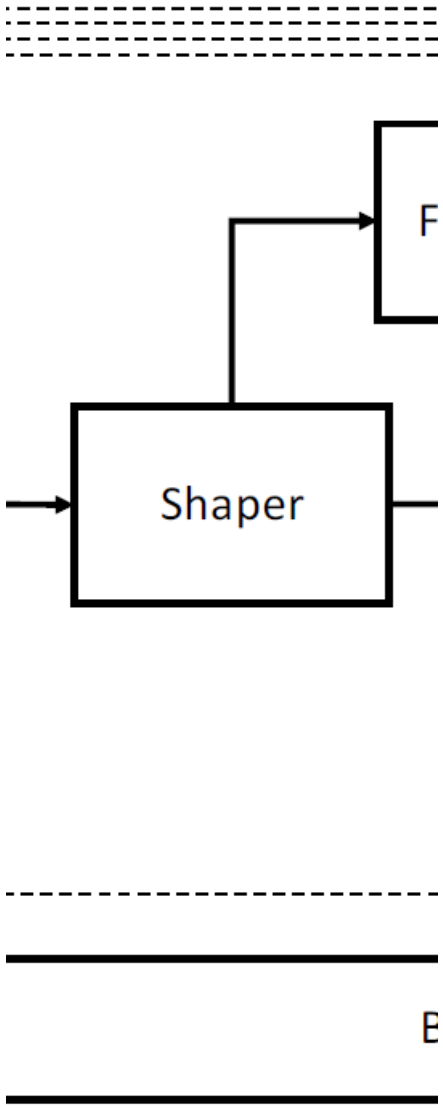


ASTRA Channels: Pre-Amp



- Charge-Sensitive Amplifier (CSA)
  - Pole-zero cancellation
  - Suitable for both input polarities
    - Inverting stage to adapt signal to the downstream modules
- 2 programmable gain configurations
  - Gain 4.2 mv/fC Input dynamic range: 1.6 - 160 fC
  - Gain 7.6 mv/fC Input dynamic range: 1 - 80 fC
- Test-pulse injection circuitry
  - Test the ASIC without detector

ASTRA Channels: Shaper

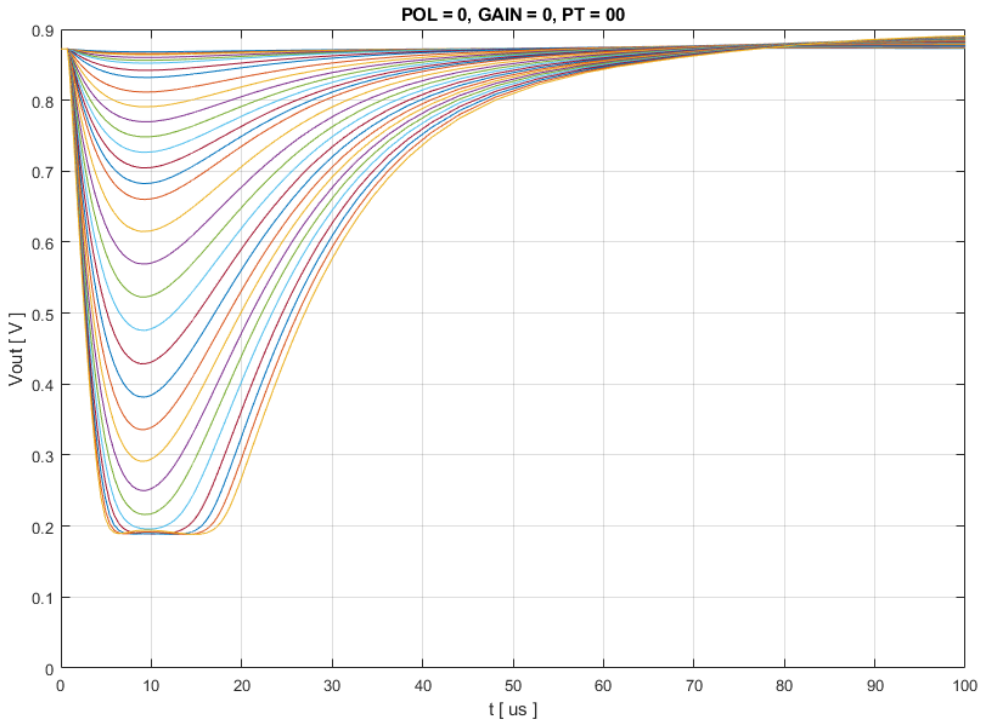


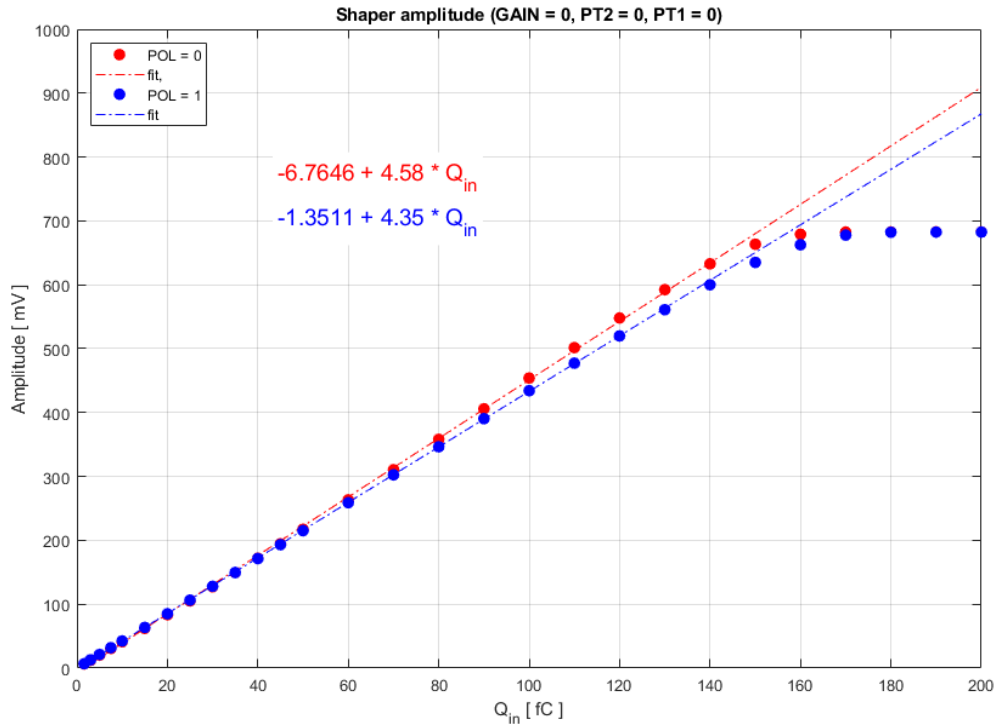
- CR-RC active shaper
- Programmable peaking time
  - 1.5 μs, 3.5 μs, 6.5 μs, 9.0 μs
- BaseLine Holder to define output DC
- 8 shaper output to dedicated pads for debug

Simulated Shaper output (Q_{in}=1.6 fC)

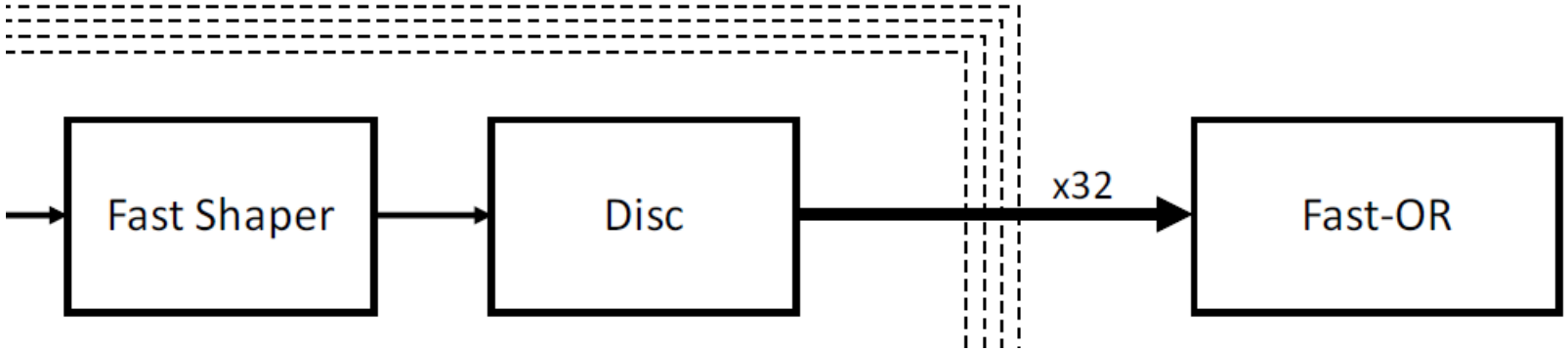
ASTRA Channels: Shaper

- Shaper response (simulated): standard gain, peaking time 9.0 µs



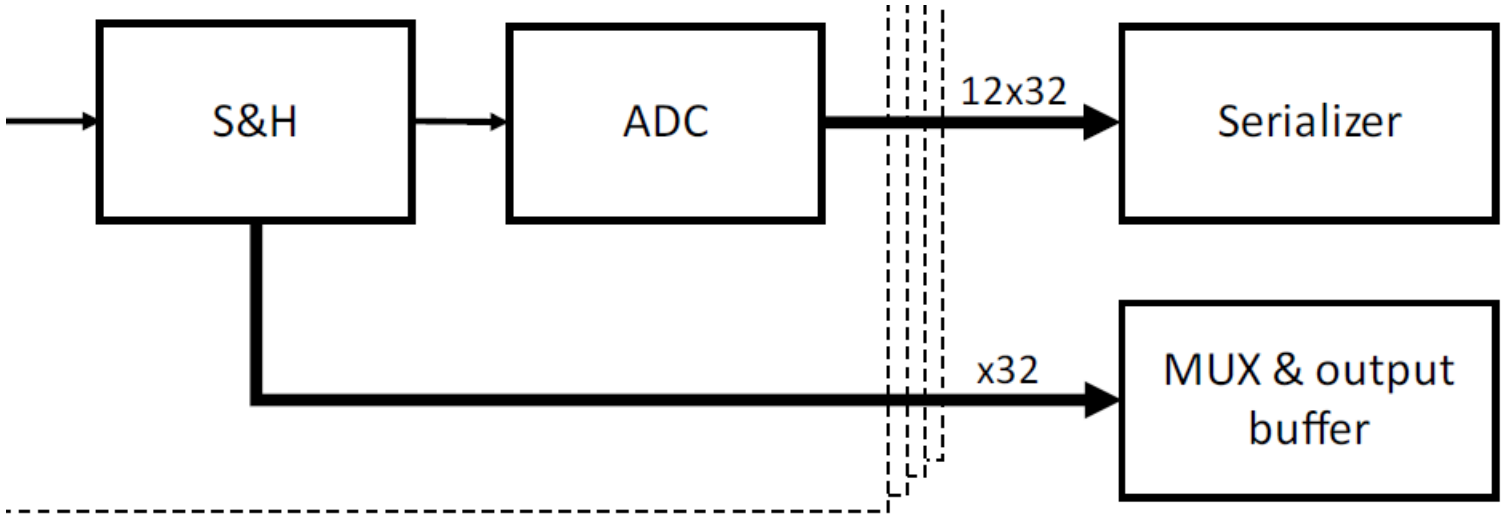


ASTRA Channels: Trigger out



- In parallel with readout, dedicated trigger chain
  - CR-RC active shaper with peaking time 800 ns
  - Differential amplifier as discriminator
  - The 32 channels feed a Fast-OR to have only 1 trigger port

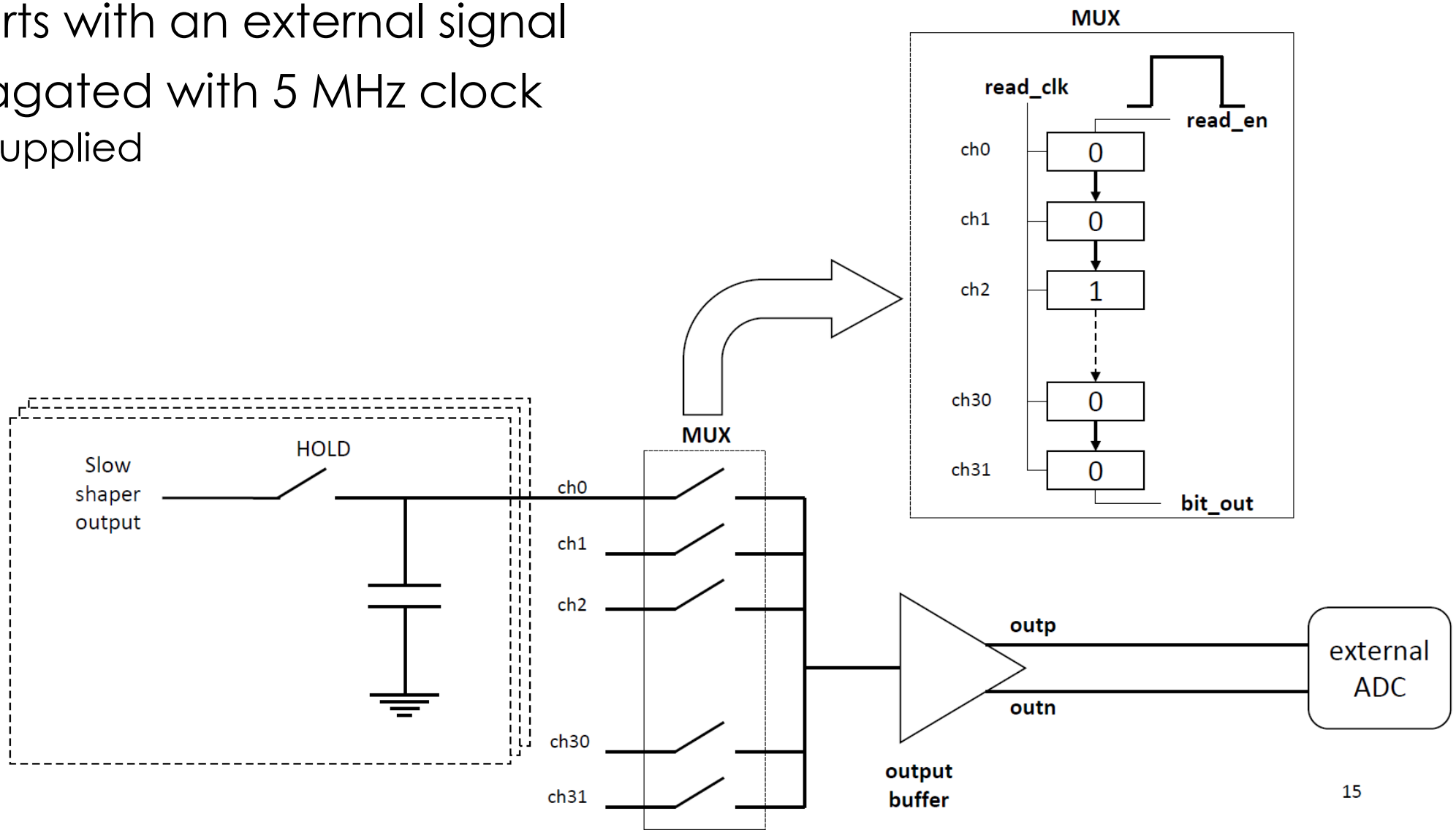
ASTRA Channels: Dual Output



- ASTRA embeds both analog and digital read-out mode
- They both use the S&H circuitry
  - Continuously samples the shaper output via a capacitor
  - Until the user asserts the HOLD signal

ASTRA Channels: Analog Read-Out

- Readout starts with an external signal
- Token propagated with 5 MHz clock
  - Externally supplied



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ASTRA Channels: Digital Output

- Wilkinson ADC
  - Programmable recharge current gives different number of bits
  - Output: Gray counter of the recharge time
    - Reduces noise and bit switches

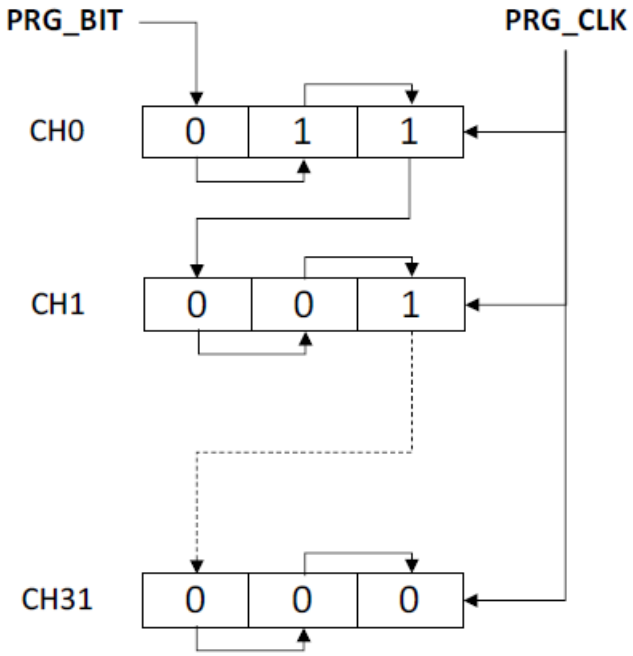
Current (nA)	Time (µs)	# bit
70	2.7	8
35	5.4	9
17	11.1	10
9	20.9	11
4.5	41.9	12

- 12-bit register + serializer
  - FastClock up to 100 MHz
  - Output: 16-bit register
    - ‘b1010_ADCdata
  - Data output at Double-Data-Rate
    - t_s= 80 ns -> t_{ro}= 2.56 µs

ASTRA Channels: Configuration

- Each channel has 3-bit configuration
  - ch_mask: masks the selected channel in readout
    - Mutes noisy channels
  - tp_en: enable the test-pulse injection circuitry
  - disc_en: enables the discriminator output
    - Prevent high-rate of triggers when there are noisy channels

- The user can write the configuration as a shift-register



ASTRA64 DAQ Block Diagram

Gb Ethernet

DAQ Board

ASTRA intf.

Hybrid Board

Electrical Interface

ASTRA

64x µStrips

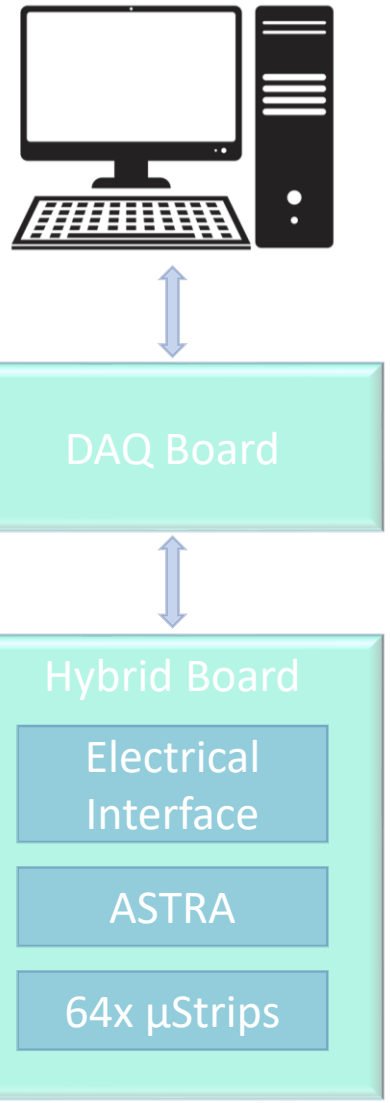
- DAQ Configuration
- DAQ Control
- ASTRA Configuration Parameters
- Long-Term storage

- ASTRA Control
- ASTRA Digital Readout
- ASTRA Analog Readout

- Host ASTRA
- Host 64-µStrip Detector
- Electrical Adaptation to the DAQ Board
- Digitization Chain for the ASTRA Analog Out

DAQ components

Acquisition PC



Non-specific PC running dedicated acquisition software

- Communicates via a Gigabit Ethernet port with the DAQ board

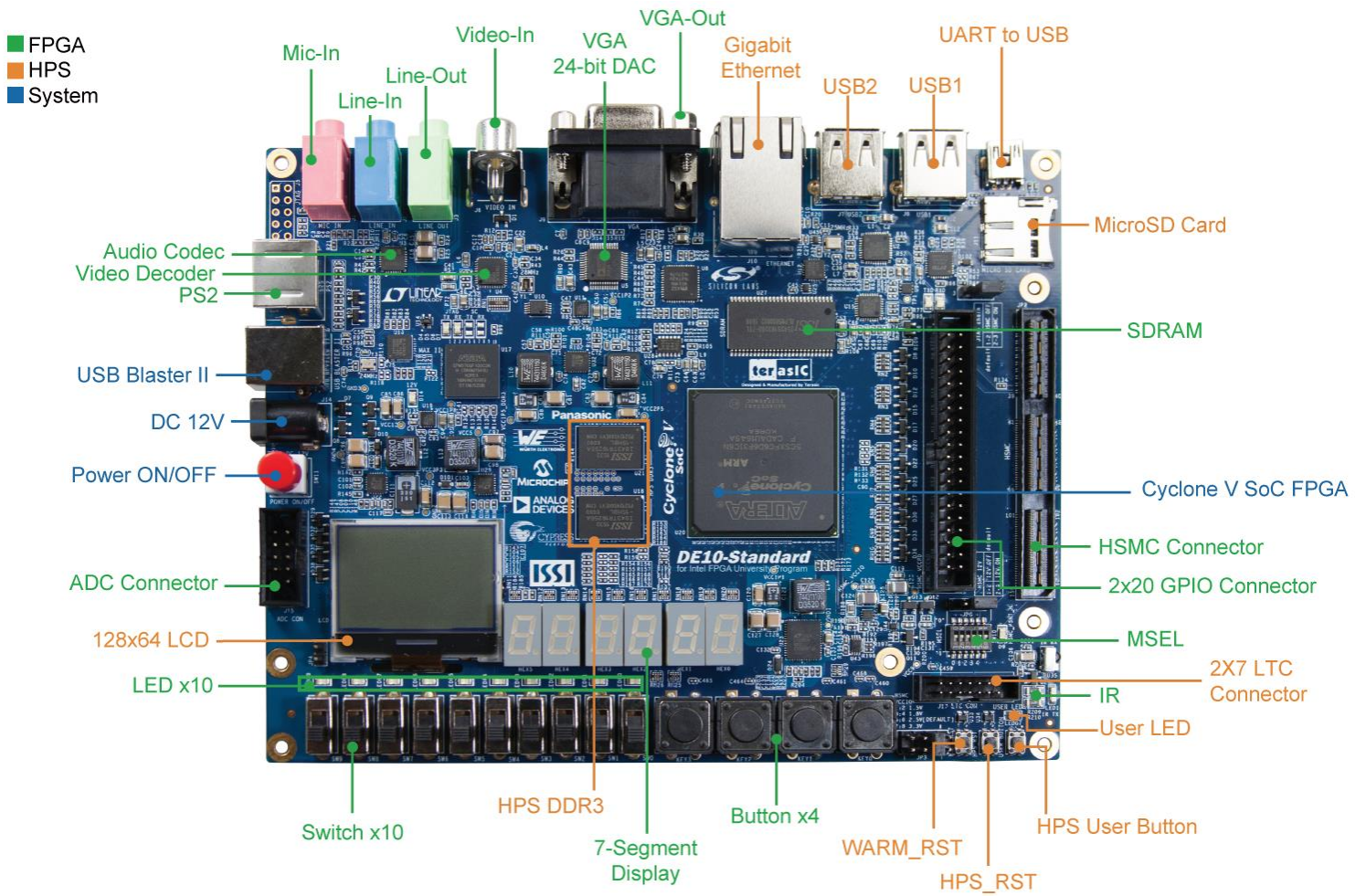
Multi-thread architecture for the DAQ interface

- Main
- Telemetries acquisition (low priority)
- Data Acquisition (high priority)

Possibly reuse pieces of software for data analysis and detector calibration developed for other experiments

DAQ components

DAQ Board: Terasic DE10-Standard



FPGA

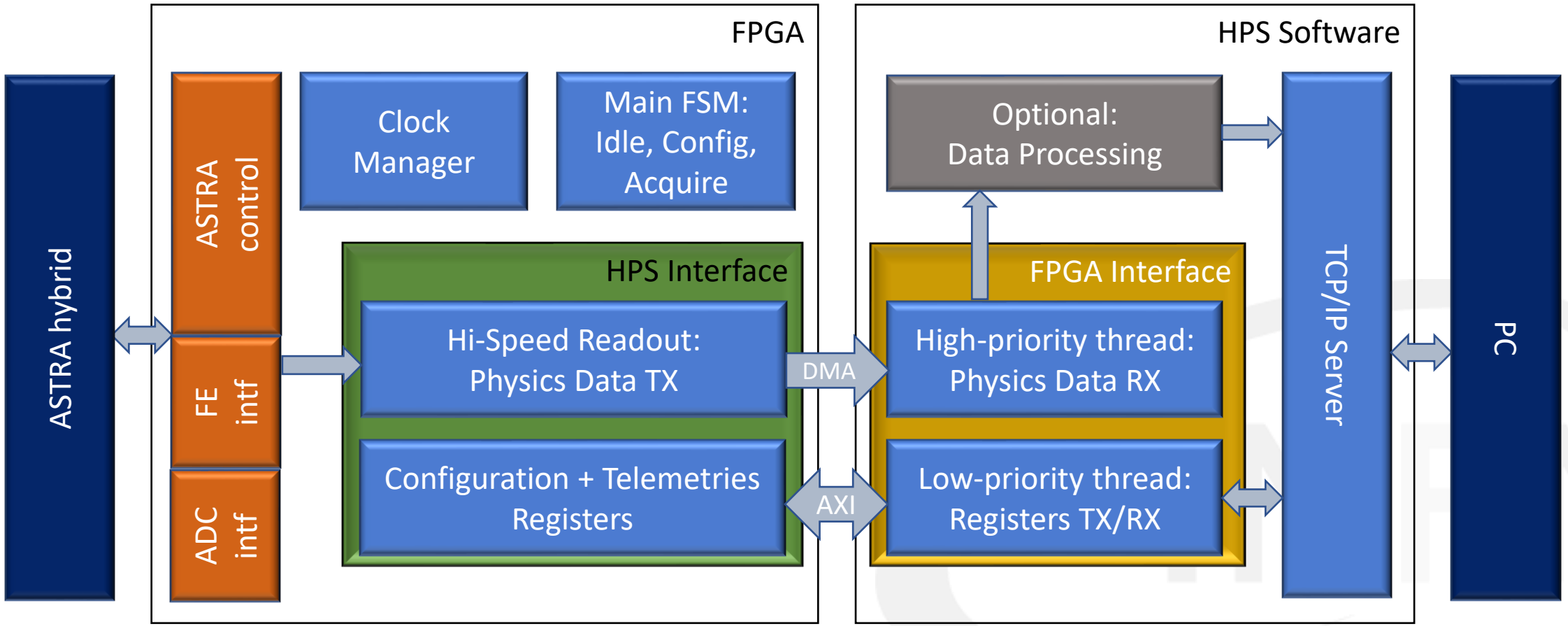
- 1x Intel Cyclone V 5CSX
- 1x HSMC with Configurable I/O standard 1.5/1.8/2.5/3.3
- 1x 40-pin expansion header
- 1x USB-Blaster II onboard for programming

HPS (Hard Processor System)

- 1x 925 MHz Dual-core ARM Cortex-A9 processor
- 1 GB DDR3 SDRAM
- 1 Gigabit Ethernet PHY with RJ45 connector

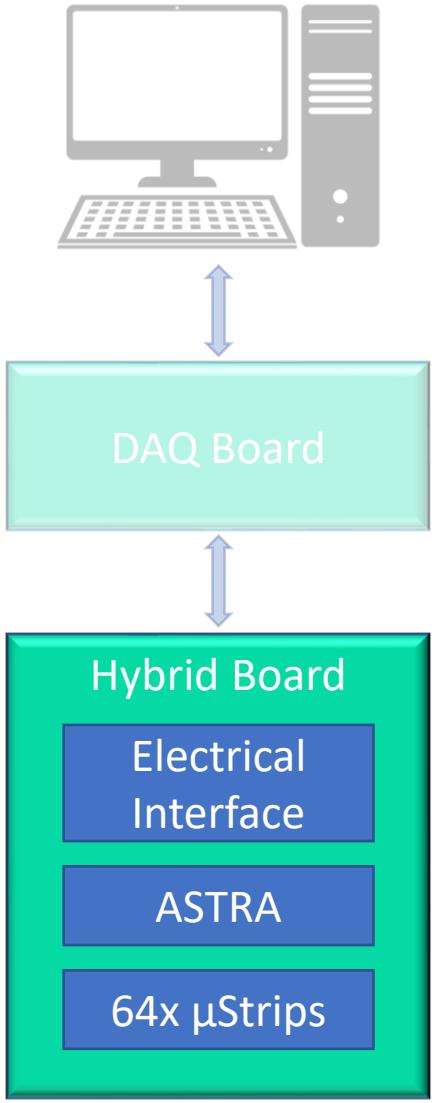
DAQ Board Architecture

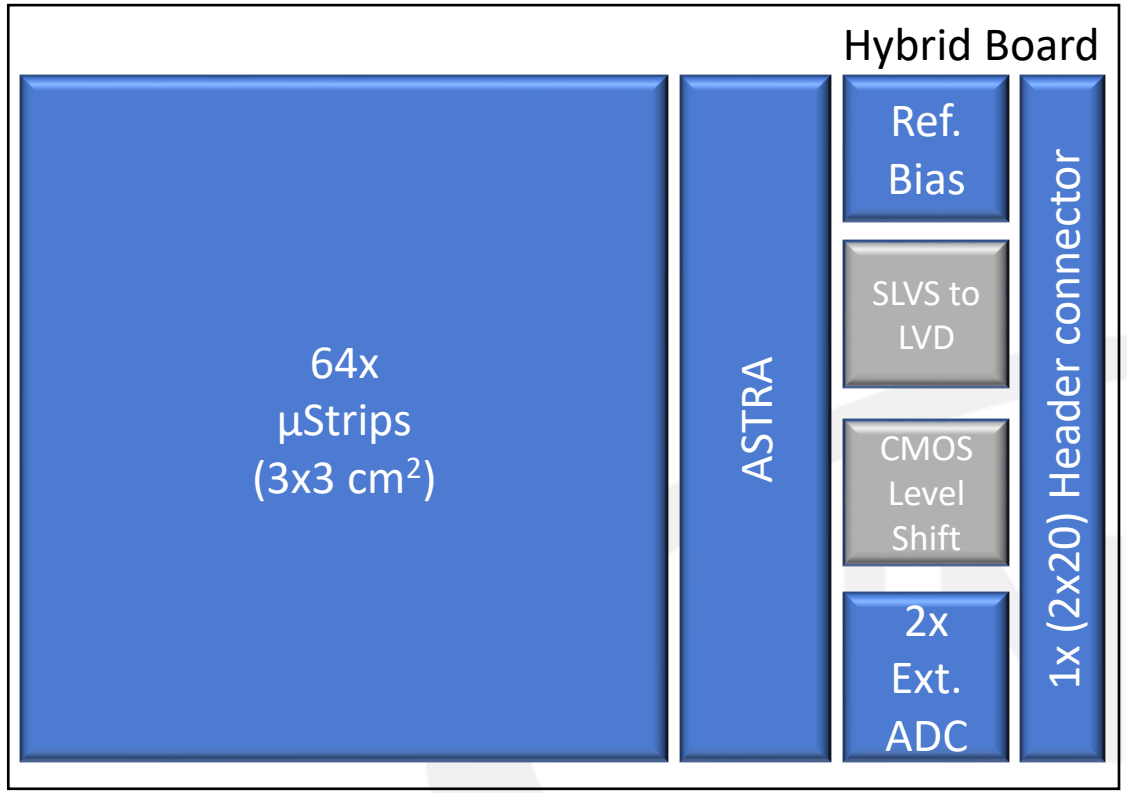
DAQ Board: A More Detailed Diagram



DAQ components

Hybrid Board: Block Diagram





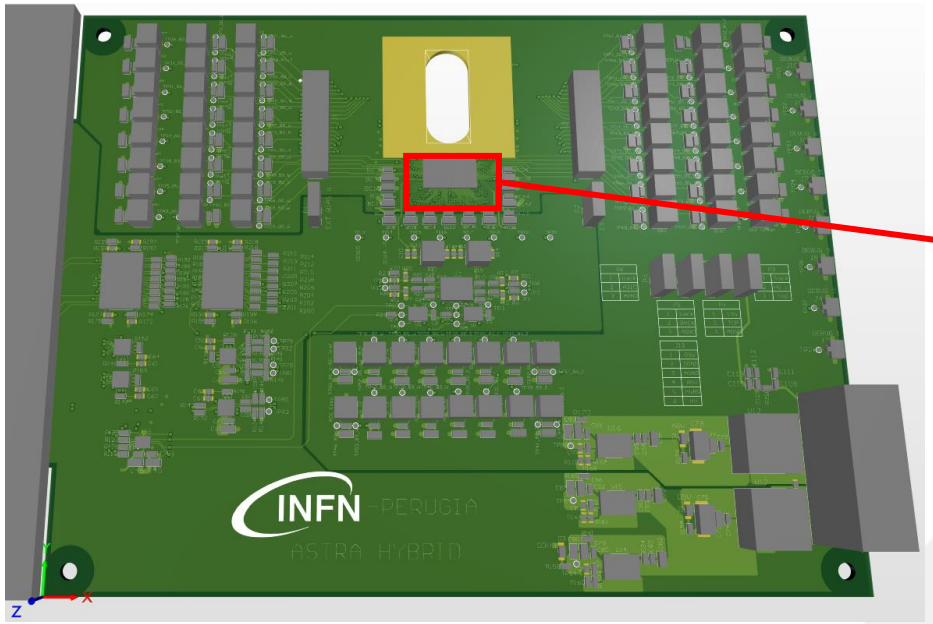
DAQ components

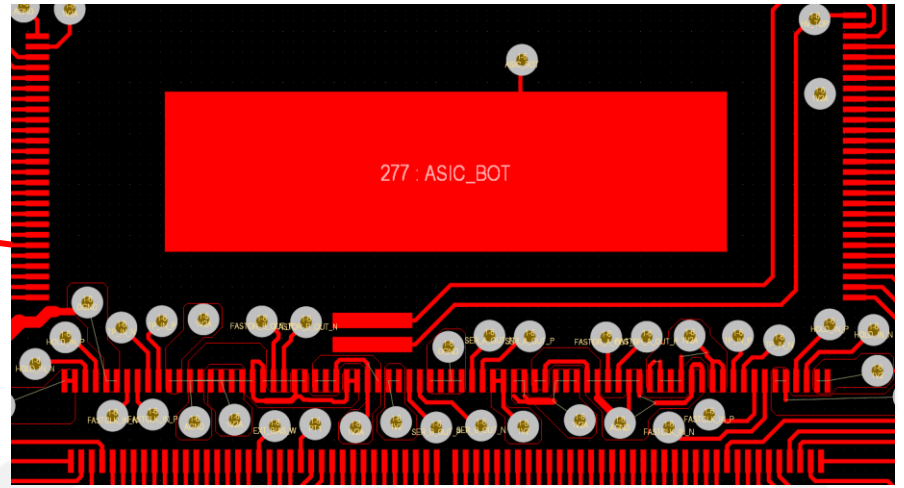
Hybrid Board: Block Diagram

DAQ Board

Hybrid Board

- Electrical Interface
- ASTRA
- 64x µStrips





Conclusions

ASTRA implements 64 channels read-out for microstrip :

- Same aspect ratio of the IDE1140 (with the V2 version)
- High Dynamic Range: 1-160 fC
- Adjustable shaping time: 1.5 μs, 3.5 μs, 6.5 μs, 9.0 μs
- Dual readout mode (analog and digital)
- Auto-Trigger capability
- Low Power consumption:
  - 630 μW/channel for analog readout
  - 830 μW/channel for digital readout
- Low Noise: < 1000 e^- for C_{in} = 100 pF

- With the DAQ, we are verifying and debugging the system