CAEN
Tools for Discovery

Digital Pulse Processing for Physics Applications

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- Introduction to Digitizers

- On-board Digital Pulse Processing (DPP)

  - DPP-PHA (Pulse Height Analysis) and its applications

  - DPP-CI (Charge Integration) and its applications

  - DPP-PSD (Pulse Shape Discrimination) and its applications

- In recent years, CAEN developed a complete family of digitizers

- Beside the use of the digitizers as waveform recorders ("oscilloscope mode"), CAEN offers the possibility to upload special firmware that implement several algorithms for Digital Pulse Processing (DPP)

- Digitizers running DPP firmware represent a complete digital replacement of most traditional acquisition chains

- From 2 to 64 channels
- Up to 5 GS/s sampling rate - Up to 14 bit
- FPGA firmware for Digital Pulse Processing

Acquisition mode: raw waveform vs DPP

STD FW

Acquisition Window

Threshold

INPUT

Trigger

EVENT DATA

| S1 |
| S2 |
| S3 |
| S4 |
| S5 |
| S6 |
| S7 |
| |
| Sn |

Typ. Nsample > 200

DPP FW

Leading Edge

INPUT

TRAPEZ → HEIGHT

SAMPLES

SUM → CHARGE

MEAN → BASELINE

TIMING FILTER

Threshold

Trigger

ZCROSS → TIME STAMP

EVENT DATA

| TIME STAMP |
| CHARGE or HEIGHT |
| (BASELINE) |
| (S1) |
| (S2) |
| (S3) |
| (S4) |

Typ. Nsample < 20

- Using digitizers as waveform recorders can produce a large amount of data to be transferred from the acquisition board to a mass storage device

- The data throughput can be extremely high: it may be no possible to transfer raw data to computers and make the analysis off-line!

- On-line Digital Pulse Processing is needed to extract only the information of interest reducing the data throughput

- The aim of the DPP is to provide FPGA algorithms able to make in digital the same functions of analog modules such as Shaping Amplifiers, Discriminators, QDCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

- Three main DPP firmware have been developed so far:

  DPP-PHA (Pulse Height Analysis)

  DPP-CI (Charge Integration)

  DPP-PSD (Pulse Shape Discrimination)

DPP-PHA
PULSE HEIGHT ANALYSIS
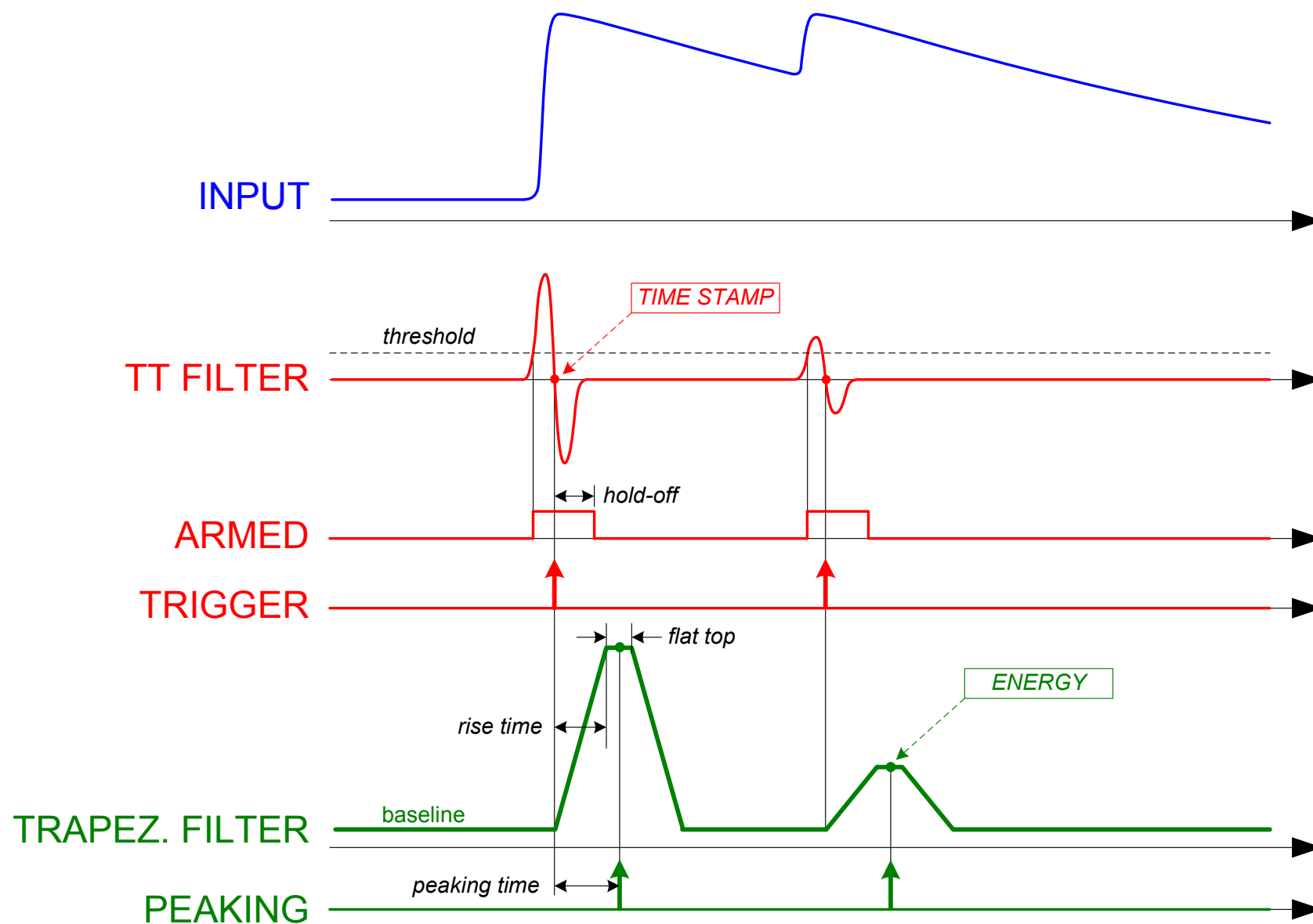
- Digital implementation of the Shaping Amplifier + Peak Sensing ADC (Multi-Channel Analyzer)

- Charge Sensitive Preamplifier directly connected to the digitizer

- Implemented in the 14 bit, 100MS/s digitizers (mod. 724)

- Provides pulse height, time stamp (10ns) and optionally raw data

- Pile-up rejection, Baseline restoration, Ballistic Deficit correction

- Low dead time => high counting rate (up to 1Mcps)

- Best suited for high resolution spectroscopy (HPGe and Si detectors)

- Also suitable for homeland security and biomedical applications

- Can work with segmented detectors (synchronizations, coincidences and neighbour triggering)

- Unlike the analog chain, in the DPP-PHA there is no conversion time

- The A/D conversion and the pulse processing is always alive; dead time in the energy filter is only given by the inability to calculate the enery due to trapezoid overlap (ΔT < Trise + Tflat)

- Although pile-up causes the loss of energy values, the timestamps is given for almost all pulses: therefore, the true rate can be calculated

- *DeadTime = RealTime * (1 - Energy Count / Time-Stamp Count)*

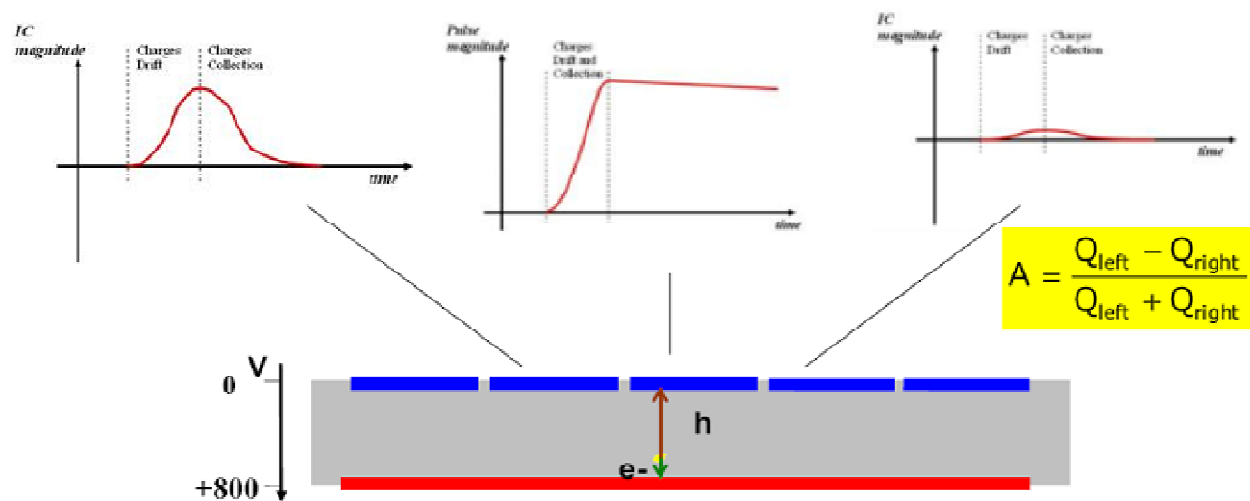- Double pulse resolution ≈ Rise Time (two pulses separated by at least the pulse rise time can be distinguished)
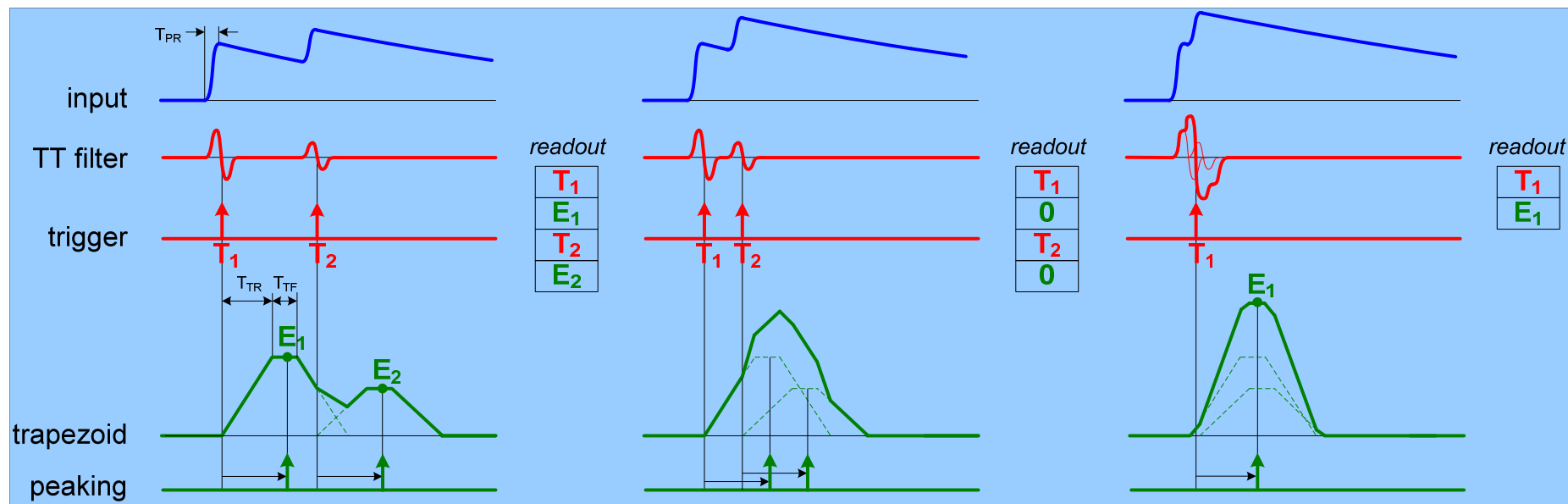
• The **Rise Time Discriminator** allows double pulses piling up on the rising edge to be detected and counted twice (the relevant energies are discarded)

• Residual multiple pulses that cannot be distinguished (despite the RTD) can be counted on a statistical basis
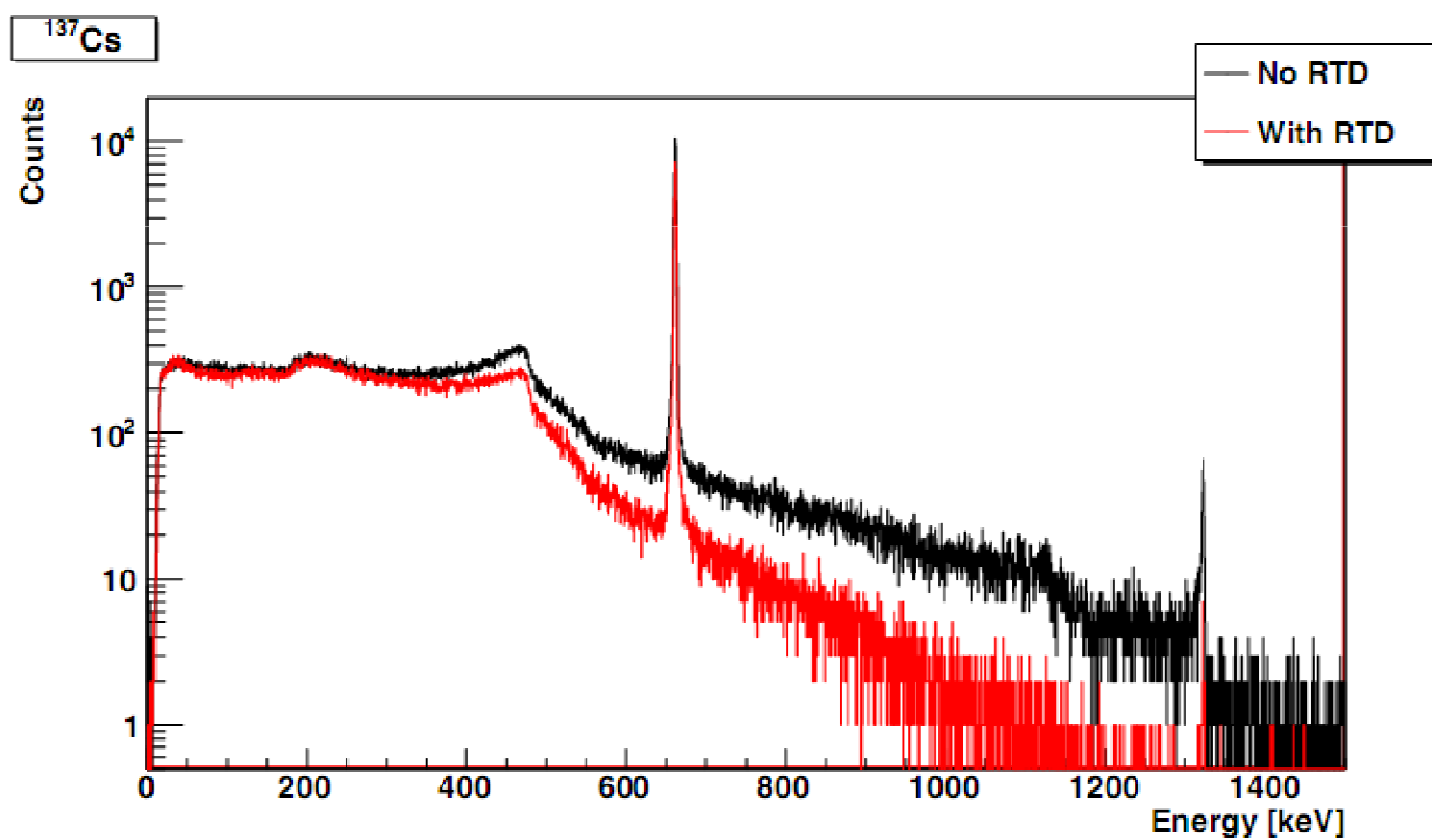
- Feature developed for the project *ProSPECTus* (Compton camera)

- Mainly needed in segmented or clove detectors

- One channel triggers itself and also neighbour channels (also from board to board)

- Individual TRG-IN and TRG-OUT lines from each channel to the Front Panel GPIO connector (8 inputs + 8 outputs)

- External trigger unit (V1495) for the coincidence matrix implementation

$$A = \frac{Q_{left} - Q_{right}}{Q_{left} + Q_{right}}$$

Segmented HPGe

V1724 digitizers with DPP-PHA

V1495 with ad hoc Trigger Logic