ALCOR and packaging

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3rd ALCOR for EIC @ Ferrara - 24.05.2023


1
42
43
82
ALCOR
version 1
4.95 mm × 3.78 mm
(before optical scaling: 5.4942 mm x 4.1944 mm)
http://personalpages.to.infn.it/~fcossio/projects/ALCOR/ALCOR_user_guide.pdf
83
126

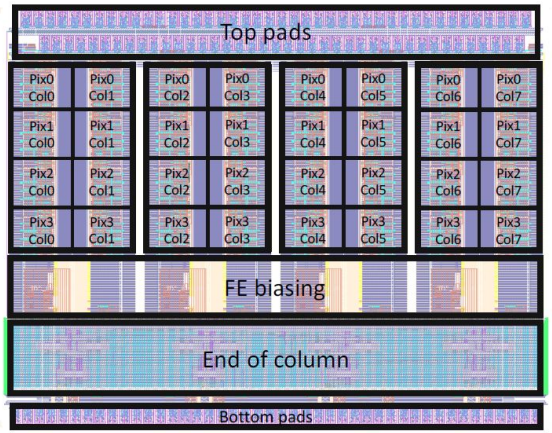
ALCOR I/Os

ANALOGUE (top)

- 16 AVDD + 4 AVDD_IO
- 16 AGND + 4 AGND_IO
- 4 AVSS

- 32 inputs
- 4 debug outputs
- 2 bias Vref

TOTAL = 44 + 38 = 82



DIGITAL (bottom)

- 6 DVDD + 2 DVDD_IO
- 6 DGND + 2 DGND_IO
- 4 DVSS

- 8 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

TOTAL = 20 + 24 = 44

ALCOR current version has 32 channels and 126 I/Os

ALCOR-64 I/Os

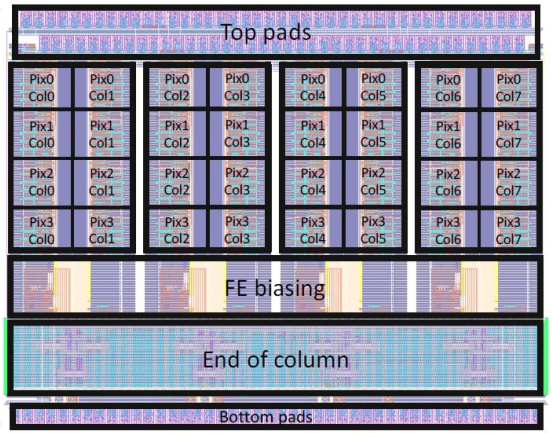
ANALOGUE (top)

- 32 AVDD + 8 AVDD_IO
- 32 AGND + 8 AGND_IO
- 8 AVSS

- 64 inputs
- 4 debug outputs
- 2 bias Vref

TOTAL = 88 + 70 = 158

2x



DIGITAL (bottom)

- 12 DVDD + 4 DVDD_IO
- 12 DGND + 4 DGND_IO
- 8 DVSS

- 16 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

TOTAL = 40 + 32 = 72

ALCORv3 64-channel version with 230 I/Os

Towards ALCOR-64

All sizes must be scaled by 0.9

Max size = 5.5 mm → 4.95 mm (0.9x scale factor)

ALCOR-32 dimensions (4.95 mm × 3.78 mm)

- **Pixel size**: 488.89 µm x 488.89 µm
- **Horizontal pixel pitch**: 1350/2 µm = 675 µm
- **Vertical pixel pitch**: 488.89 µm
- **EoC_bias height**: ~555 µm
- **EoC height**: ~800 µm
- **Serializer height**: ~120 µm
- **Padframe height**: 165 µm (ESD → 90 µm)
- **Padframe pitch**: 120 µm

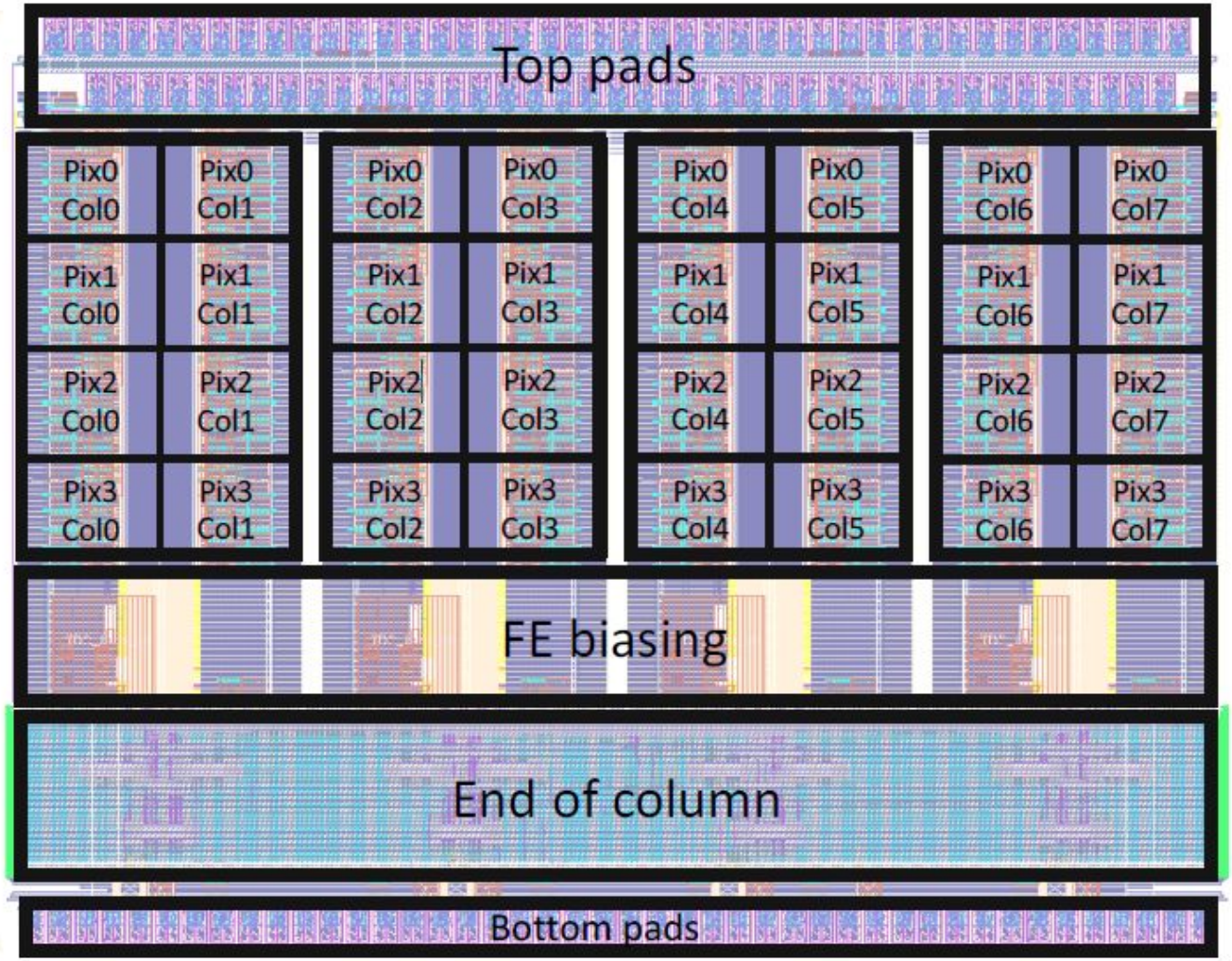
➢ **8 columns pixel height** = 488.89 µm x 8 = 3911.12 µm

➢ **pixel column + EoC** = 3911.12 µm + 555 µm + 800 µm + 120 µm = **5386.12 µm**

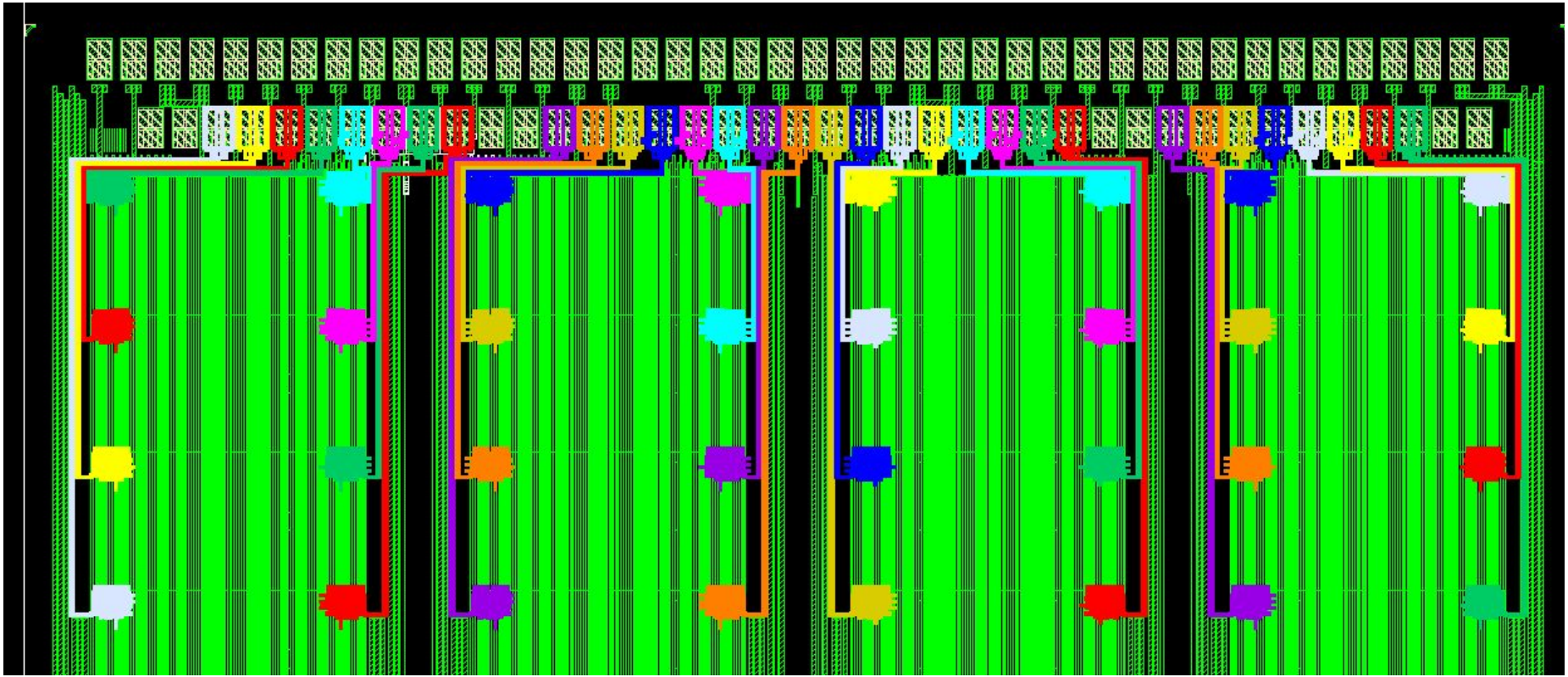
★ No space for padframe → we need to increase chip height above 5 mm

ALCOR-32

Space between each sector is used to route the pixels input to the Top pads and for decap capacitance



ALCOR-32



ALCOR-64 wire-bond version (8x8 matrix)

Top side padframe is already staggered (2 rows)

- ❏ need to find where to put extra inputs and P/G pads
- ❏ need to to route input pads to input pixels

Only way seems to place padframe also on both sides of ALCOR to provide extra pads for:

- external columns pixel inputs (8 + 8)
- Power and Ground

★ <u>This implies that also the chip width will be > 5 mm</u>

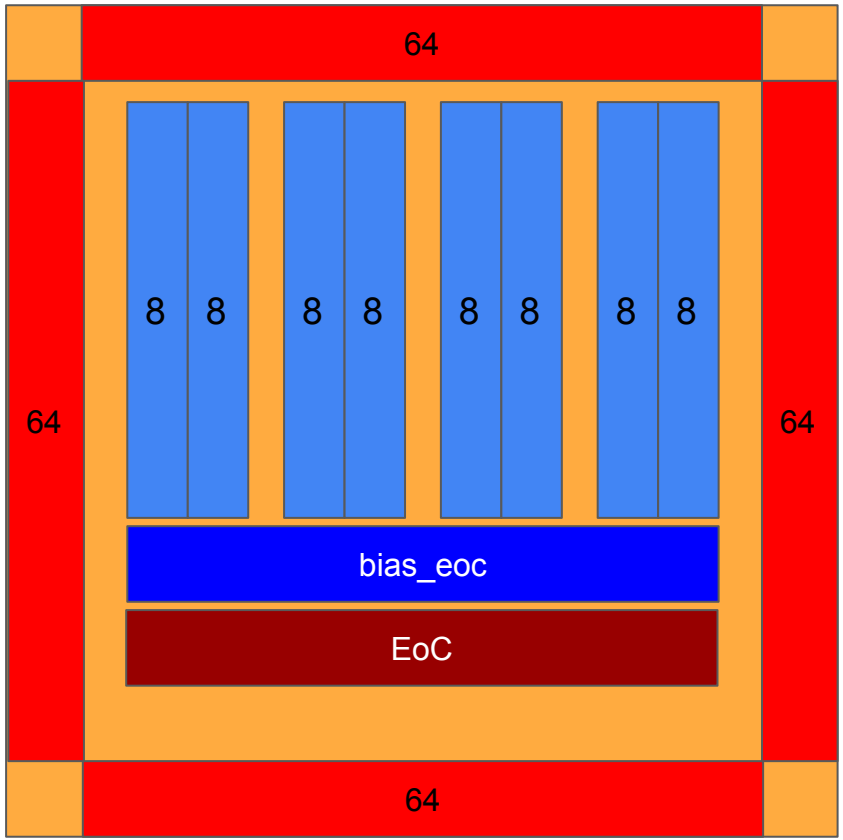
ALCOR-64 wire-bond version (8x8 matrix)

TOP (64)

- 48 inputs
- 8 AVDD
- 8 AGND

EAST/WEST (51)

- 8 inputs
- 12 AVDD
- 12 AGND
- 4 AVDD_IO
- 4 AGND_IO
- 4 AVSS
- 2 debug outputs
- 1 bias Vref
- ----------
- 2 DVDD
- 2 DGND



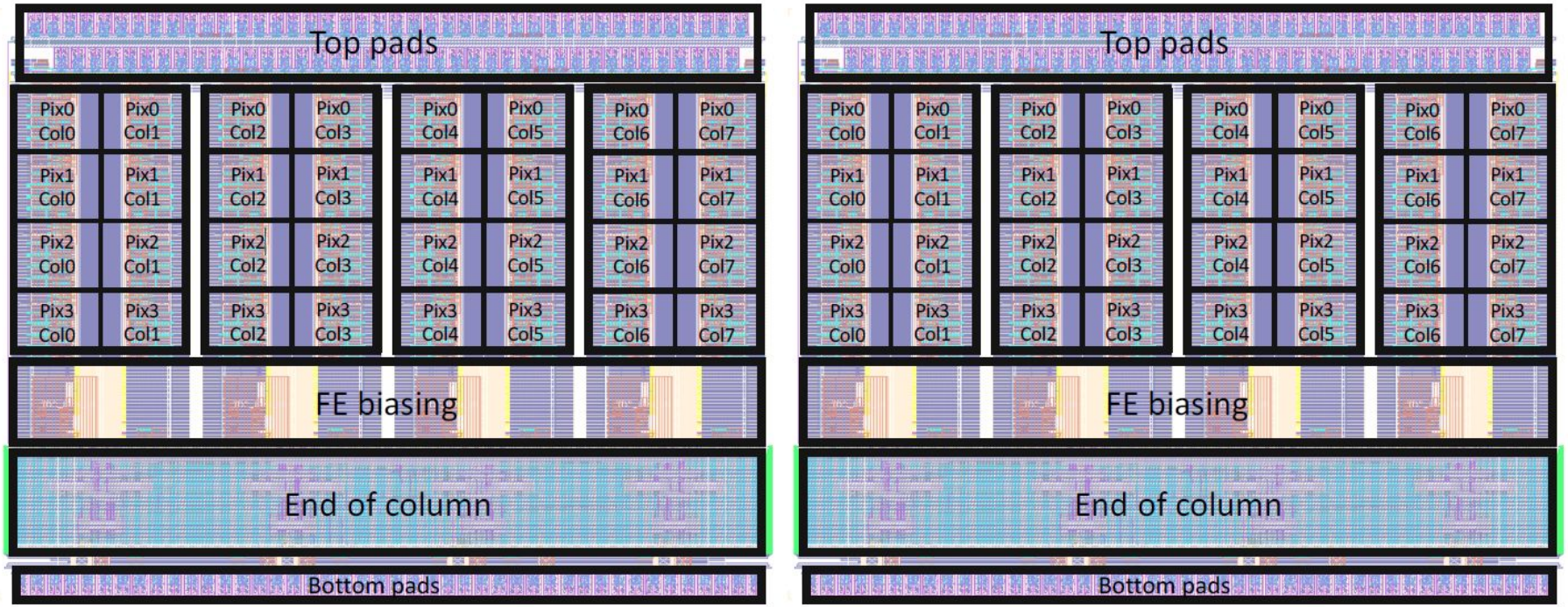
BOTTOM (64)

- 8 DVDD
- 8 DGND
- 8 DVSS
- 4 DVDD_IO
- 4 DGND_IO
- 16 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

Y > 5 mm due to increased number of pixels per column

X > 5 mm due to added padframe (and higher number of input interconnections)

ALCOR-64 wire-bond version (4x16 matrix)



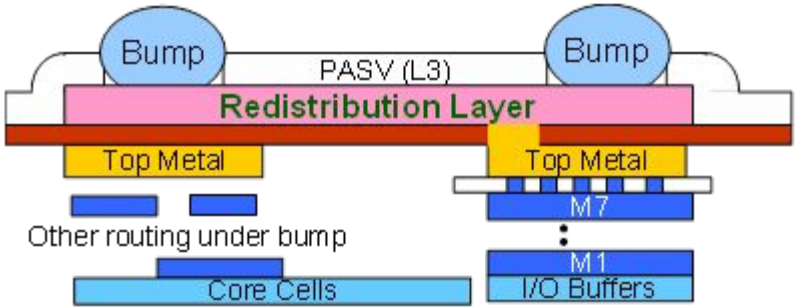
X ~ 10 mm *vs* Y < 4 mm

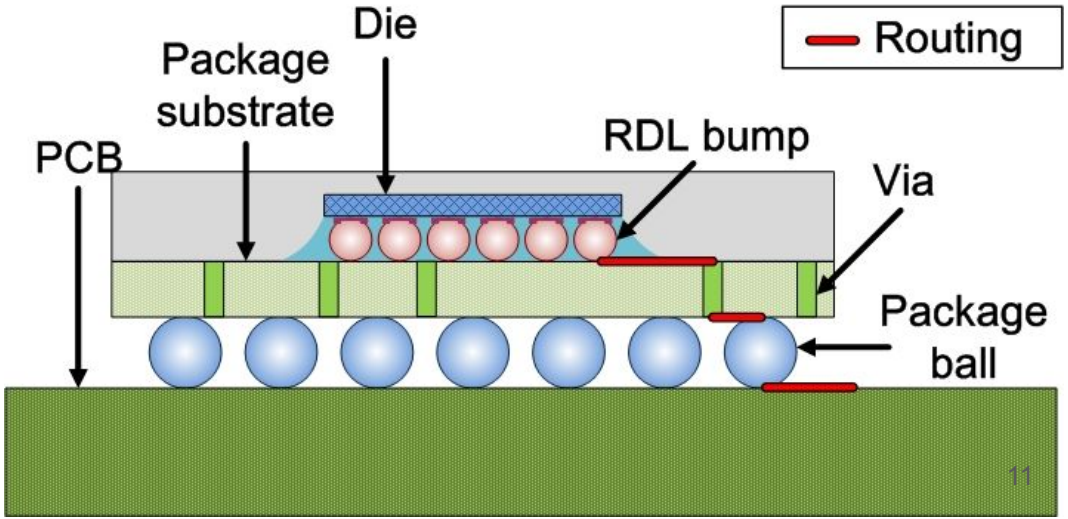
Flip-chip BGA packaging

➔ Reduces chip area while supporting more IOs
➔ Reduces inductance, allows high-speed signals, and carrys heat better.

RDL (redistribution layer): extra metal layer connecting IO pads and bump pads, which are usually placed in a grid pattern

➢ **BGA package, 256 pins, flip-chip**
- 16x16 bump bond matrix
- 8x8 pixel matrix



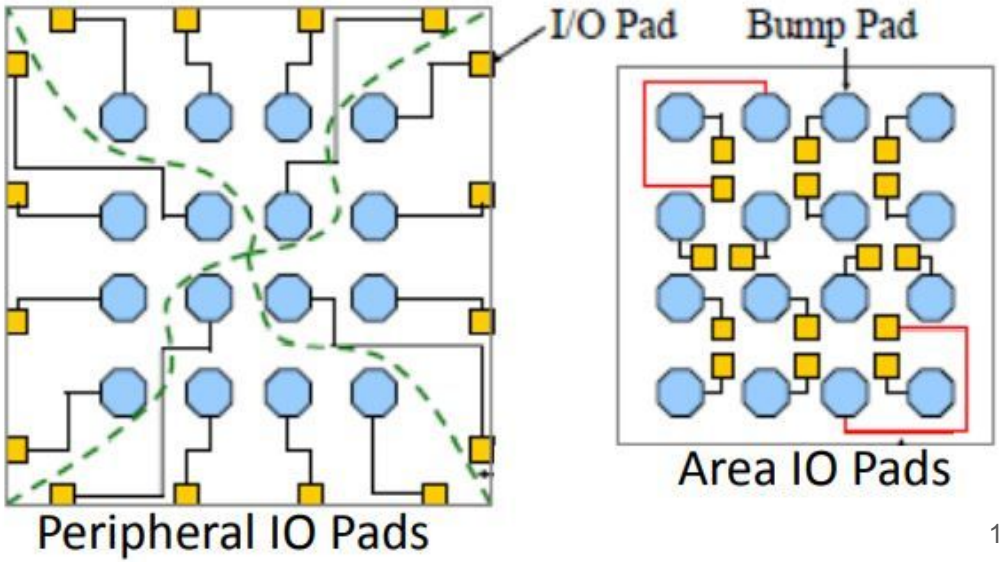


Flip-chip BGA packaging

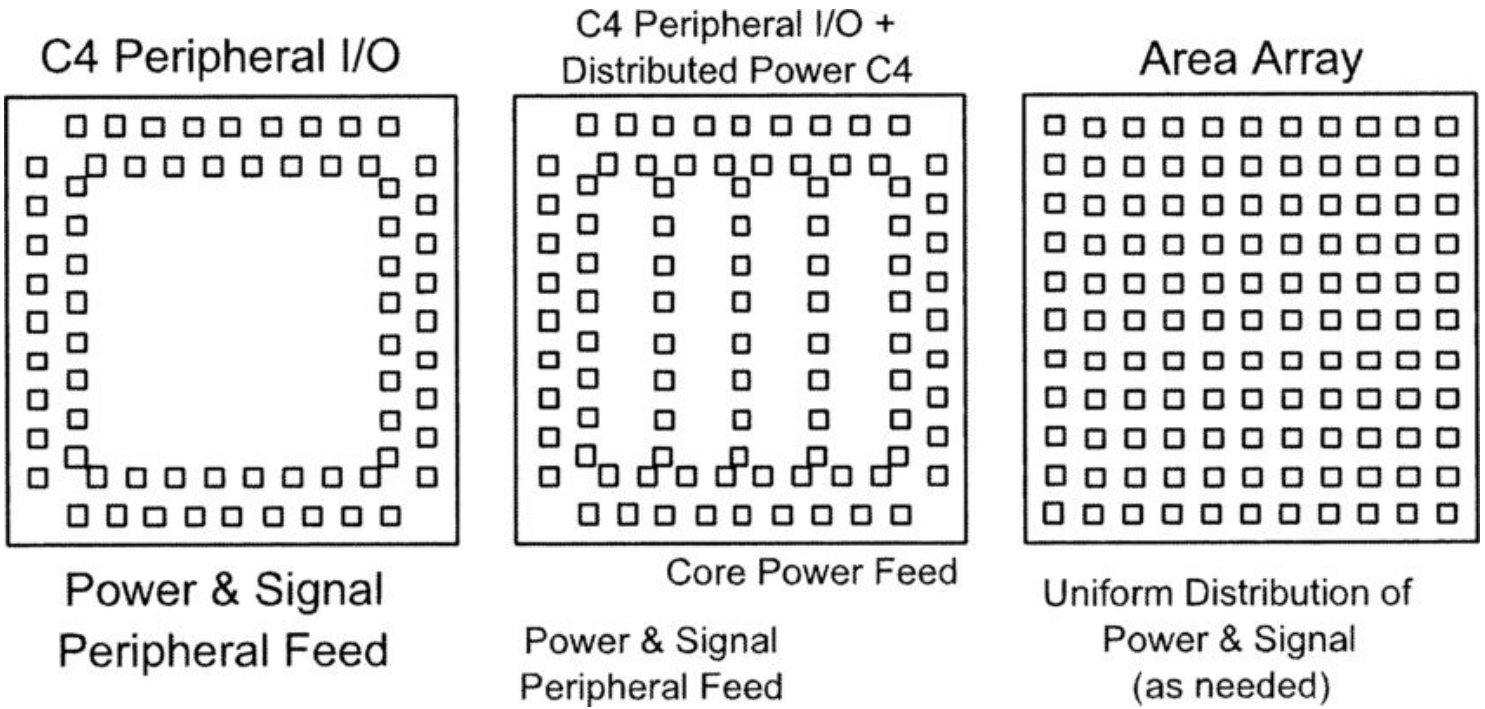
Bump pads: pads to be connected to package interposer, usually placed in a grid pattern

IO pads: pads providing connection to core cells of the chip, provide also ESD protection, geometry can be *peripheral* (wire-bond like) or *area*

RDL: extra metal layer (inside the ASIC) connecting IO pads and bump pads



Flip-chip BGA packaging



ALCOR-64 bump-bond version (Area I/O)

TOP (42)

- 16 AVDD
- 16 AGND
- 6 AVSS
- 2 AVDD_IO
- 2 AGND_IO

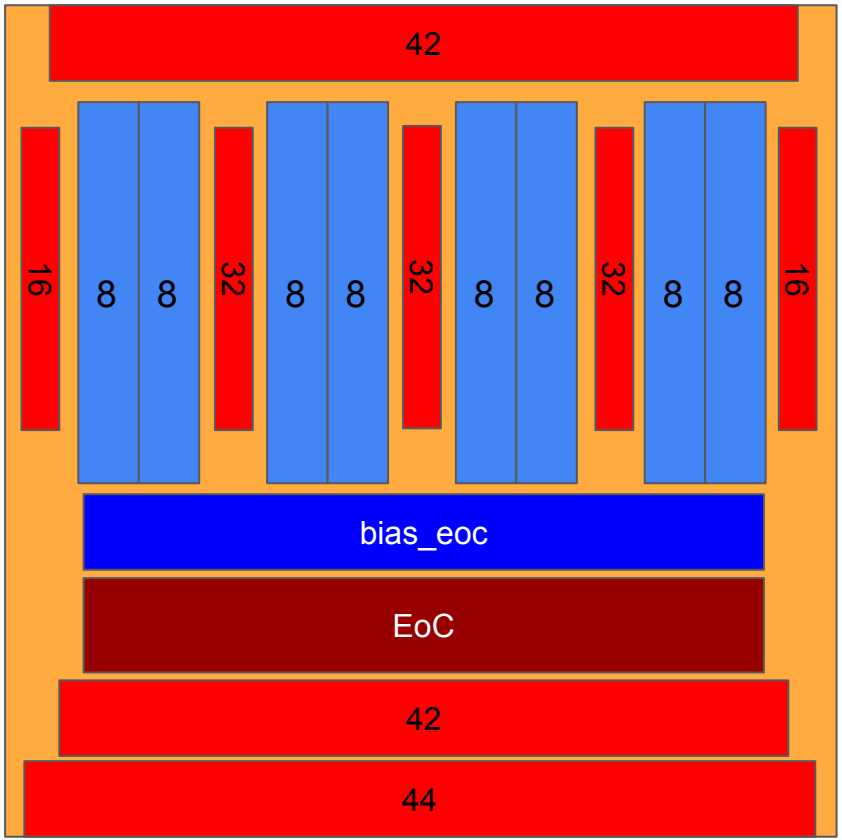
Pixel sectors (32 * 4)

- 16 inputs
- 6 AVDD
- 6 AGND
- 2 AVSS
- 1 AVDD_IO
- 1 AGND_IO

Special sectors to accommodate:

- 2 bias Vref (external)
- 4 debug outputs (internal, need buffers)

Special sectors for external columns



BOTTOM 1st row (44)

- 12 DVDD
- 12 DGND
- 8 DVSS
- 4 DVDD_IO
- 4 DGND_IO

BOTTOM 2nd row (42)

- 16 Tx
- 2 clk
- 2 reset
- 2 test-pulse
- 2 clk_out
- 8 SPI
- 4 DVDD_IO
- 4 DGND_IO

Preventivi 2024

1. ALCOR-32 senza package:
   - modifiche interne: parte analogica + shutter
   - stessa architettura di ora per I/O e padframe → no package, stessa scheda ALCOR-dual di adesso
   - MPW ad inizio 2024
   - MPW da 5x5 → 35 keuro
   - produzione ALCOR-64 con package nella prima metà 2025 (sviluppo già nel 2024)
2. ALCOR-64 con package:
   - modifiche interne: parte analogica + shutter
   - **nuova** architettura per I/O e padframe → sviluppo **package** + nuova scheda ALCOR-BGA + scheda socket per testare chip in package pre-assemblaggio su scheda finale
   - MPW a metà/fine 2024
   - MPW da 5x10 → 70-75 keuro (ulteriore maschera per RDL verso bump-bond)
   - spese per sviluppo, prototipazione, assemblaggio package da definire (per avere preventivo serve fornire dettagli su architettura chip, geometria bump bond e specifiche segnali critici) → 100 keuro ???
   - possibilità di tenere nel 2024 solo ALCOR-64 e mettere le spese per package e/o schede ad inizio 2025

ALCOR v1 FE

M_1: input transistor (CG)

M_2: CG bias

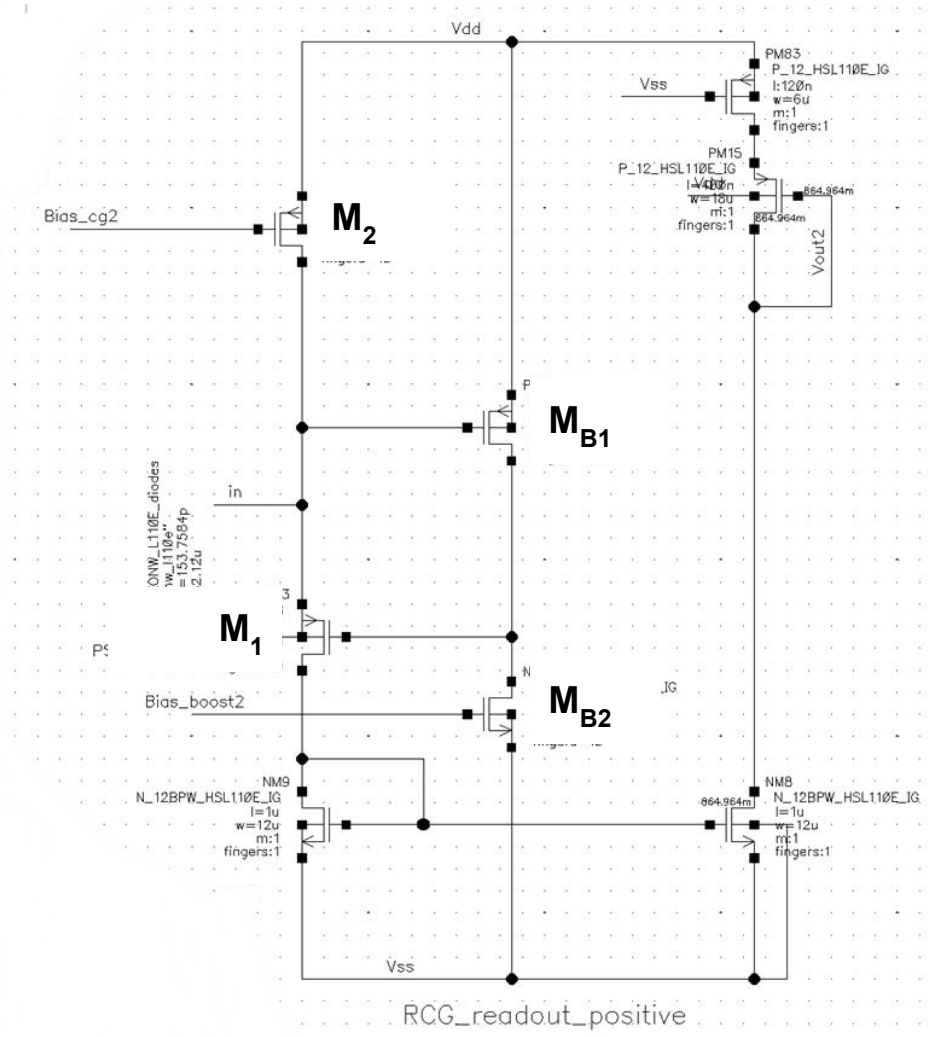
M_{B1}: boost transistor

M_{B2}: boost bias

$M_{B1} + M_{B2}$ = CS amplifier

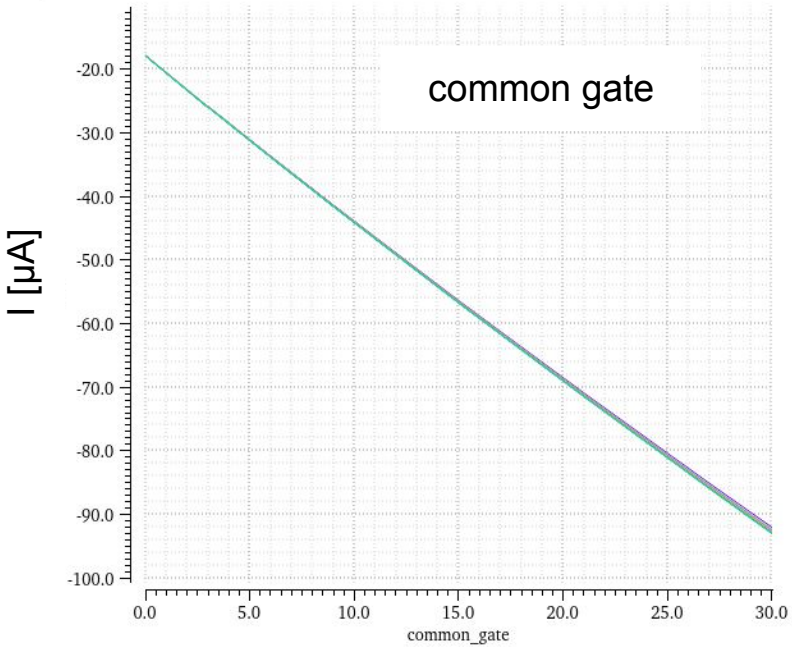
$A = gm_{B1} * R_p$

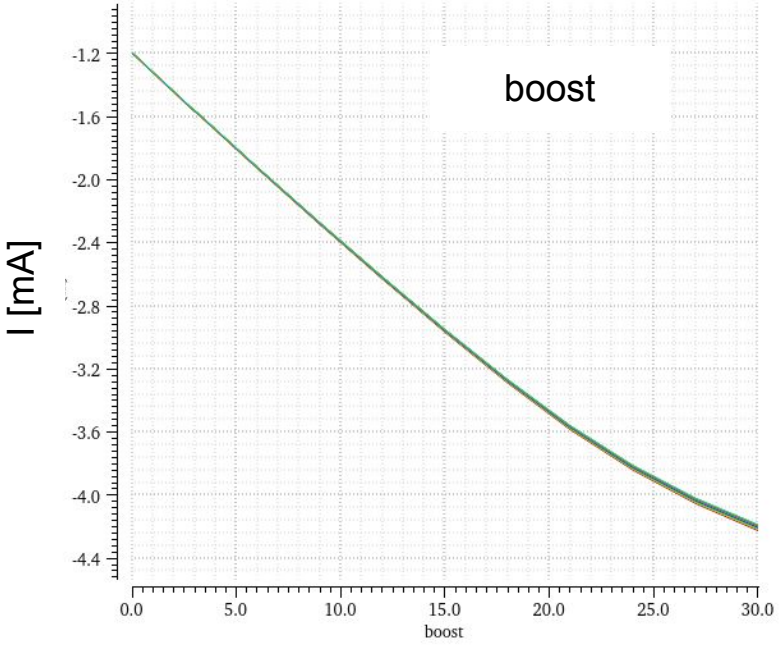
$Zin \approx 1 / (A * gm_1)$



ALCOR v1 jitter simulations

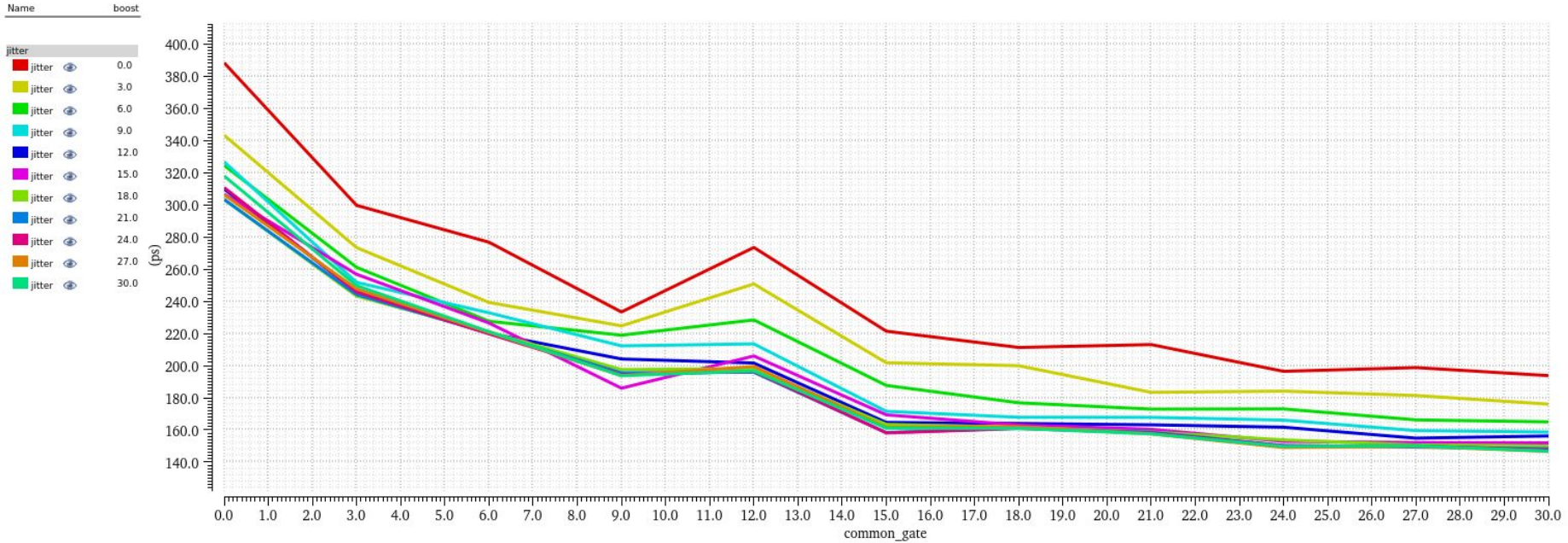
Common gate and Boost bias scan





ALCOR v1 jitter simulations

Common gate and Boost scan



ALCOR v3 internal modifications

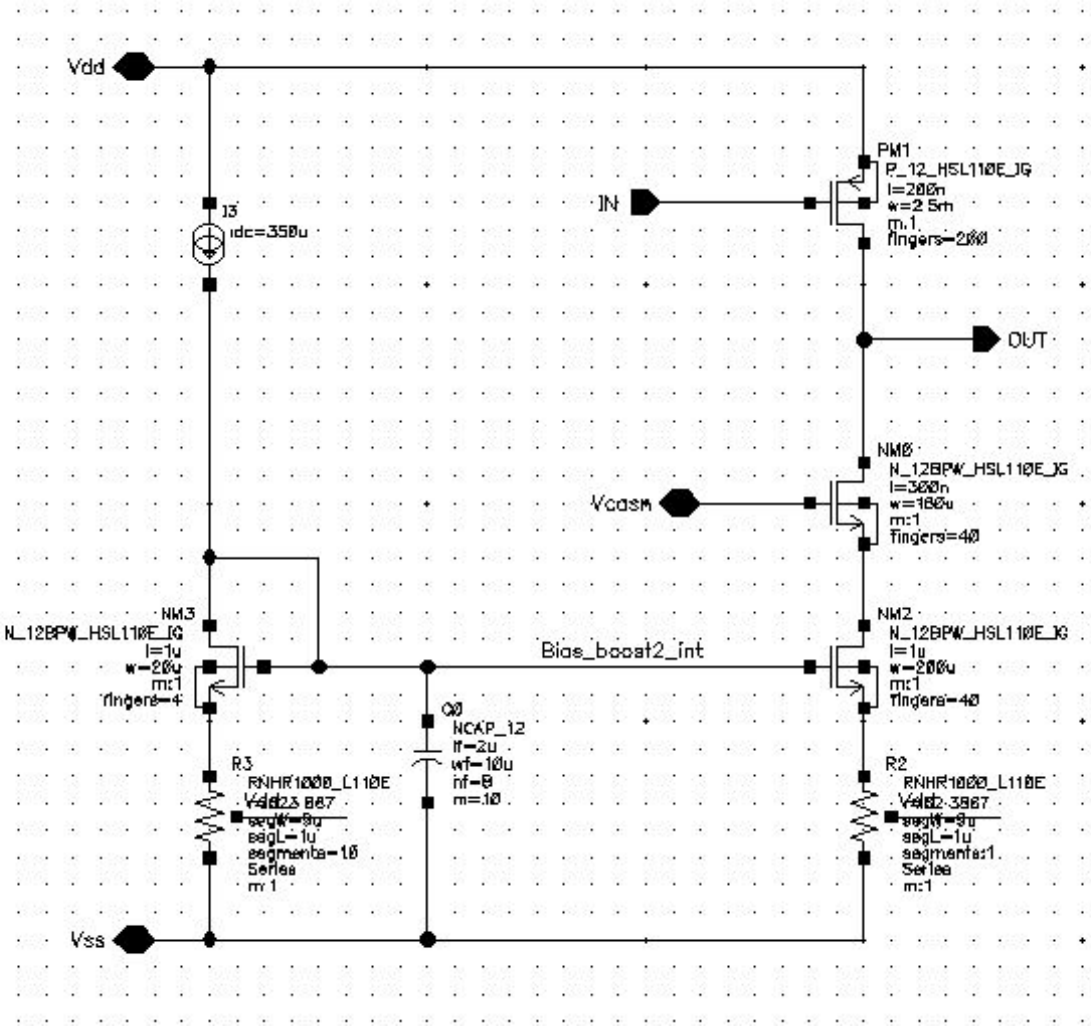
- Upgrade Front-End to improve time resolution
- Add hysteresis to discriminator to remove re-triggering on slow falling edge

- Add digital shutter to reduce data throughput
- Consider removal of ToT2 and SR operation modes
- Fix minor bugs in pixel logic occurring for events close in time

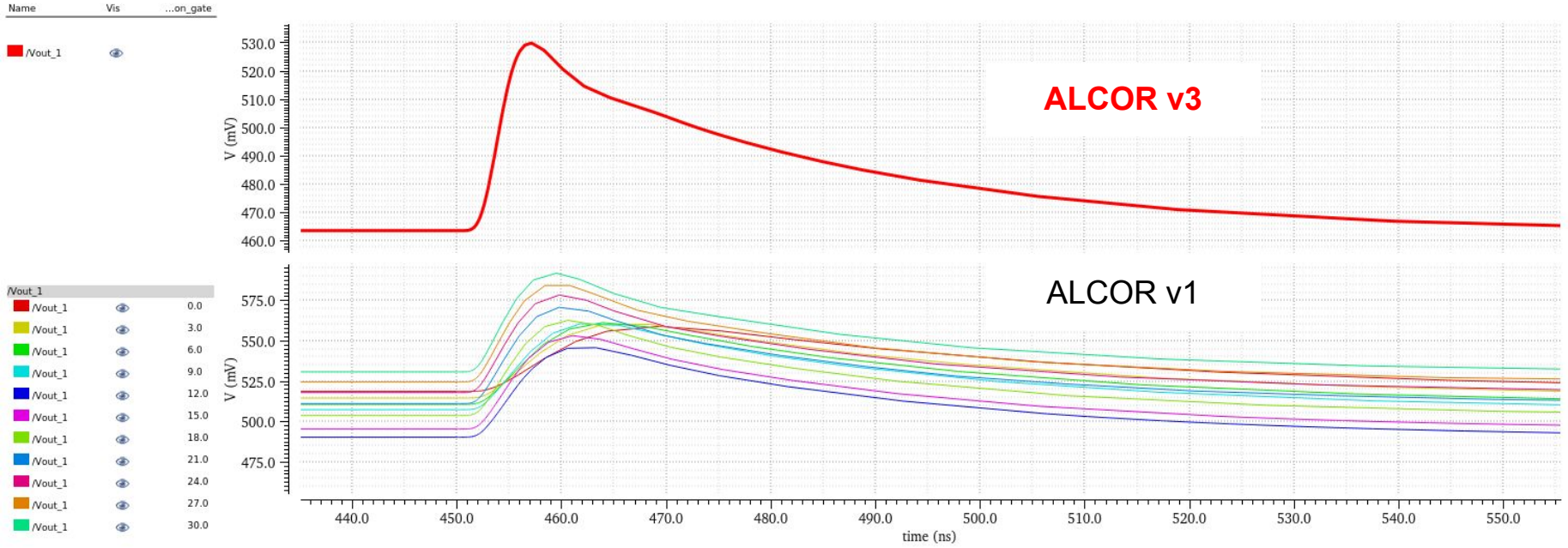
New FE (CS)

Add *cascode* to CS stage to increase R_p and thus A → lower Z_{in}

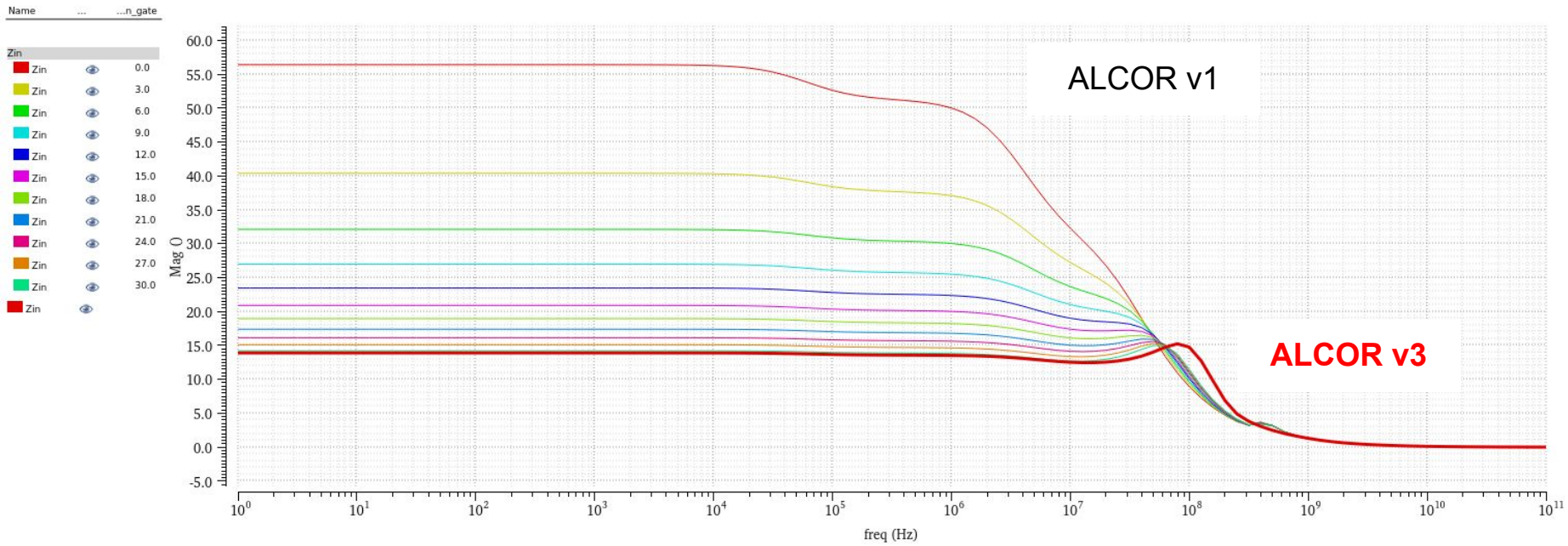
Bias transistor with source degeneration to reduce its contribution to noise



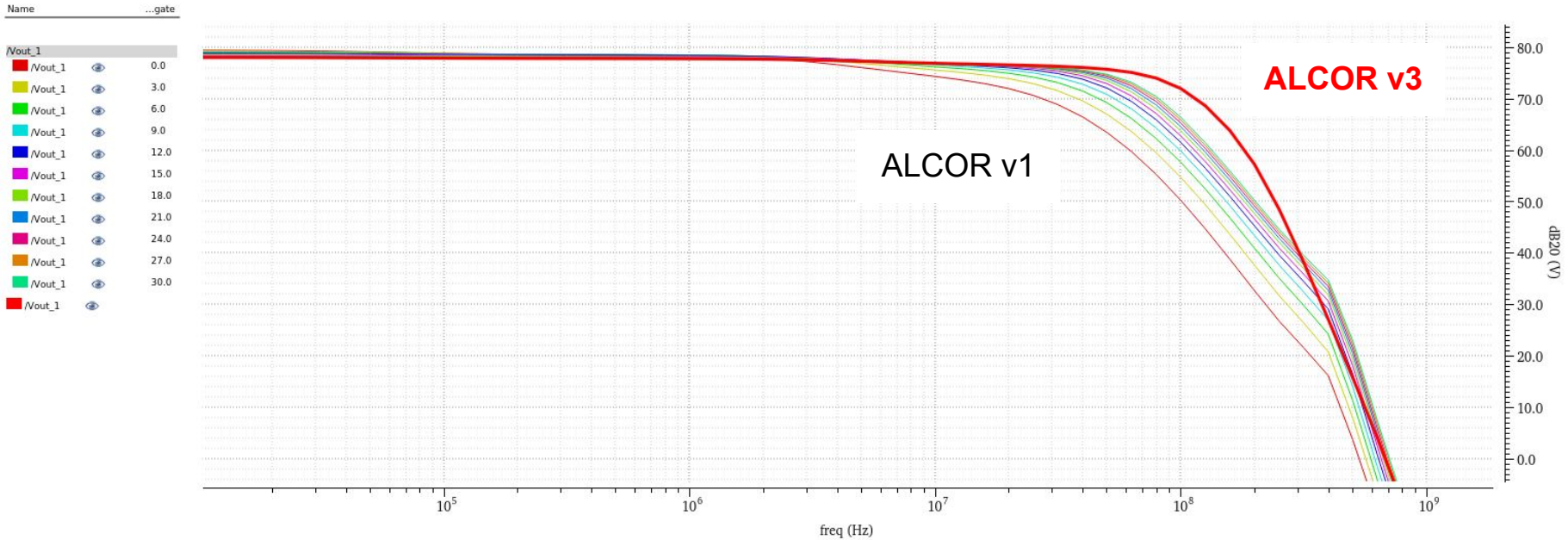
Time response



Zin


Name ... ...n_gate
Zin
Zin 0.0
Zin 3.0
Zin 6.0
Zin 9.0
Zin 12.0
Zin 15.0
Zin 18.0
Zin 21.0
Zin 24.0
Zin 27.0
Zin 30.0
Zin
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
Mag ()
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10} 10^{11}
freq (Hz)
ALCOR v1
ALCOR v3

Frequency response



New FE vs old FE

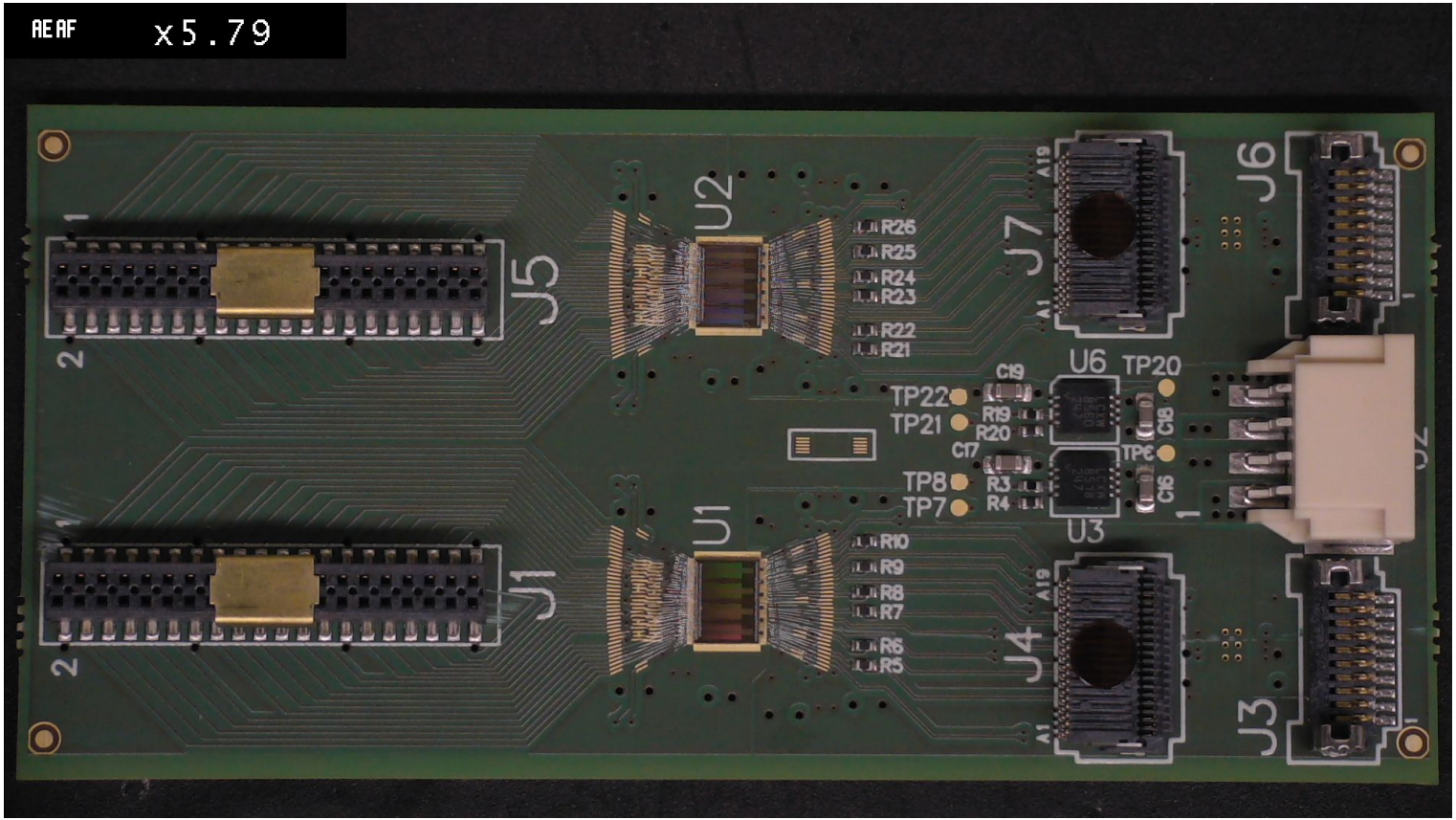
Old FE with bias configuration for best performance

Bias

- I common gate: 89 µA *vs* 86 µA (old FE)
- I boost: 3.4 mA *vs* 4.2 mA (old FE)

Time response

- rise time: 5-6 ns *vs* 8-9 ns (old FE)
- jitter: 90 ps *vs* 150 ps (old FE)


AE AF
x5.79
J5
J1
U2
U1
J7
J4
J6
J3
U6
U3
TP20
TP22
TP21
TP8
TP7
R26
R25
R24
R23
R22
R21
R10
R9
R8
R7
R6
R5
C19
R19
R20
C17
R3
R4
C18
C16