

XII Front-End Electronics Workshop

12th – 16th June 2023

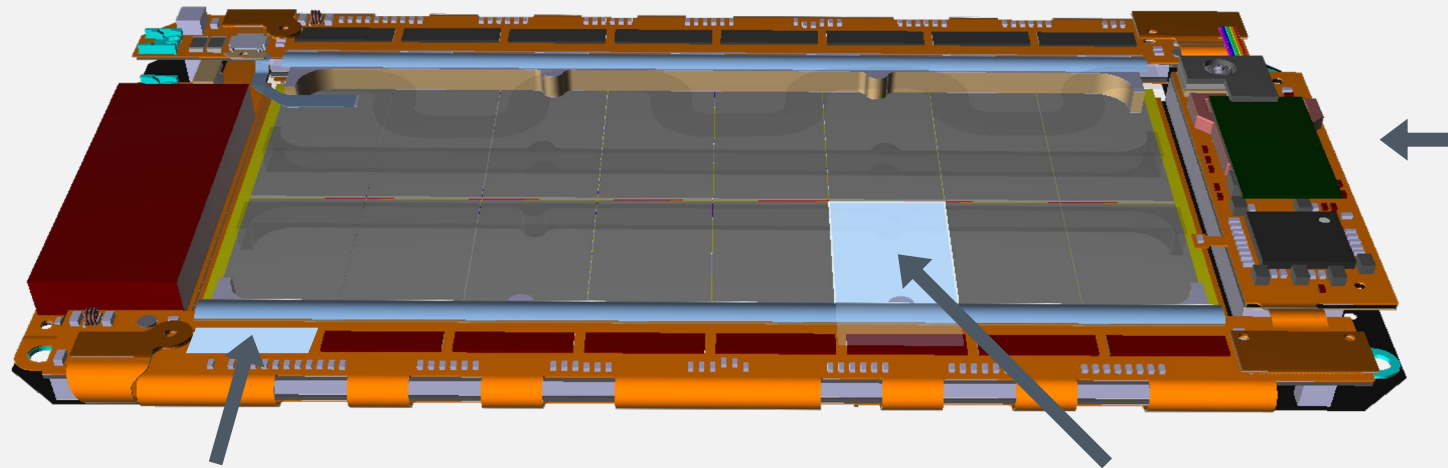
The CMS Outer-Tracker ASICs



Alessandro Caratelli

on behalf of the CMS OT ASICs working-group

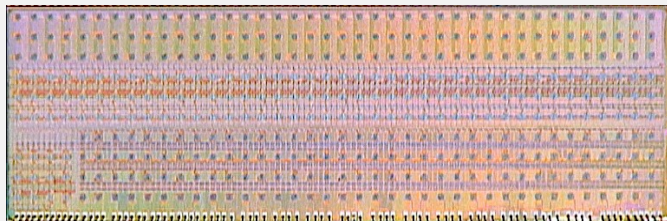
CMS Outer Tracker ASICs



SSA ASIC

DESIGNED AND TESTED BY:

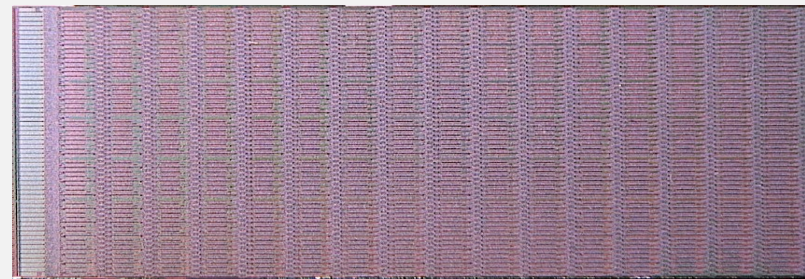
- A. Caratelli • G. Bergamin • D. Ceresa,
- J. Kaplon • K. Kloukinas • S. Scarfi



MPA ASIC

DESIGNED AND TESTED BY:

- D. Ceresa • G. Bergamin • A. Caratelli • J. Kaplon,
- K. Kloukinas • A. Nookala • S. Scarfi

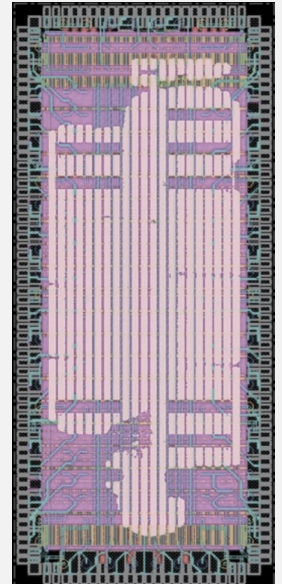


CIC ASIC

DESIGNED AND TESTED BY:

- L. Caponetto • G. Galbit,
- B. Nodari • S. Viret • S. Scarfi
(IP2I Lyon university)

With contributions from
A. Caratelli, D. Ceresa



Total of:
~ 185 000 chips

Few years back.. Requirements for the HighLumi tracker upgrade [1]

Phase-2 upgrade tracker requirements:

- Higher luminosity
- Increased pileup events per BX
- Increase radiation tolerance
- Reduced material budget
- Participate in the L1 trigger
- Improve trigger performance



Requirements for the tracker electronics:

- Increase granularity
- Introduction of a pixelated sensor in OT
- Radiation tolerance up to 100 Mrad or more
- Quick and on-chip particle discrimination
- Higher trigger rate (1MHz) and longer latency (12.5 μ s)
- Power density < 100 mW/cm²
- Add tracking information to the Level-1 trigger decision

[1] CMS collaboration. "The phase-2 upgrade of the CMS tracker." CMS-TDR-014 (2017).

Few years back.. Introduced a novel particle detector electronic system

The outer tracker detector can **provide for every event additional information for the trigger decision** leading to a significant improvement of the particle recognition efficiency



The complete real time tracker readout is not feasible



HOW? The readout electronics in the detector can send pre-selected information for the Level-1 event reconstruction



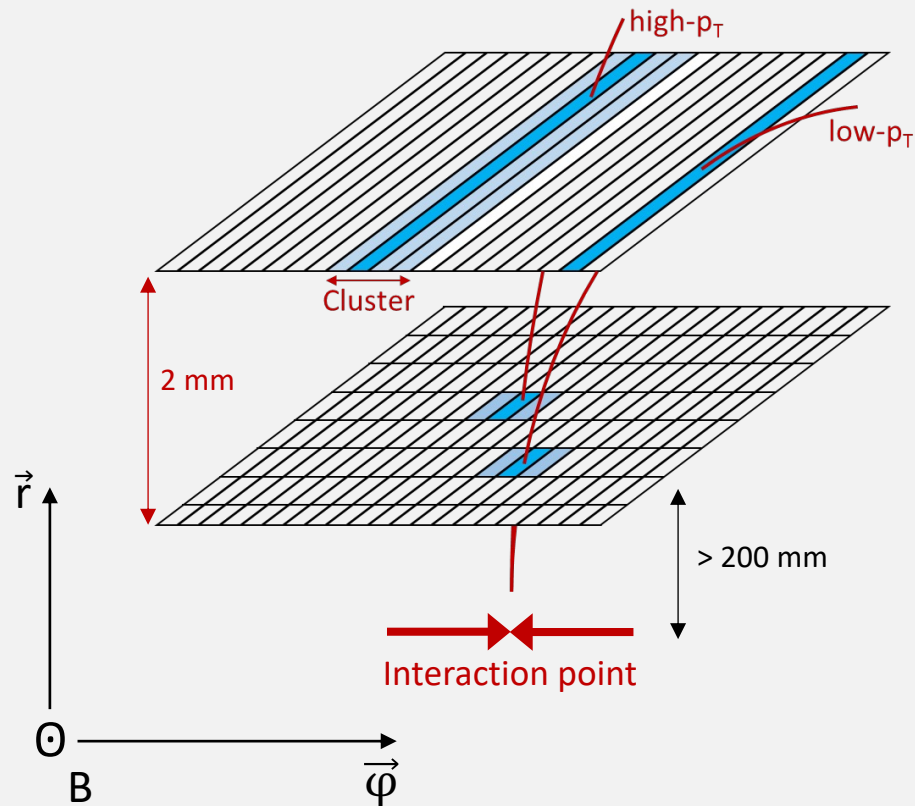
Intelligent pixel particle detector capable to locally self-select interesting signatures of particles interesting for the physics, without relying on an external trigger system

Detector capable of providing particle transverse momentum information in addition to simple geometrical positioning and energy measurements

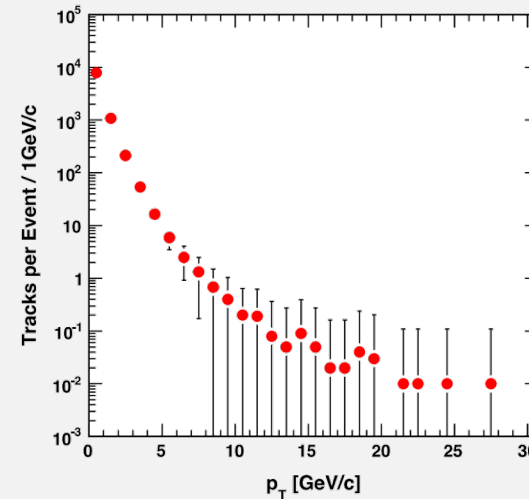
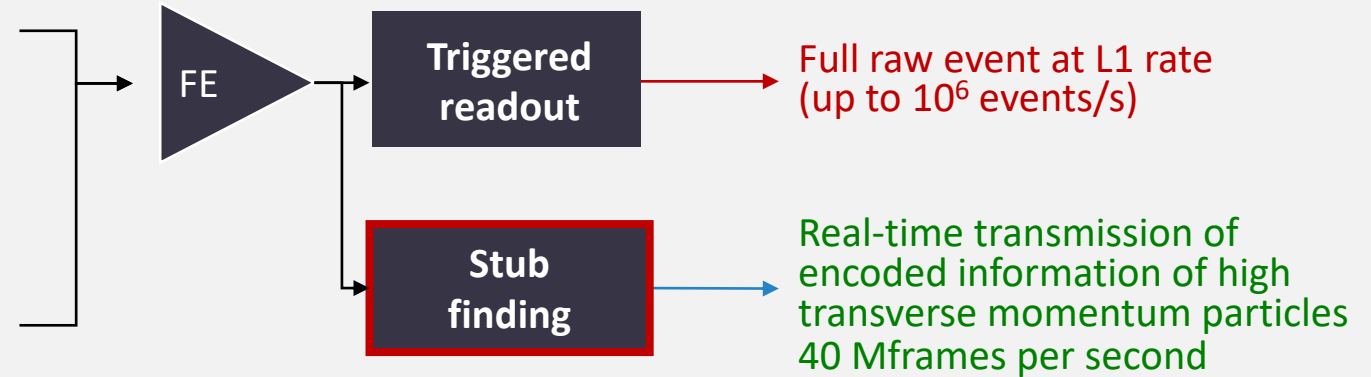


This approach allows for a **significant data reduction efficiency improvement**

An intelligent particle tracking system based on p_T discrimination



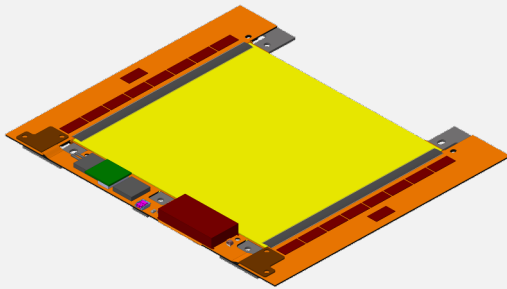
3.8T provided by the superconducting solenoid



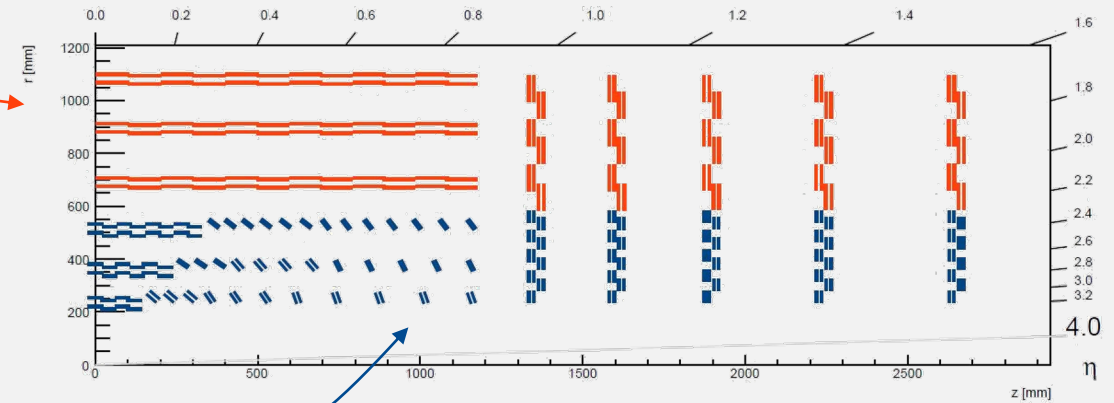
The p_T threshold should be chosen to provide a good rejection of the background and therefore a significant data reducing factor, but not too high to filter the interesting decay products with consequent impact in the performances.

The CMS Outer Tracker modules [1, 2]

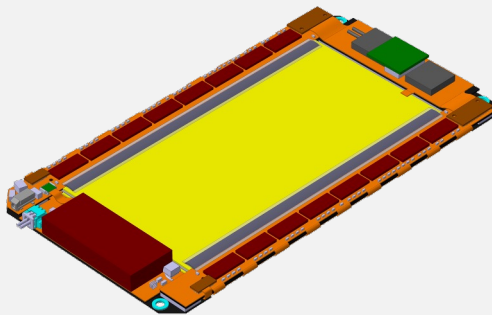
2S module



Active area:	2 x 90 cm ²
N strips:	4096
Strip size:	5 cm x 90 μm
Operating V:	1.2 V
Max power:	< 5 W
Power density: ...	< 100 mW/cm ²



PS module

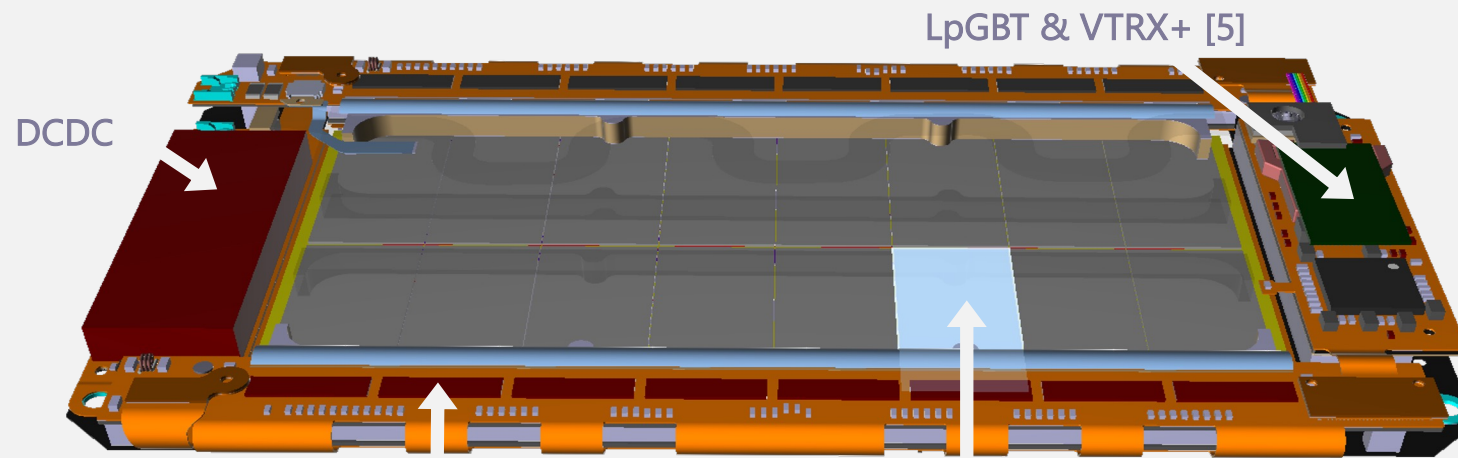


Active area:	2 x 45 cm ²
N pixel/strips:	1920 strips + 30 720 pixels
Strip size:	2400 mm x 100 μm
Pixel size:	1.5 mm x 100 μm
Operating V:	1.0 V for digital + 1.2V for analog
Max power:	< 5 W
Power density: ...	< 100 mW/cm ²

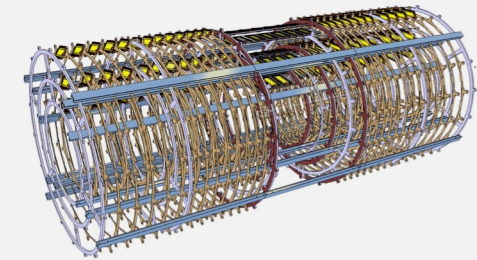
[1] CMS collaboration. "The phase-2 upgrade of the CMS tracker." CMS-TDR-014 (2017).

[2] Abbaneo, Duccio. "Upgrade of the CMS Tracker with tracking trigger." Journal of Instrumentation 6.12 : C12065.

The Pixel-Strip module

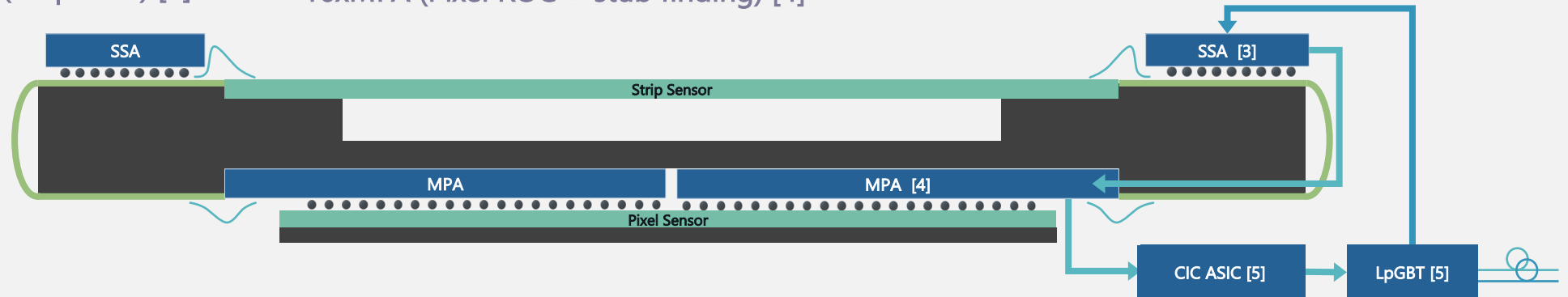


13296 Modules
 44 Mstrips + 174 Mpixels
 200m² of silicon area



16 x SSA ASICs (Strip ROC) [3]

16xMPA (Pixel ROC + stub finding) [4]



[3] Caratelli, Alessandro, et al. Characterization of the first prototype of the Silicon-Strip readout ASIC (SSA). No. CMS-CR-2018-286. 2018.

[4] Ceresa, Davide, et al. Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities. No. CMS-CR-2018-279. 2018.

[5] Moreira, Paulo. "The LpGBT project status and overview." ACES. 2016.

[6] Nodari, Benedetta, et al. A 65 nm data concentration ASIC for the CMS outer tracker detector upgrade at HL-LHC. No. CMS-CR-2018-278. 2018.

MPA and SSA ASICs: system level architecture choices

Initially several system design choices needed to be taken:

- Define **which functionality** are implemented in the SSA and which in the MPA
- How to **minimise system power** requirements
- How to **minimize bandwidth** requirements
- **Maximize the particle recognition** efficiency
- **Optimize bandwidth** among ASICs
- Data encoding
- Transmission FIFOs depth
- Data compression
- Particle hit clustering at SSA level
- Several others

Analytic approach but the functionality and the efficiency depends on physics statistics, particle rates and hit occupancy (no simple inputs)

Becomes necessary a Simulation framework capable of providing:

System Studies and performances evaluation

Design Verification

- Study and compare different system implementation
- Evaluate **tradeoff between performances and power optimization**
- Report **efficiency parameters** by comparison with a **system reference model**
- Evaluate the **efficiency of the particle recognition** and of the data readout
- **Realistic stimuli generation** from Monte-Carlo simulations of complex interactions in high-energy particle collisions

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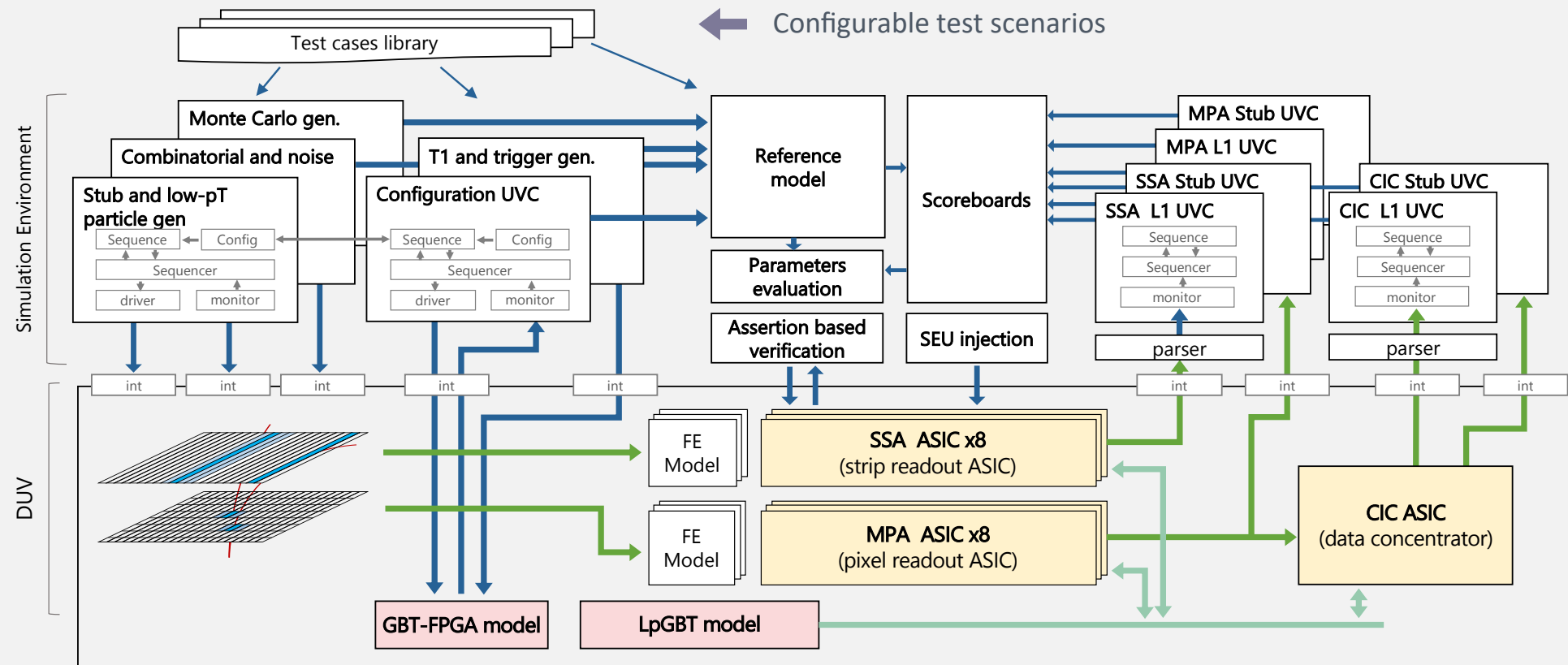
Design Verification

- **Verify** the RTL implementation and the **chip-set functionalities**
- Generation of **realistic activity information** for precise power analysis
- Verify post-layout netlist
- Verify at clock-cycle level precision the **subsystems integration and the communication among modules the ASICs**

System level simulation framework [7]

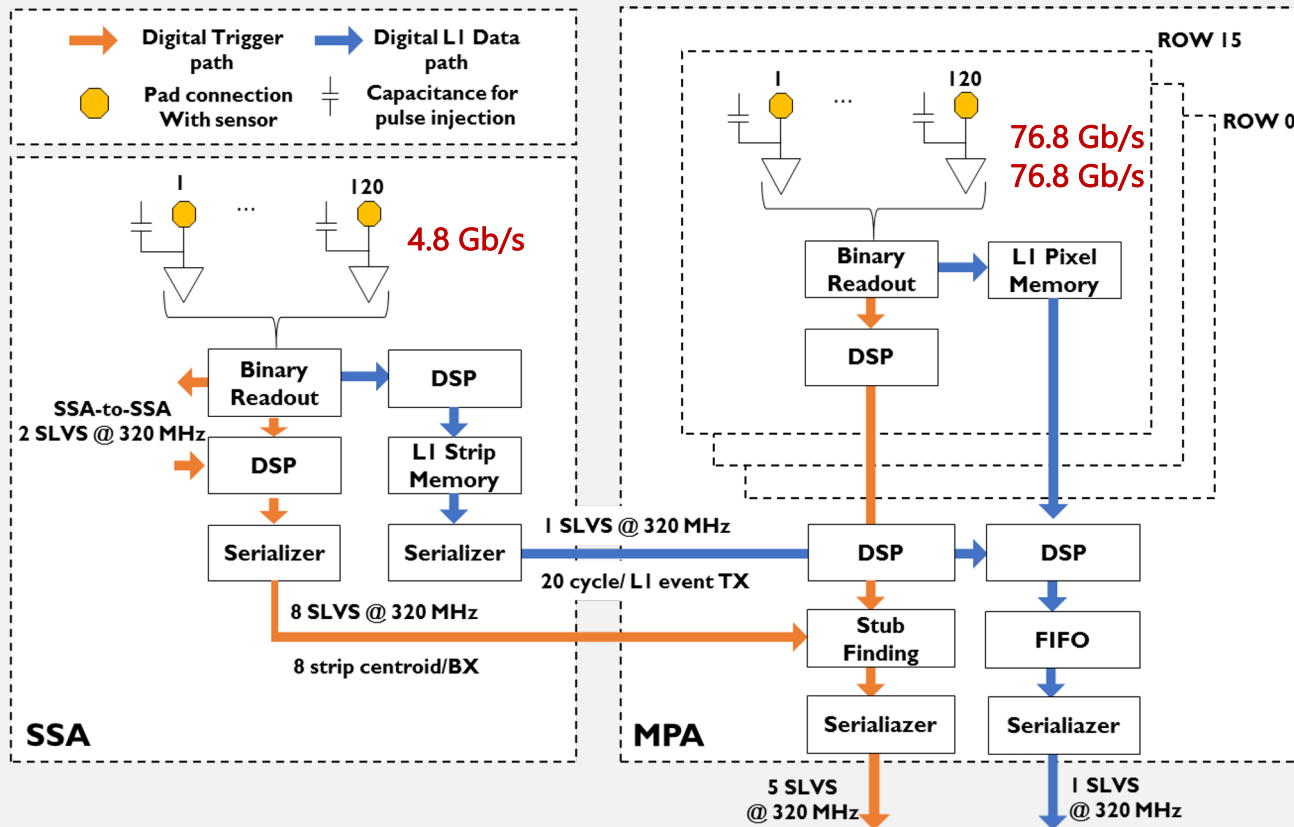
Implemented in: SystemVerilog HDL / UVM + Python

Randomized stimuli
emulating particle
detector hits and noise.
Emulation according the
CMS tracker geometry



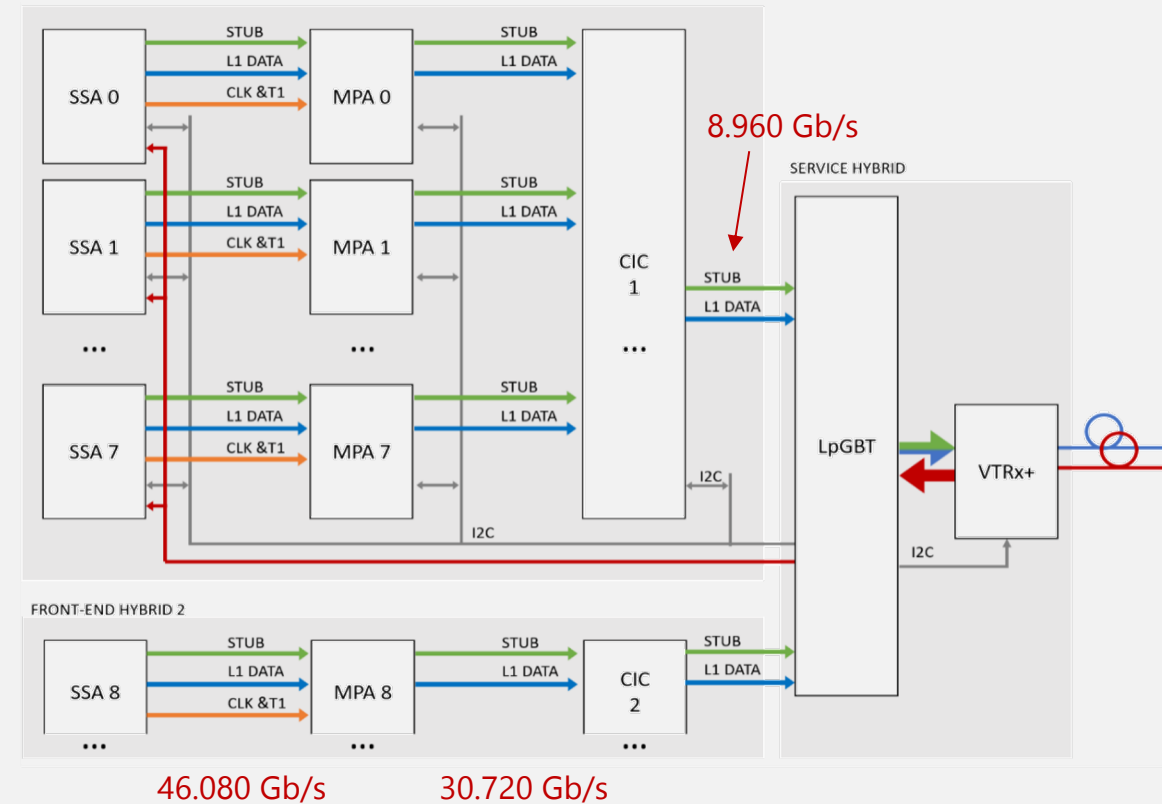
[7] Caratelli, Alessandro, et al. "System Level simulation framework for the ASICs development of a novel particle physics detector." 2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME). IEEE, 2018.

System architecture definition [8]

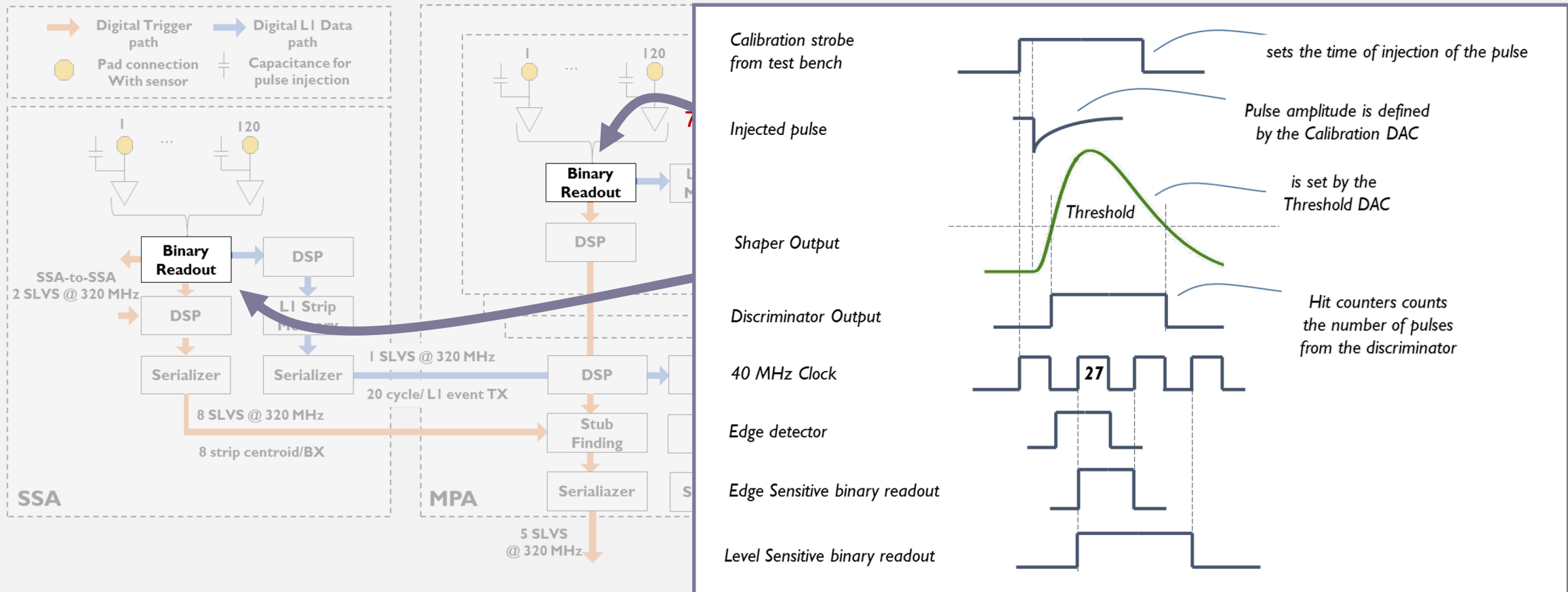


40 MHz rate for high-pT particles
1.6 Gb/s - latency: < 500 ns

Full frame at L1 trigger rate (1MHz)
320 Mb/s

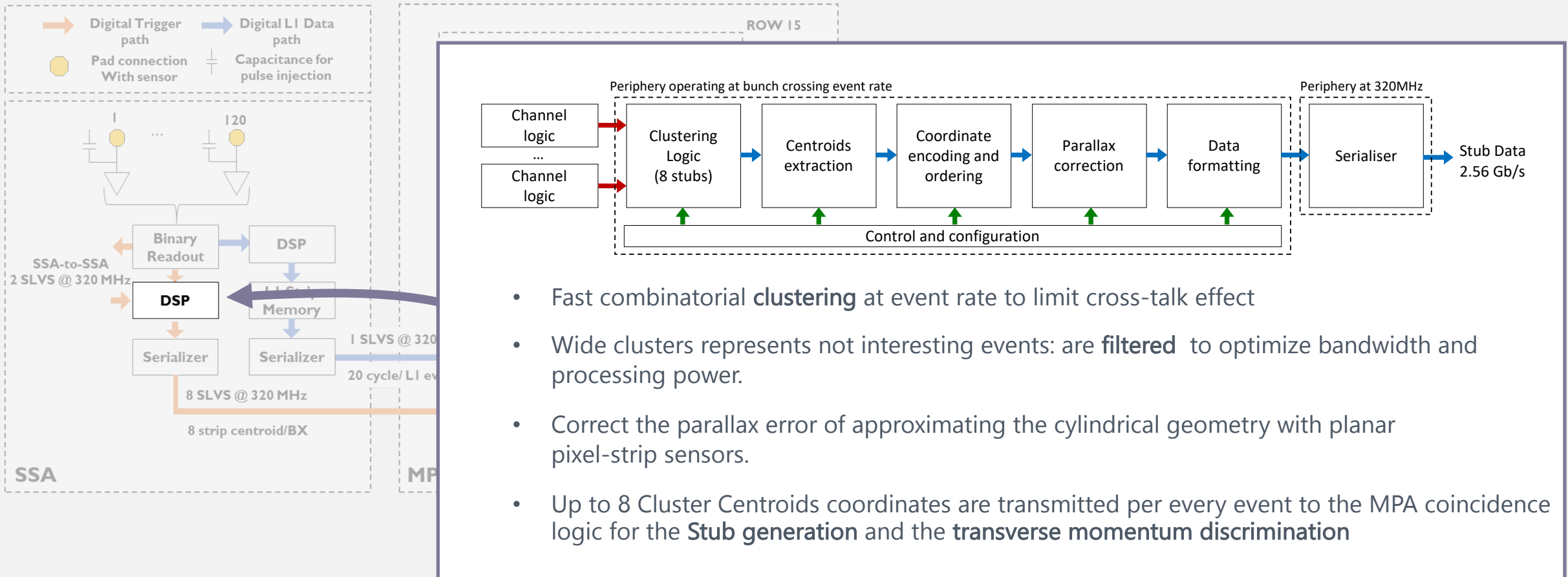


MPA and SSA ASICs architecture [9]



[9] D. Ceresa, A. Caratelli, G. Bergamin, J. Kaplon, K. Kloukinas, S. Scarfi "MPA-SSA, design and test of a 65nm ASIC-based system for particle tracking at HL-LHC featuring on-chip particle discrimination." 2019 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC). IEEE, 2019.

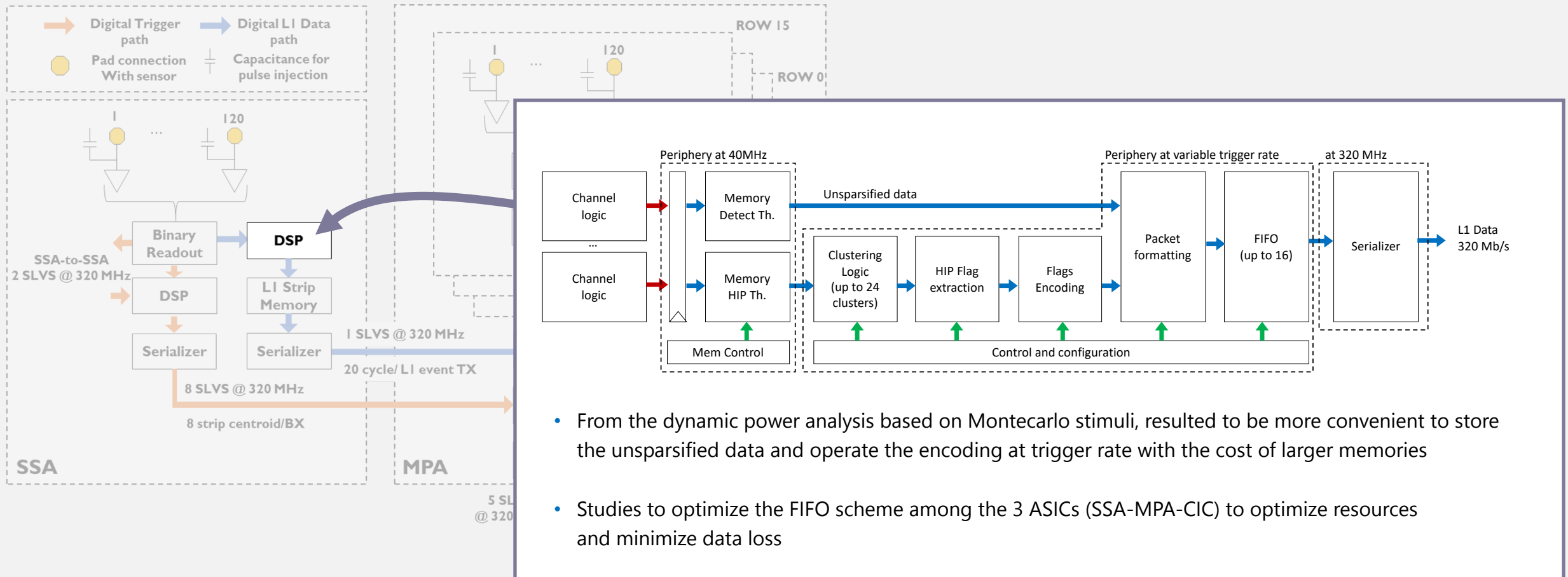
MPA and SSA ASICs architecture [9]



- Fast combinatorial **clustering** at event rate to limit cross-talk effect
- Wide clusters represents not interesting events: are **filtered** to optimize bandwidth and processing power.
- Correct the parallax error of approximating the cylindrical geometry with planar pixel-strip sensors.
- Up to 8 Cluster Centroids coordinates are transmitted per every event to the MPA coincidence logic for the **Stub generation** and the **transverse momentum discrimination**

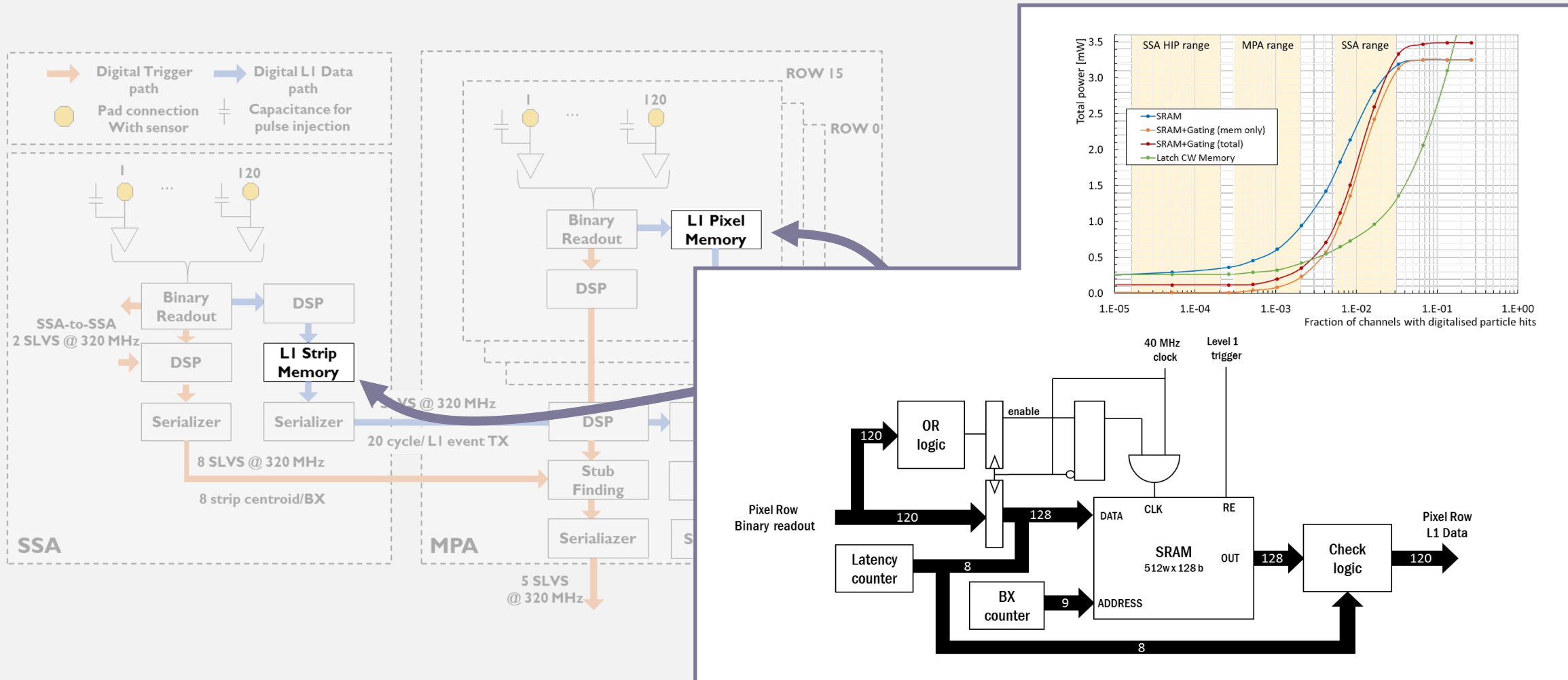
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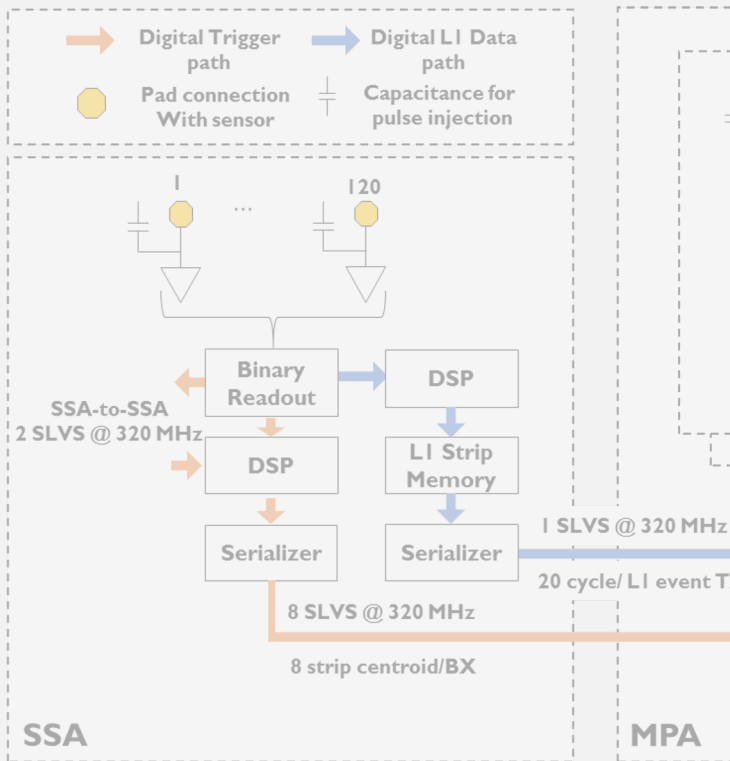
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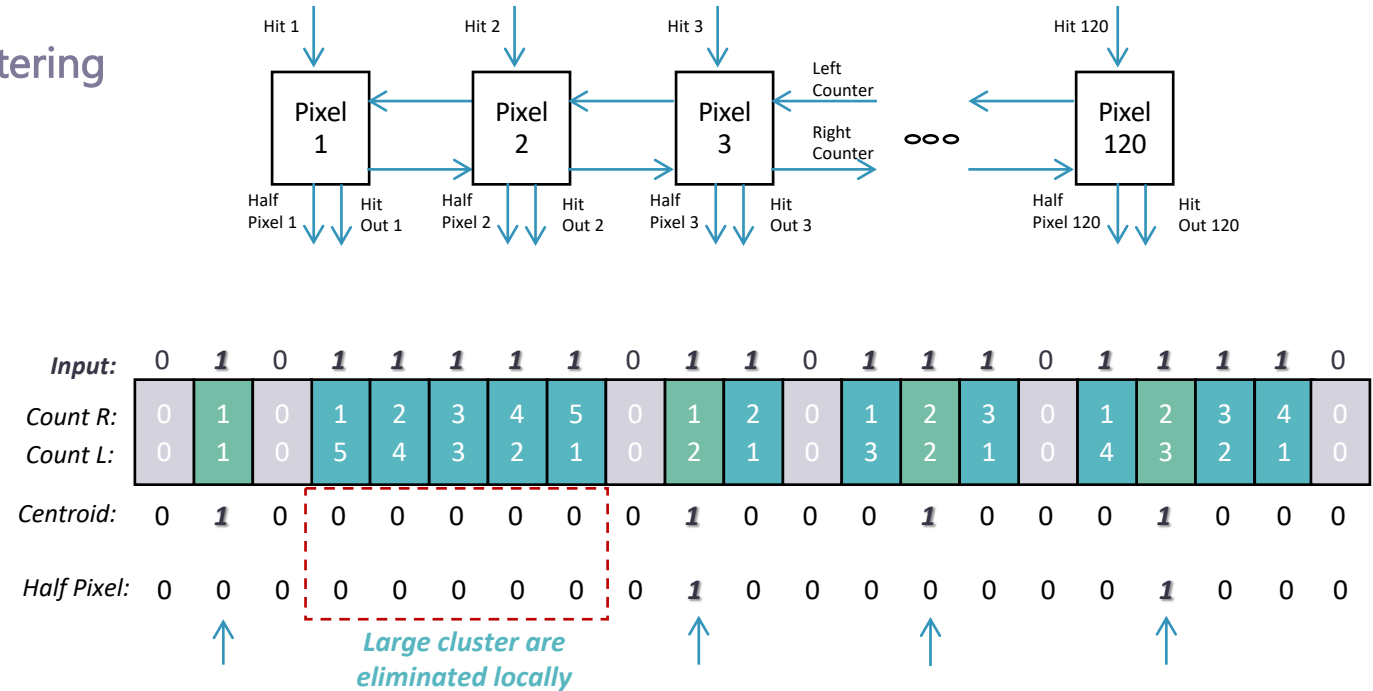


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System architecture definition



Pixel clustering



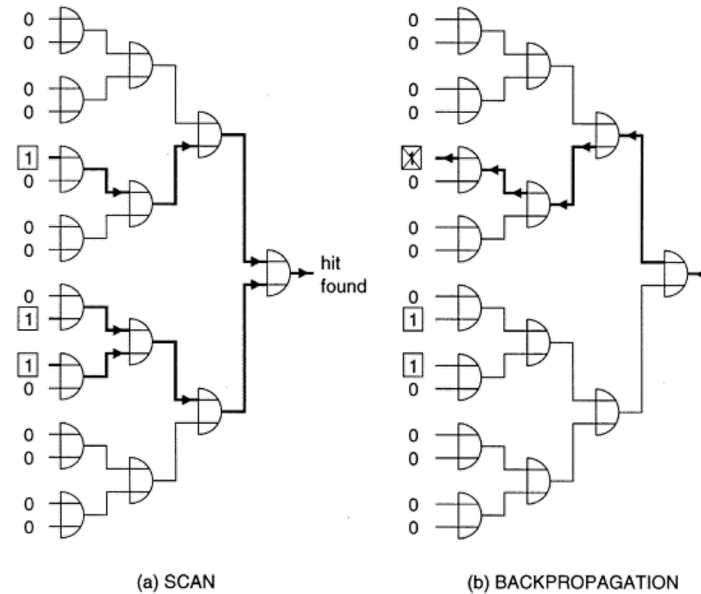
Reduce drastically the data flow from the pixel array to the periphery logic with a consequent significant power consumption reduction

Coordinate encoding

MPA

Mephisto Encoder

Up to 2 coordinate per cycle
Significantly less power consumption

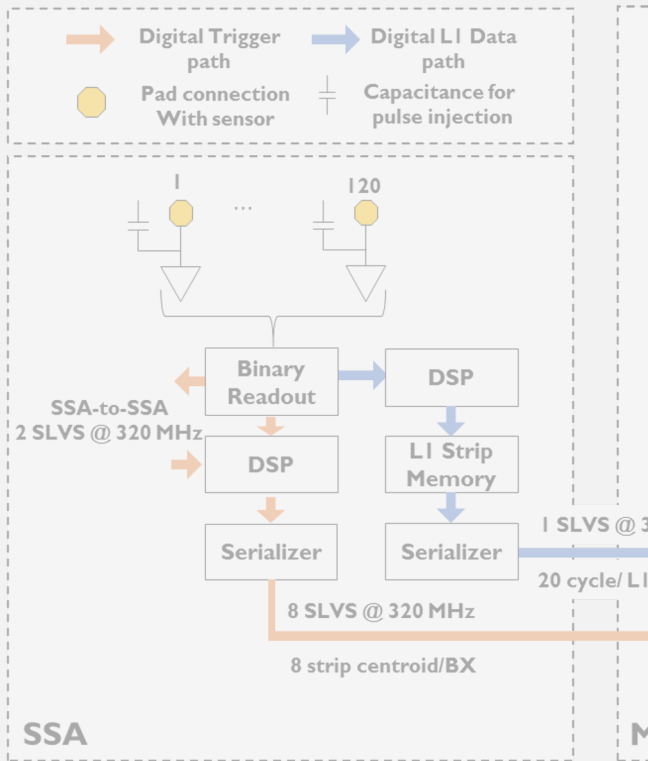
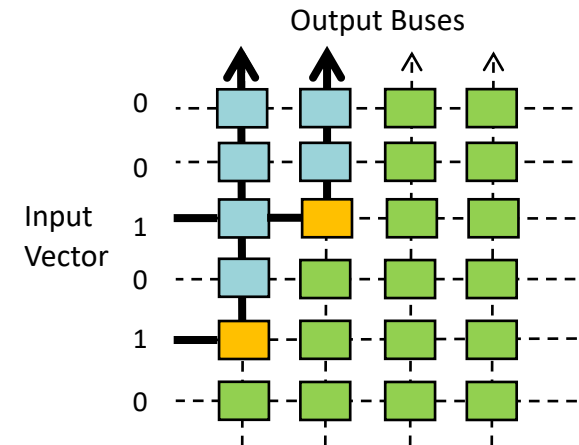


SSA

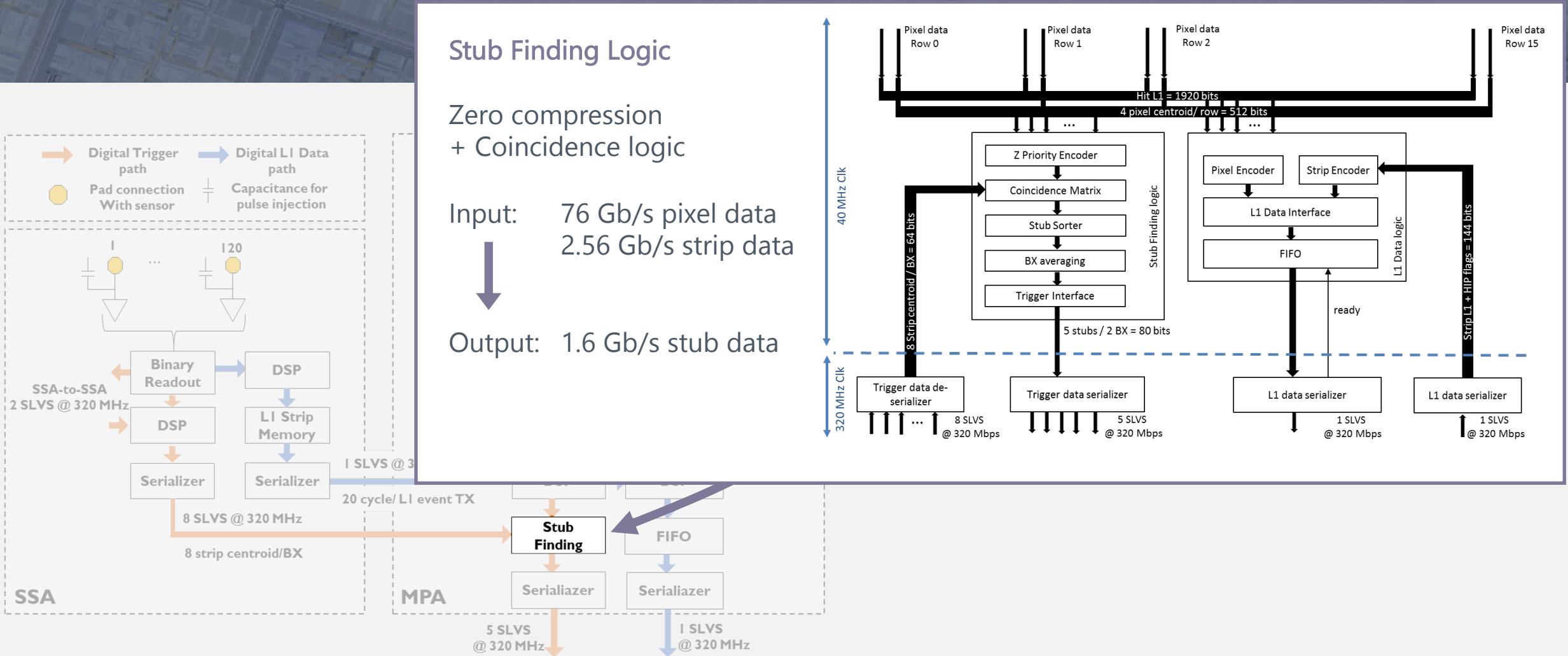
Priority Encoder

Encodes up to 8 centroids over the 132 bits vector in the periphery logic
Less power efficient, but minimizing latency in SSA reduce much more the consumption in the MPA

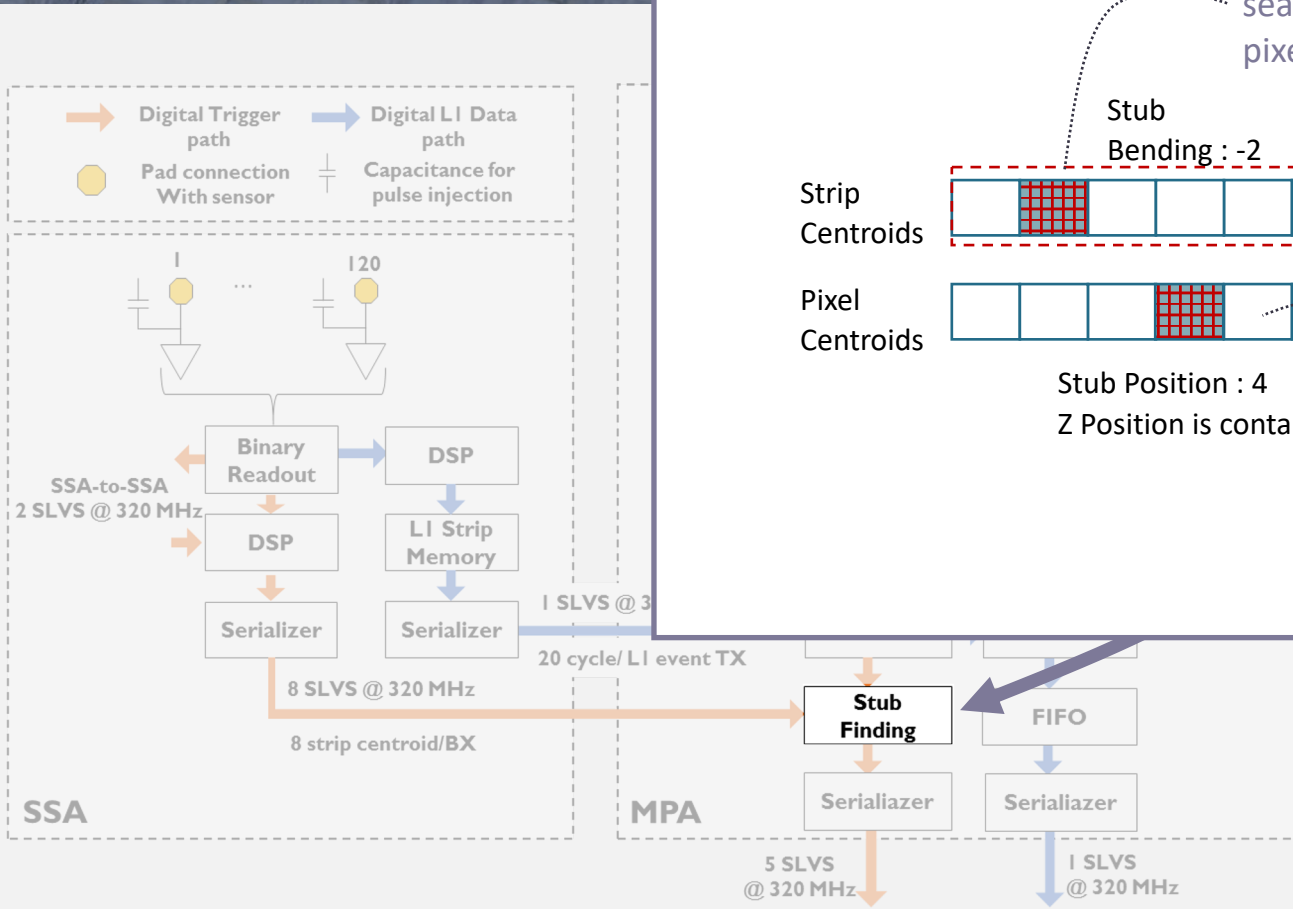
What counts is the overall power!



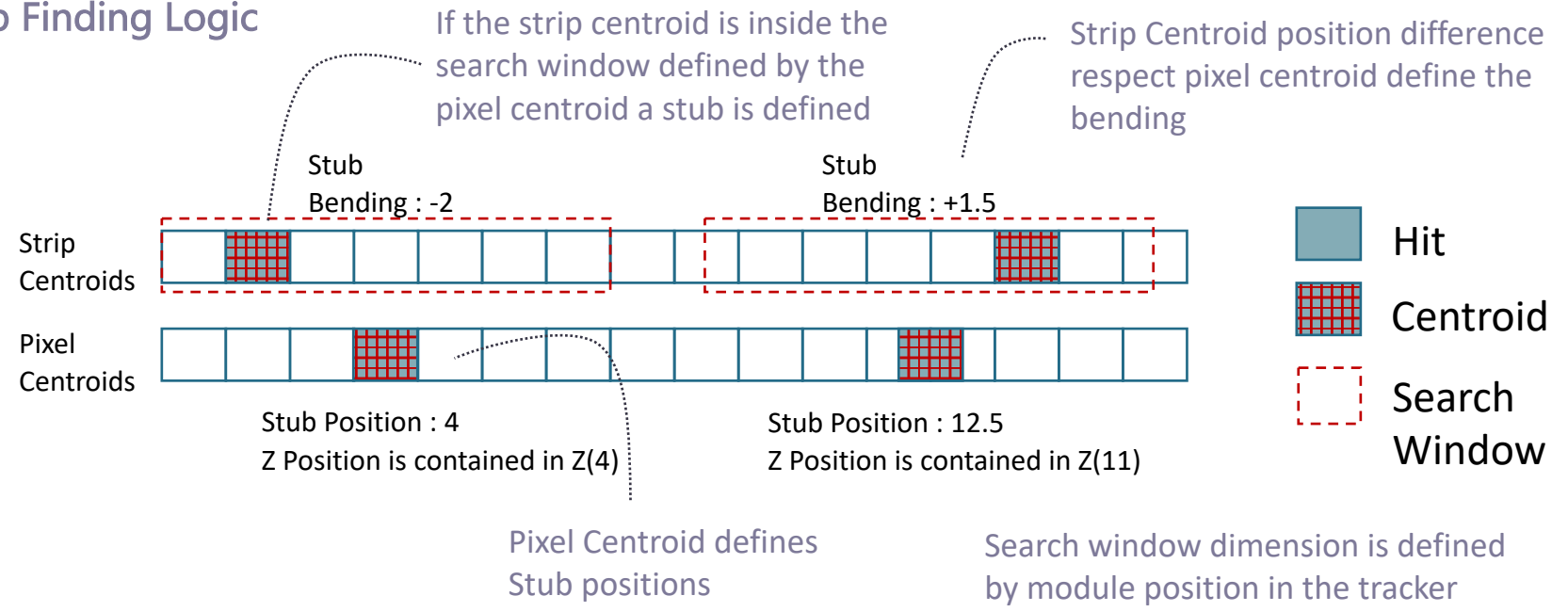
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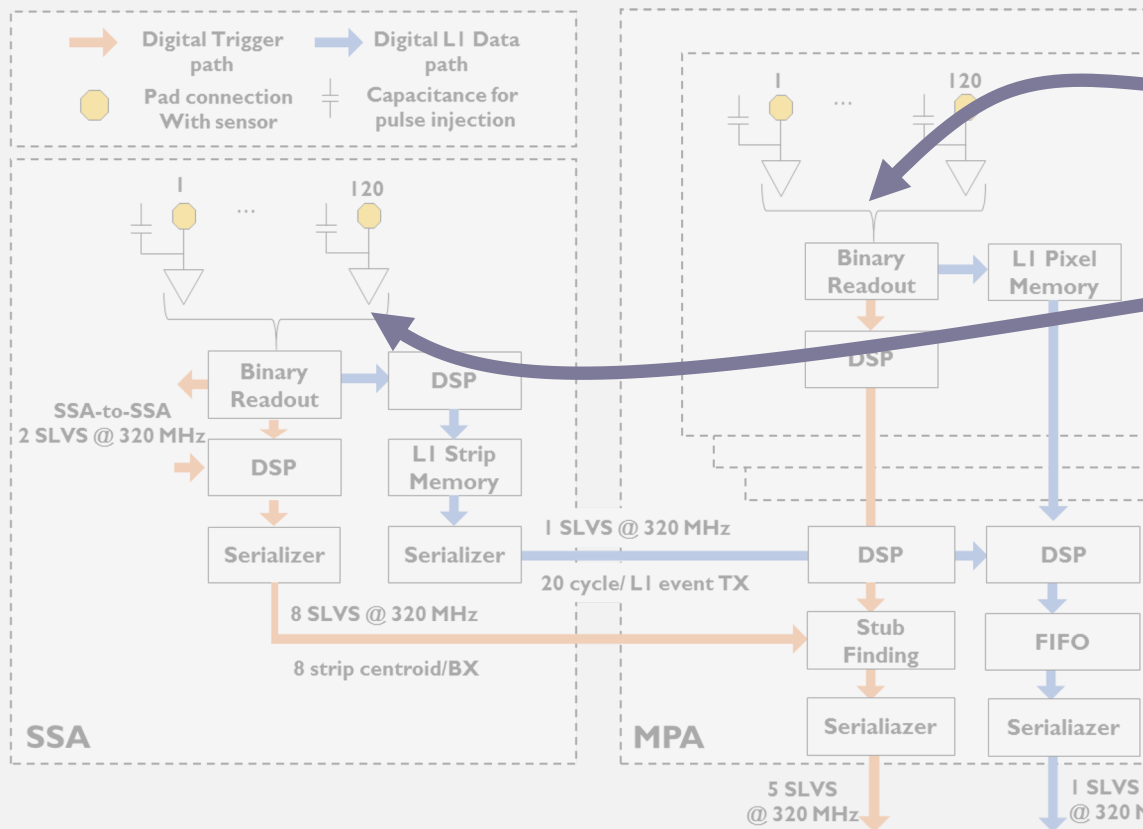


Stub Finding Logic

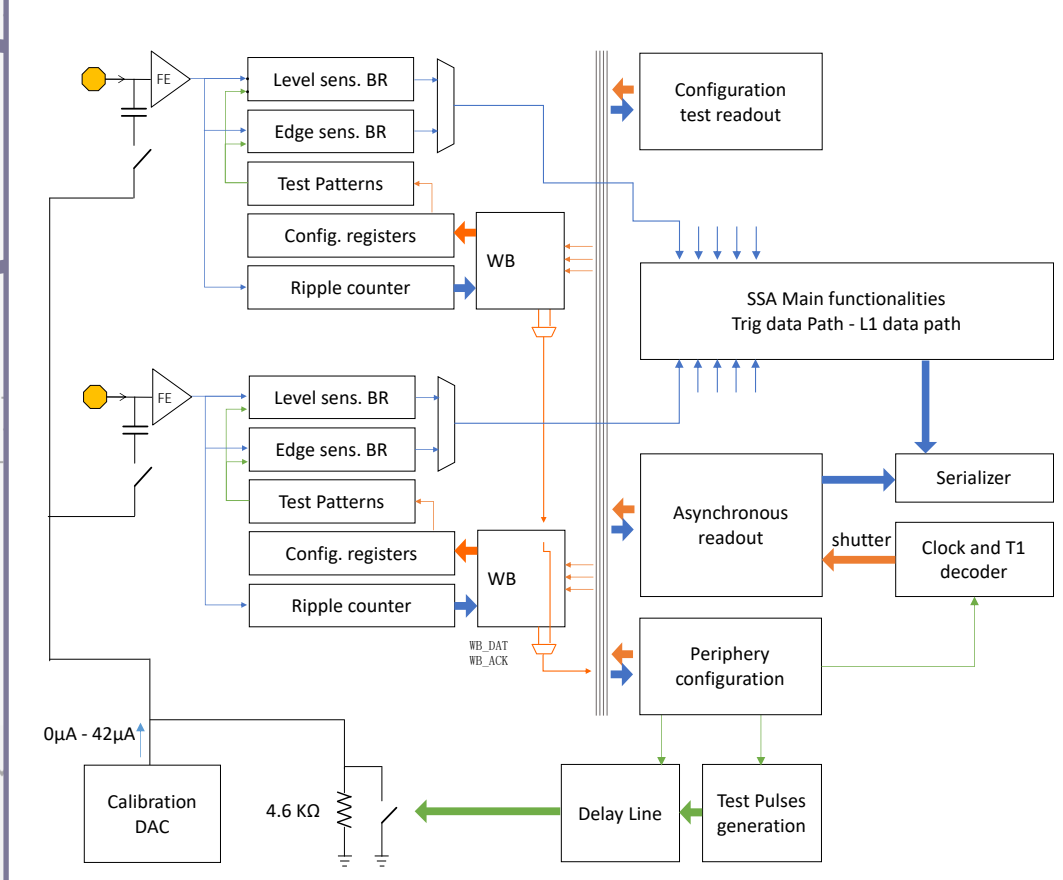


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MPA and SSA ASICs architecture [9]



Calibration circuit



[9] D. Ceresa, A. Caratelli, G. Bergamin, J. Kaplon, K. Kloukinas, S. Scarfi "MPA-SSA, design and test of a 65nm ASIC-based system for particle tracking at HL-LHC featuring on-chip particle discrimination." 2019 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC). IEEE, 2019.

Design for Testability

Memory Built-In-Self-Test

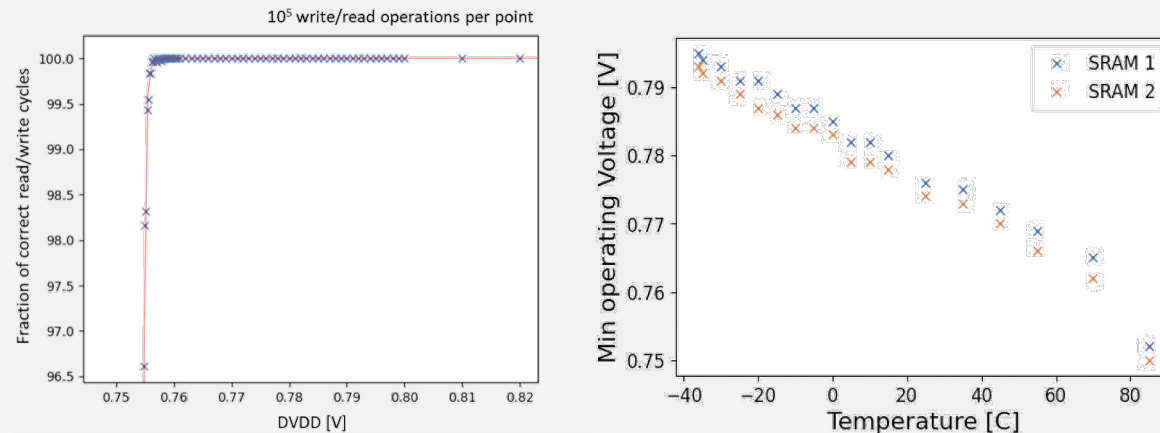
- Test full memory functionality in < 10 ms
- Results saved in internal registers accessible via slow-control
- Few additional hardware self contained hierarchical block
- Clock gating during normal operation (only leakage power)

Periphery Scan Chain

- FSM Easy to access – standardized approach with TRL
- 92% of fault coverage in SSA (300ms)
- ~95% of fault coverage and 25k ff in MPA (750ms)

Logic Built-In-Self-Test for pixel array

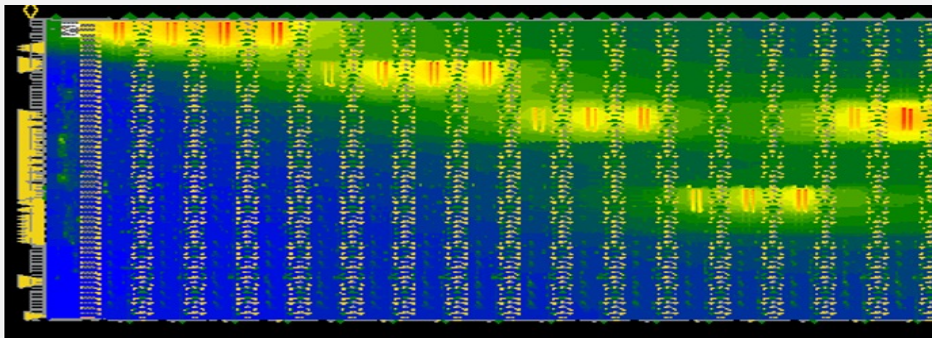
- FSM embedded in Pixel Array logic and vectors from configuration
- Requires compression / decompression logic
- ~90% coverage



Power Reduction Methodology

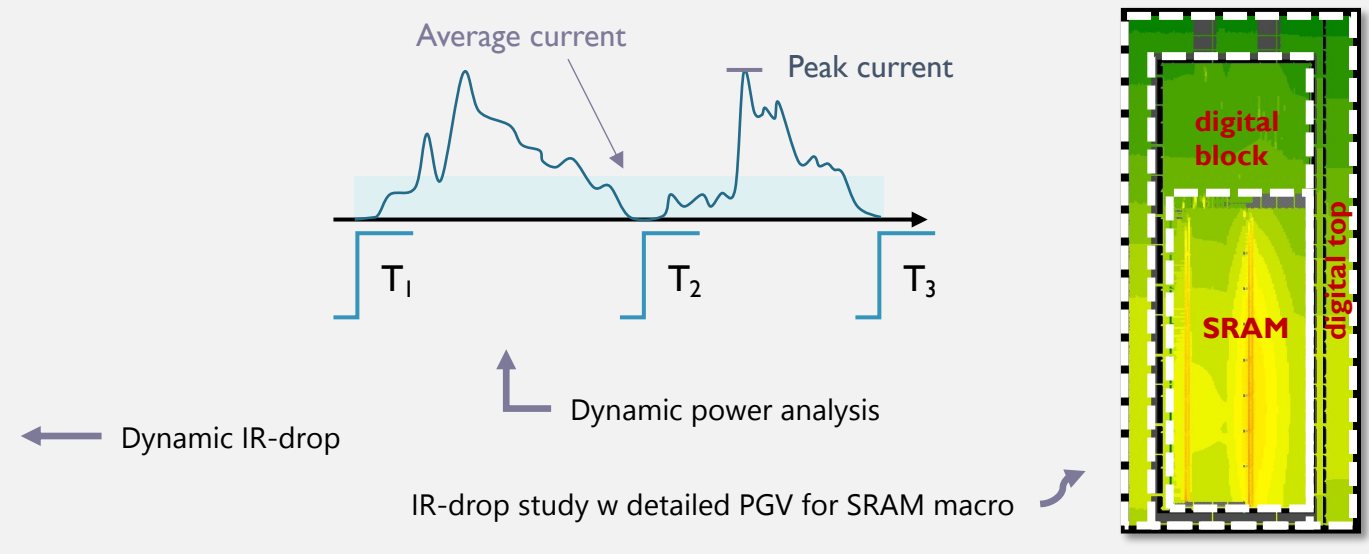
Power optimization

- Clock gating in all configuration registers and logic
- Architecture studies to minimize power consumption
- Use Multi-VT standard cells
- Use gated SRAM blocks
- Multi-supply voltage (1.0V – 1.2V)
- Find power hungry and low activity blocks and optimize their implementation



Power study:

- Static and **Dynamic power** analysis
- Voltage drop analysis on different scenario
- Power-Grid-View (PGV) for Macro



Total Ionizing Dose effects hardening

Digital domain:

- 9-tracks library selected as compromise between power consumption and radiation tolerance considering the operating range $-40^{\circ}\text{C} / 0^{\circ}\text{C}$
- **Characterization of the digital cells** parameters (prop. delay, transition time, setup/hold, etc.) for radiation corner
- Increased margins for TID degradation (setup uncertainty jitter + **additional 8% of clock period** – **reduced max transition** – **derate factors**)
- Due to narrow channel effects → **Removed minimum-width cells** (D0, D1) and delay elements
- **Only thin-oxide devices** → 1.2V max (CMOS IO and SLVS)
- **Custom ESD structures** latch-up resistant

Memories:

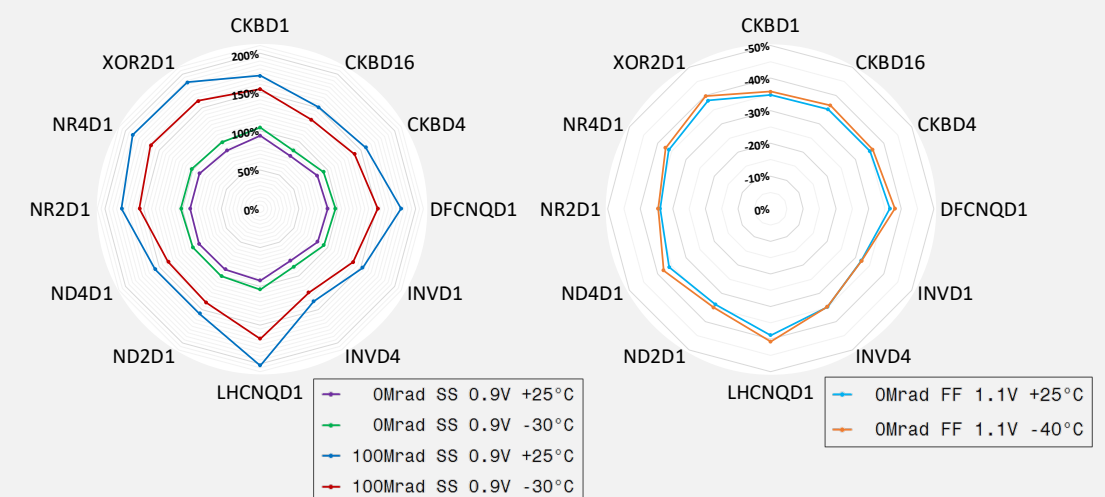
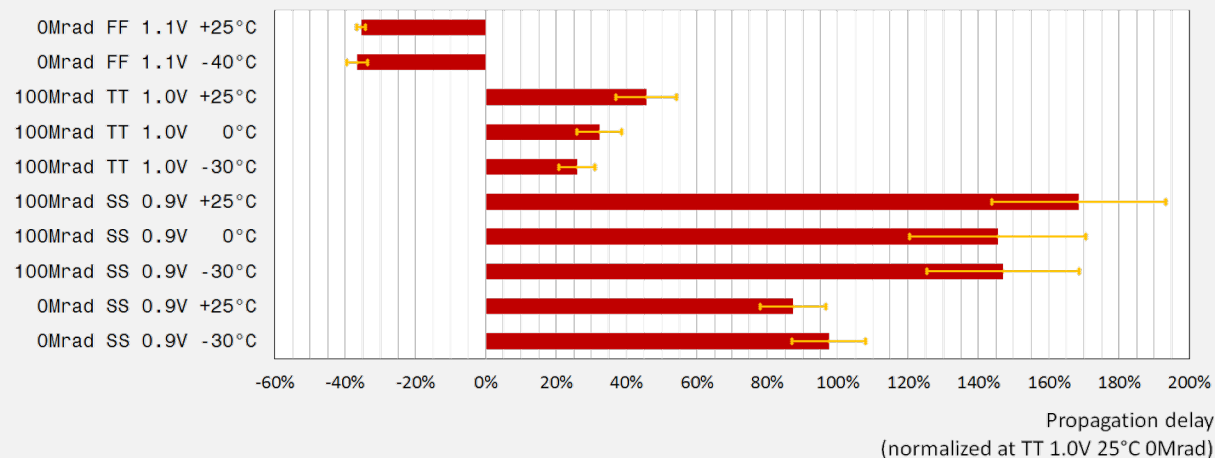
- A custom memory compiler allowed to generate a SRAM with cell transistor featuring nMOS $W > 200\text{ nm}$ pMOS $W > 500\text{ nm}$
- Protection against latch-up is reached by placing p^+ guard bands between n^- regions.

Usage of **ELT** devices in input stage:

- To prevent the **radiation induced drain-to-source leakage** current increase due to the charge trapped in the shallow trench isolations (STI).
- To **mitigate the 1/f noise** increase on irradiated devices due to side-effects of the STI region in nMOS operated at low drain current.

Digital library choice and delay corner comparison

- Supply voltage scaling
- 9 tracks library chosen as compromise between power consumption and radiation tolerance
- Temperature inversion effect prevent the SSA from using a high-Vt library cells at 0.9V.
- Mix of standard-Vt and low-Vt digital cells at 1.0V+10% as compromise of power consumption, memory operation and propagation delay at -40°C



Single Event Effects tolerance

State machines

- Triple module redundancy (FULL)
- Triplicated Clock-trees
- Triplicated Reset distribution
- FF minimum distance 15um

Latch FIFOs

- Control and header fields triplicated
- Data latches not protected

Data pipeline

- No SEU protection applied due to limited power budget

Clock tree

- Clock tree triplicated
- The non-triplicated logic uses the **voted clock** in critical areas
- The non-triplicated logic **uses one of the branches** in non-critical areas:
 - Simplify scan-chain insertion
 - Helps in reducing buffering for hold fix (power)
 - Allow for CPPR on the 3 branches

Triplicated pads for

- Clock
- Control
- Reset
- Scan-Chain IOs

Configuration registers

- Triple module redundancy with error detection and self-correction
- Clock enabled only during
 - asynchronous readout operation,
 - configuration operations
 - self-correction

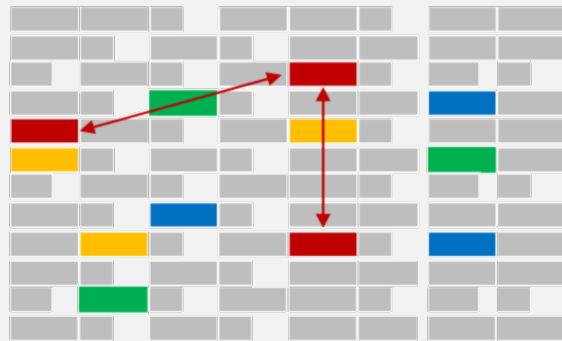
Glitch filters

- Reset inputs
- TEST-MODE signal
- Scan-chain TEST POINTS control (on the control of the **system clock / test clock selection multiplexers**)

Single Event Effects tolerance

Physical implementation

- Use of **instance space groups** among triplicated registers
- **Avoid logic simplification** by synthesis and P&R flow
- Spacing for clock and reset buffers in all periphery logic



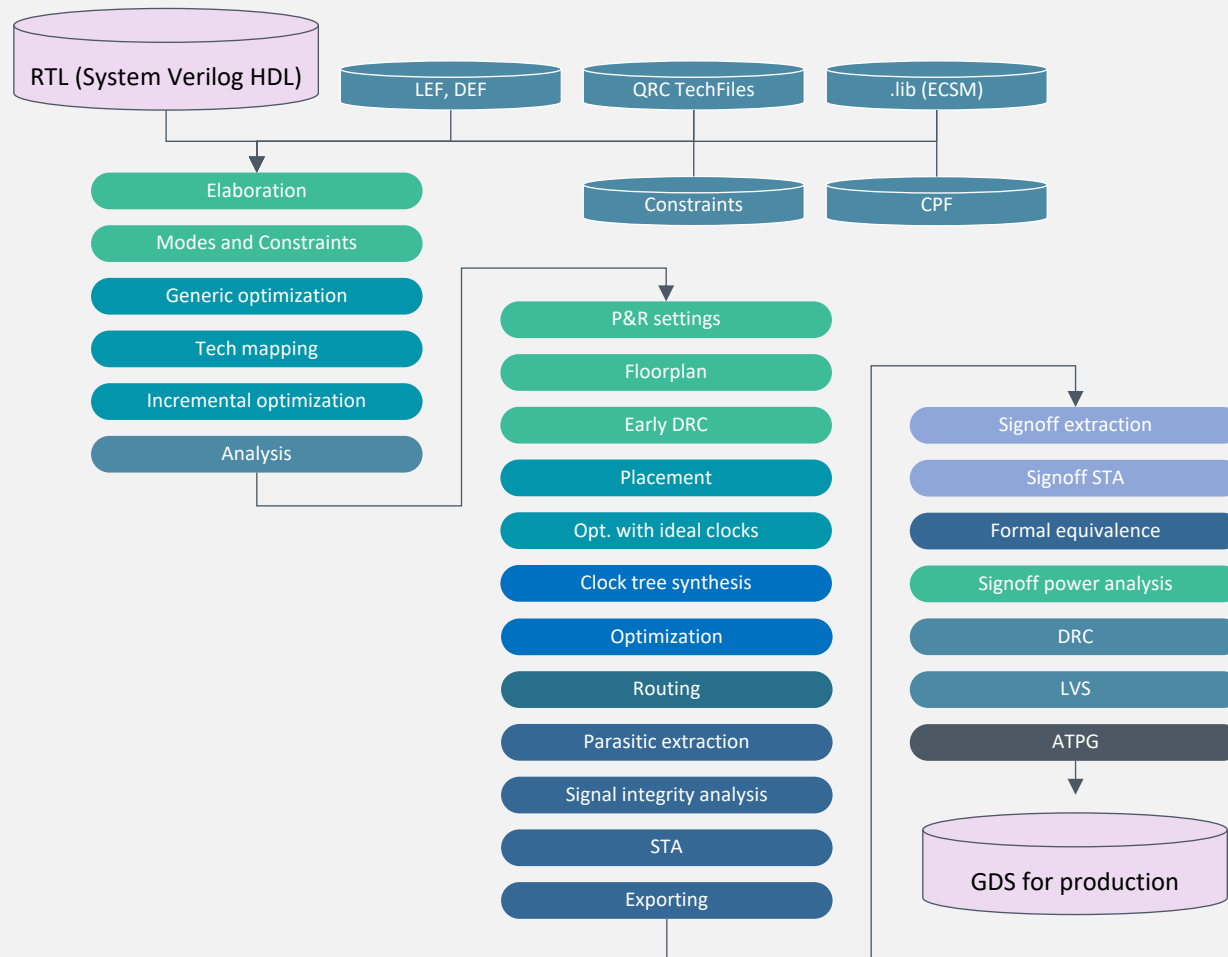
Functional simulation

- System Verilog UVC for **randomize the injection** (constrained from the specific test case)
- The **randomization is constrained** accordingly: Error probability, average SEE rate, minimum time split, etc..
- Injection of single event effects in **multiple ASICs at the same time** to evaluate the consequences that SEE in an ASIC have on the other ASICs part of the chipset
- Possibility to focus the SEU injection on particular module or subsystem and evaluate the **effect at system level**
- Possibility to inject SEU in **hundred of cells per clock cycle** (register grouped in non-interacting categories)

Additional checks

- Script to verify that no triplicated instance is optimized out
- Script to verify placement constraints after chip assembly

Physical Implementation flow



- Digital-on-top design flow
- Hierarchical implementation
- Multi supply voltage $1.0\text{ V} \pm 10\%$ – $1.2\text{ V} \pm 10\%$
- 3 independent power and ground domains to reduce noise coupling with guard-ring isolation
- Multi-Vt design (Low-Vt used only in critical timing arcs)
- C4 bump floorplan + wirebond for wafer probing
- Complex CTS and timing closure due to triple clock tree balancing and SEU hardening
- Constraints for TMR and digital cells placement
- Skew balancing among triplicated and voted clock trees
- Strip cell sampling clock guarantees $<200\text{ps}$ skew in all corners
- Non-default CTS rules to mitigate cross-coupling
- QRC extracted information already at the optimization stage due to design size

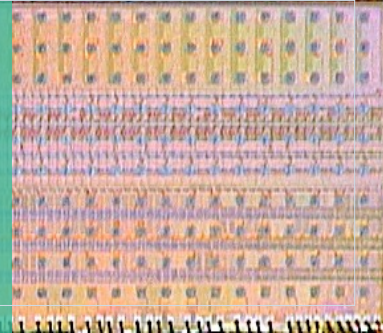
The ASICs

SSA2 ASIC

Short-Strip readout ASIC
for the CMS OT

DESIGN AND TESTING TEAM:

G. Bergamin • A. Caratelli • D. Ceresa
• J. Kaplon • K. Kloukinas • S. Scarfi

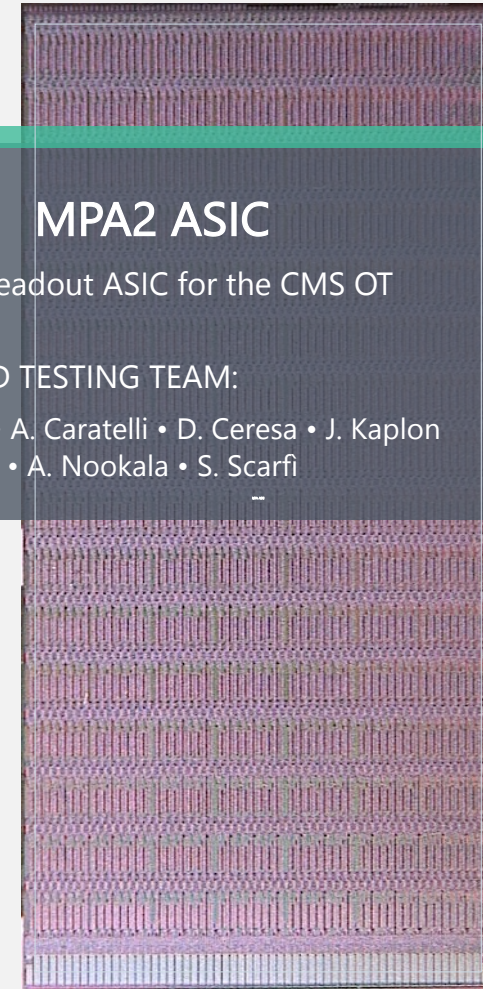


MPA2 ASIC

Pixel readout ASIC for the CMS OT

DESIGN AND TESTING TEAM:

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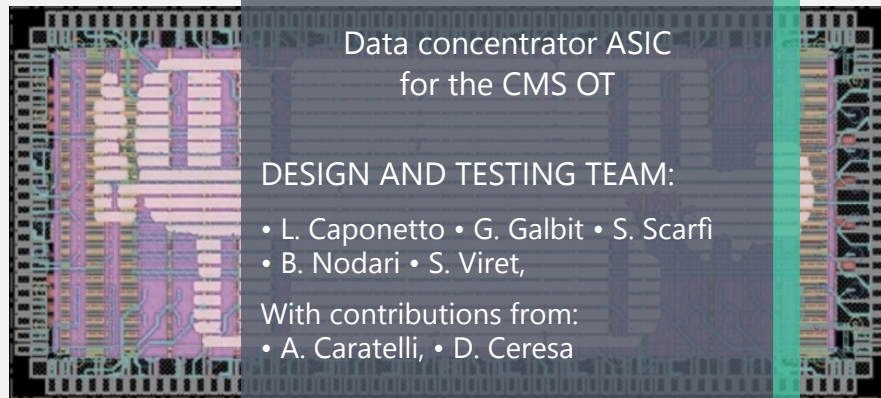
CIC2 ASIC

Data concentrator ASIC
for the CMS OT

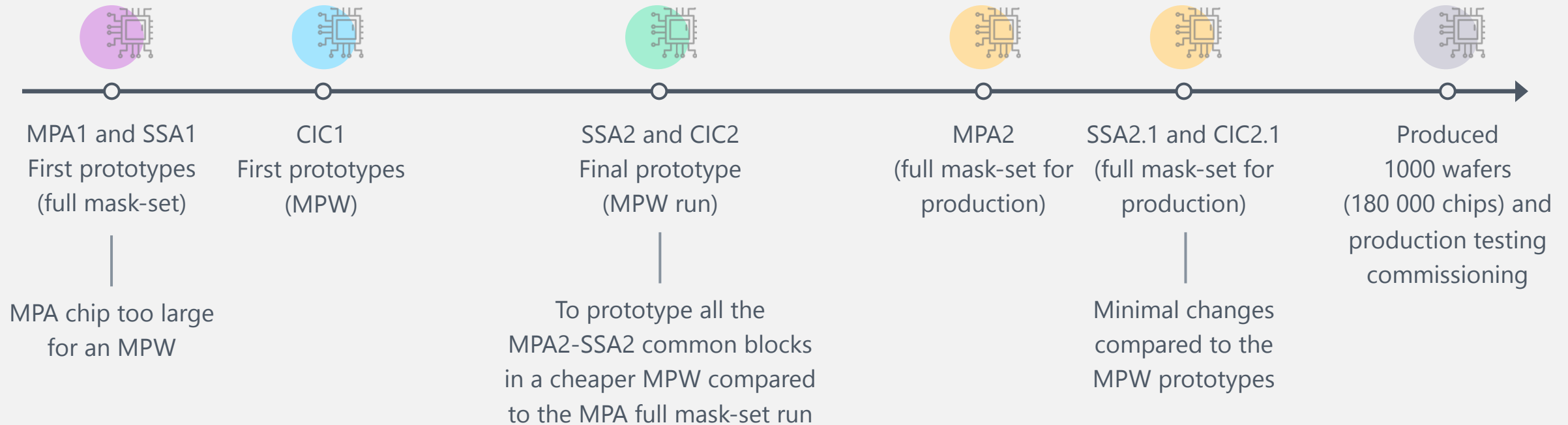
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With contributions from:
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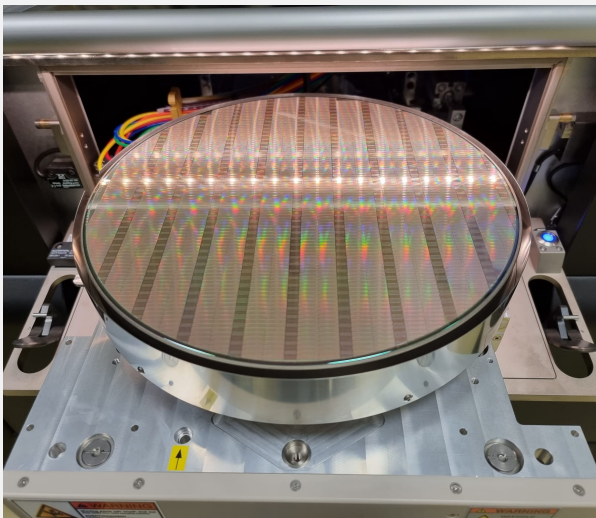


MPA-SSA-CIC Timeline



ASICs testing

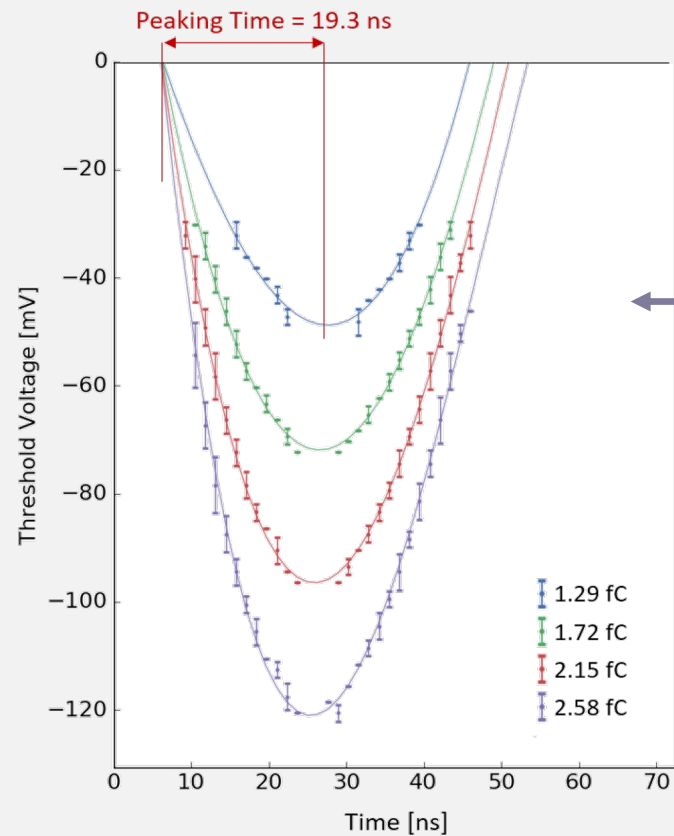
- The SSA, the MPA and the CIC were produced in a full mask-set engineering run
- The first 6 wafers have been tested at CERN by the ASICs designers
- Test routine includes:
 - Scan-chain test for production defects
 - Analog bias parameter characterization
 - Noise analysis
 - Functional test of digital circuits
 - Front-end characterization
 - Serial ID and trimming in e-fuses
- The wafer have been diced and the chip bonded on carrier boards for radiation tests and detailed cractarization



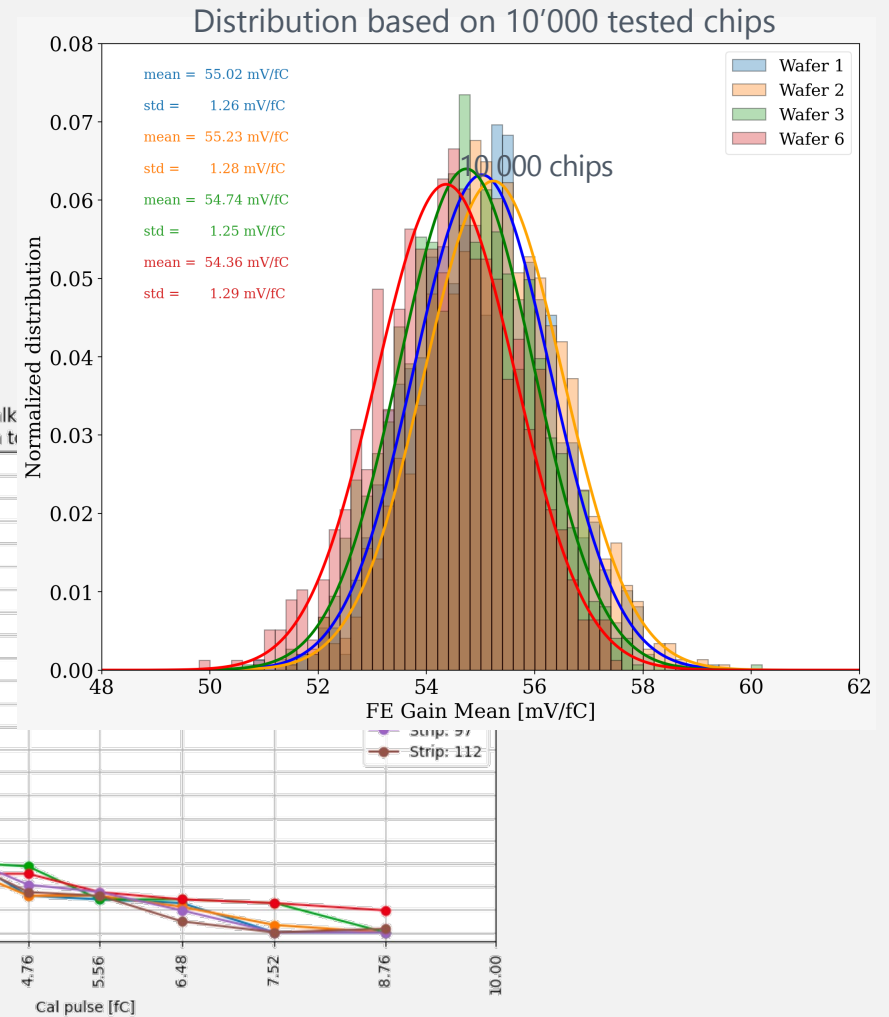
SSA test results

Shaper pulse reconstruction

by injecting a known charge via the SSA calibration system and acting on threshold, calibration pulse delay-line and clock deskewing DLL.

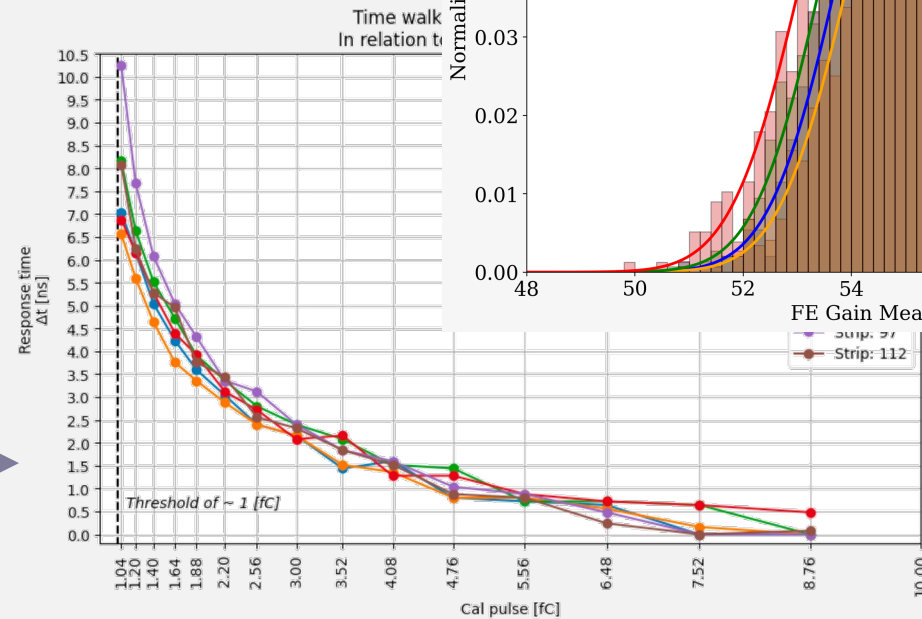


Gain distribution
for a non-trimmed SSA ASIC



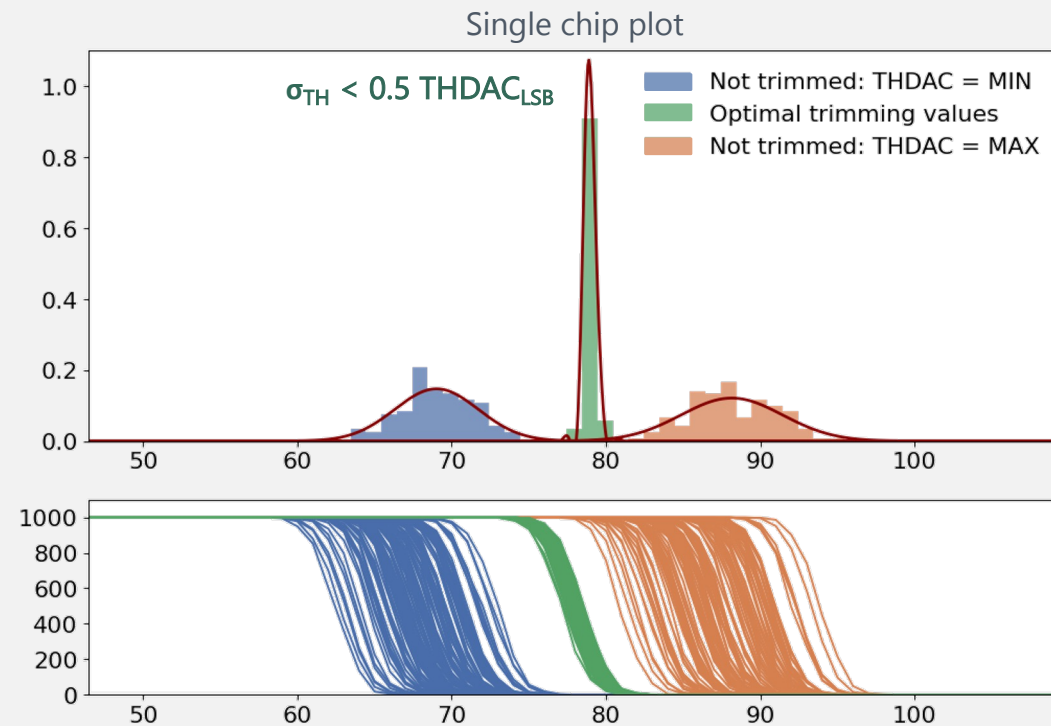
Peaking time < 25ns
with linear behavior
and up to 8fC

Time walk



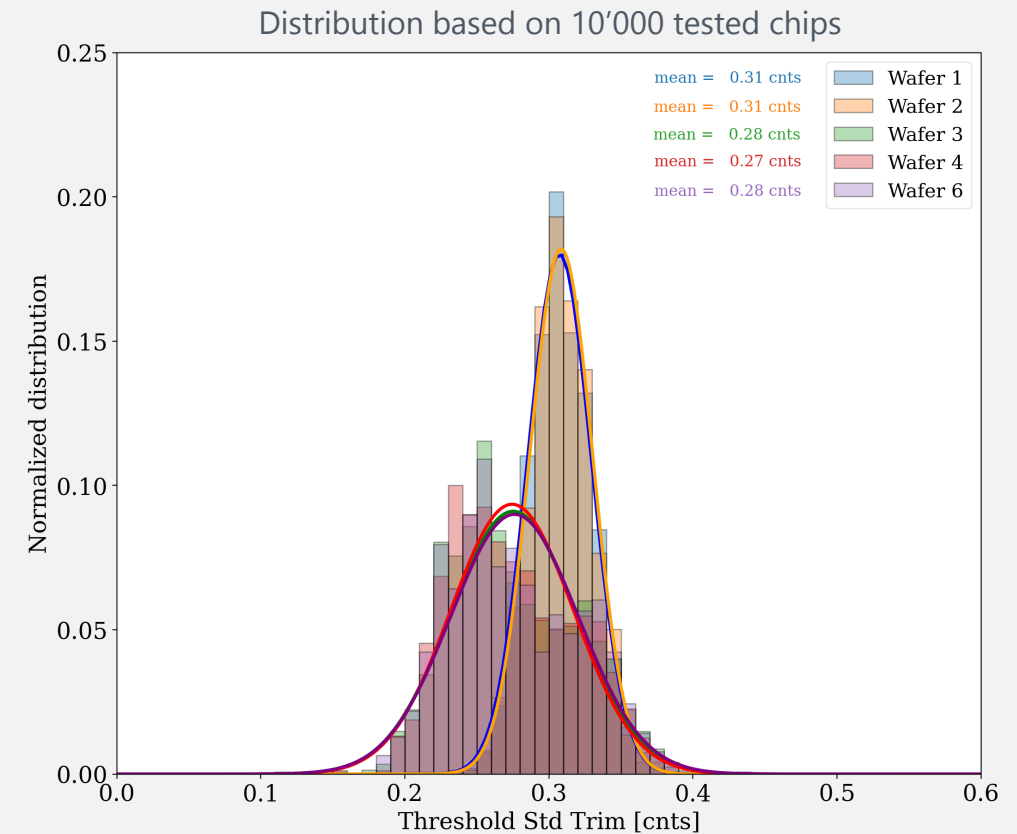
MPA-SSA test results

SSA Threshold trimming procedure



Trimming performed at 2.0 fC.
Threshold spread evaluate for 2.0 fC and 1.25fC

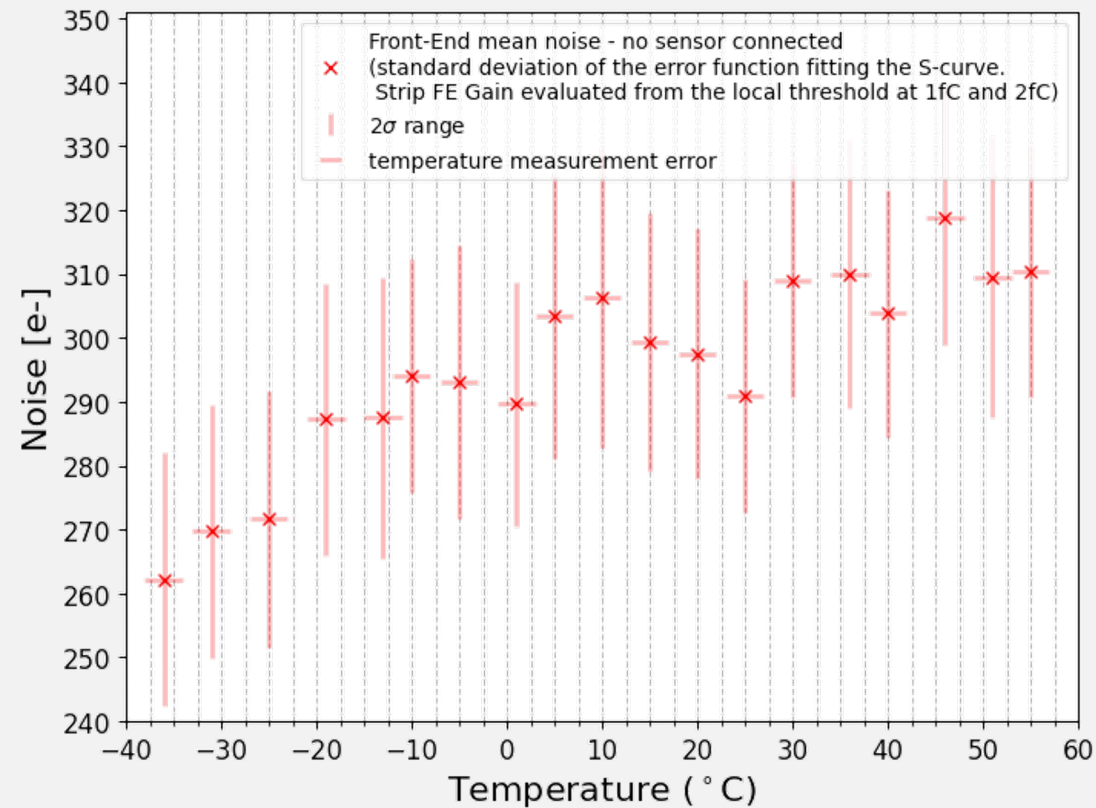
SSA Threshold distribution after trimming



MPA-SSA test results

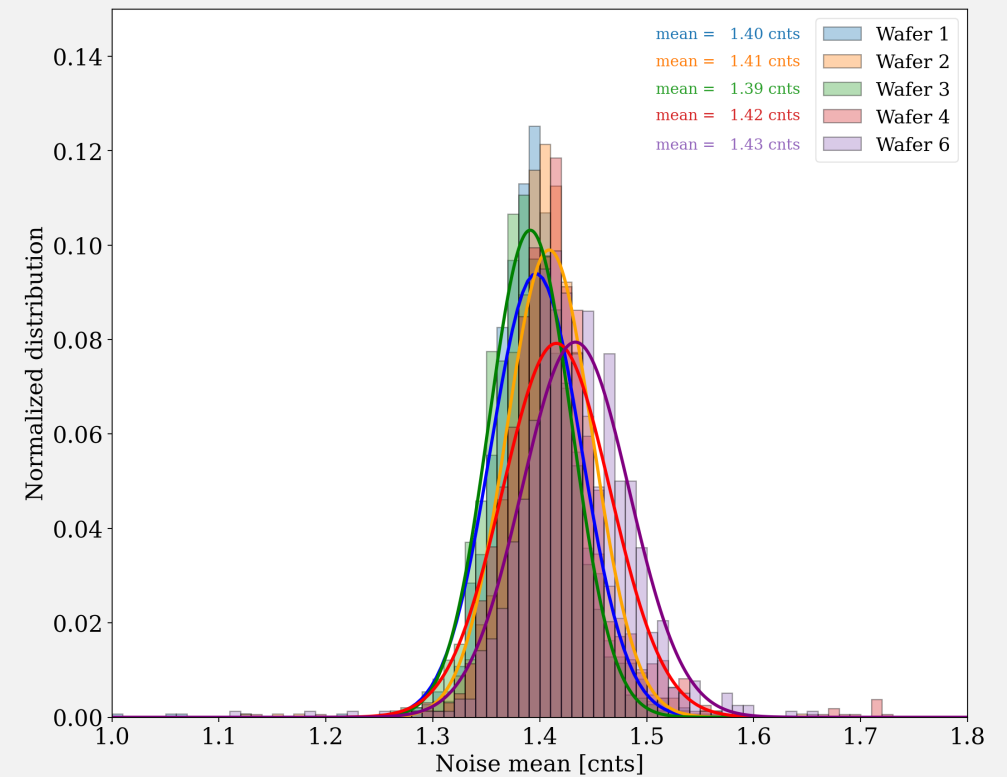
SSA Analog Front-End Noise vs Temperature

Plot based on 3 tested chips in climatic chamber



SSA Front-end noise measurements

Distribution based on 10'000 tested chips

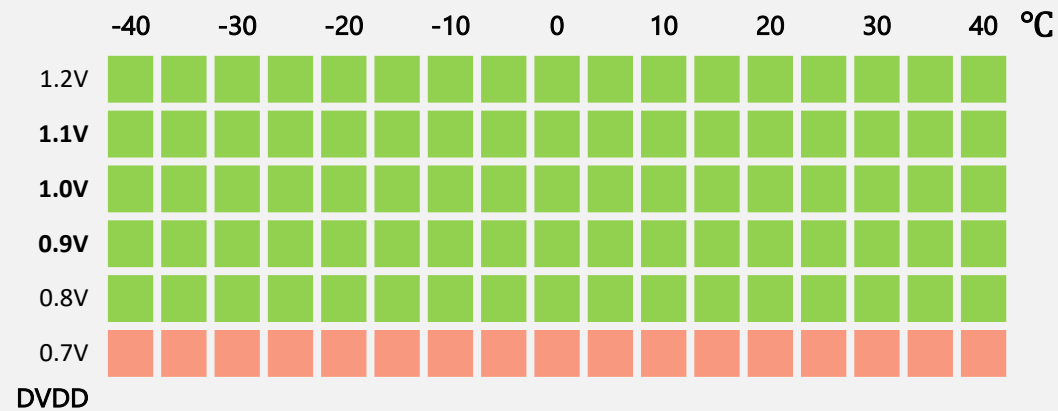


Channel input noise evaluated as the standard deviation of the error function fitting the S-Curves (1.25 fC and 2.0 fC)

MPA-SSA test results

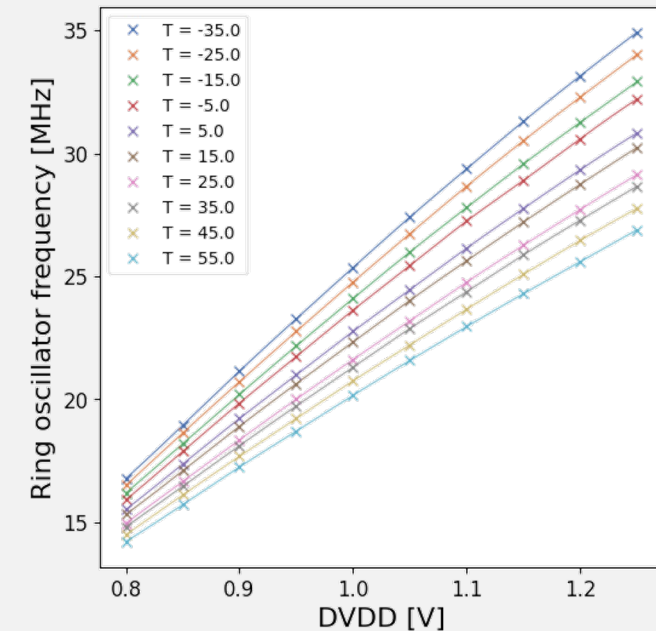
Temperature Characterization summary

- No errors or timing issues observed on digital logic



- No errors or issues observed in analog FE
- Bias structures variation within compensating range
- FE noise change within expectation

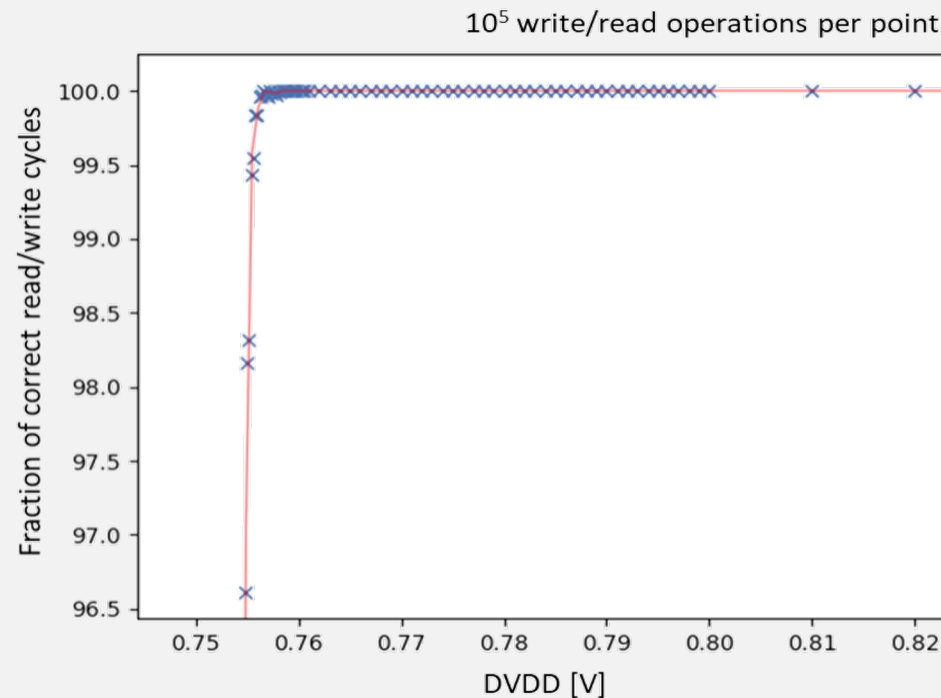
- Full set of digital functionalities tests
- Tests of memories (with BIST) and configuration
- Characterization of all bias parameters
- S-Curve for FE Gain, Noise and Trimming
- ADC, E-Fuses, Voltage swipes and several others



MPA-SSA test results

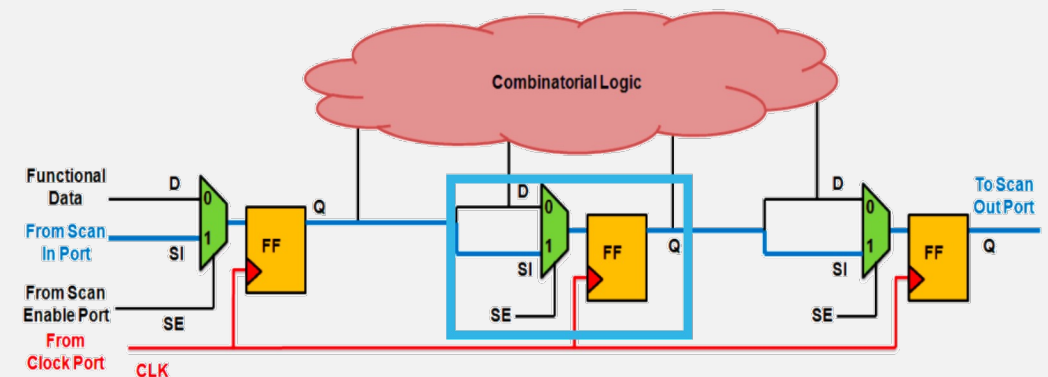
Memory Built-In-Self-Test

- Test full memory functionality in <1 ms
- Results saved in internal registers accessible via slow-control
- Clock gating during normal operation (only leakage power)



Scan Chain

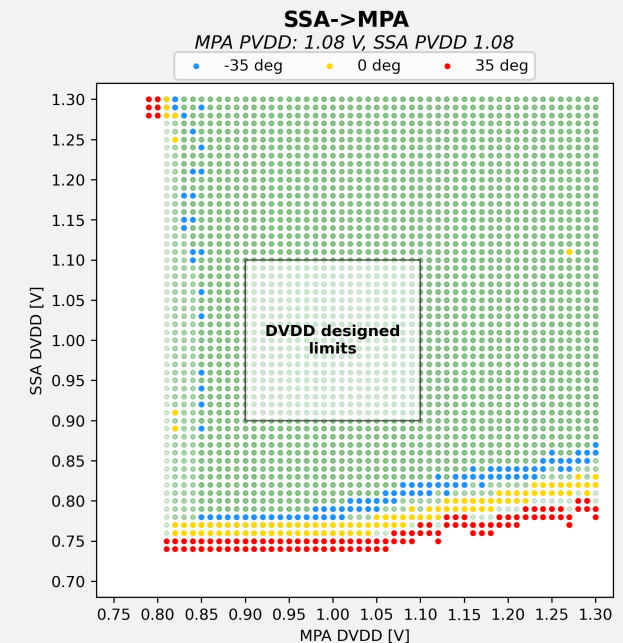
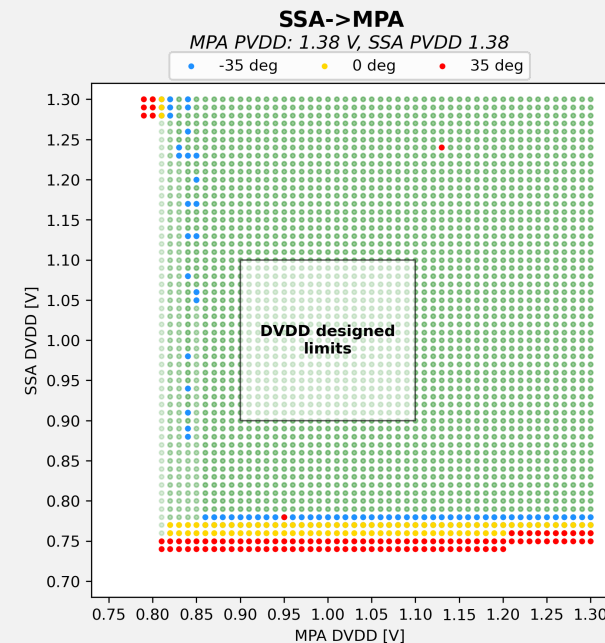
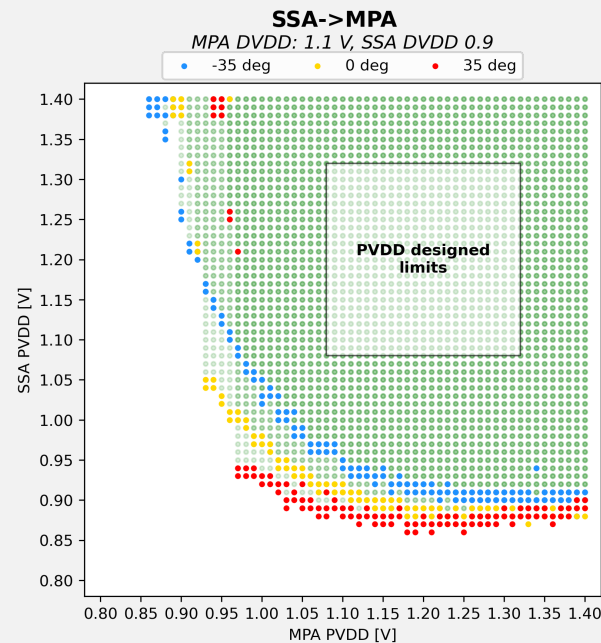
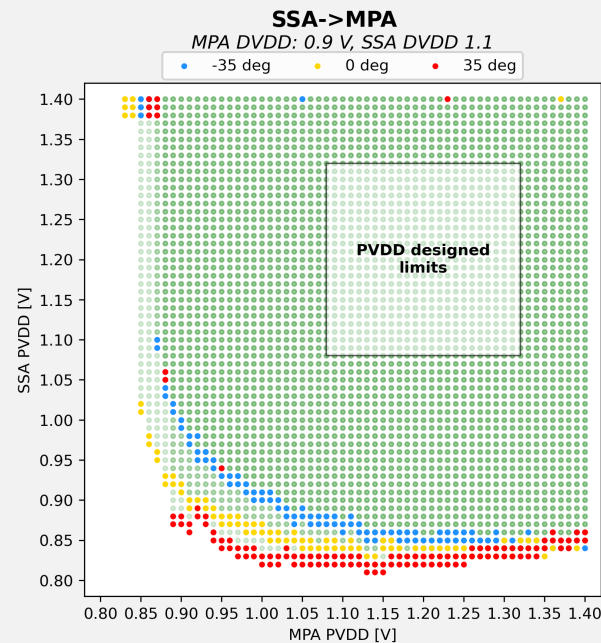
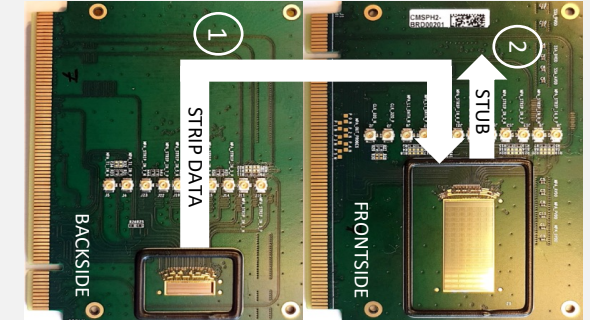
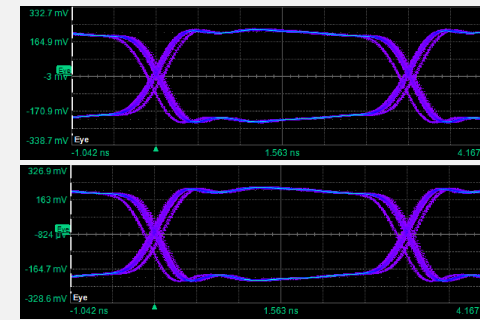
- 92% of fault coverage in SSA ASIC
- Custom approach for triplicated design
- SHIFT, RESET and CAPTURE tests
- A total of ~950 test vectors required
- Full test duration < 300 ms
- Scan-chain in SSA operates correctly up to 20MHz



MPA-SSA test results

SSA → MPA Communication

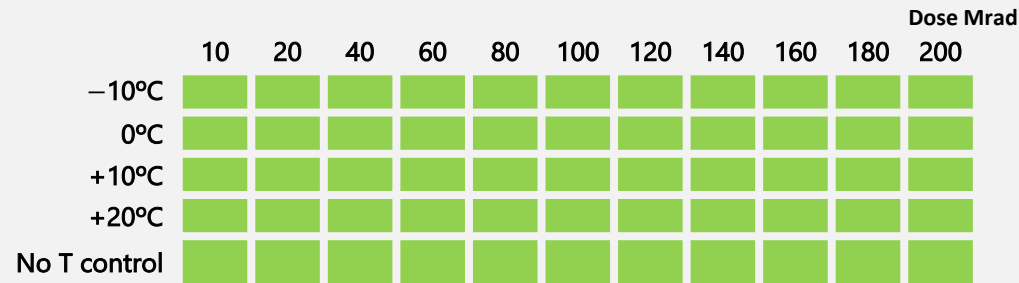
- No phase aligner at MPA input due to power restrictions
- The communication rely on precise design of the timing
- SSA-MPA communication timing was verified in static timing analysis and simulated post-layout in all cross-corner combinations (UVM verification environment)



Total Ionizing Dose characterization

X-ray TID Characterization summary

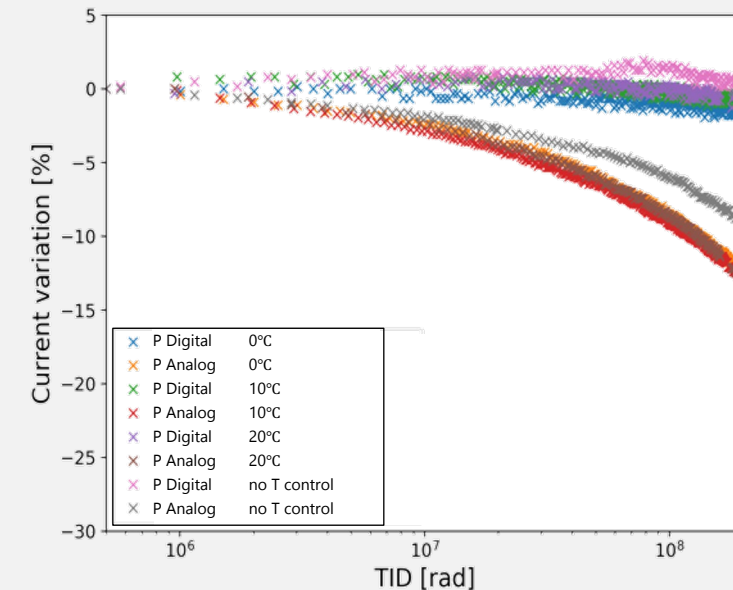
- 8 chips have been irradiated up to 200 Mrad
- No errors or timing issues observed on digital logic



- Bias structures variation **within compensating range**
- FE noise** change **within expectation**
- ADC reference voltage **variation larger then expected:**
 - Needed **changing the target reference voltage** to keep stable the DAC output up to 200Mrad.

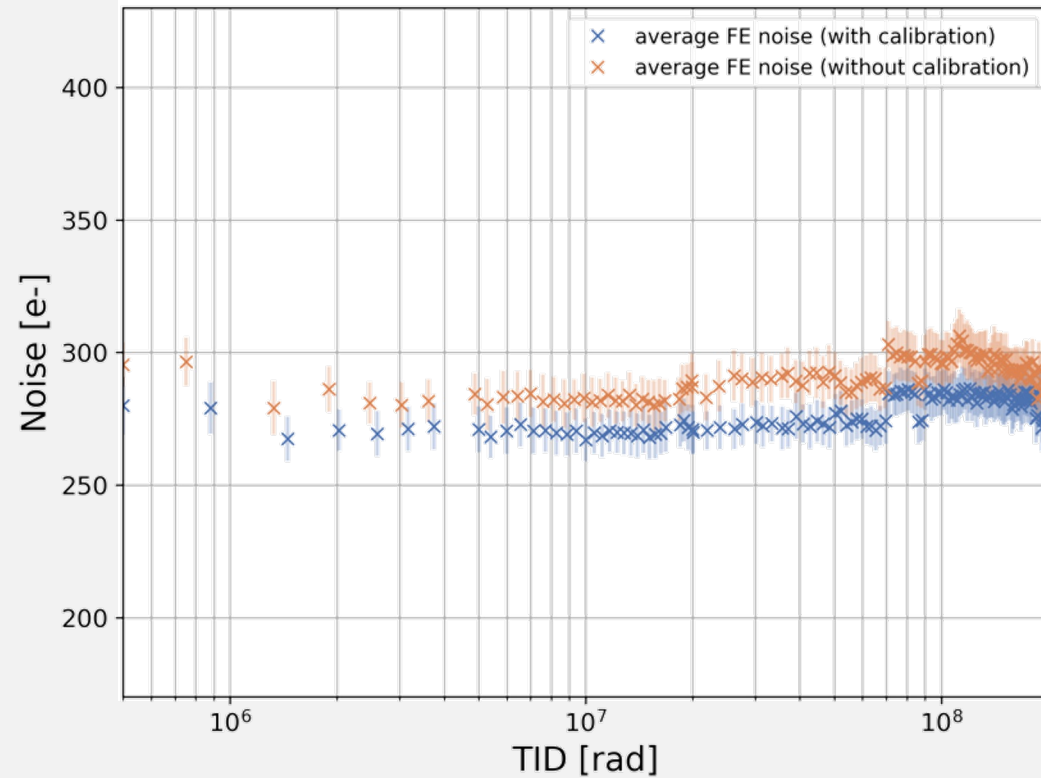
TID Test routine:

- Full set of digital functionalities tests
- Tests of memories (with BIST) and configuration
- Characterization of all bias parameters
- S-Curve for FE Gain, Noise and Trimming
- ADC, E-Fuses, Voltage swipes and several others

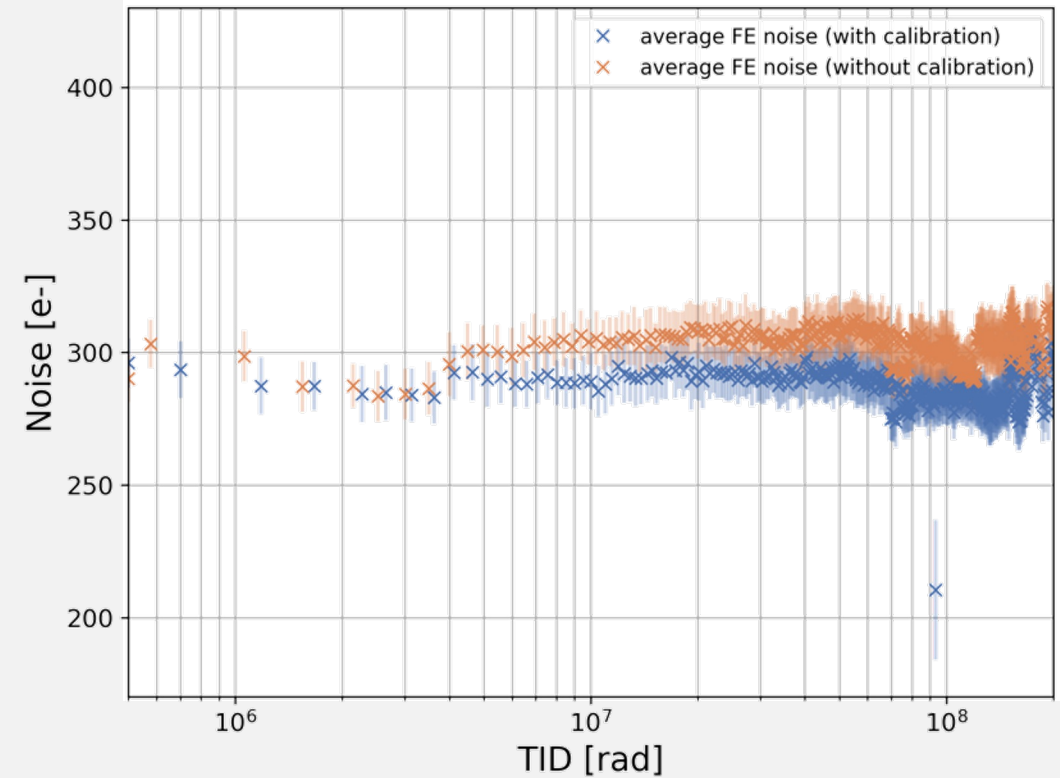


SSA Front-End equivalent noise evolution with TID and temperature

SSA 2.1 average FE noise* vs TID at -10°C



SSA 2.1 average FE noise* vs TID at +20°C

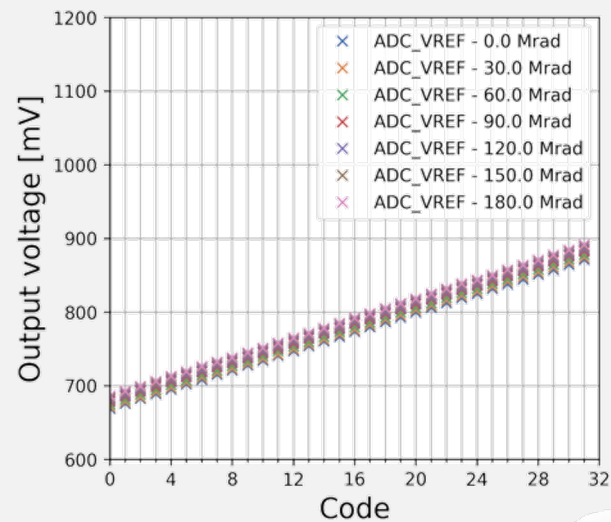
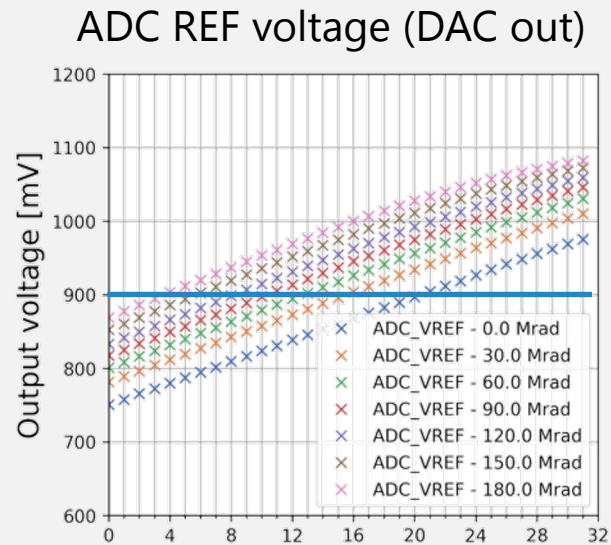


* FE noise evaluated on the S-Curves – 2 fC internal charge injection – Sensor inputs floating

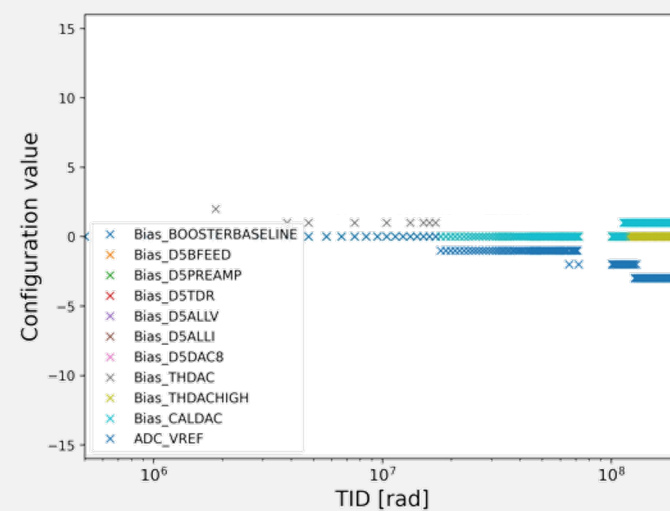
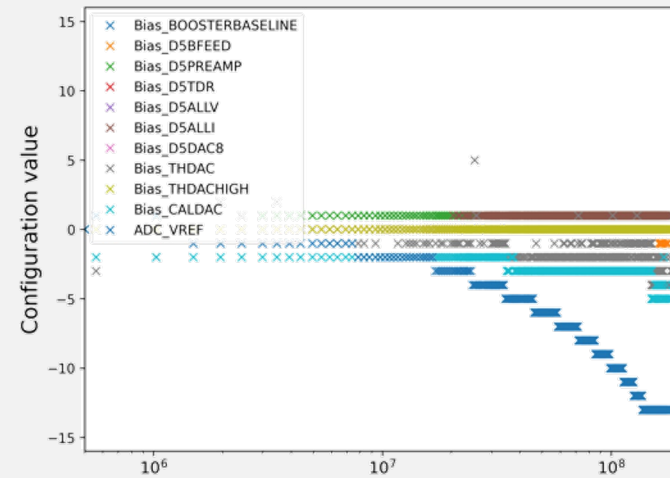
ADC reference voltage variation with TID (5-bit DAC for corner compensation)

SSA2.1

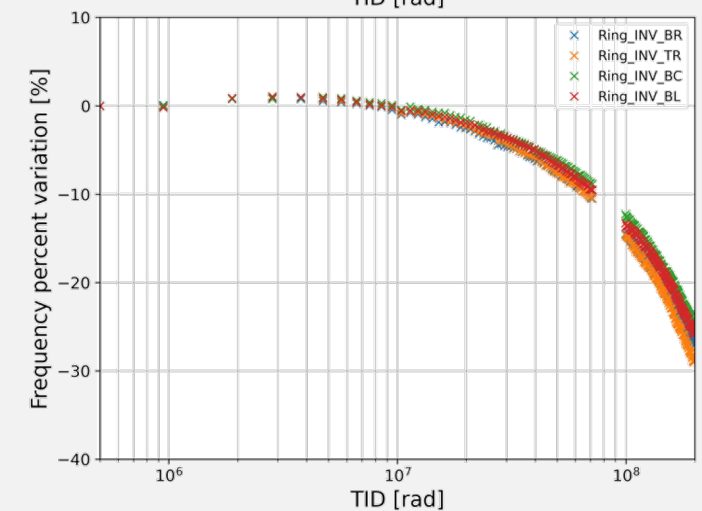
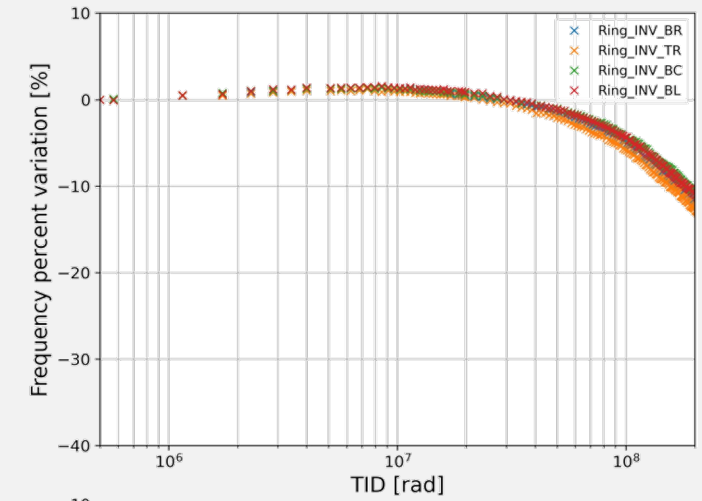
Production



Calibration value to compensate



Ring oscillators



SSA Single-Event Effect tests with heavy ions

SEE testing carried out in UCL at Louvain-la-Neuve, Belgium

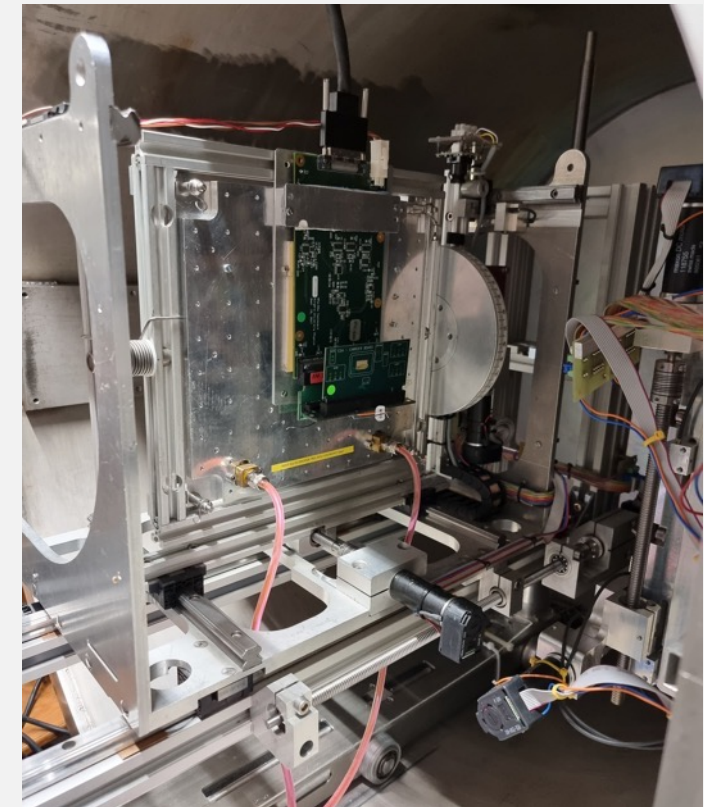
No hard errors observed

- No loss of control observed
- No loss of synchronisation observed
- No chip locks or control errors in general

Configuration system error-free

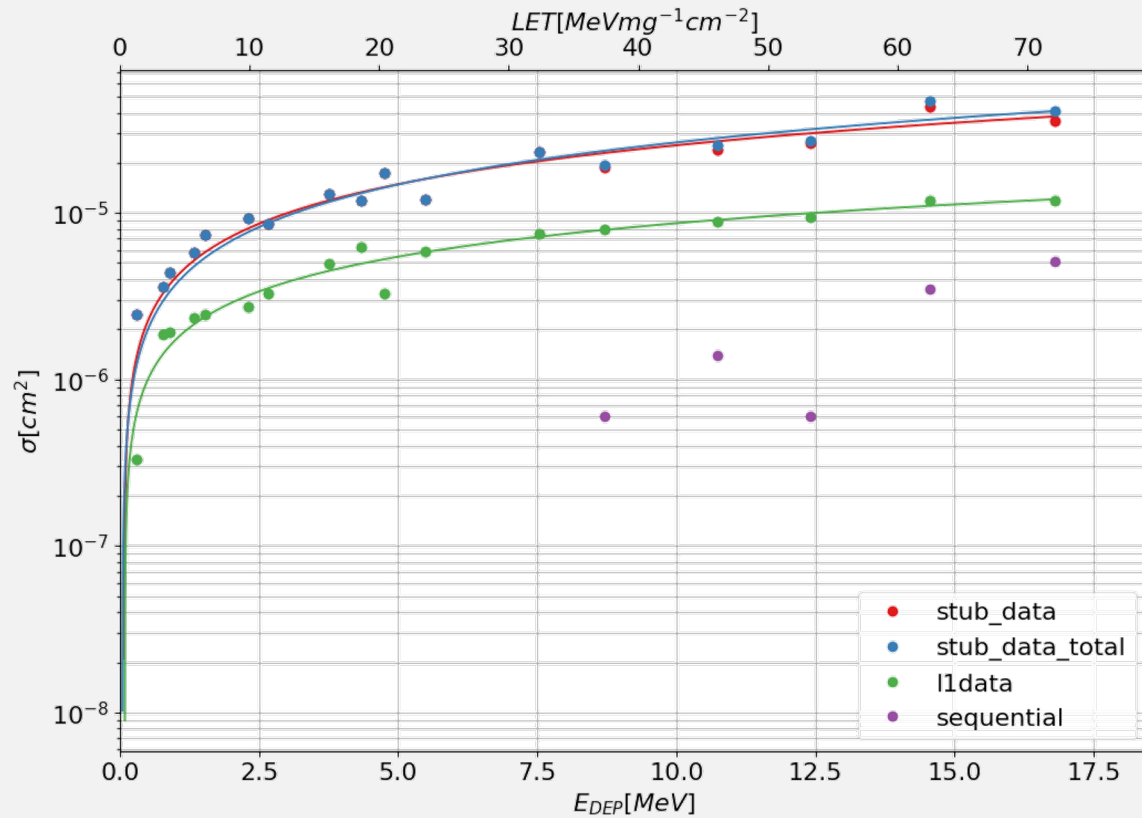
- Verified by readout and comparison of full chip configuration at each test iteration (30 seconds)
- SEU correction counter monitoring

Limit cross section for 10h test $\sim 5 \cdot 10^{-9} \text{ cm}^2$



SSA Single-Event Effect tests with heavy ions

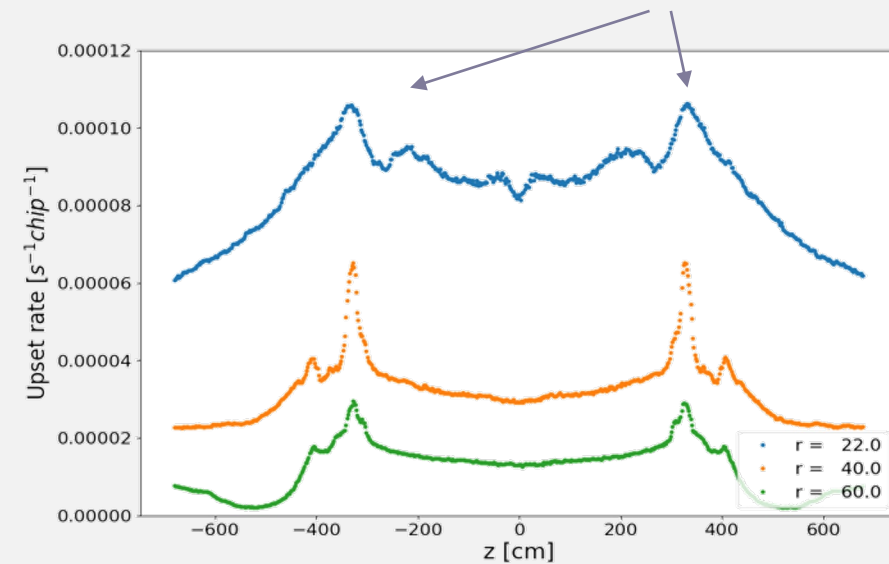
Stub and L1 data SEE cross-section:



Bit error rate estimation

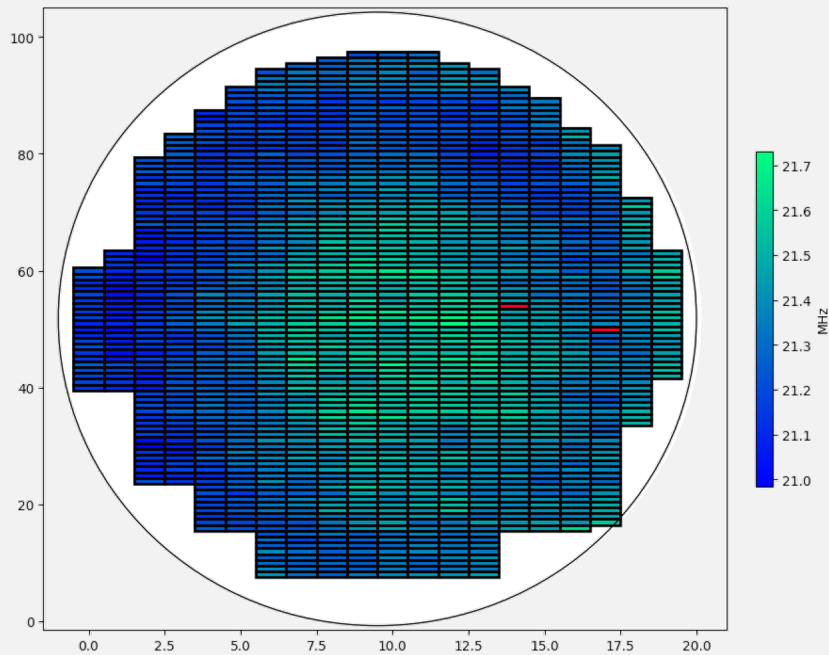
(based on OT fluxes from FLUKA simulation)

	Maximum SSA bit-error rate expected
Stub data	$1.2 \cdot 10^{-11} \text{ BX}^{-1}$
L1 data (12.6 us latency)	$1.0 \cdot 10^{-11} \text{ BX}^{-1}$
L1 data (2.5 us latency)	$9.7 \cdot 10^{-11} \text{ BX}^{-1}$



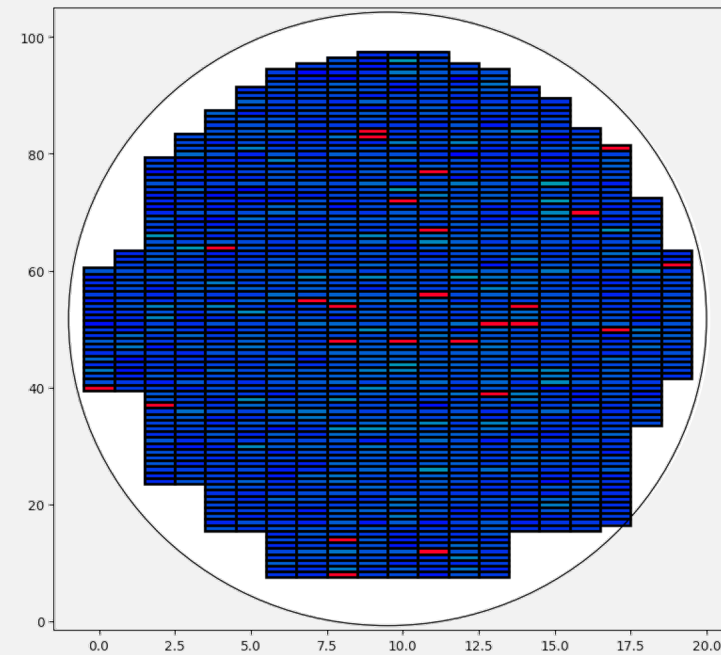
SSA Wafer Probing - process and analog performance

Ring oscillators Frequency



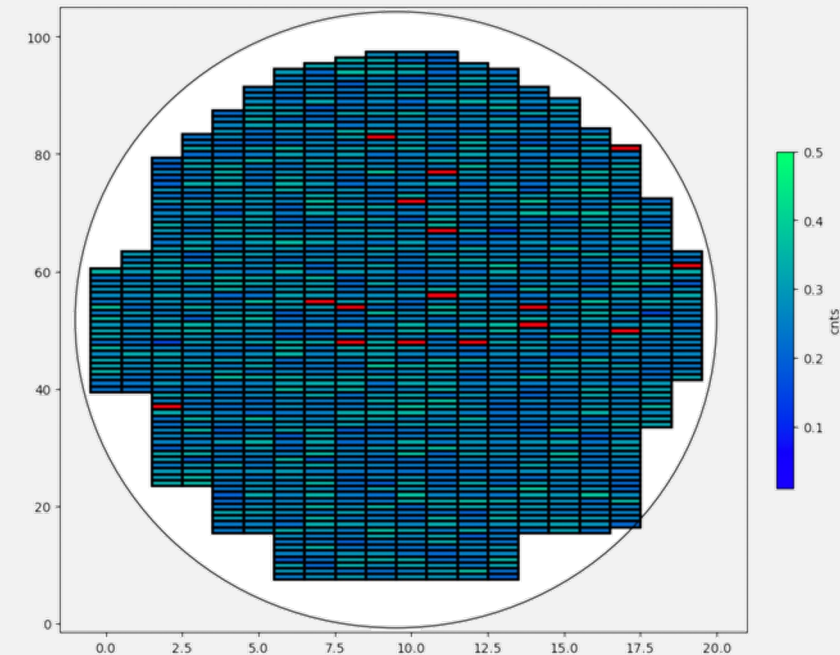
- The SSA includes different types of ring oscillator to monitor variations in: Process – Temperature – Total Ionizing Dose

FE Noise Performance Tests



- Map of the average FE noise
- Cut criteria noise < 1.7 LSB

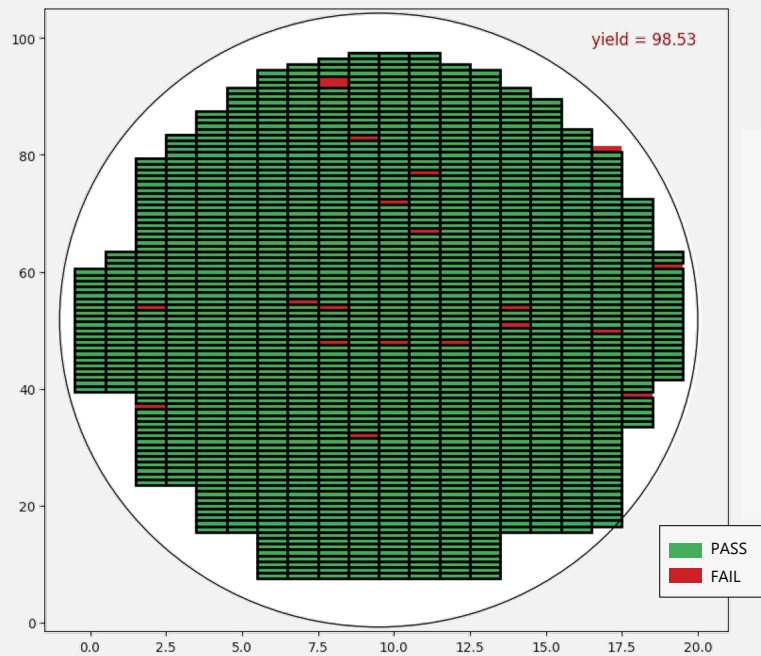
FE Threshold Trimming



- Map of the threshold spread after the trimming procedure
- Cut criteria $\text{std}(\text{Th}) < 0.5 \text{ LSB}$

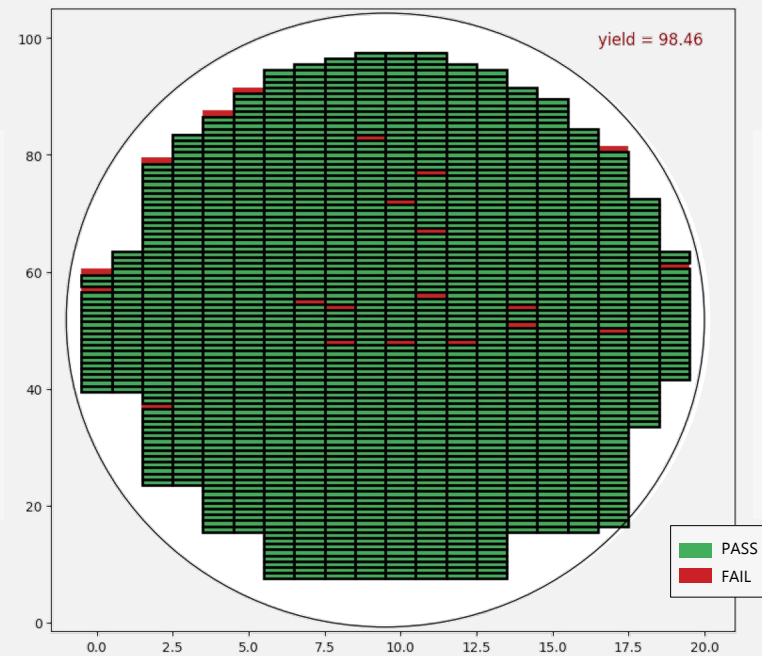
SSA Wafer Probing - yield

Digital Tests summary map



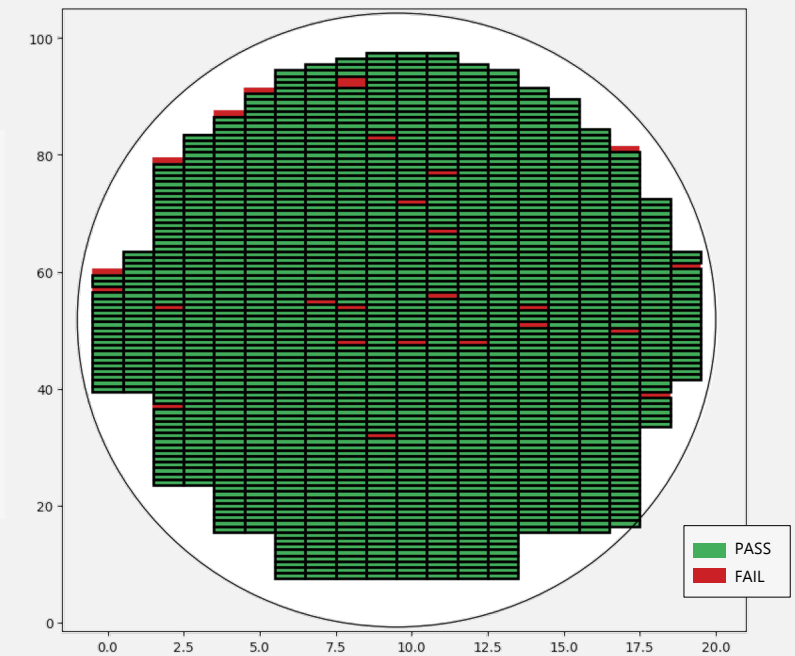
- Stub data [0.9V, 1.0V, 1.1 V]
- L1 data [0.9V, 1.0V, 1.1 V]
- Memory BIST [0.8V, 1.0V, 1.2 V]
- Configuration and all other digital functionalities

Analog Tests summary map



- Analog bias calibration
- FE functionality
- FE Threshold trimming
- Noise analysis

Total yield map



Overall yield (all tests) > 97%

MPA Wafer Probing - yield

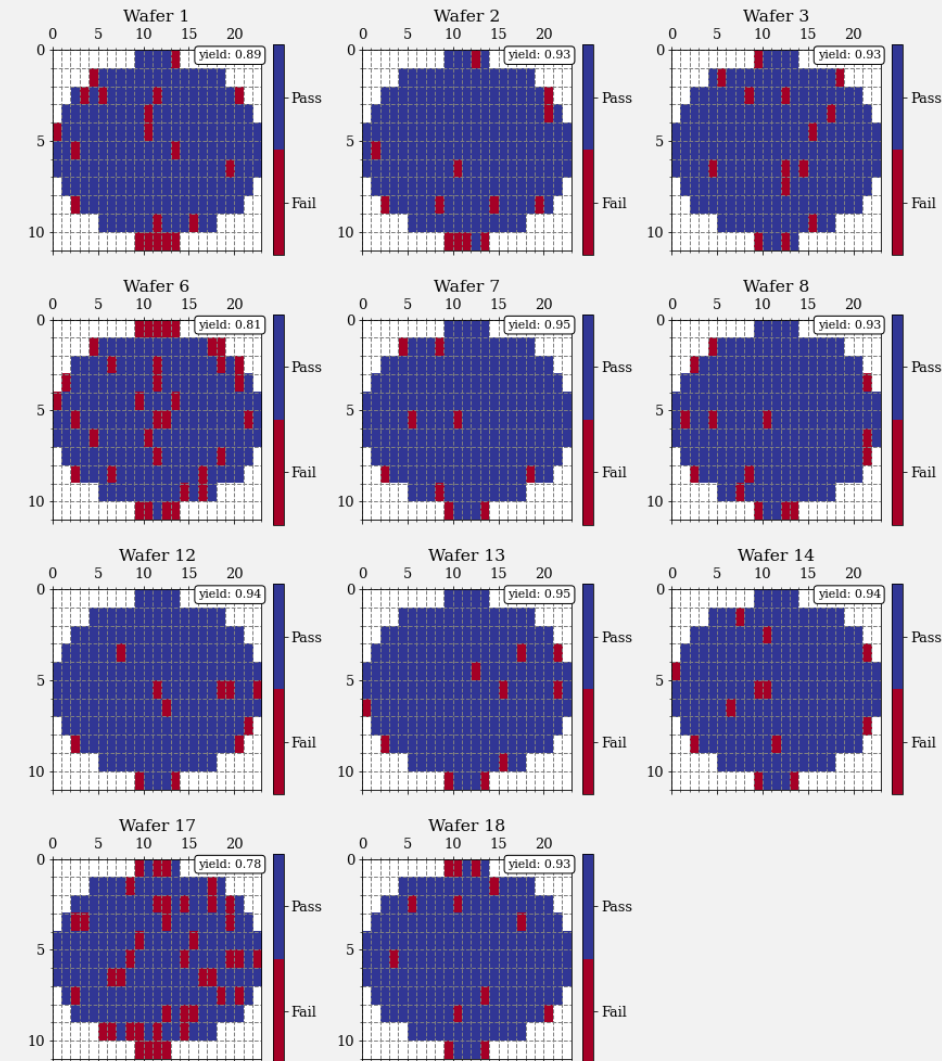
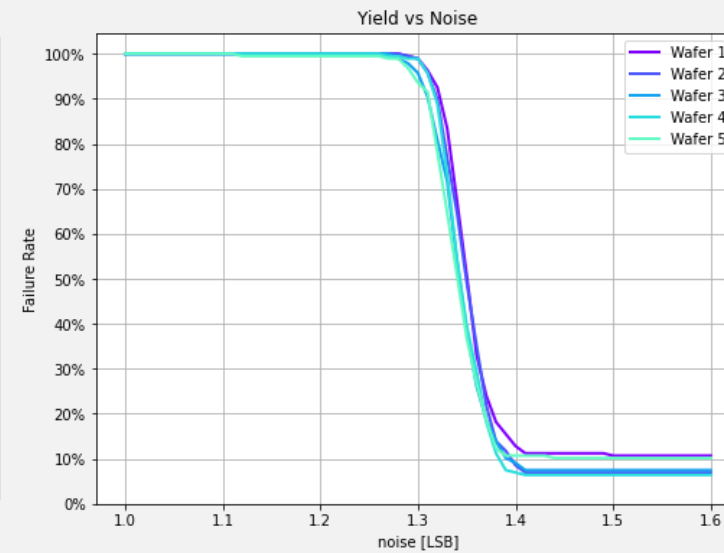
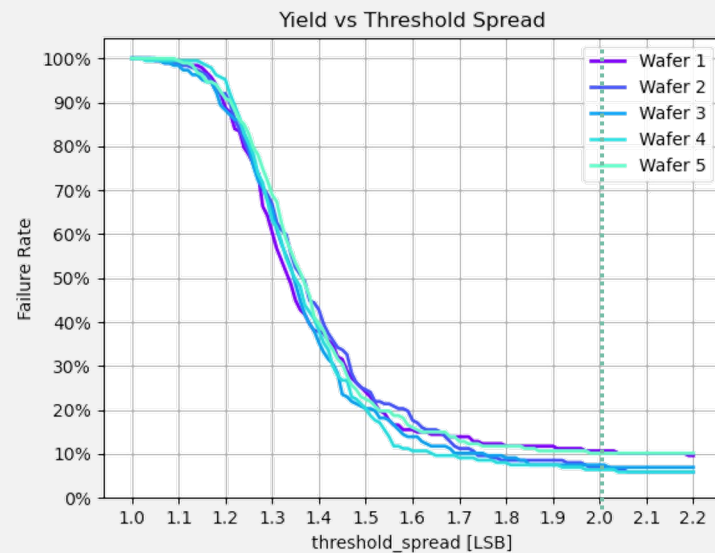
Criteria for passing:

- Pass all the digital and power tests
- Threshold Spread < 2.0 LSB
- Noise < 2.0 LSB

MPA2 Lot 1:

17 Wafers
3178 Chips

Yield $> 91\%$

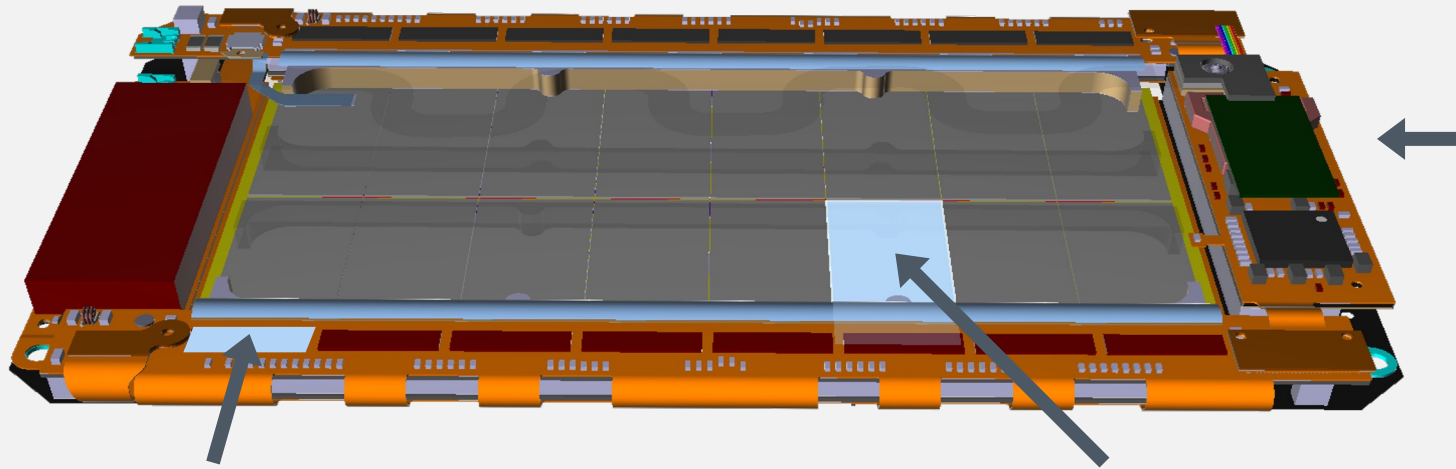


Summary

- System-level studies allowed to define the architecture of the PS-Module ASICs
- After testing the prototypes, the final version of the ASICs (MPA2, SSA2 and CIC2) have been submit to production in a full mask-set engineering run.
- The tests on the final version of the chips show results in agreement with the expectation
 - Front-end performances fulfil specifications
 - X-Ray TID test confirms radiation harness up to 200 Mrad
 - Heavy Ion test confirms the functionality of the chosen hardening strategy
 - Climatic chamber tests shows a parameter variation within the calibration range
- Wafer-level testing show a high yield, which allowed us to move to the next steps of ordering the production wafer and define the automated production test procedure.

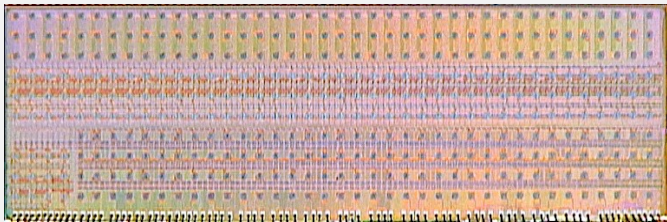
Production plans

- Testing for preproduction (1st lot 25 MPA wafers + 25 SSA-CIC wafers):
 - First 11 MPA tested by the ASICs designers for MAPSA preproduction
 - First 8 SSA-CIC wafers tested by the ASICs designers for module preproduction
- Testing for production
 - ~900 MPA wafers (300 already delivered) + ~200 SSA-CIC wafers (100 already delivered):
 - Wafer Testing for production will be performed at Rood Microtec:
 - Test procedure already defined by ASICs designers team
 - Probe-card currently in design by Rood Microtec (production 4-6 weeks estimated TAT)
 - Bumping will be performed at Winstek
 - Aiming for test system debugging in July 2023 and first 25 wafers tested by August 2023



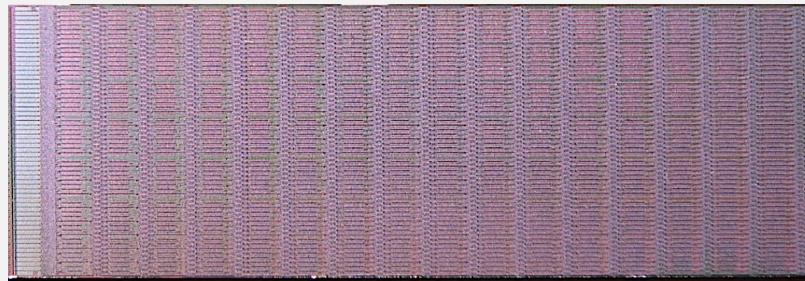
SSA ASIC

DESIGNED AND TESTED BY:
A. Caratelli, G. Bergamin, D. Ceresa,
J. Kaplon, K. Kloukinas, S. Scarfi



MPA ASIC

DESIGNED AND TESTED BY:
D. Ceresa, G. Bergamin, A. Caratelli, J. Kaplon,
K. Kloukinas, A. Nookala, S. Scarfi (CERN EP-ESE)



CIC ASIC

DESIGNED AND TESTED BY:
L. Caponetto, G. Galbit,
B. Nodari, S. Viret,
(IP2I Lyon university)

With contributions from
A. Caratelli, D. Ceresa S. Scarfi

