A Digitally Integrating Charge Pump Frontend with Pipelined Digitization and a Flexible Event-by-Event Hit Processing for Hybrid Pixel Detectors

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XII Front-End Electronics Workshop

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Introduction

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- Requirements of next-generation X-ray sources (ESRF, Diamond, XFEL, …) are challenging:
  Higher energies, higher photon rate
  ⇒ Next-generation sources need next-generation readout systems.

- We are presenting the **XIDer ASIC.**
- Collaboration with, and funding from ESRF in XIDer project.

- STFC about to join the collaboration ⇒ XIDer becomes XIDYN.

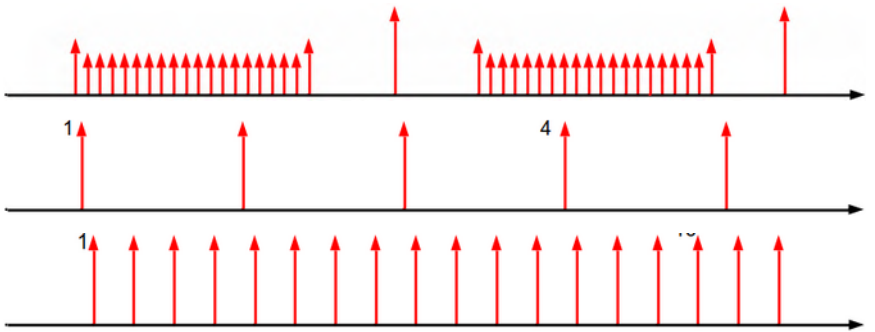
Motivation

“Flexible Event-by-Event Hit Processing“

- Sensor concepts are often similar, but the details vary: Sensor materials, photon energy, …
  ⇒ Flexibility needed in the analog frontend.

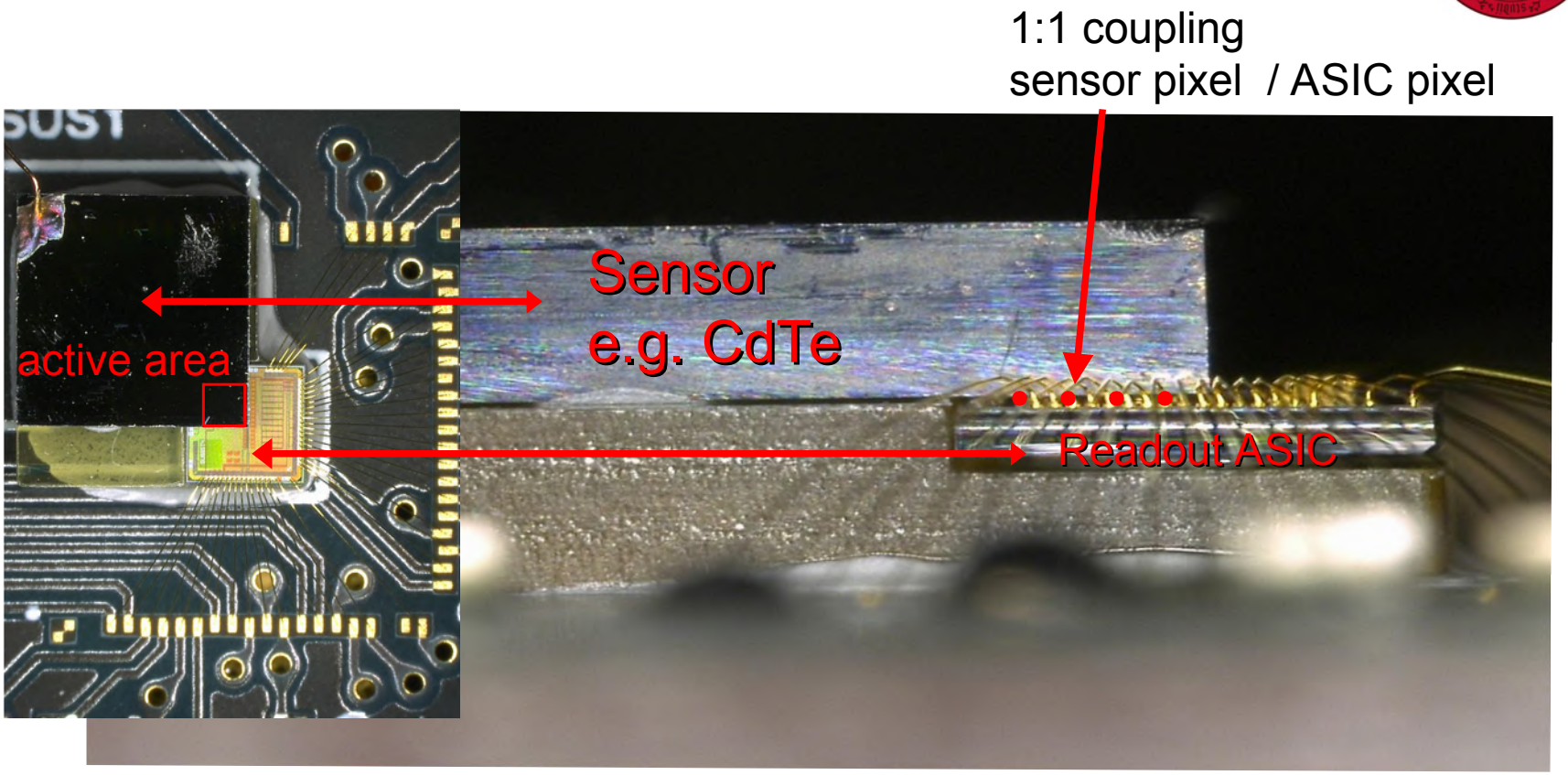
- Even a single machine has different run modes
  ⇒ Different timing requirements.

- Here: Trying to cover
  - ESRF & Diamond,
  - Cd(Zn)Te & Si,
  - high & low energy.
  - + some headroom in every direction to cover even more.

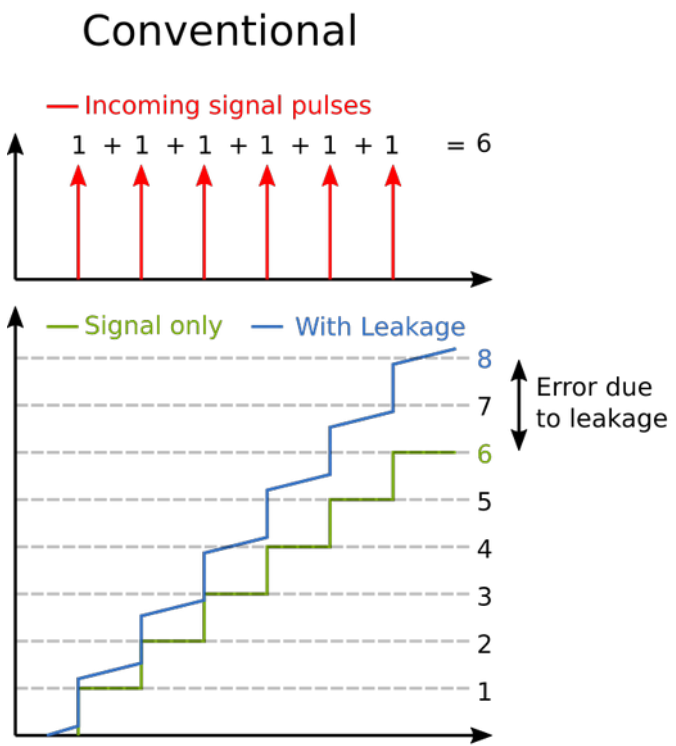


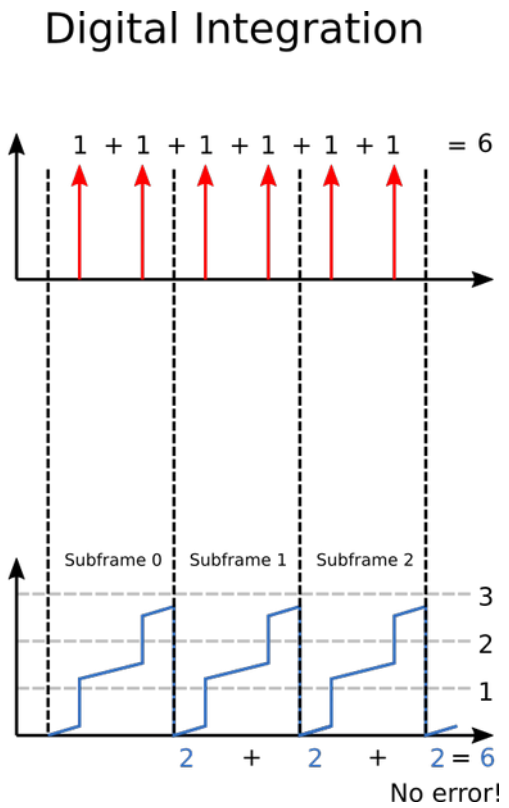
ESRF filling modes

Hybrid Pixel Detector



Frontend Concepts
Digital Integration

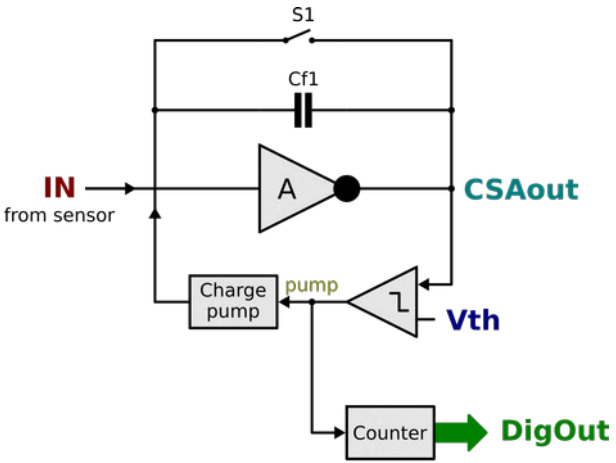


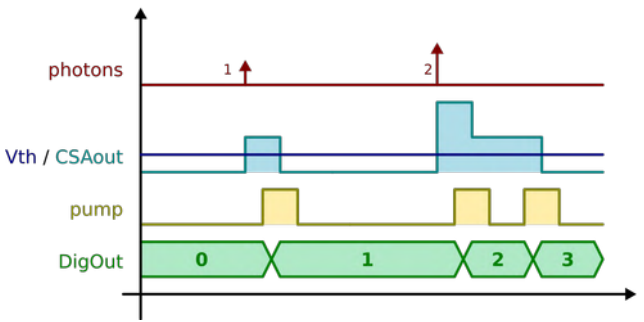


- Long integration times
  ⇒ noise / leakage accumulate
- **Digital Integration:**
  Integrate for short **subframes**, then add up the counts
  ⇒ Errors do not accumulate.

Frontend Concepts

Digital Integration with a Charge Pump



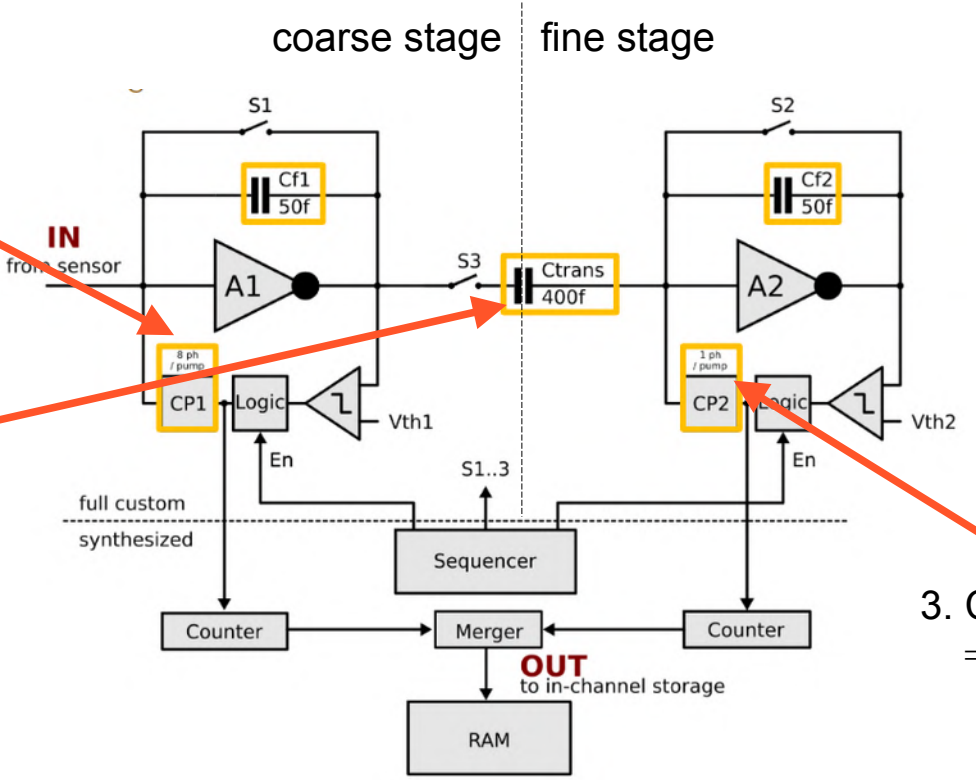


- Charge-sensitive amplifier (CSA) collects charge.
- Charge pump removes well-defined charge packets (eq. to *n* photons) from the input node.
- **Single-photon resolution** for *n*=1.
- **Infinite dynamic range** (ultimately limited by counter depth).
- Photon counting linearity only depends on charge pump.
- Mostly insensitive to CSA saturation.
- But: Pumping must be **fast** enough to handle the photon rate.

Frontend Concepts
Pipelined Digitization

1. Count in coarse steps
   ⇒ large range,
   high-rate capable

2. Transfer to second stage



Note:
Coarse and Fine stages run in parallel.

3. Count the remainder.
   ⇒ Single-Photon resolution

Did I miss anything?

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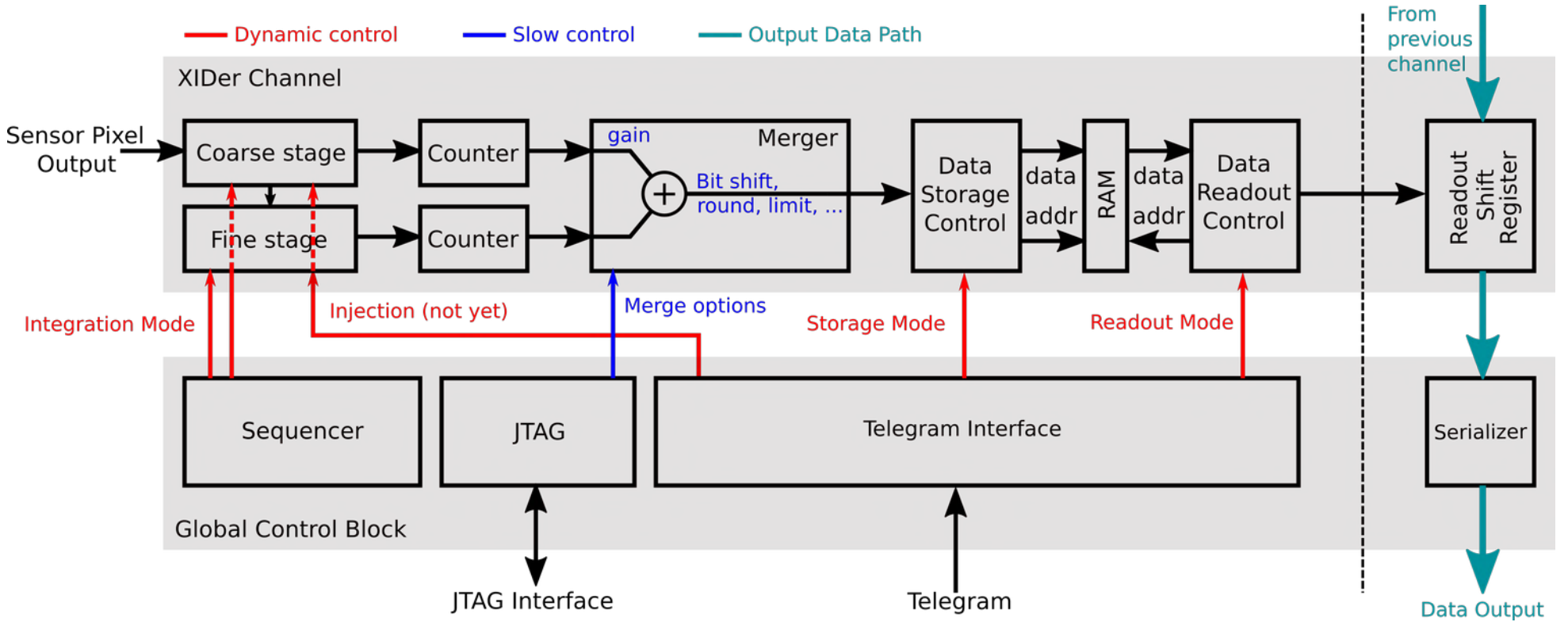
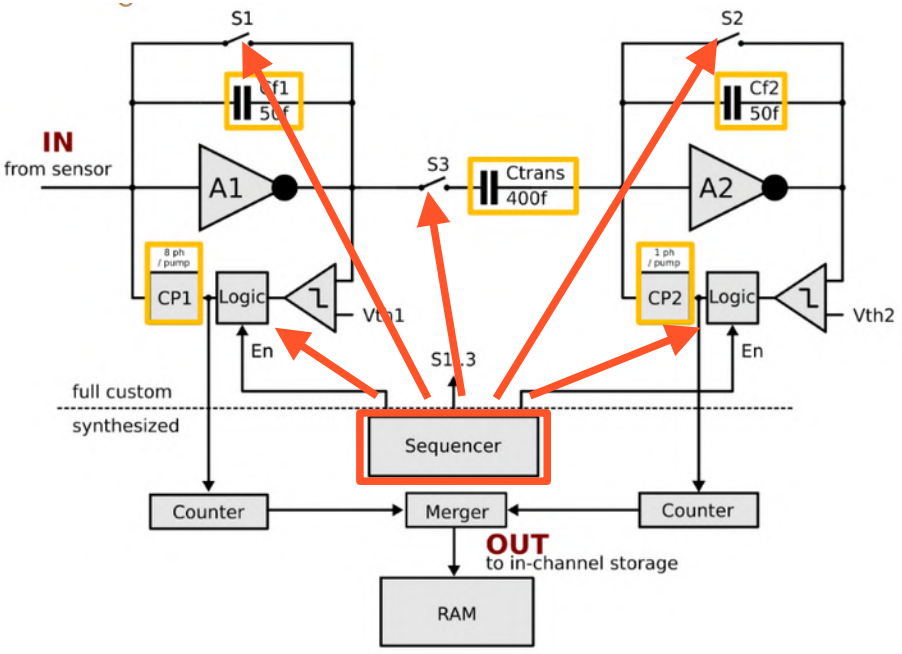
A **Digitally Integrating** ✓ **Charge Pump Frontend** ✓
with **Pipelined Digitization** ✓ and a
Flexible Event-by-Event Hit Processing ✓
for **Hybrid Pixel Detectors** ✓

XIDer ASIC Block Diagram



Concepts for Flexibility
Sequencer

- The analog frontends need precisely timed control signals to align the ASIC operation to the bunch structure.
- Many different bunch structures
  × many different measurements
  = A lot of different scenarios for measurements
  ⇒ many different sequences to be implemented.
- Too many to hardcode, many still unknown
  ⇒ make them programmable[1].
- Independently programmable „tracks“ with ~2.5 ns resolution.
  (DDR mode for slow digital clocks.)



[1] Stored in JTAG register.

Concepts for Flexibility
Data and Readout Handling

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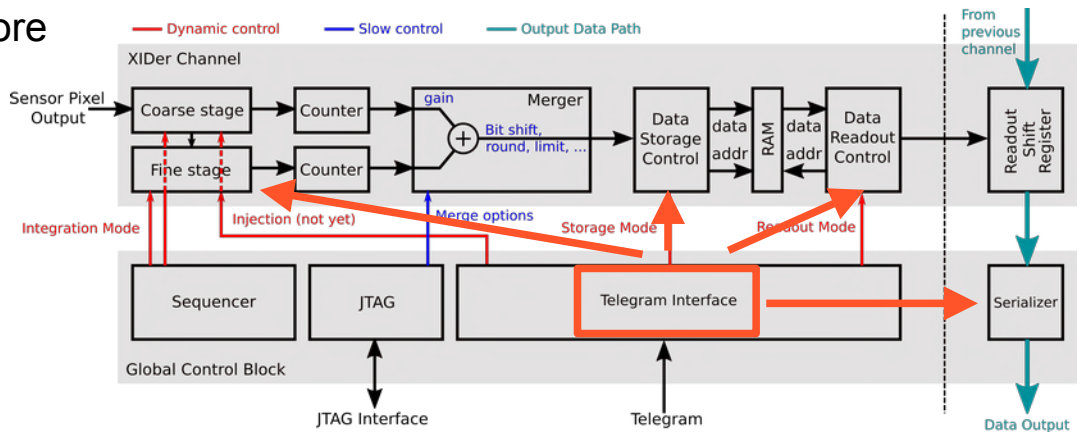
- After every subframe, the photon count is stored in the in-pixel RAM.
  Multiple modes available:
  - Store the count at the given address.
  - Add the count add the given address.
  - Increment the value at the given address + the current count: „Histogram mode“.

- Readout is always from the RAM (random access).

- This allows for several operating modes:
  - „Standard“ readout mode: Take a frame, immediately read it out.
  - Triggered mode: Keep history of frames at different RAM addresses, read out the latest frames on trigger.
  - Burst Mode: Fill the RAM with short frames, then read out (deadtime).
  - Histogram Mode: Store the distribution of different counts a different RAM addresses.

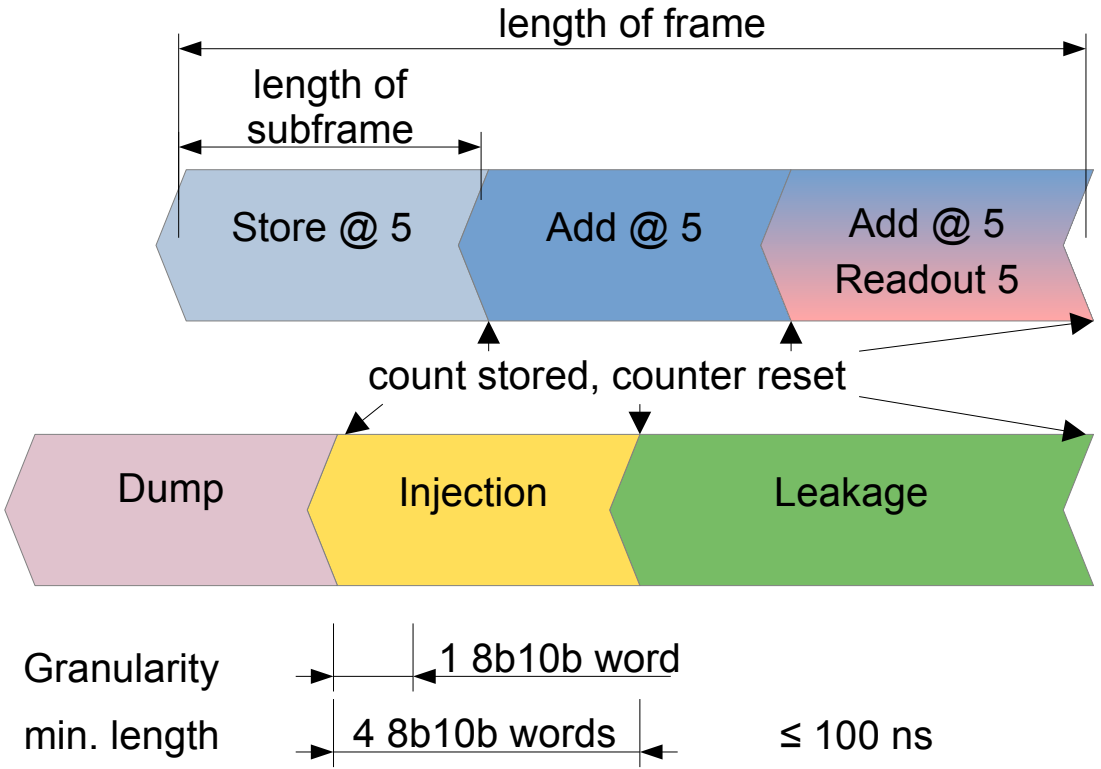
Concepts for Flexibility
Telegram

- Broadcast command stream to all ASICs.
- Each telegram defines the operations during one subframe (identical for all pixels).
- Orchestrating the different measurement setups in the digital domain.
  Synchronized to the sequencer handling the analog domain, and the synchrotron..
- Contains all data required during one subframe:
  - Length of the subframe (by sending fillers before the start word of the next telegram).
  - Data storage mode.
  - Start of readout.
  - Type of subframe (leakage, …).



Telegram Operation

Digital Integration Control & more



Telegram data stream into the ASIC.
During data taking:

- Defines how data are stored,
- and when readout is started.

Additional functions (from T7):

- Define a subframe as „leakage only“ ⇒ leakage calibration runs.
- Control test injections.
- Dump incoming charge for the duration of the subframe.

Bit clock derived from synchrotron frequency for sync. 400…880 MHz.

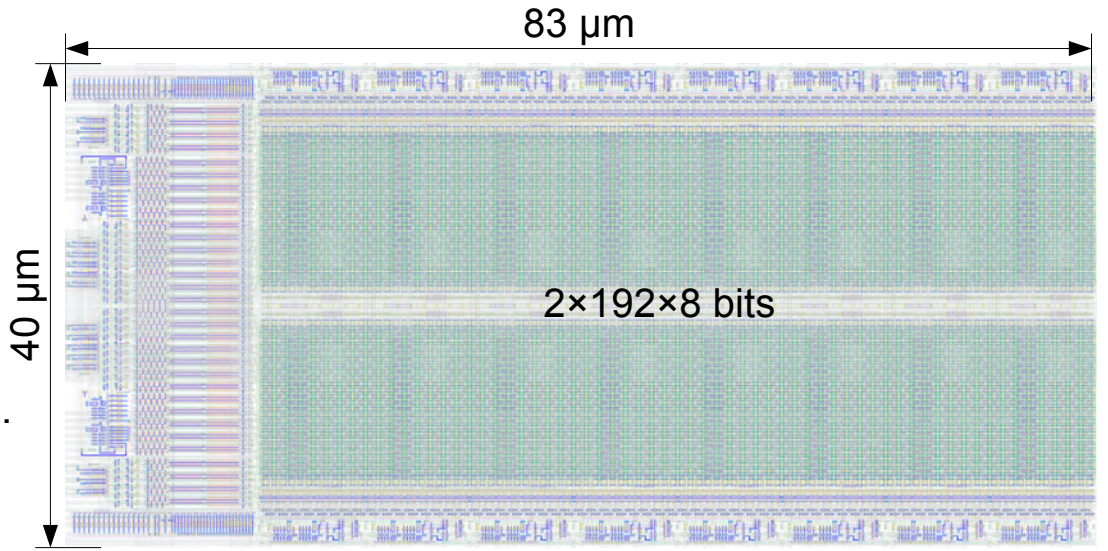
In-Pixel RAM

Unconventional full-custom RAM design.
Highly optimized for our usage pattern.

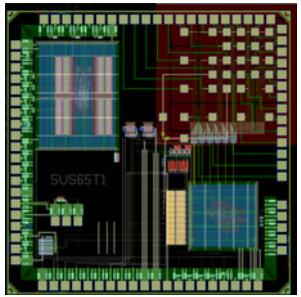
– Deliberately slow for low power consumption.
– No sense amplifiers.

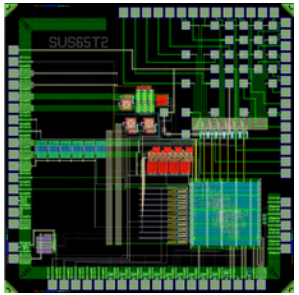
– Optimized precharge:
  • Slow for reduced crosstalk (no current spikes).
  • Low-voltage (<V_{sup}) for low power consumption.
  • No precharge if address does not change (optimized for our access pattern).

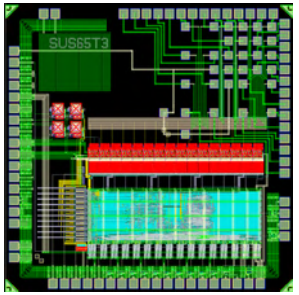
– Not clocked, no sequential elements.

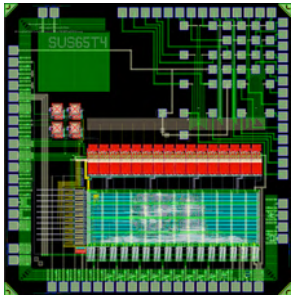


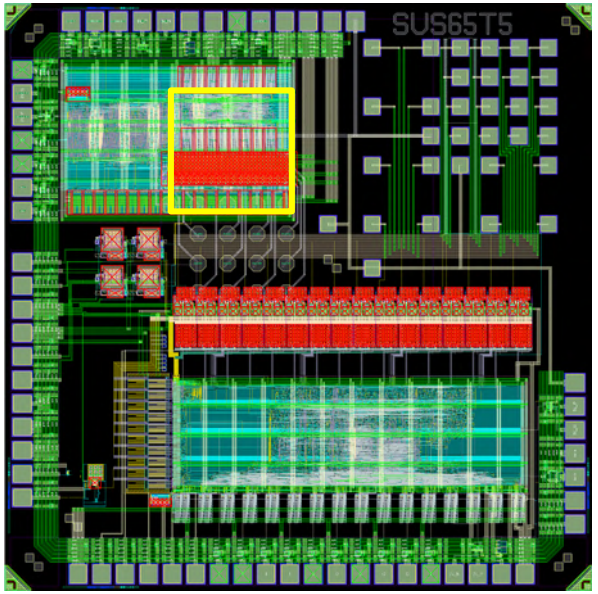
XIDer Chip Gallery



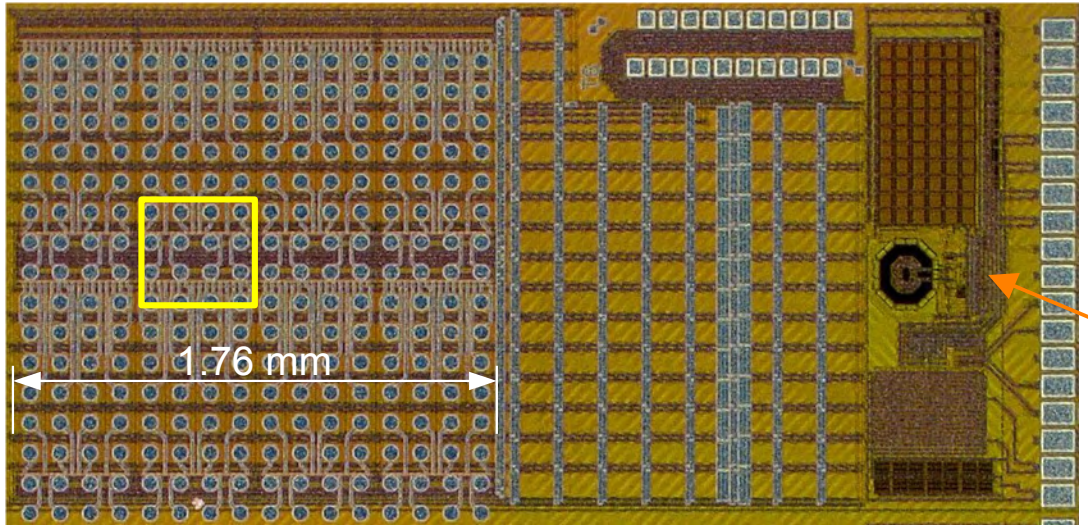








T5: 4×4 pixels in dense mixed-mode array



T6:
16×16 pixels, Aurora Serializer by STFC.

ASIC Requirements

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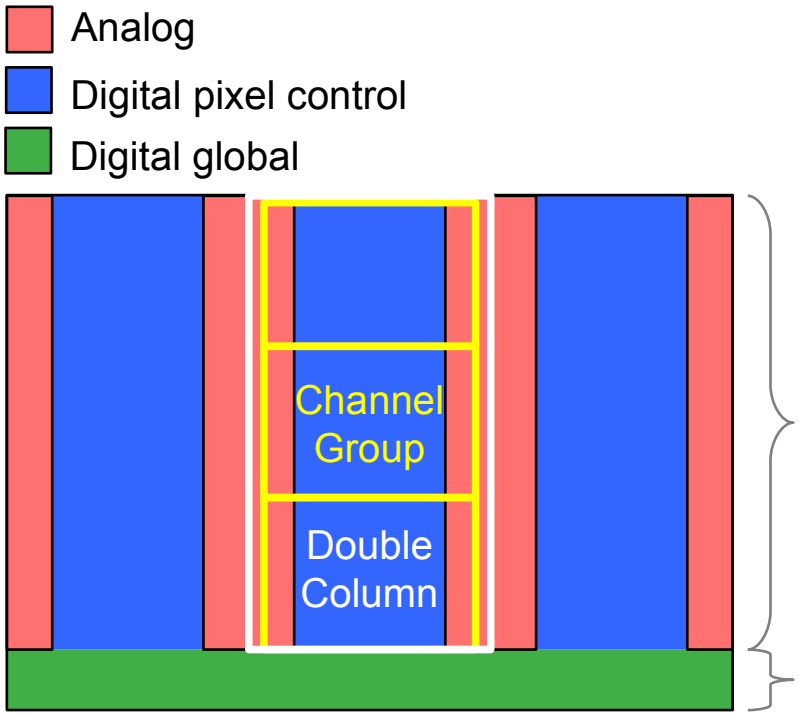
- Operation at ESRF and Diamond.
- Wide input range:
  Si 10 keV…50 keV, **Cd(Zn)Te 20 keV…100 keV** (0.44 fC…3.62 fC)
- Flux: **10^{11} photons/mm²/s (~1 photon/ns/pixel)**
- **110 µm pitch**
- ≥ 128 × 128 pixels (~1.4 cm × 1.4 cm)
- Noise < 1 photon over entire range.
- Per-pixel threshold and charge gain trim.
- Leakage compensation (current sensed during „empty frames“).

Design Choices for a Large ASIC

Still Preliminary

- Max. 880 MHz digital clock, suitable for synchronization with Diamond and ESRF.
- Max. 200 MHz pump frequency.
- Three-side Buttable Design.
  Power pins only on one side ⇒ only ~1 mW/pixel allowed.
- 3×14 GBit/s Aurora output links (contributed by STFC)
  ⇒ 50 kframes/s sustained
- ≥192 words in-pixel RAM.
- TSMC 65nm, 9 metal layers + AP, 1.2V core supply.

Layout Organization



Digital design needs to be contiguous.
⇒ several „fingers“ with the analog blocks in between.

Layout organized in ChannelGroups (32 pixels)
& DoubleColumns (one „finger“).

Pixels + Readout

Global: Serializers, Sequencer, Control, DACs, …

Layout Details

Building Block “ChannelGroup“

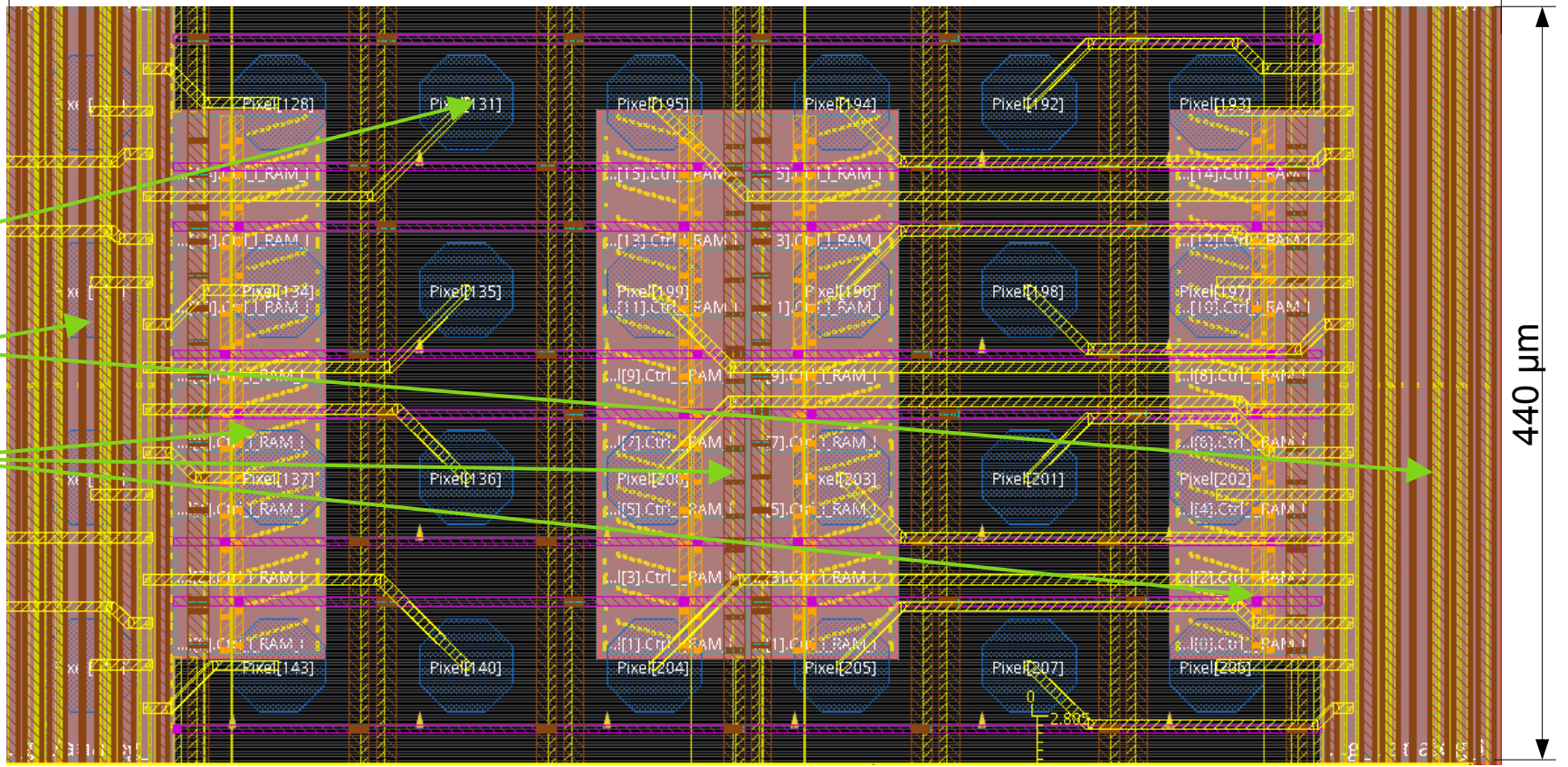
One Verilog module with shared resources:

32 Pixels

32× Analog FE in 2 blocks

32× RAM

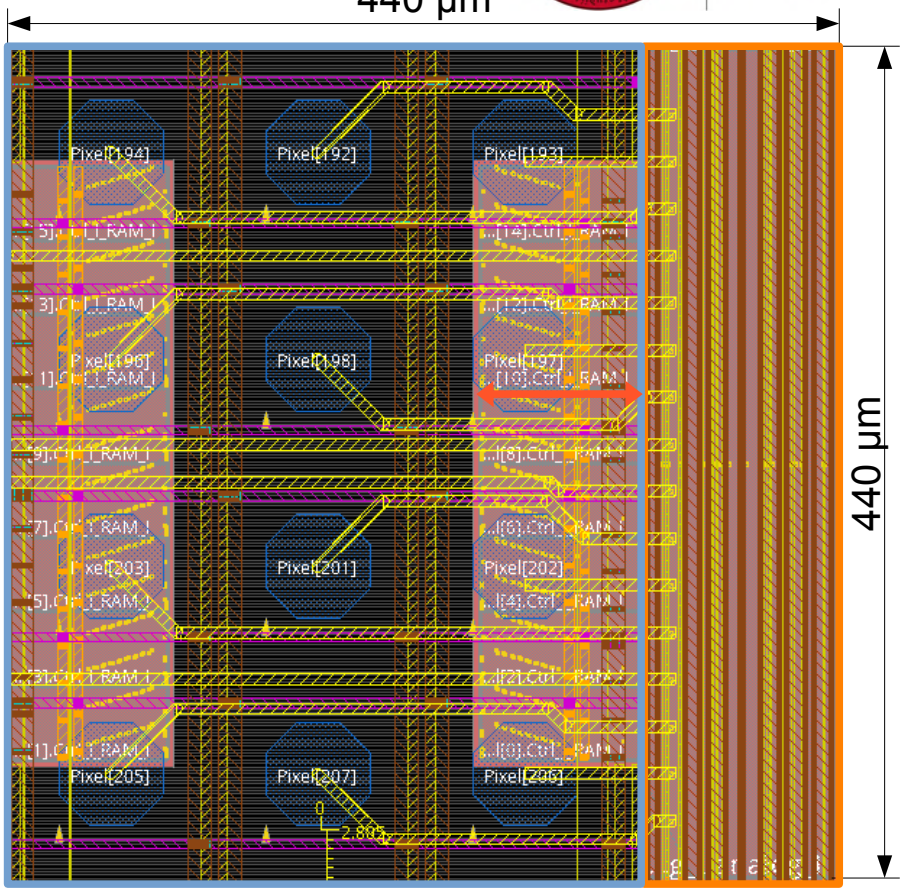
stackable in x & y



Layout Details

Crosstalk (noise) from digital to analog parts reduced by:

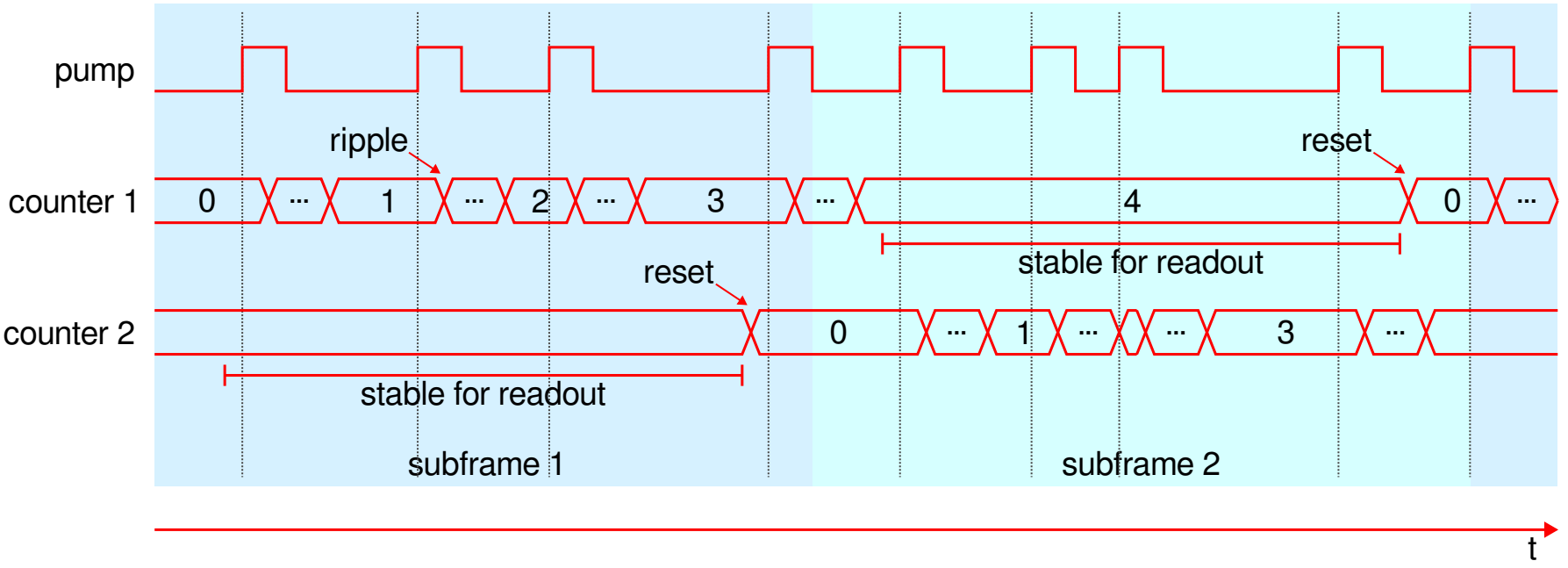
- Distance: The „quiet“ RAM acts as a spacer.
- Shielding: All of the analog part is in a deep n-well.
- Design: No fast clocks in the pixel digital design.
- Few flip-flops, lots of combinational logic
  ⇒ spreading out switching activity over time.
- ~ 320 standard cells / pixel



One Small Detail
Ripple-Carry Counters

- Initial design: Pumps are counted with synchronous counters.
  ⇒ Need to be as fast as the sequencer tracks = 2.3 ns
  ⇒ Fast clock, high power consumption.
- New design: Pump signal clocks a ripple-carry counter.
  Data as a clock = big no-no in digital design. I believe, I know what I'm doing…
- We do not know when the counter is done (within the constrained timing)
  ⇒ need to give it time to settle.
  ⇒ Two counters. One counting, one settling and being accessed.

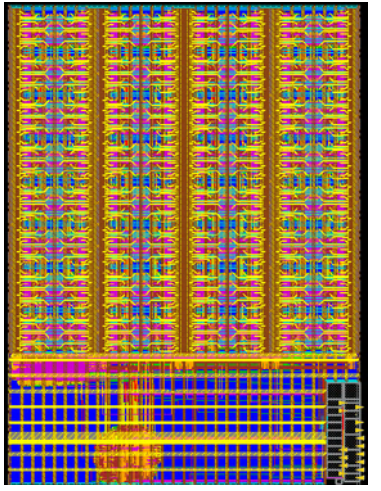
Ripple-Carry Operation



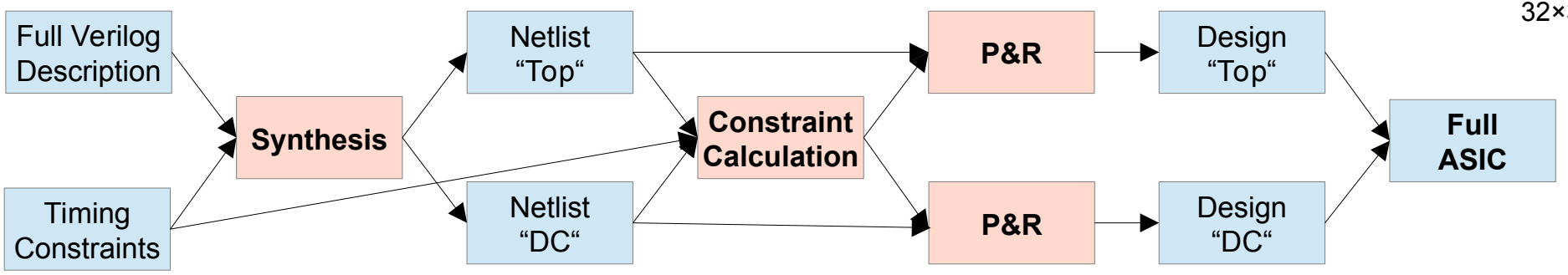
Synthesis Flow

Using „Digital-on-Top“ Approach

- Hierarchical flow: Identical DoubleColumns are repeated along the width of the ASIC.
  ⇒ Time savings.
- Physical synthesis to optimize for the large design from the start.
- Synthesis output: Two netlists for the toplevel, and for one DoubleColumn (DC).
- Both designs placed separately after deriving the timing requirements at the interface.
  ⇒ Passing almost exclusively signals in the slowest clock domain.



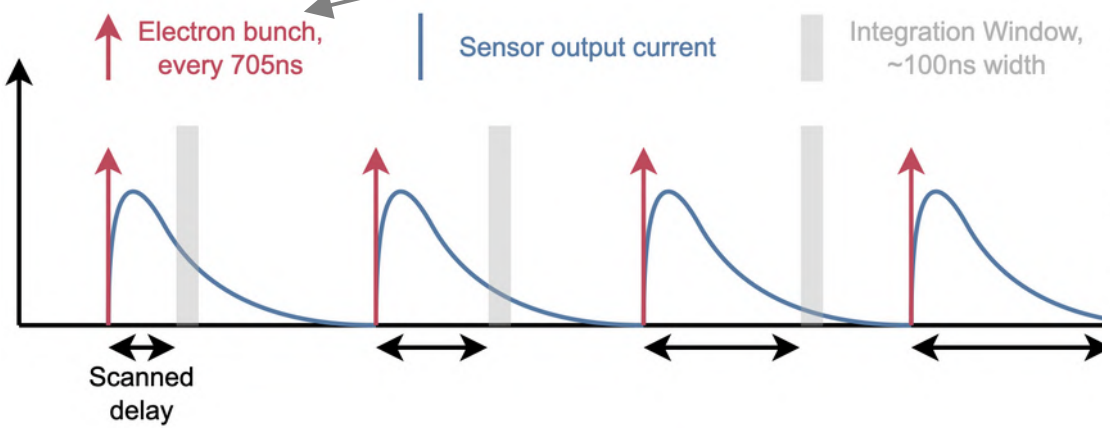
32×32 test

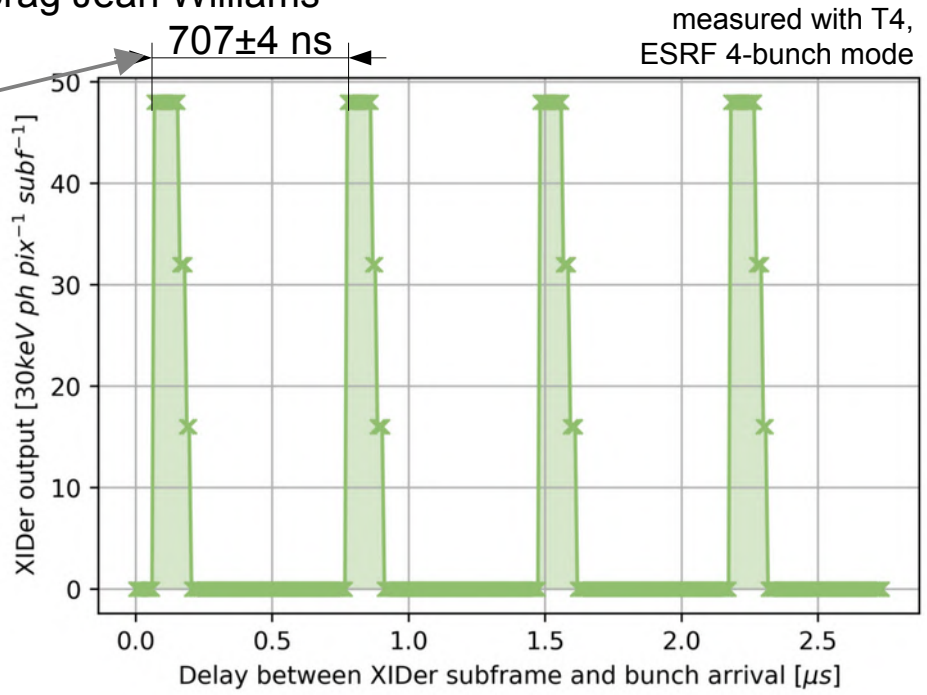


Bunch Structure Scan

Showing Things Work Nicely Together

- Measured by ESRF team: Paolo Busca, Marin Collonge, Morag Jean Williams
- Telegram and Sequencer synchronized to the synchrotron.
- Integrator working.
- Charge Pump operating.





Summary

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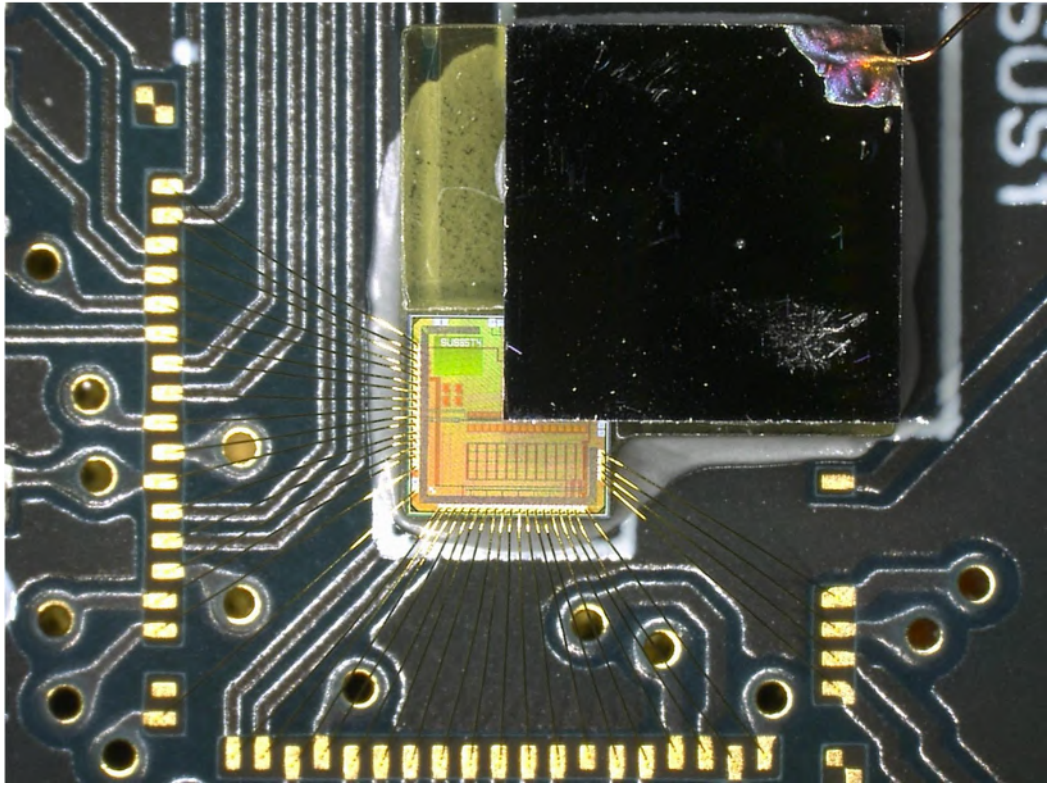
- We are designing pixelated readout ASICs for Cd(Zn)Te & Si detectors,
  covering a wide range of photon energies.
- Pipelined Digital Integration scheme for single-photon resolution and large dynamic range, high rate operation.
- Flexible readout and data handling with Sequencer and Telegram.

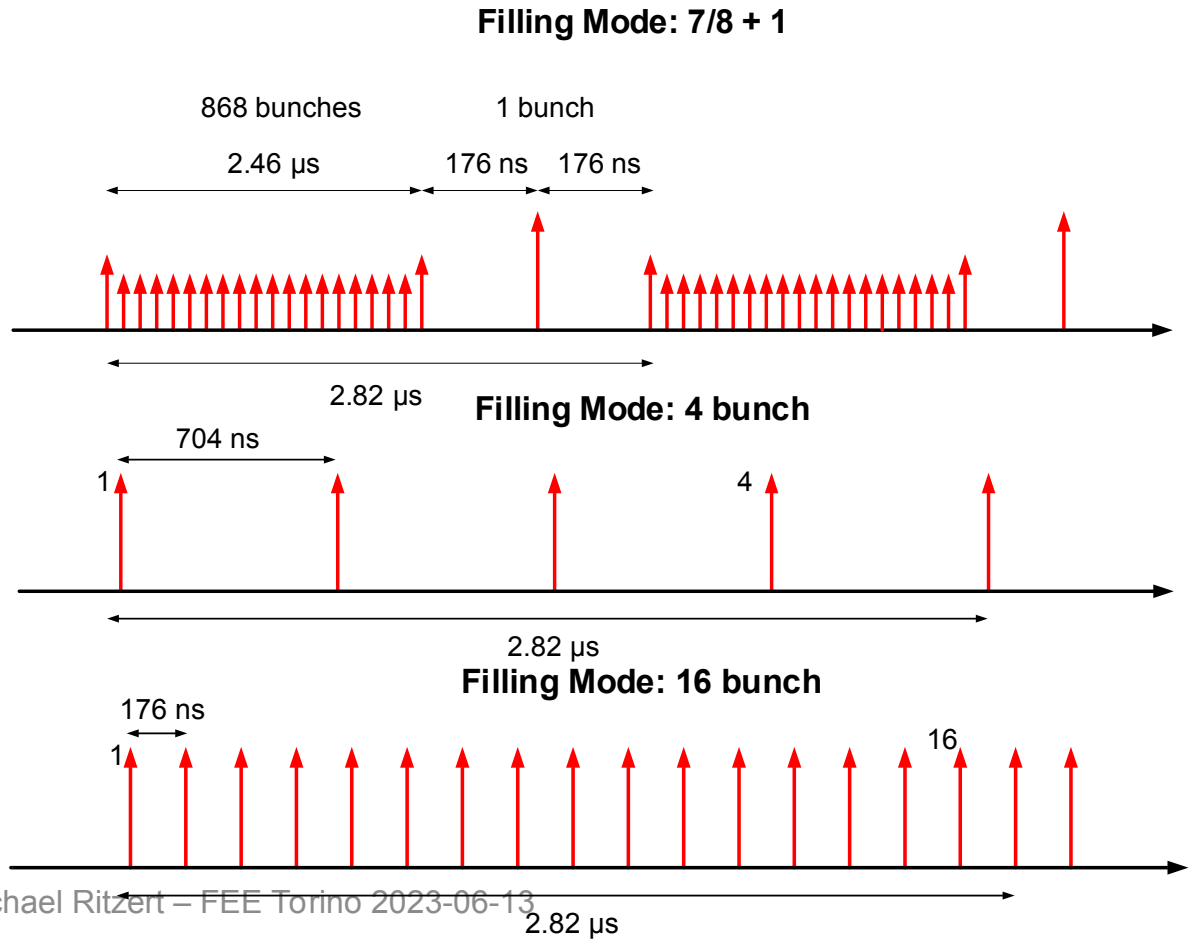
- 6 Test Chips submitted. Latest Iterations contain pixel designs ready for scaling to large chips.

- Very promising results:
  - Digital integration concept succesfully operating.
  - Good analog performance.
  - Digital control and readout working.



Thank you!

ESRF Filling Modes



⇒ Defines the largest allowed minimum subframe length ≤ 176 ns.

Linearity Measurement @ BM05, ESRF

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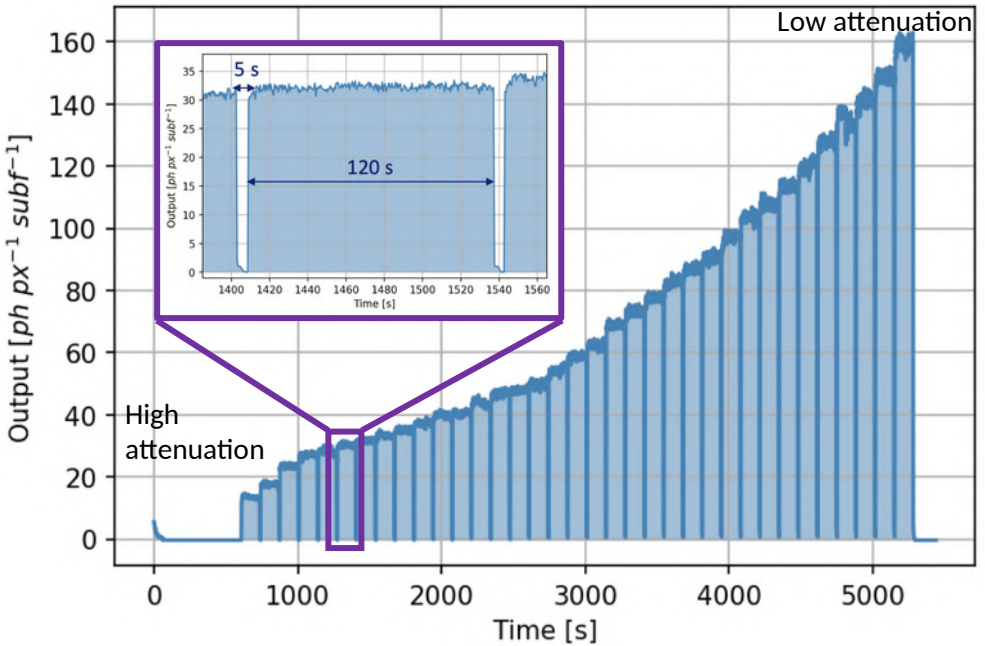
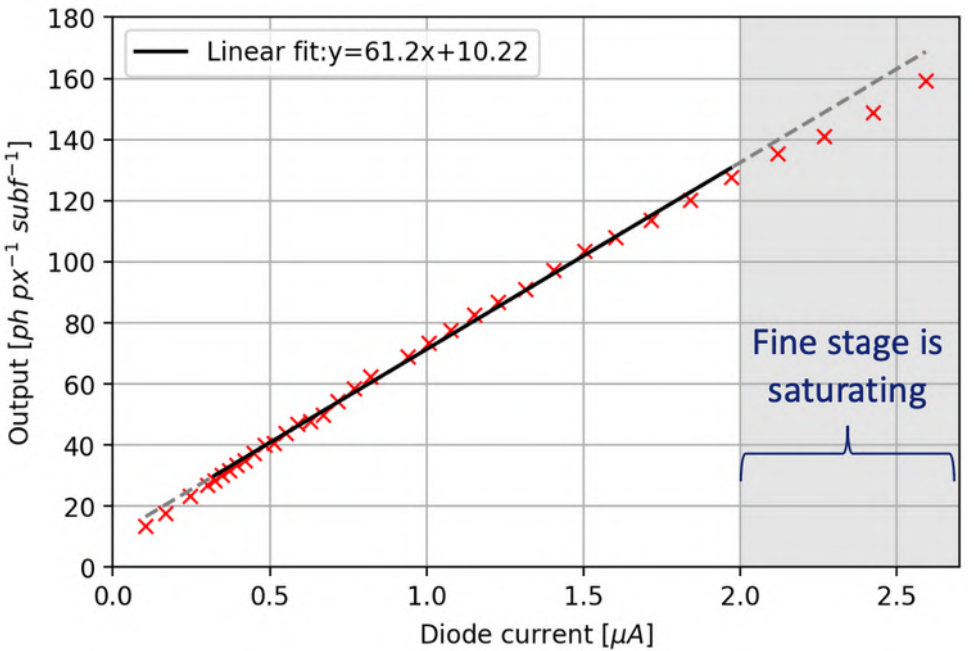
Flux pattern measured with XIDer
CdTe 100µm pitch

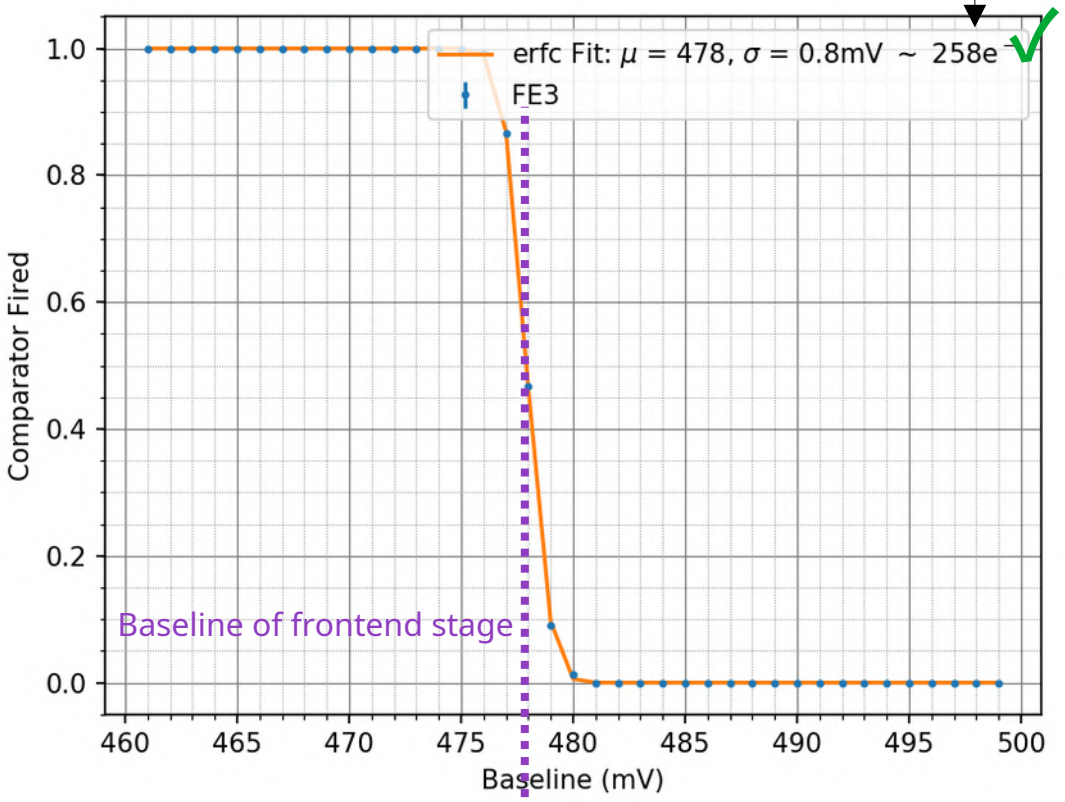


XIDer output vs. reference diode



First Stage Noise

Goal: ≤ 300e⁻ (input referred noise)



For comparison:
30 keV photon ~ 6000e-

According to dark rate simulations,
we want to be below 300e⁻

Noise Improvements

T4 vs T5

Digital-to-analog Crosstalk
T4: Large design, no deep n-well
T5: „smart“ condensed design, deep n-well
Same Measurement (Treat results as a.u.)