中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

3D-bonded SOI pixel detectors

Yunpeng Lu*, *yplu@ihep.ac.cn

Yang Zhou, Jia Zhou, Hongyu Zhang, Jing Dong, Mingyi Dong, Qun Ouyang

Institute of High Energy Physics, Beijing, China

FEE 2023, XII INTERNATIONAL MEETING ON FRONT-END ELECTRONICS for Particle Physics, Photon Science and related applications,

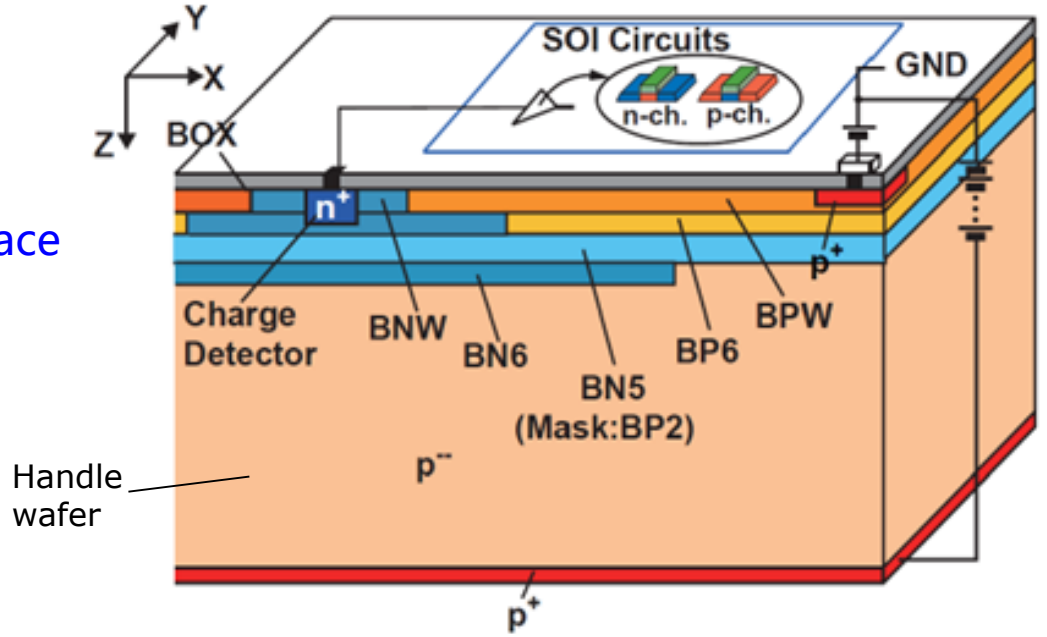
Turin, 12-16 June 2023

Outline

- Introduction
  - Development of SOI pixel sensor for the CEPC experiments
  - 3D process steps
- Design of the CPV-4 chip
  - 3D architecture
  - Sensor, Analog frontend, 3D verification
- Electrical test results
  - On single chips before 3D-integration
  - On completed chips after 3D-integration
- Summary and Outlook

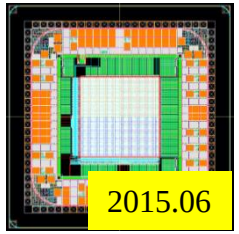
SOI pixel detector

- High Resistive handle wafer to detect charged particles and X-ray photons
- Pinned Depleted Diode optimized for
  - Low capacitance
  - Control the back-gate of transistors
  - Suppressing the leakage at the Si-BOX (Buried Oxide) interface
  - Shielding the charge injection through the BOX layer
- 200 nm FD-SOI circuit process
  - Low leakage low power industrial applications
  - 1 Poly 5 Metal layers
  - MIM Capacitor (1.5 fF/um^2), DMOS
  - Core voltage = 1.8 V, IO voltage = 1.8/3.3 V
  - Well-developed PDK including all the customized sensor layers



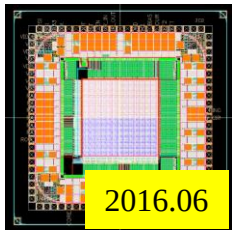
Development of the CPV SOI pixel sensor

- SOI activities for the proposed CEPC experiment
  - CPV-1&2 for the study of position resolution of small pixels with binary readout (FEE2018)
  - CPV-3 for the study of PDD structure (NIMA 1040 (2022) 167204)
  - CPV-4 for the 3D integration (this talk)



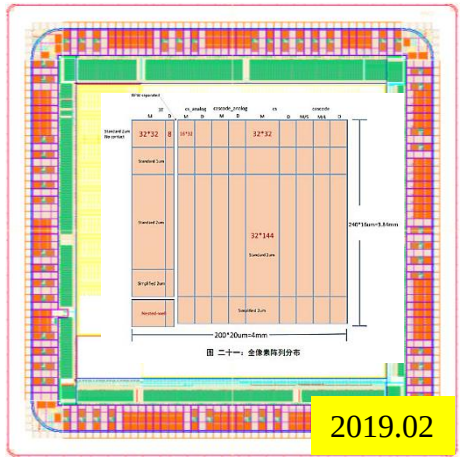
CPV-1

Process assessment



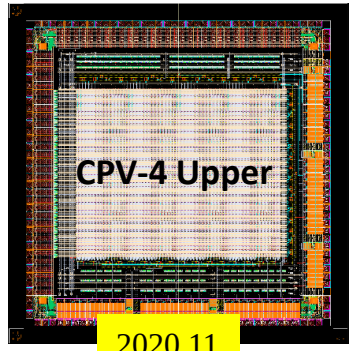
CPV-2

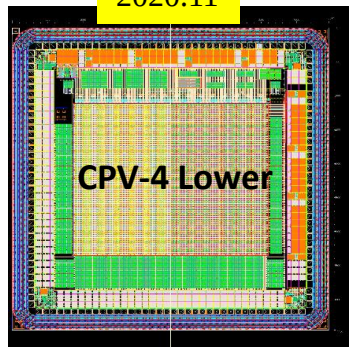
S.P. Resolution 2.3 μm;
Thinned to 75 μm



CPV-3

Pinned Depleted Diode;
Optimized for low FPN 12 e⁻





CPV-4

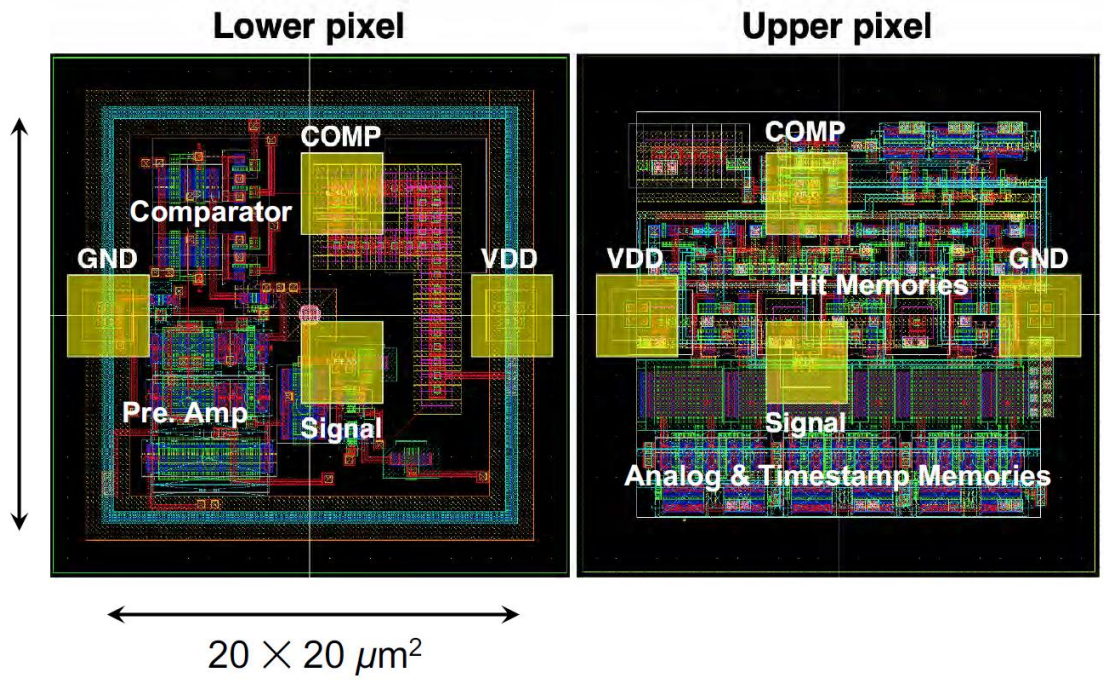
3D architecture;
Stacking process;

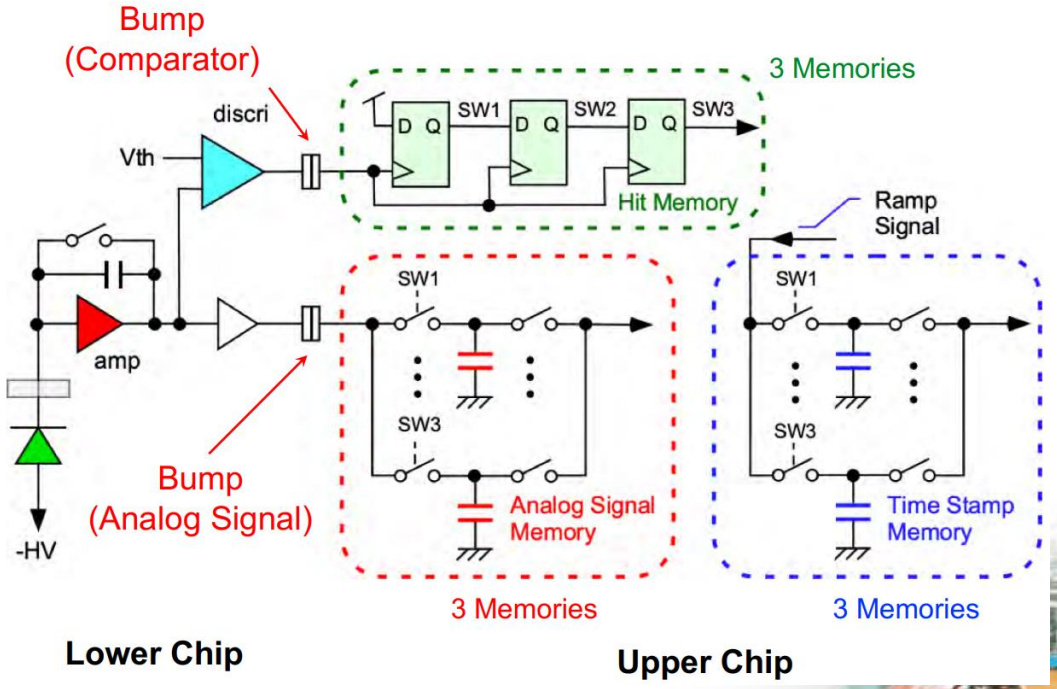
Compact Pixel for Vertex (CPV)

3D-SOI vertical integration

- Pioneered in the development of SOFIST for the ILC experiments
  - Yasuo Arai, Miho Yamada, et al.
  - Shrunk the pixel layout dramatically: 30 x 30 um^2 (SOFIST-3) → 20 x 20 um^2 (SOFIST-4, 3D)
  - One analog signal for amplitude, one comparator output for timing, and a pair of power/gnd

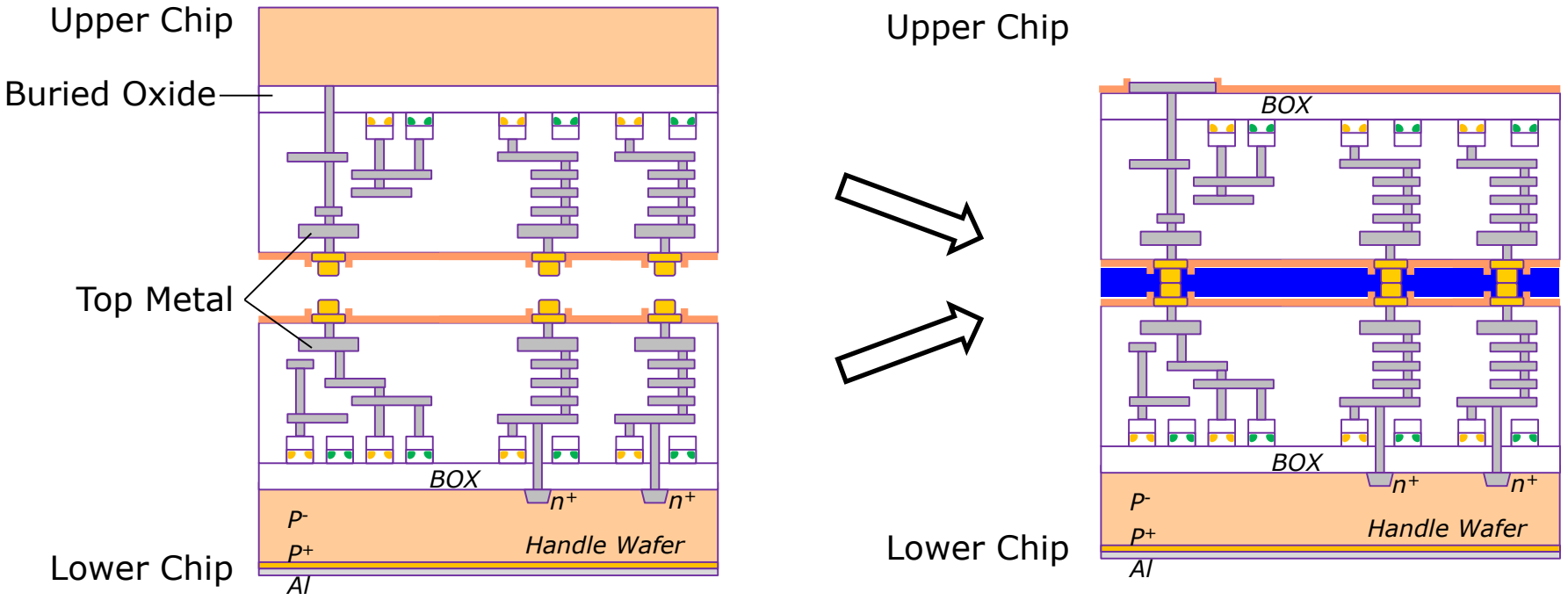
SOFIST-4 Layout and block diagram





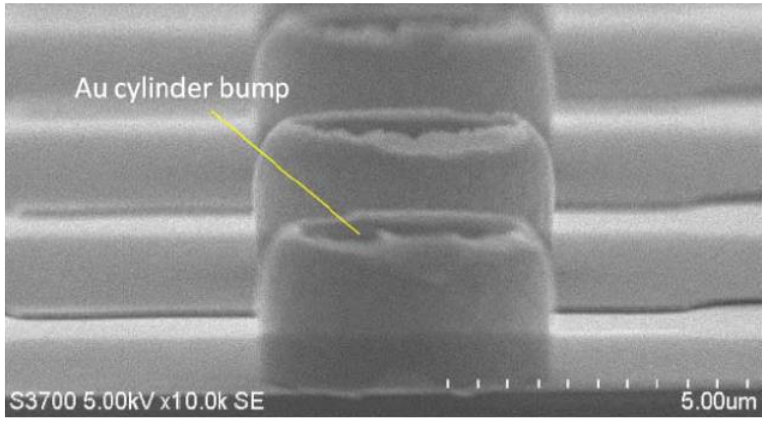
Vertical connections in flip chip bonding

- Micro bump for inter-chip connections
  - Multiple bumps for each pixel, signals and power/ground
  - Optional to connect the original bond pads face to face via micro bumps (i.e. I/O for test purposes)
- Trough Box Via used for building new bond pads from the top side
  - Access to the upper chip
  - as well as the lower chip through the inter-chip connections



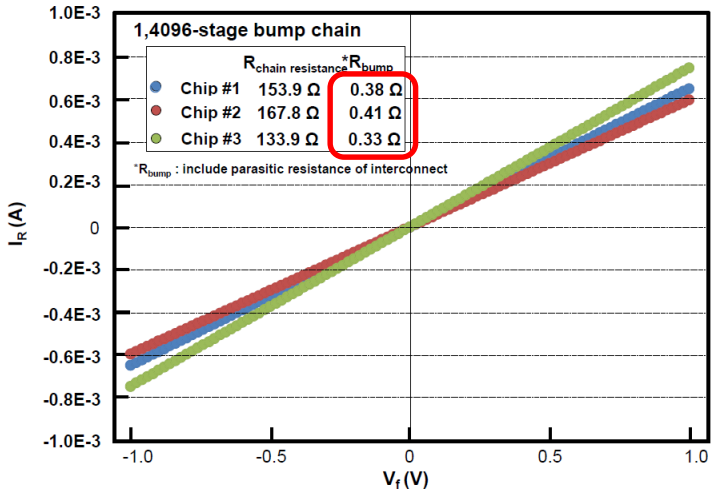
Micro bump

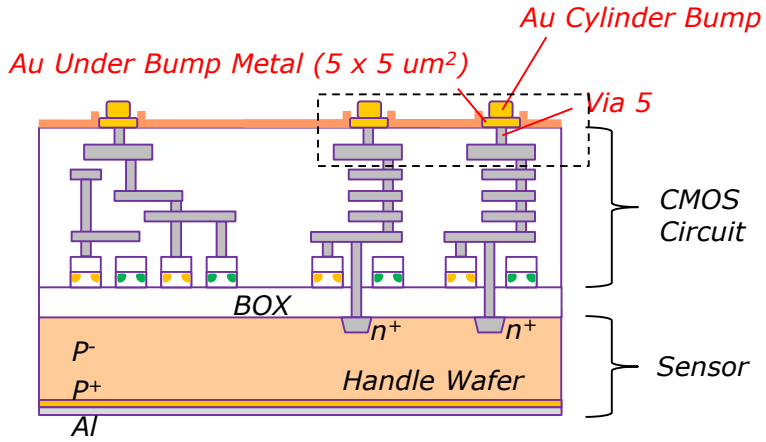
- Au cylindrical bump selected after trying different metals and process
  - Indium bump, round pillar, cone shape, …
  - Size down to 3.5 um in diameter
  - Pitch down to 7 um
  - Thin wall of Au ~ 100 nm
- Key technology
  - Inverse-tapered photoresist
  - Low incident-angle Au sputtering

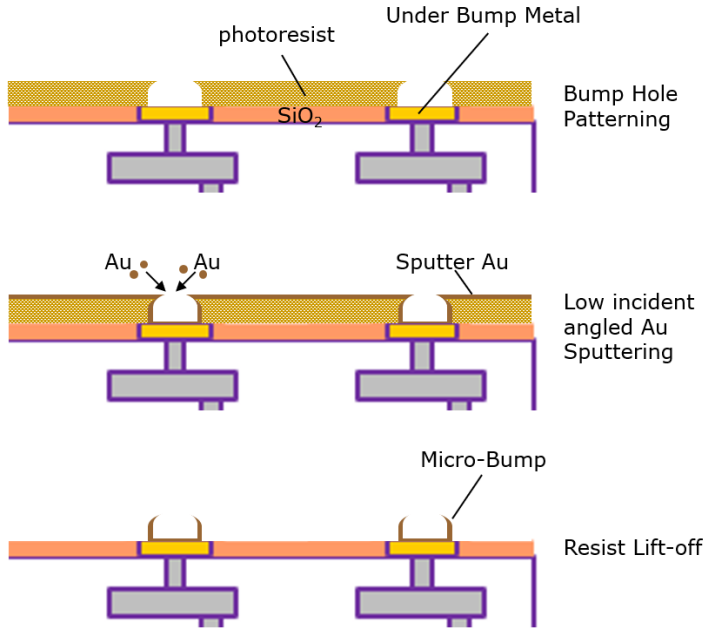


SEM image of Au micro-cylinder bump

Bump Resistance (0.3 ~0.4Ω)





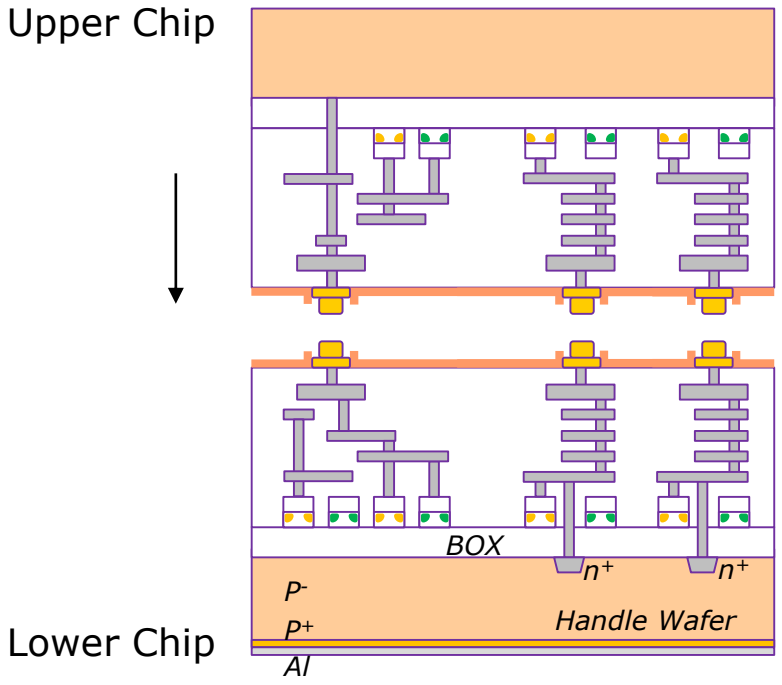


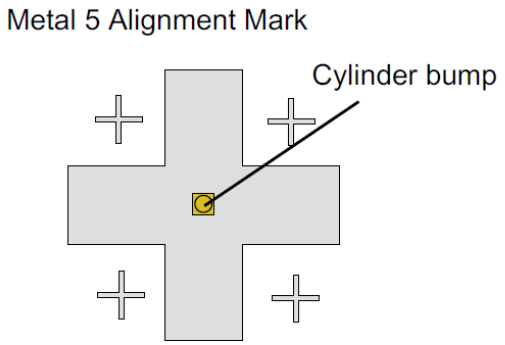
Processed by T-Micro

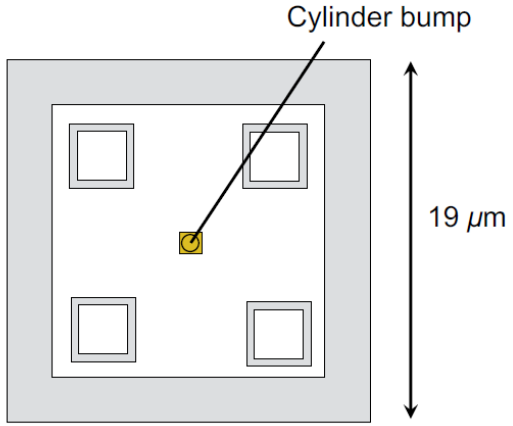
Alignment and stacking

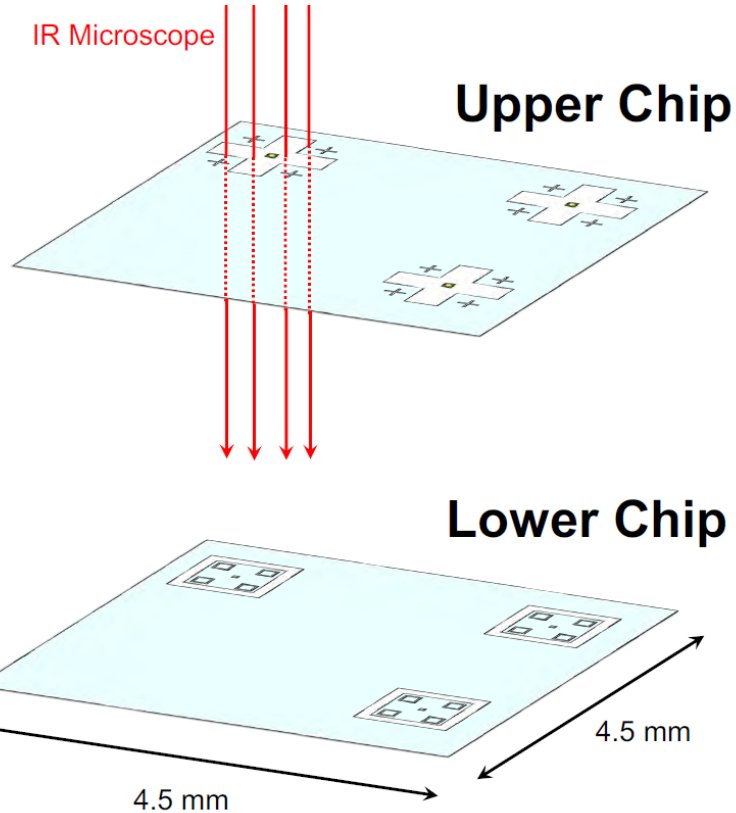
- Initial alignment better than 1 um under IR microscope
  - Self-aligned after bumps being heated and fused
- Large bonding margin and low temperature
  - Cylindrical bumps easy to deform
  - Process temperature < 200 °C

Alignment with marks on the chip corners



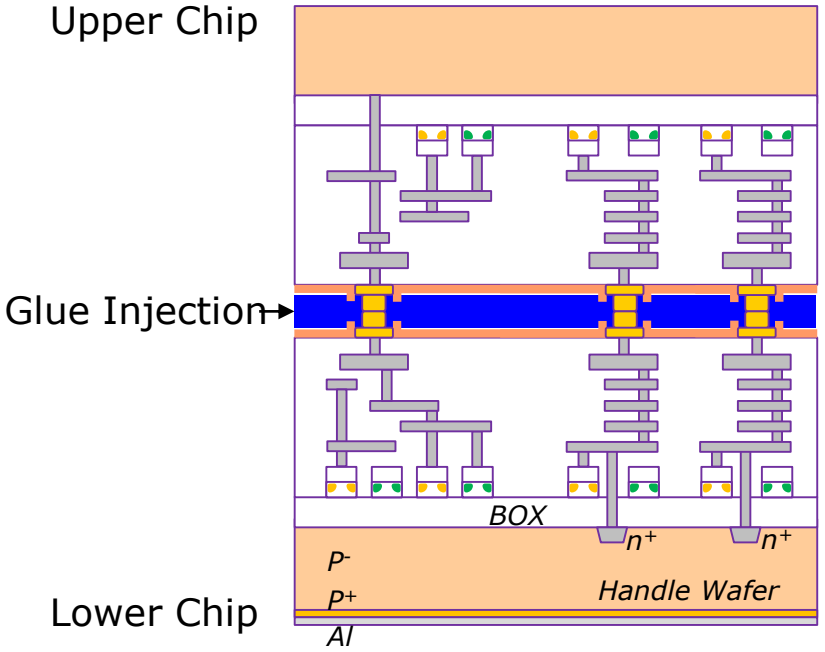




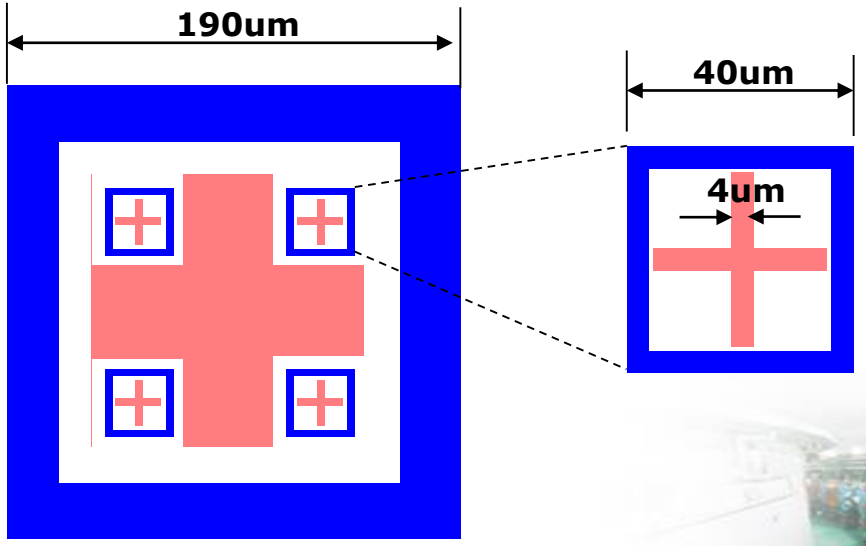


Glue injection and curing

- Adhesive glue used to enhance the mechanical strength of micro bumps
  - Uniformity of glue injection affected by the bump layout and adhesive parameters → voids without glue
  - Slipping of stacked chips may occur during the glue curing as the viscosity of adhesive decreases in the early stage of curing
  - Necessary to optimize the parameters to avoid problems

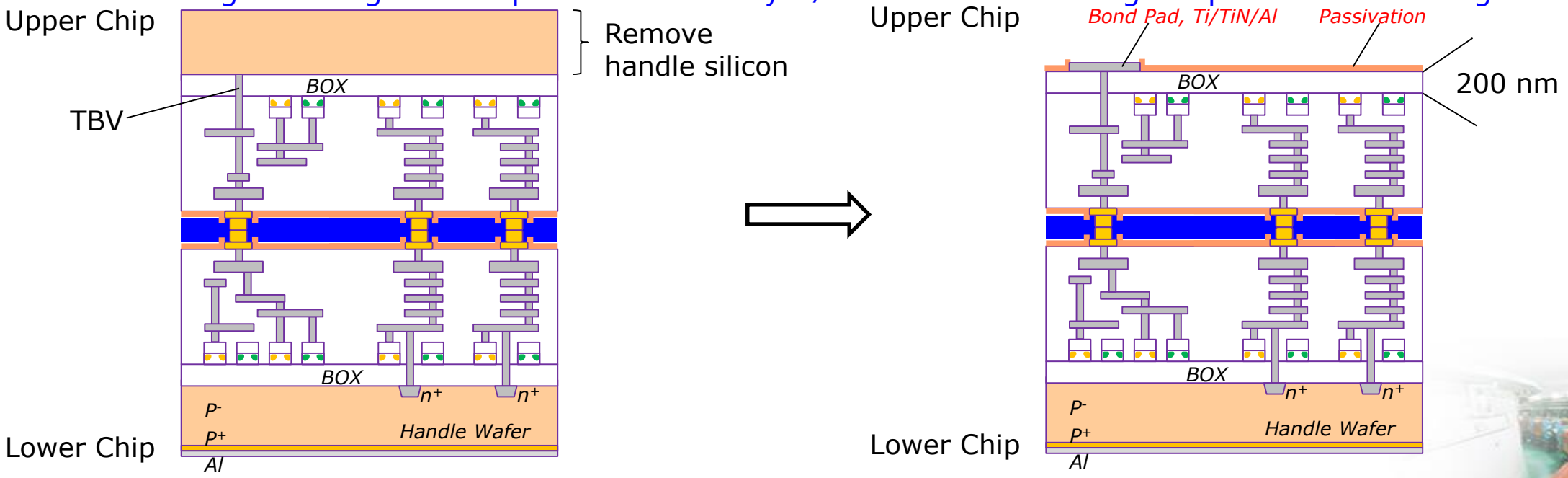


Alignment marks can be used to monitor the bonding results



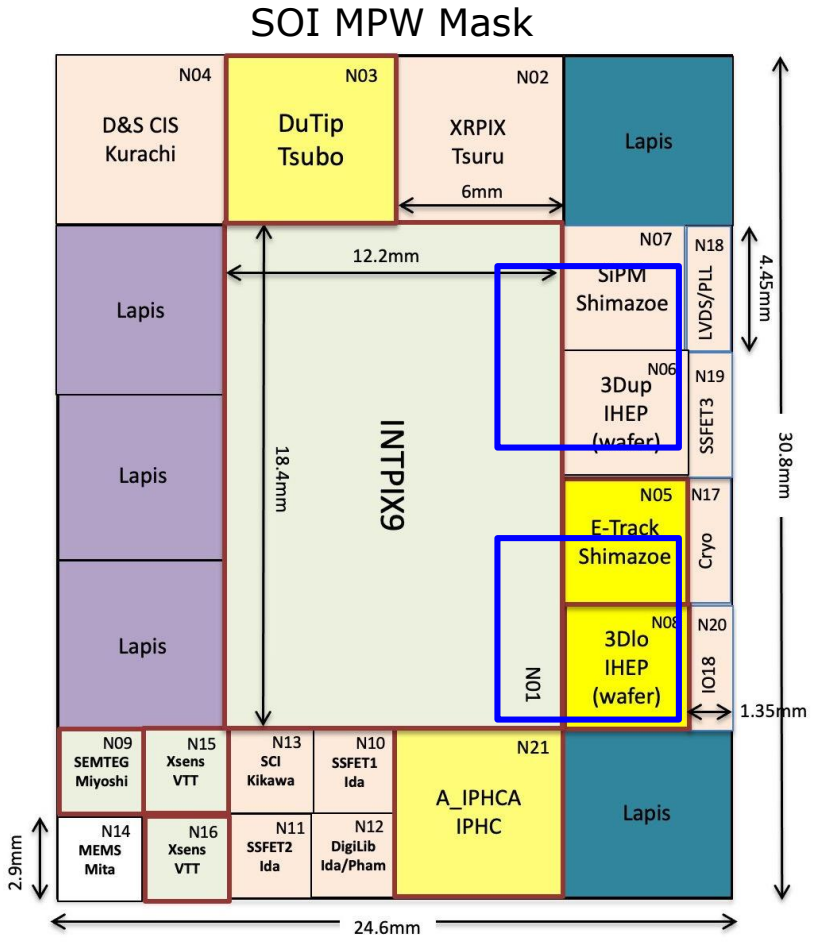
Backside connections

- Backside connection is by Through Box Via (TBV)
  - The same mask layer as the connection to the sensing diode
  - 0.32 um hole implemented already in the SOI foundry
- Handle silicon of the upper tier being removed by wet etching until the BOX and TBV are exposed
- Additional metal layer formed for the bond pad and the back gate electrode (optional)
  - 3D bond pads are placed right on top of the original bond pads
  - Removing of the original bond pads not discussed yet / can be used to test single chips before 3D bonding



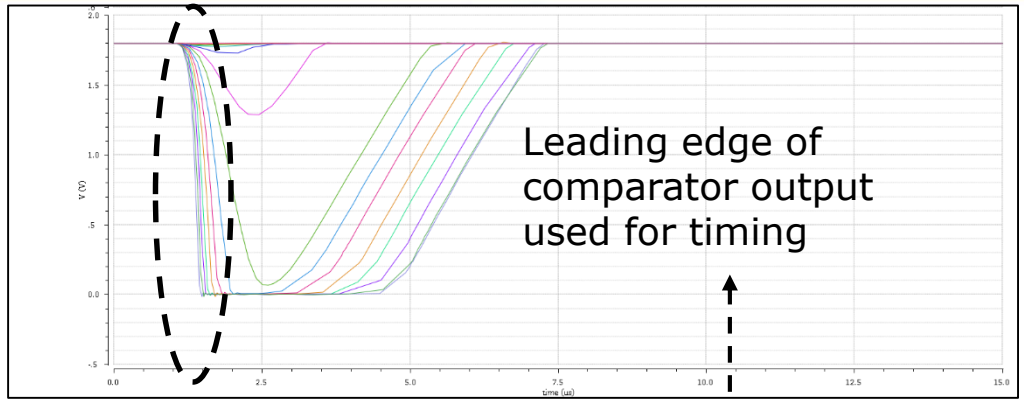
Chip-On-Chip bonding

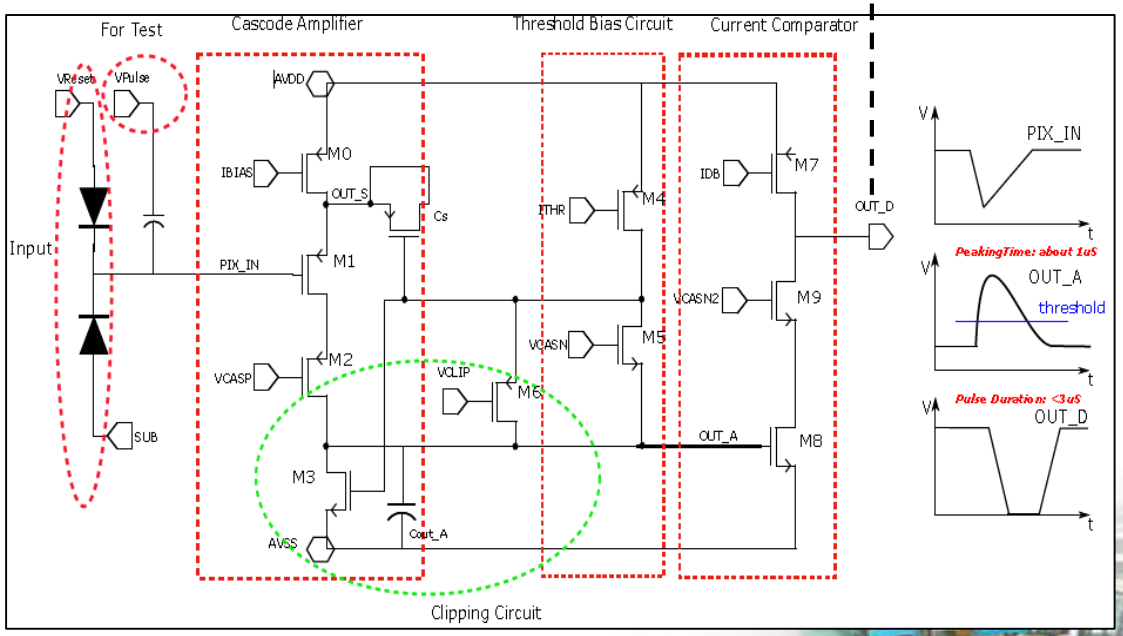
- Tape-out at LAPIS and 3D-bonding at T-Micro
  - All the data stored in a single GDS file, including the 3D layers
- Multiple reticles firstly diced from a dedicated wafer (but still MPW)
  - for the formation of Via 5, UBM, Au-Bump
- Single chip diced again for
  - Stacking, Glue injection, Thinning, Bond pad



CPV-4 design scheme

- **Low power** front-end: amplifier and comparator
  - The same topology as ALPIDE design
  - Using the leading edge of OUT_D pulse for timing
  - A short interval of time uncertainty < 1us
  - A D-flipflop used as the HIT register





amplifier and comparator

CPV-4 design scheme (cont'd)

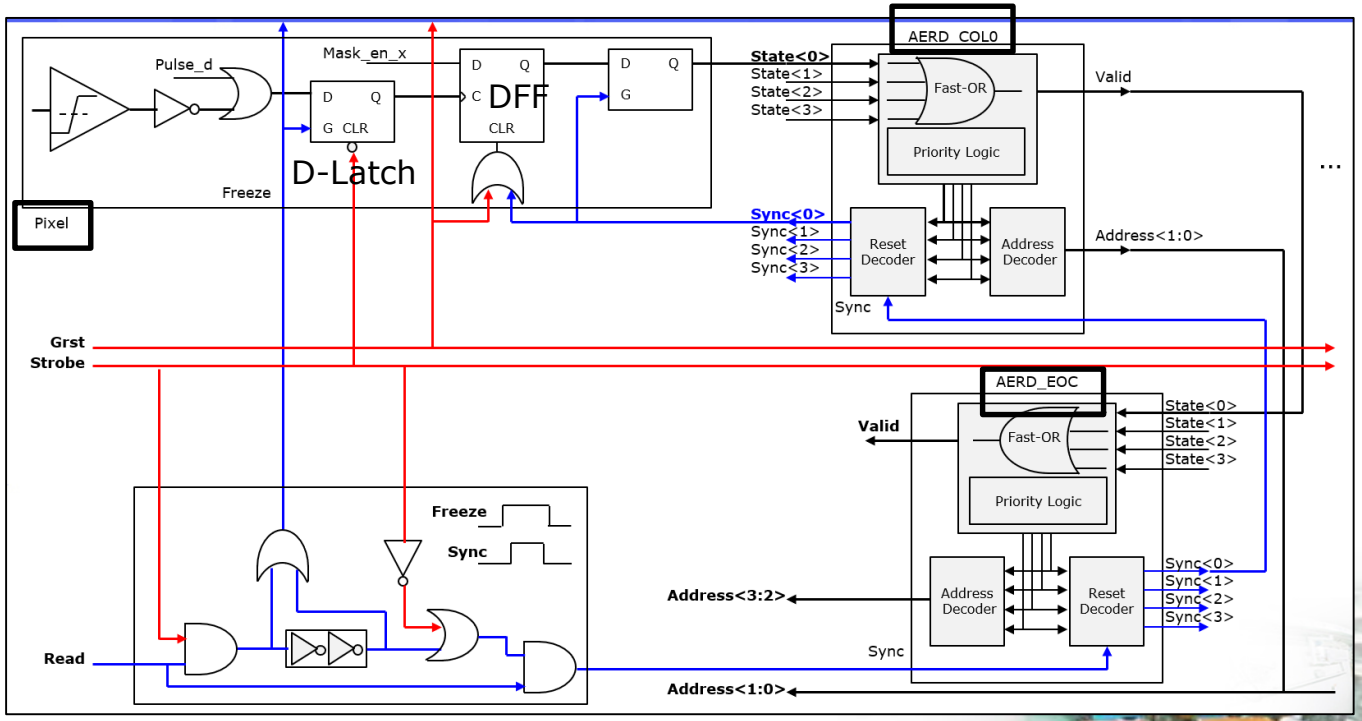
- Data-driven readout
  - A D-latch to freeze HIT state
  - **HIT** address encoded: low bits in the column and high bits at the end of column
  - **READ** signal issued and decoded in an inverse way to clear the HIT bit

} AERD

  - **STROBE** signal asserted either constantly in the **continuous** readout mode, timing by the leading edge; or asserted for a short period, timing provided by the external **trigger** pulse (timing diagram in the backup slides)

Asynchronized Encoder and Reset Decoder (AERD)

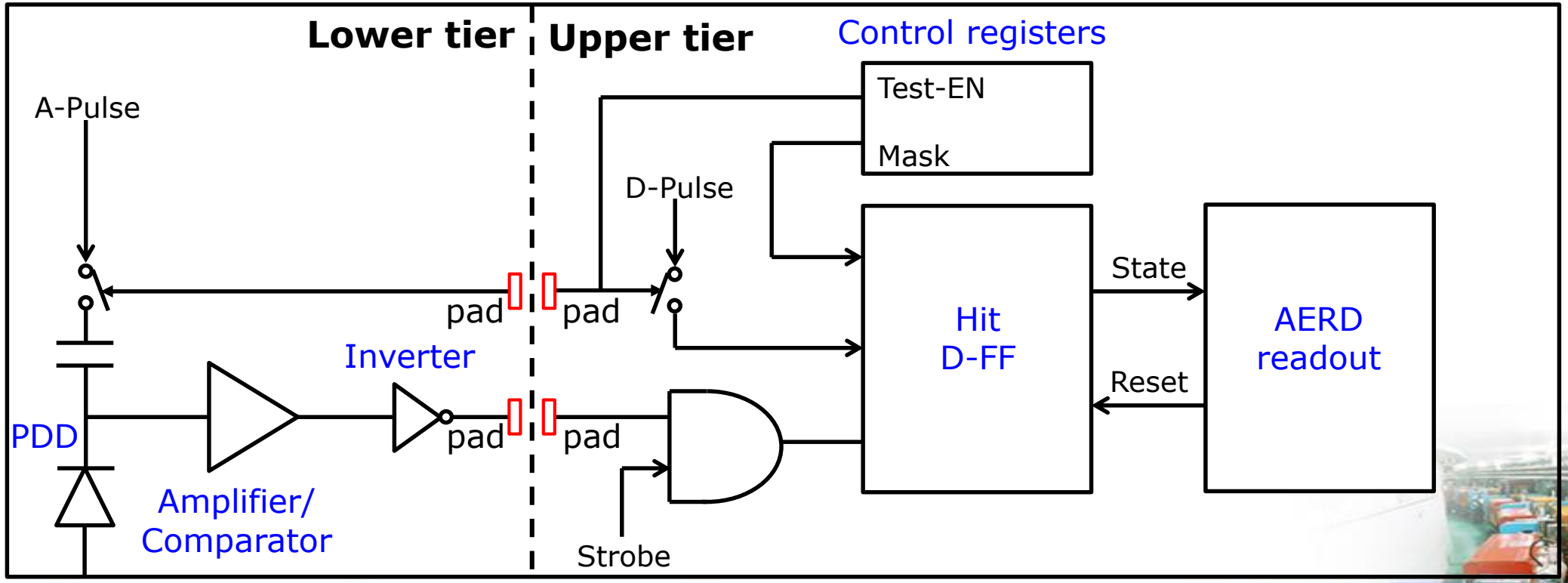
*Ping Yang et al., NIMA 785 (2015) 61-69



Explanatory diagram of CPV4 design scheme

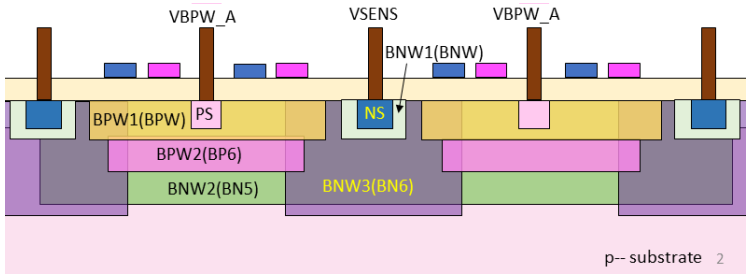
Division of upper and lower functionality

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit D-Flipflop + Control register + AERD readout
- **2 vertical connections** in each pixel: comparator output and switch of test pulse
  - Analog and Digital power/ground separated, with dedicated bond pads on each chip
  - Transition from Analog to Digital domain at the Inverter

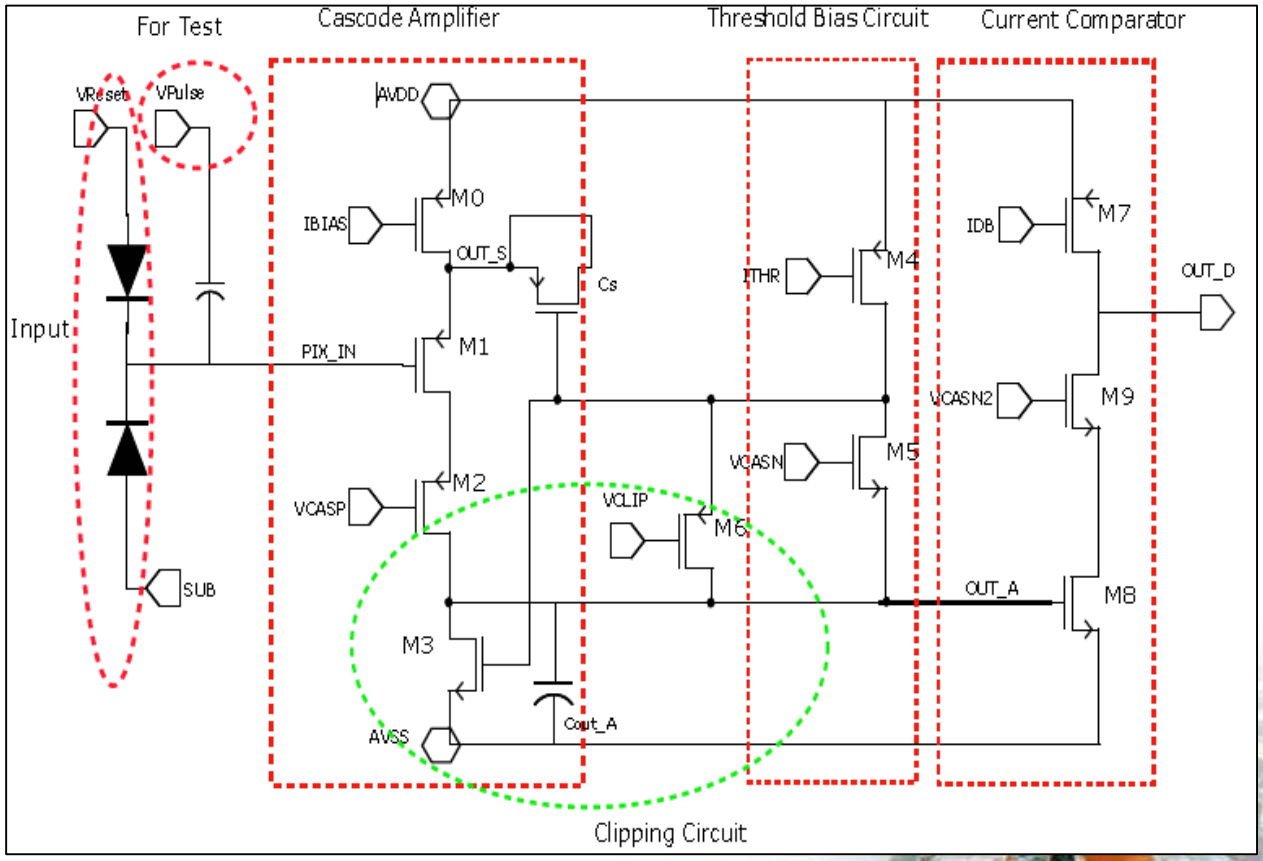


Management of Vth shift

- The Buried P-Well required to be -4V (BPW shown below) in order to minimize electrode capacitance Cd of the sensing diode (PDD).
  - **Back-gate** effect in MOS transistors characterized and modeled in HSPICE by KEK
  - Vth decreased 70 mV for PMOS and increased 50 mV for NMOS
- Influence on the front-end assessed
  - Input branch of current mirror matched with BPW=-4V (for M0, M4, M7)
  - Other transistors compensated by proper offset on their gate voltage (VCASN, e.g.)
  - **Confirmed by circuit simulation**



PDD requires -4V applied on BPW



Pixel design

- **Transistor size** selected roughly according to ALPIDE design* to minimize FPN as a first order approximation
  - The same bias current for a weak inversion working point
  - Different types of transistor used, lv/nv/hv in combination with bf/bt/st

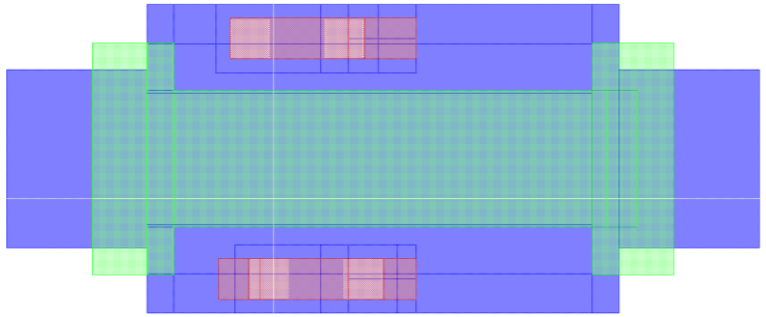
Transistor	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9
W/L	1.8/8.5	1/0.4	1/0.4	1/5	2/8.05	0.63/4.94	0.63/3	1/5	1/0.4	1/1

- Simulation results of **threshold and noise**

	Threshold	Gain@Thr	Vnoise@Thr	ENC
Pre-layout	75 e^-	32mV/10e^-	4.33 mV	1.34 e^-
Post-layout	**125 e^-**	8.6mv/10e^-	2.92 mV	**4 e^-**

- TID radiation enhancement
  - H-gate transistors used for ITHR current branch (M5)
  - Compensation of TID-induced Vth shift may be applied on the BPW layer

H-gate NMOS layout

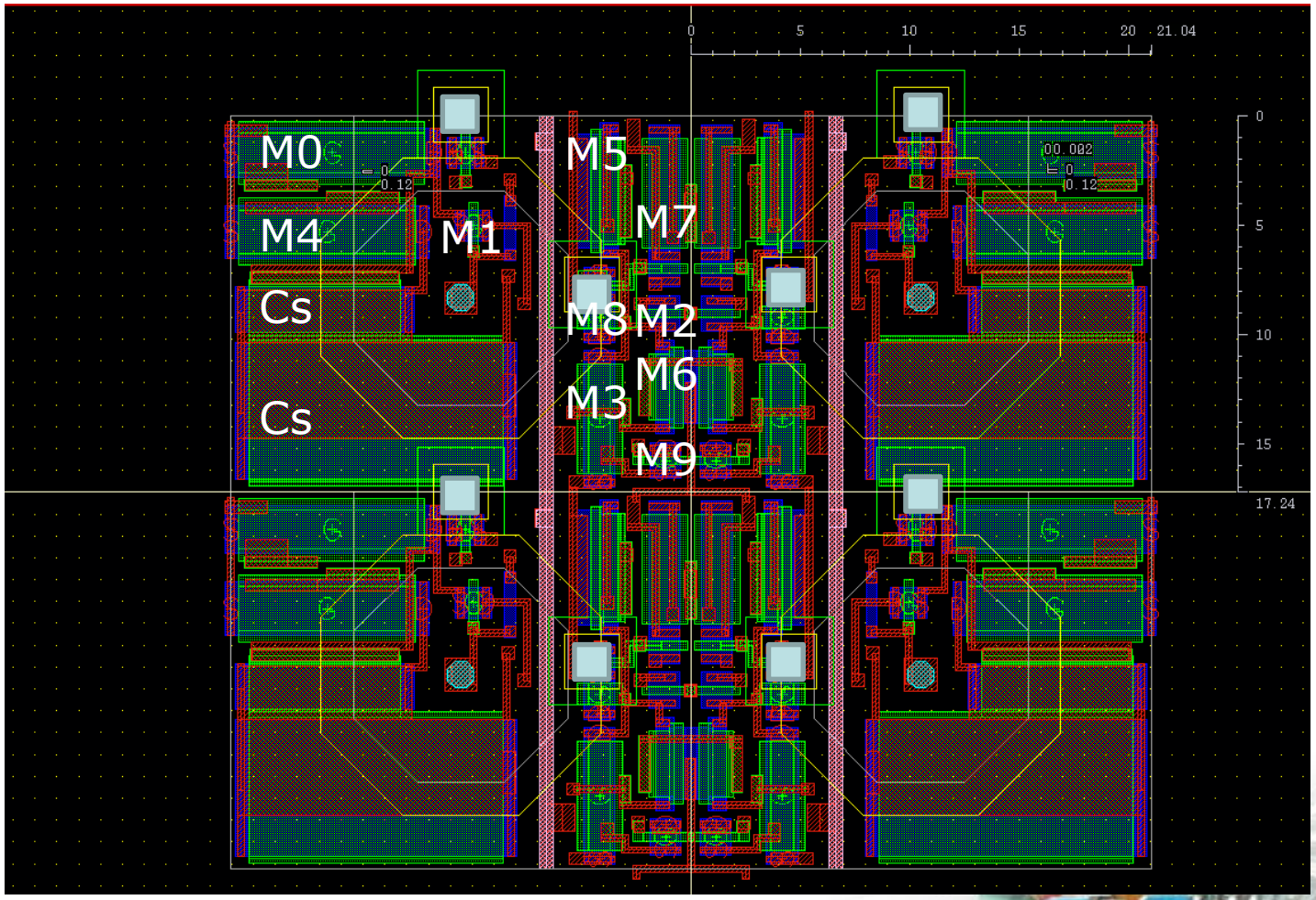


*Ref: D. Kim et al., 2016 JINST 11 C02042

Pixel layout

- A lot of efforts to minimize the layout size
  - 21.04 um * 17.24 um
- Y-axis mirrored, to protect the **sensitive input node** against the possible interference from the output node
  - To minimize the crosstalk

3D bumps marked with

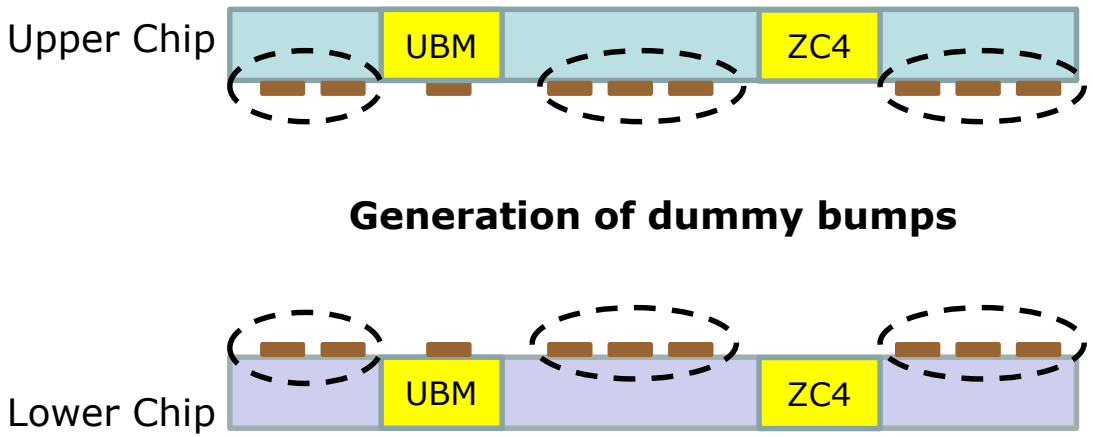


4 pixels arranged in two columns

Dummy 3D bumps

- A uniformly distributed dummy 3D bumps on the whole chip
  - To **relieve the mechanical stress** of upper tier
  - Generated automatically in the user-designated area
- The dummy 3D bumps not allowed in
  - The pixel matrix
  - The p-stop of guard rings
  - The alignment marks

dummy 3D bumps avoid UBM and Masking layer (ZC4)

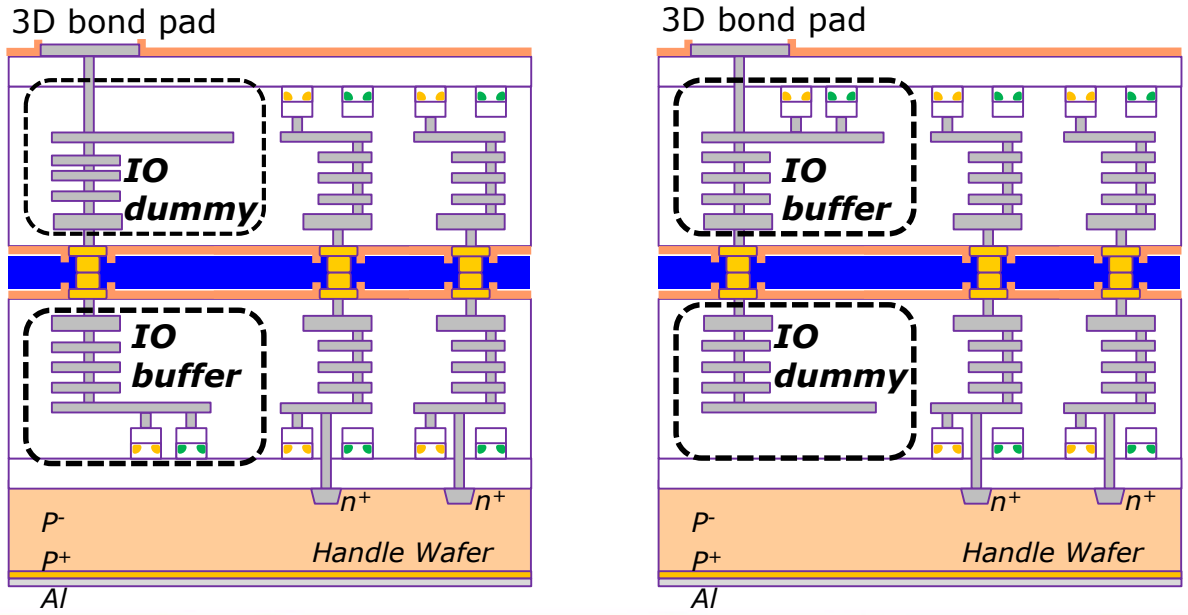


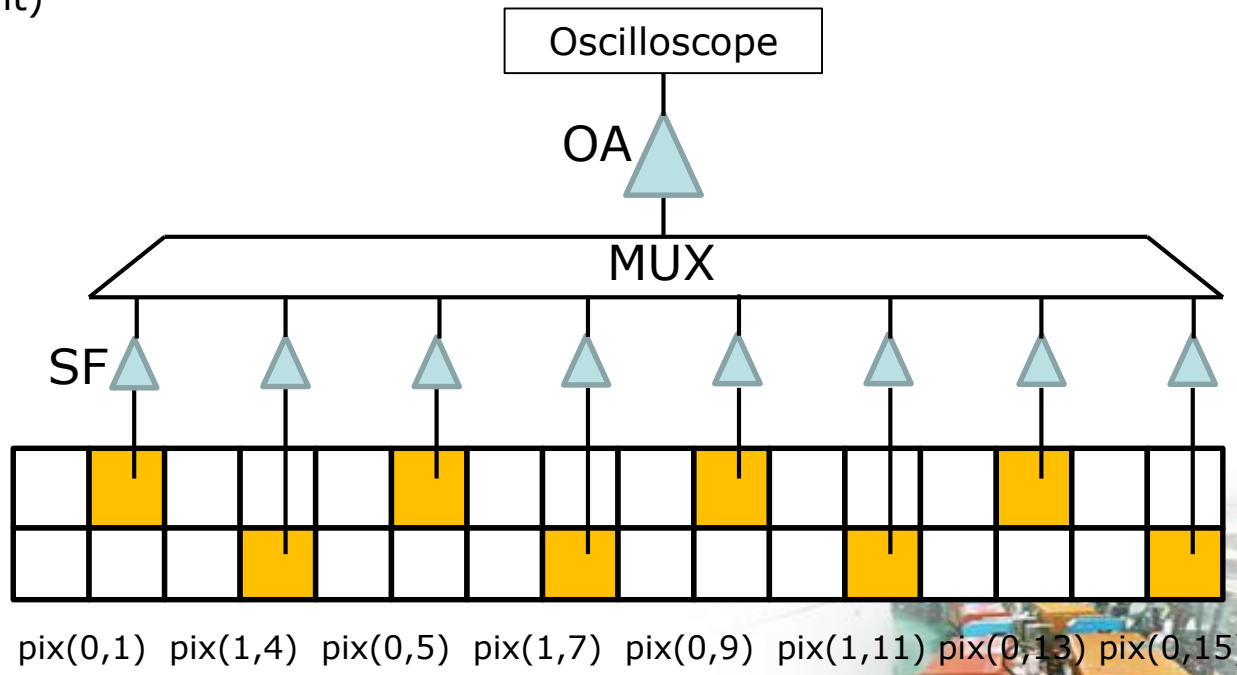
Generation of dummy bumps

Design for test

- Configuration of Bond pads and IO buffers
  - Original bond pads remained on both lower and upper chips, **accessible before 3D integration**
  - Functional IO buffers always stacked up with dummy IO to avoid conflicts of buffers
- Internal signal waveform are routed out of test pixels with buffers for oscilloscope observation
  - **Critical node** in the analog front-end
  - Two-stage buffers: Source-Follower and Operational Amplifier

Configuration for the access to ***lower tier***(left) and ***upper tier***(right)

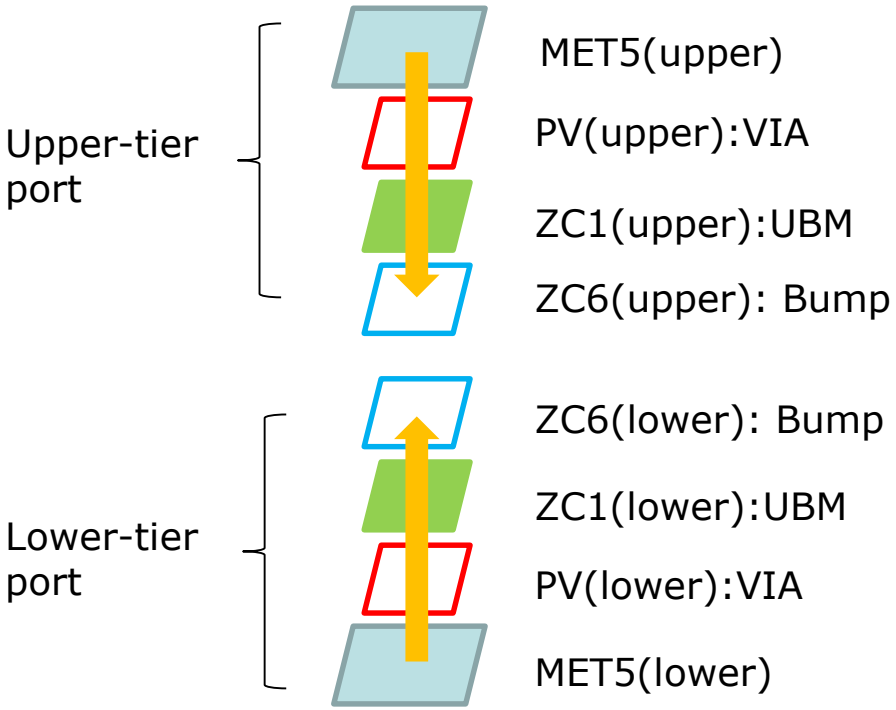




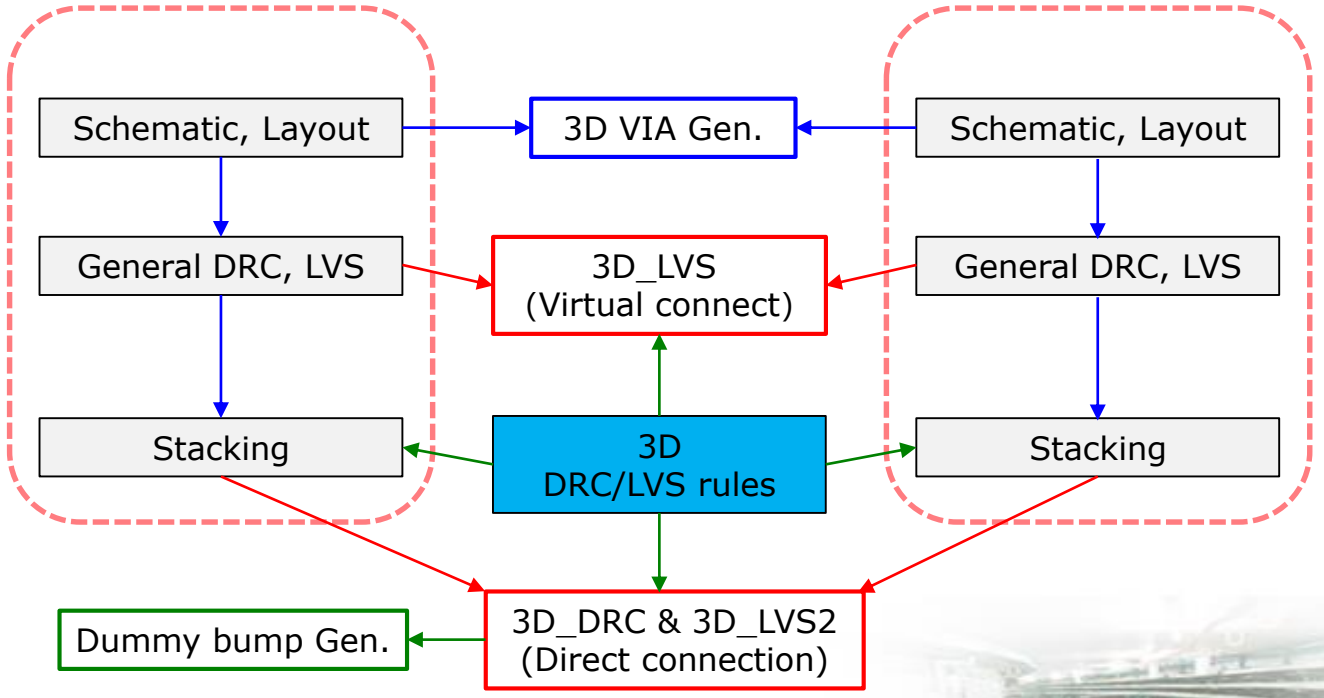
Design flow established

- Conventional SOI tape-out plus a special 3D add-on process
  - 3D related **rules** integrated into the EDA tools
  - On the basis of single layer SOI design flow

stack-up of 3D layers



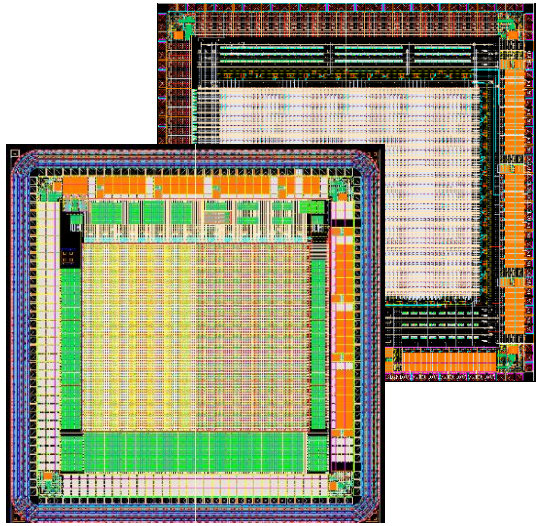
flow chart of SOI-3D design



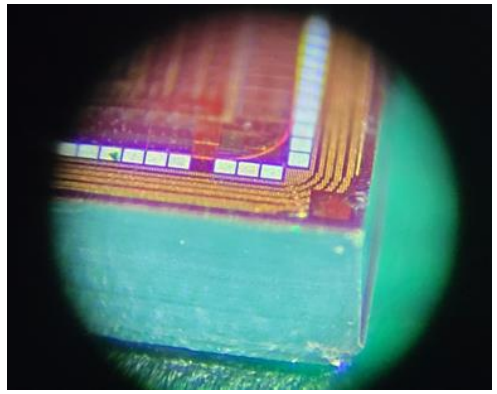
Manufacturing and 3D processing

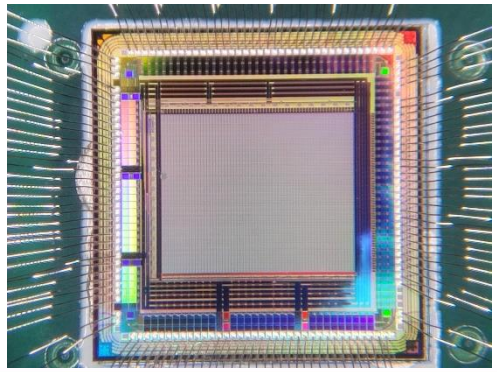
- CPV-4_U and CPV-4_L submitted to LAPIS in Dec. 2020
  - Single chips delivered in June 2021
  - Tests on single chips before the 3D integration
- 3D integration done on one MPW wafer ordered additionally
  - 3D chips delivered in the summer 2022

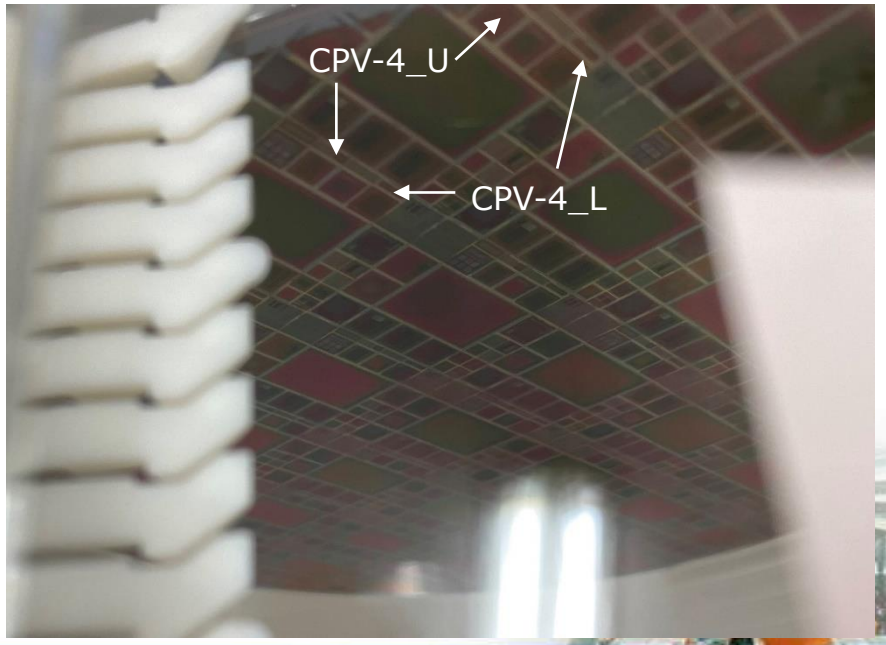
Layout of CPV-4_U



Layout of CPV-4_L

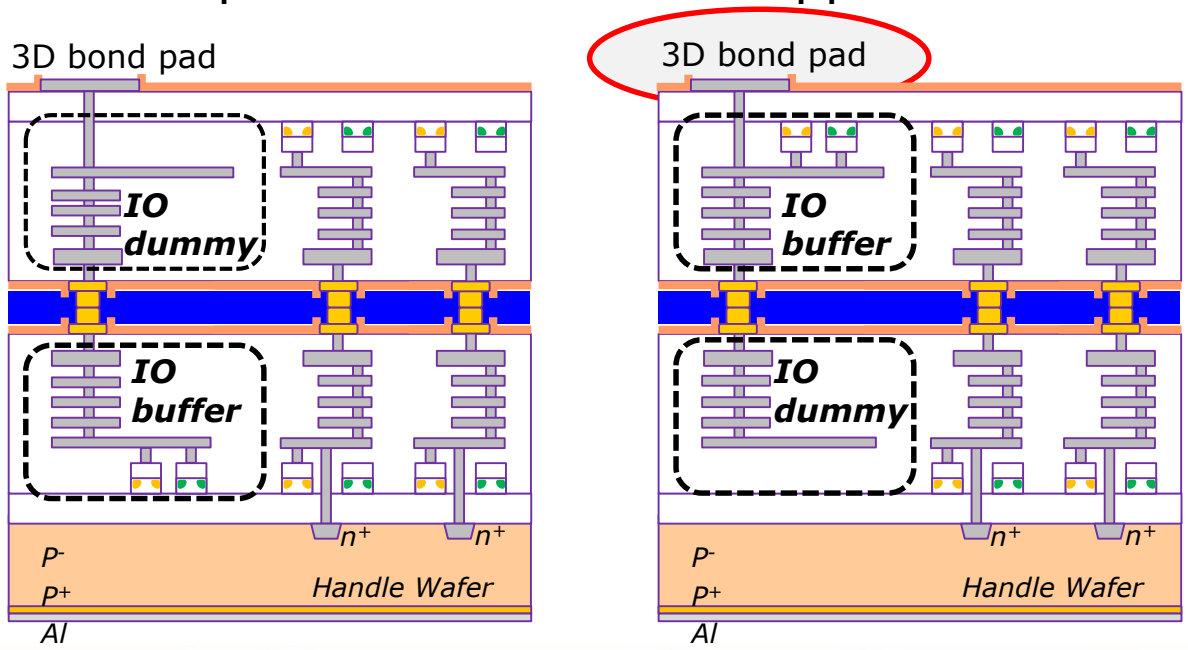


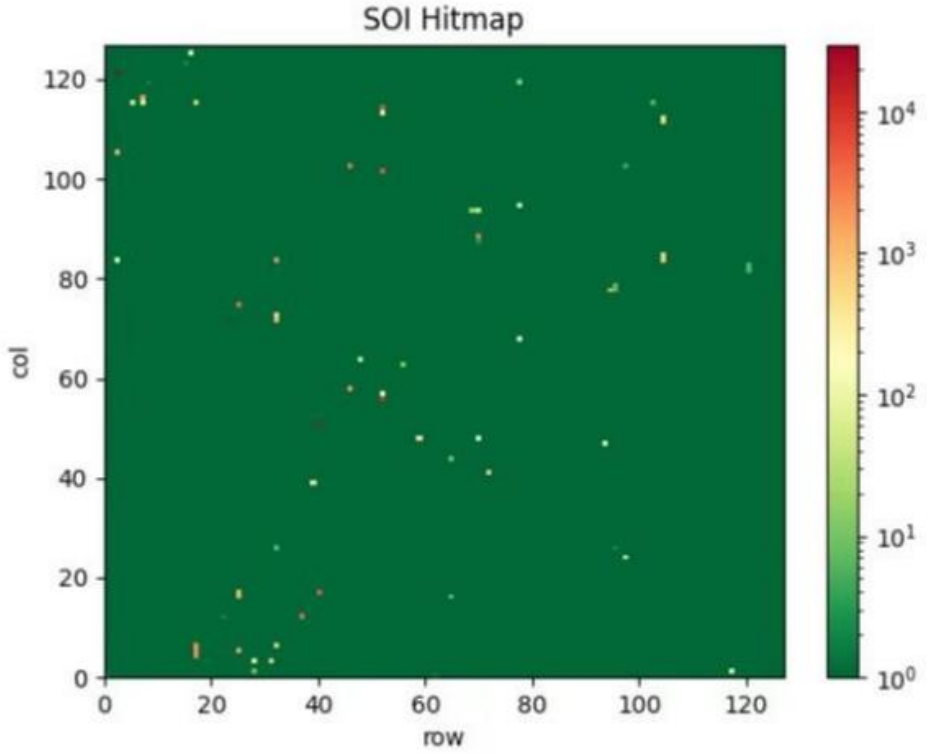




Tests on the upper chips

- Single upper chip tested before 3D integration, logic interaction with an FPGA
  - ✓ Write to pixel configuration register
  - ✓ Injection of digital test pulse and hit readout
- Same tests repeated on the upper tier of 3D chips
  - ✓ **One chip was found fully functional so far (3D chip #009)**
  - ✓ A couple more chips partially functional
- Bond pad connections to the upper tier established





Hit map of the full matrix in digital pulse test, with masked pixels and noisy pixels visible.

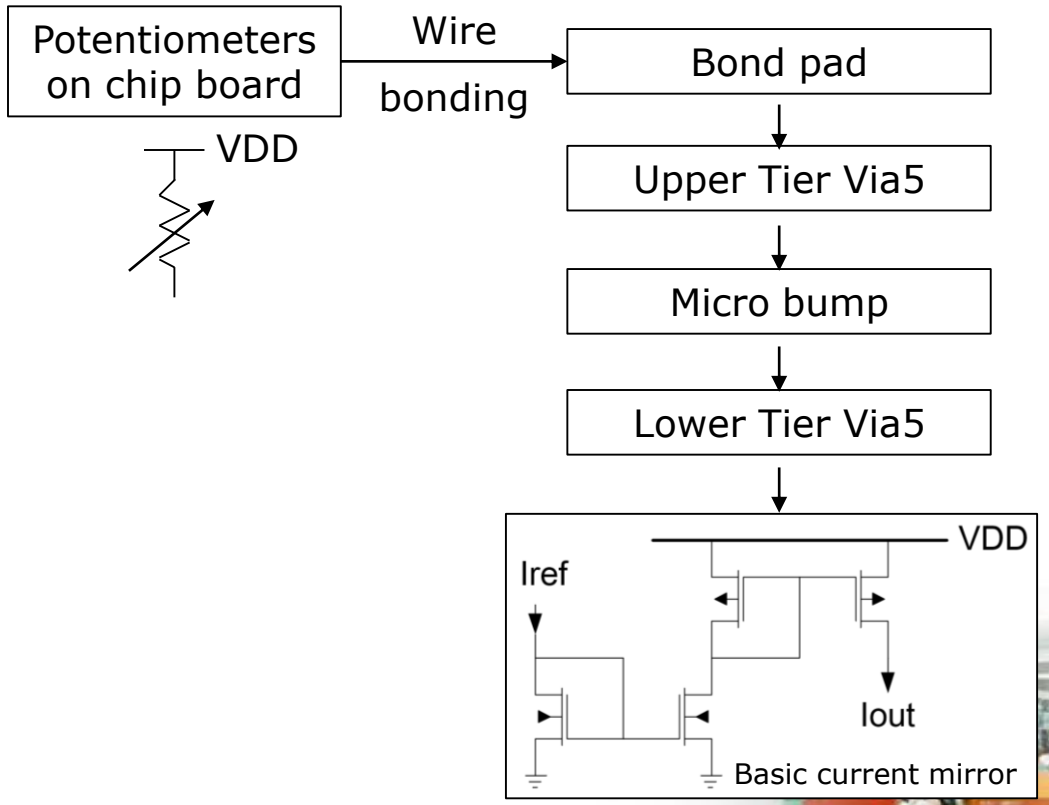
Tests on the lower tier of 3D chips

- Verification of the vertical connection to the lower tier
  - The bias current on **sensing diode** responded to light illumination
  - Current mirrors in **Lower Tier** worked properly
  - Multiplexer logic in **Lower Tier** worked properly
- Bond pad connections to the lower tier established

Comparison of current source channels between single lower chip and 3D chip

Current source channels	Single lower chip #008	3D chip #018
NSF	+24.3 uA	+23.9 uA
IOB	+73.0 uA	+70.8 uA
IDB	-0.86 uA	-0.75 uA
ITHR	-0.88 uA	-0.85 uA
IBIAS	-0.81 uA	-0.77 uA

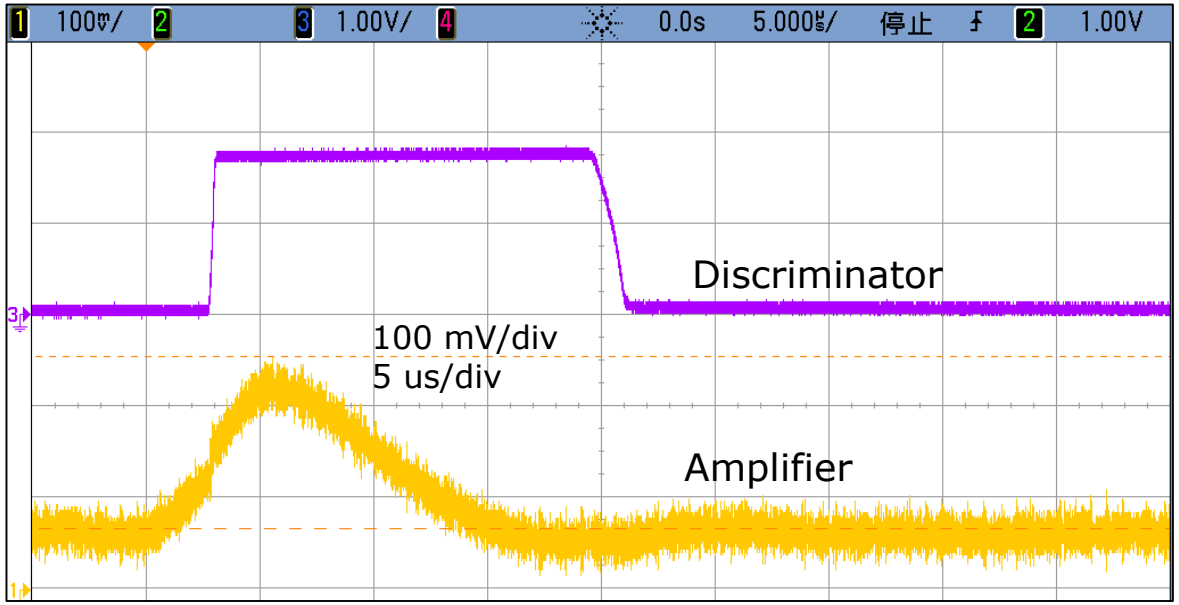
Electrical connection to the current mirror in lower tier



Tests on the lower tier of 3D chips (cont'd)

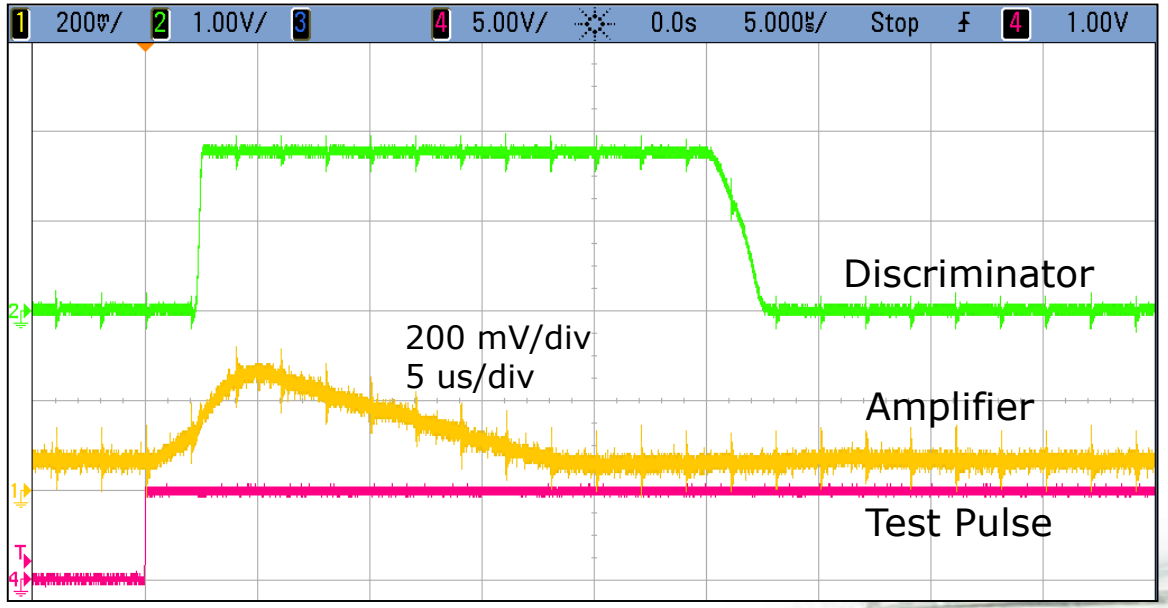
- Observed waveforms of amplifier and discriminator on the lower tier of 3D chips
  - One chip was found fully functional so far (3D chip #004)
  - Pulse test of equivalent input charge ~ 160 e^-

Waveforms from **single lower chip #008**



Analog frontend w/o Sensing Diode
Test charge injected ~ 100 e^-

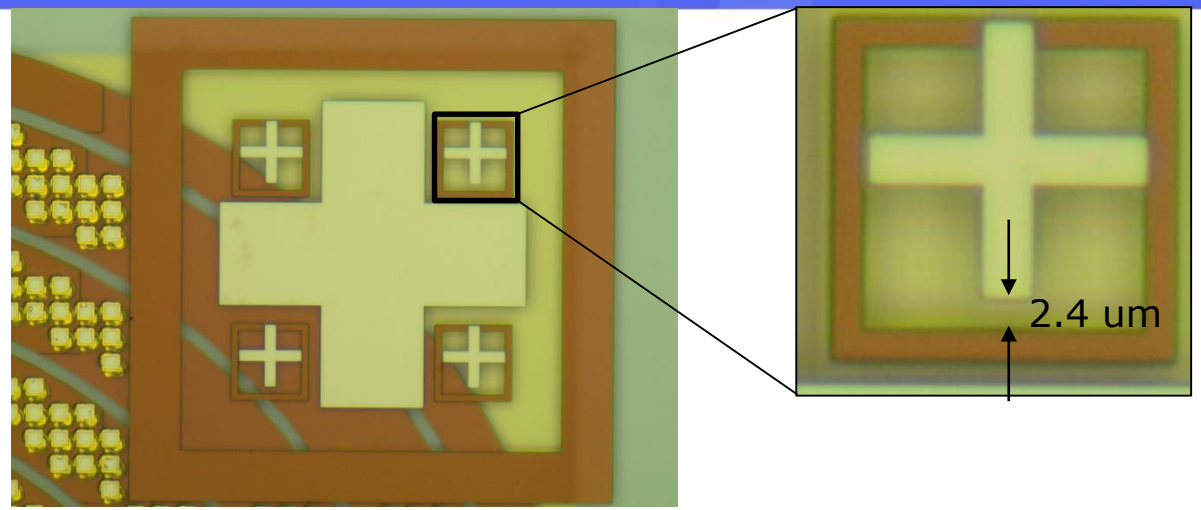
Waveforms from **3D chip #004**



Analog frontend w/o Sensing Diode
Test charge injected ~ 160 e^-

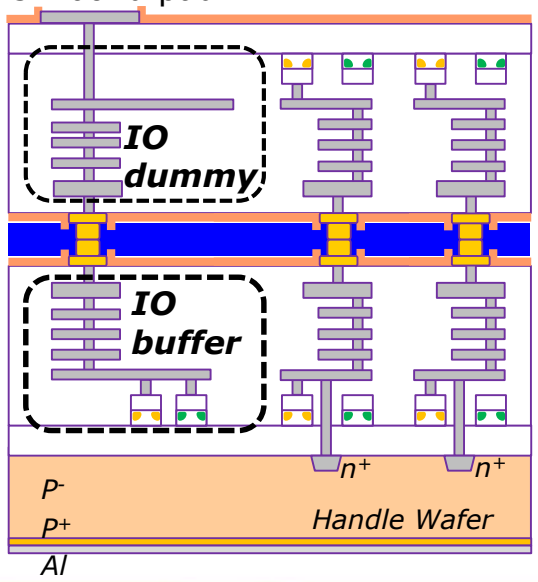
Method to verify the various connections further

- From bond pad to the upper tier
  - Resistance between two DVDD pads or DVSS pads
  - Good yield, 2~6 Ohm
- From bond pad to the lower tier
  - Resistance between two AVDD pads or AVSS pads
  - Low yield to be understood
- Pixel to pixel connections
  - May be indicated by the misalignment of marks



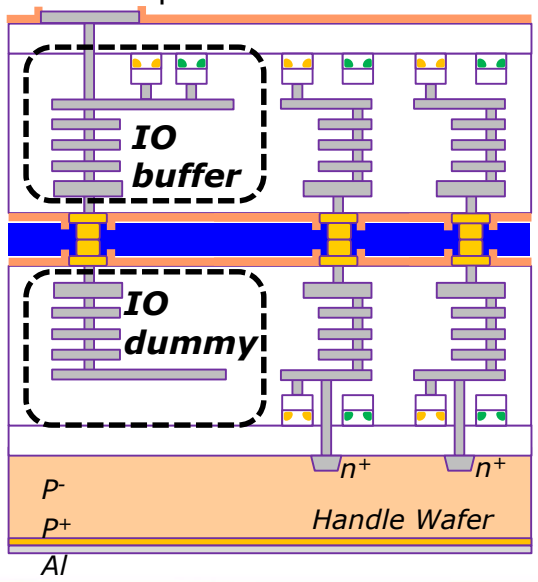
AVDD or AVSS

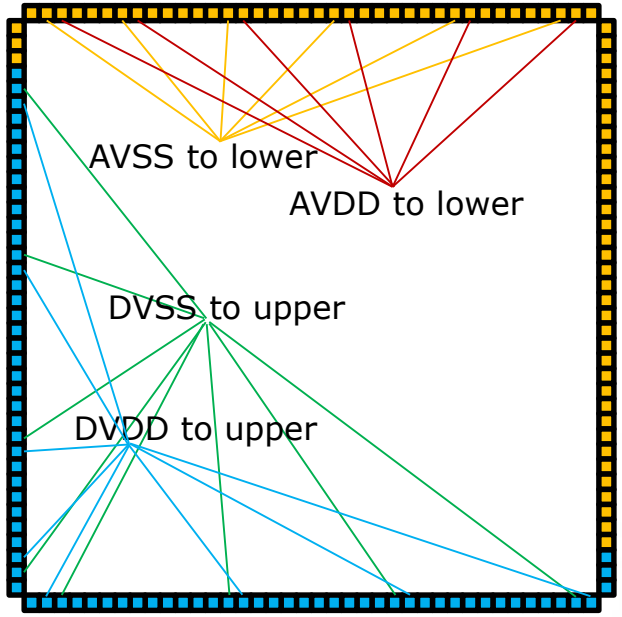
3D bond pad



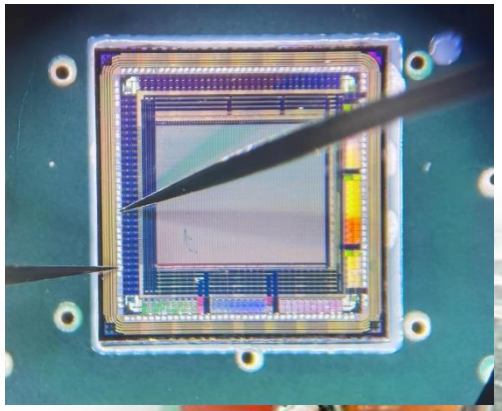
DVDD or DVSS

3D bond pad





Probed pads on
3D chip #020



Summary and outlook

- SOI pixel detector features
  - PDD sensing diode, low capacitance and low leakage
  - 200 nm FD-SOI circuit process
- 3D chip-to-chip bonding being pursued for high granularity of pixel with complex functionality
  - Micro bump pitch down to 7um, providing vertical connections in pixel level
  - Compatible with the existing SOI process, low temperature Stacking, TBV, thinning, …
- First trial of CPV-4 finished with encouraging results
  - A few samples identified with lower and upper tier operational
- Investigation of 3D connection yield will continue on a second wafer
  - Process tuning with T-micro is critical

Acknowledgment

- The SOI pixel detector and 3D bonding process have been developed in the framework of SOIPIX collaboration. The authors thank all the collaborators, especially Yasuo Arai, Ikuo Kurachi, Makoto Motoyoshi and Miho Yamada.

- This work is supported by the National Natural Science Foundation of China under grant number 11935019, 11575220.

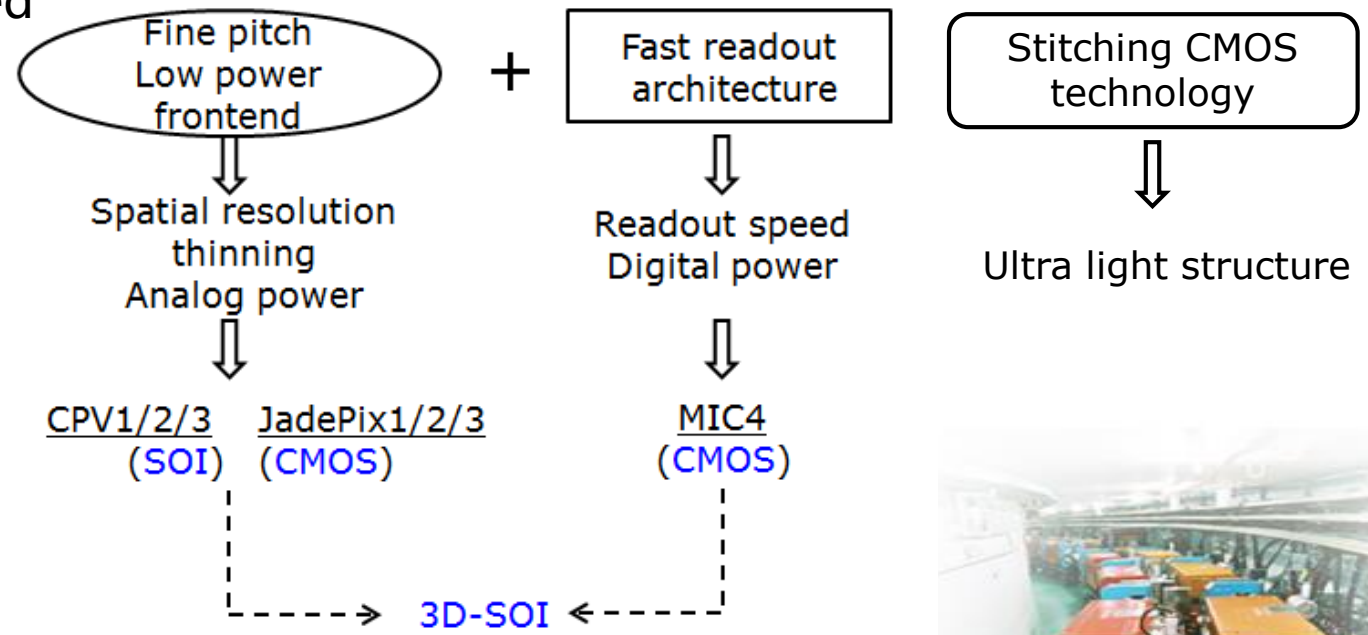
Grazie!

Thanks for your time!

Backup slides

Overview of pixel sensor R&D

- CMOS and SOI development in synergy
  - Following the same roadmap
  - Using the same readout system
- JadePix3 and CPV3 tests in parallel
- CPV4-3D design is done
  - Similar design scheme considered for the JadePix4
- Stitching CMOS technology is being explored



Specification of Vertex detector

- high spatial resolution, low material budget and fast readout required by the flavor tagging
  - Pixel sensor, the core part to construct a vertex detector

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs → Pixel sensor specs

$\sigma_{s.p.}$ ~ 2.8um → **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer → **Thinning to** ~ 50um

→ **low power** ~ 50mW/cm^2

r of Inner most layer ~ 16mm → **fast readout** ~ 1us

→ **radiation tolerance** ~

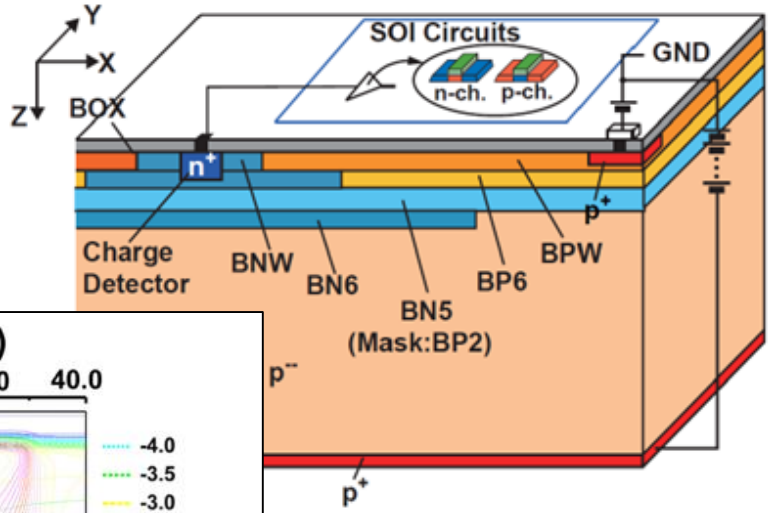
$\leq 3.4\ Mrad/year$

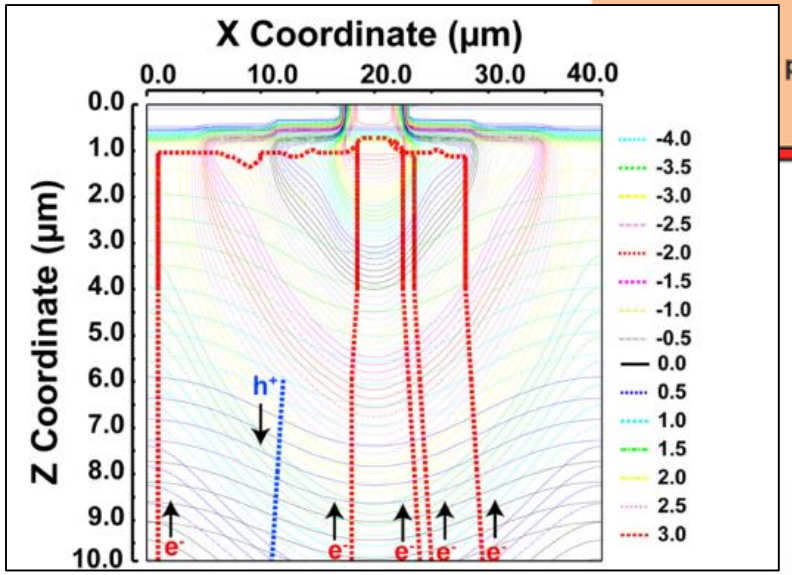
$\leq 6.2\times10^{12} n_{eq}/(cm^2\,year)$

- Two options to pursue:
  - Option #1: implement the specs in two **complementary** design (CDR baseline scheme)
  - Option #2: **explore new technology**, promote the performance (advanced scheme)

PDD sensing diode system

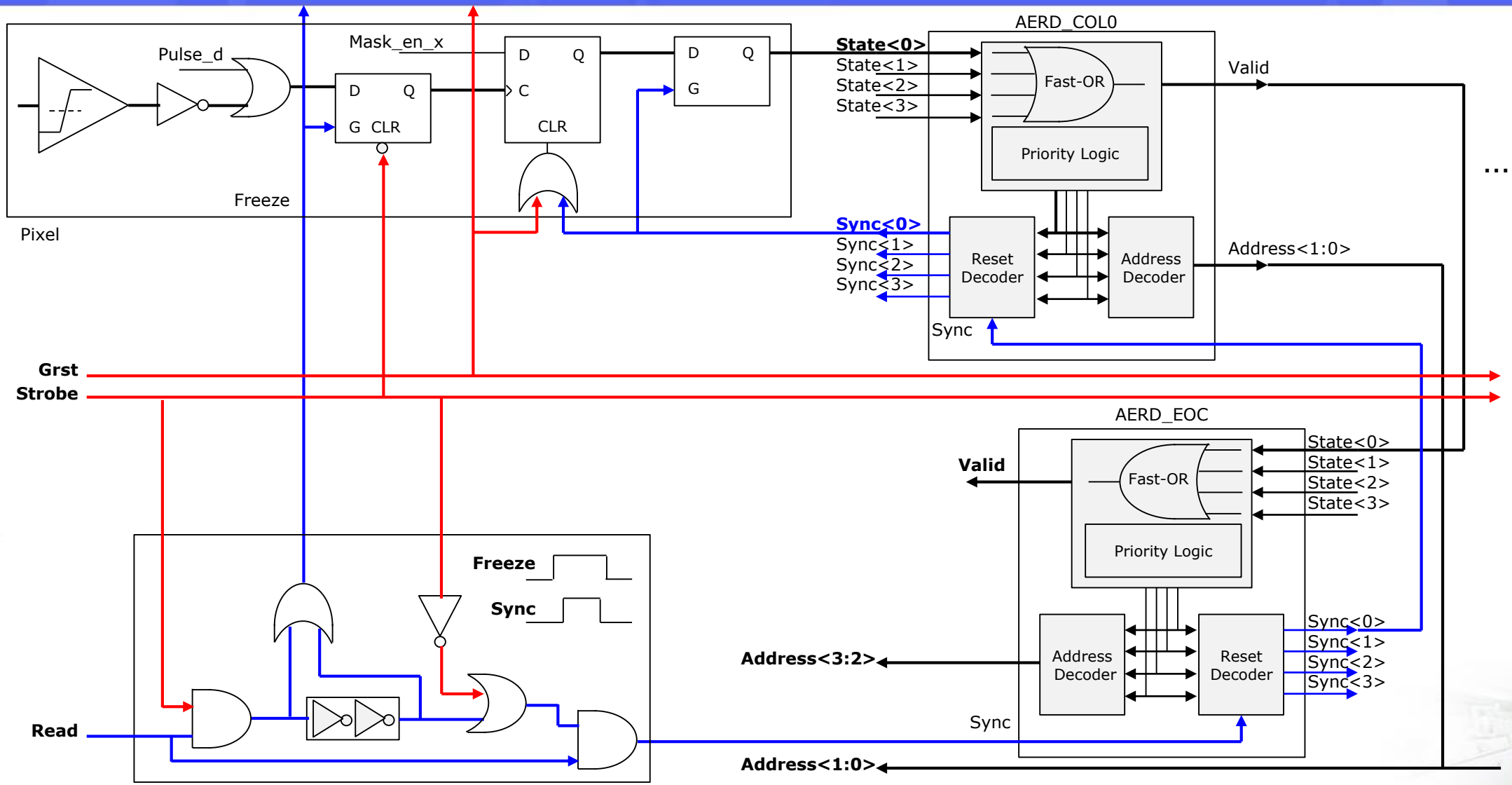
- Not 3D-specific, but the most active part of study in SOI pixel **sensor** technology
  - Evolution of years' development: BPW, Nested-wells, Double SOI, and PDD (Pinned Depleted Diode)
- **All-in-one solution** in the sensor part:
  - Control back-gate of transistors
  - Maximize charge collection efficiency
  - Suppress leakage current of Si-SiO_2 interface
  - Minimize the capacitance of electrode (Cd)
  - Shield the capacitive coupling between the sensor and pixel circuit





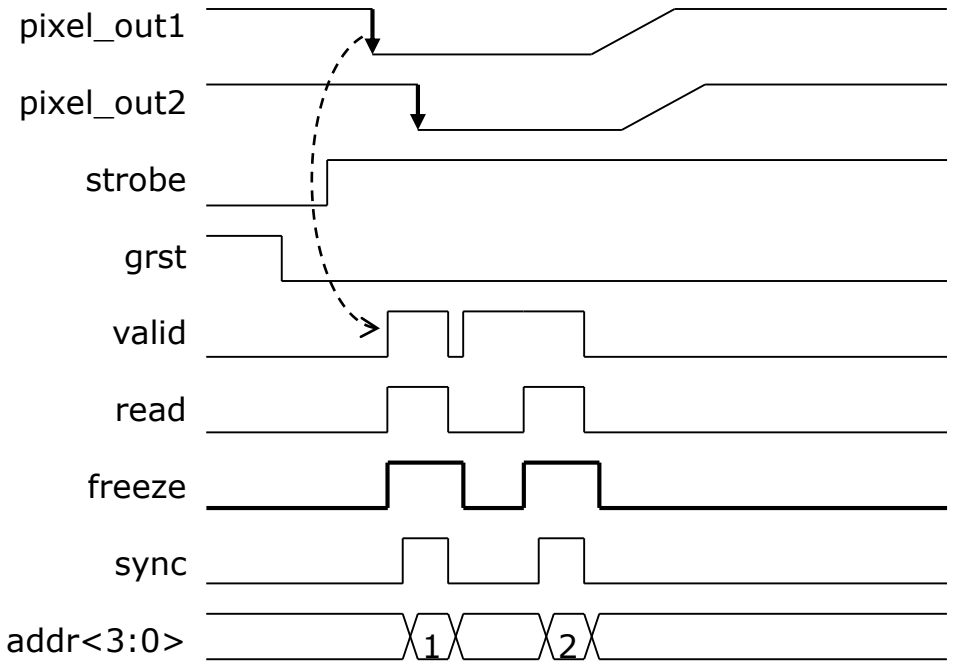
Electric field and e- transportation simulation in PDD structure:
Ref: doi:10.3390/s18010027 by Shoji Kawahito

Readout Architecture



Readout mode

- Continuous mode
  - Valid asserted by the falling edge of pixel_out1
  - Pixel_out2 froze before pixel_out1 is done
  - Timing resolution of falling edge < 1us



- Triggered mode
  - Strobe as the gate control
  - Readout after trigger (strobe)
  - Timing resolution of pulse width < 10us