AGH UNIVERSITY OF SCIENCE
AND TECHNOLOGY

The FLAME and FLAXE ASICs

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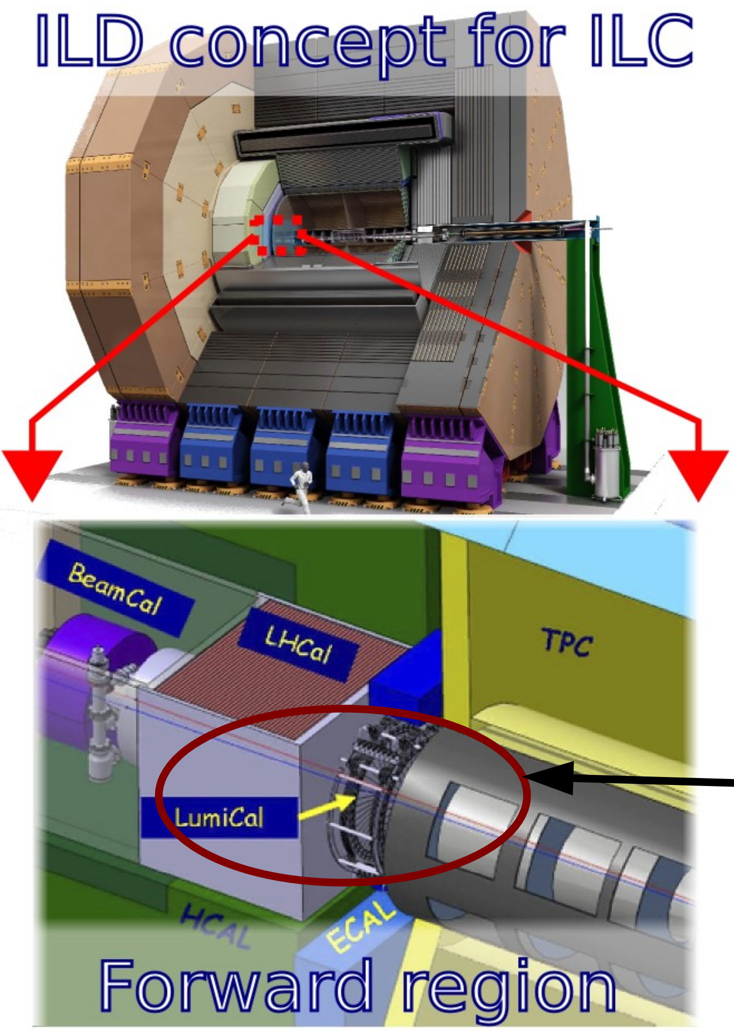
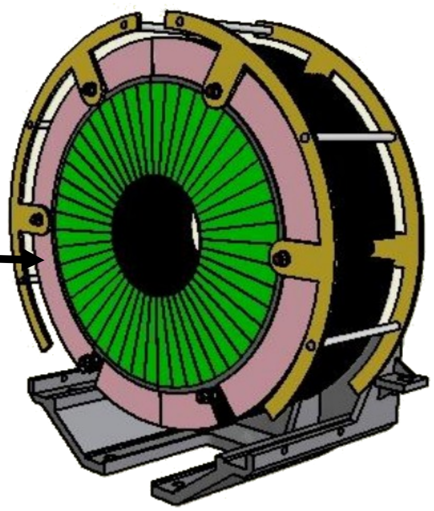
Outline

- Motivation
- FLAME design
- FLAME lab measurements
- FLAME on testbeams
- FLAXE ASIC for LUXE experiment
- To do / New developments and Plans

Motivation (~2015)
Readout for ILC forward calorimeter



Development of readout electronics for a compact very forward region calorimeter – LumiCal - for the measurement of luminosity in future Linear Collider



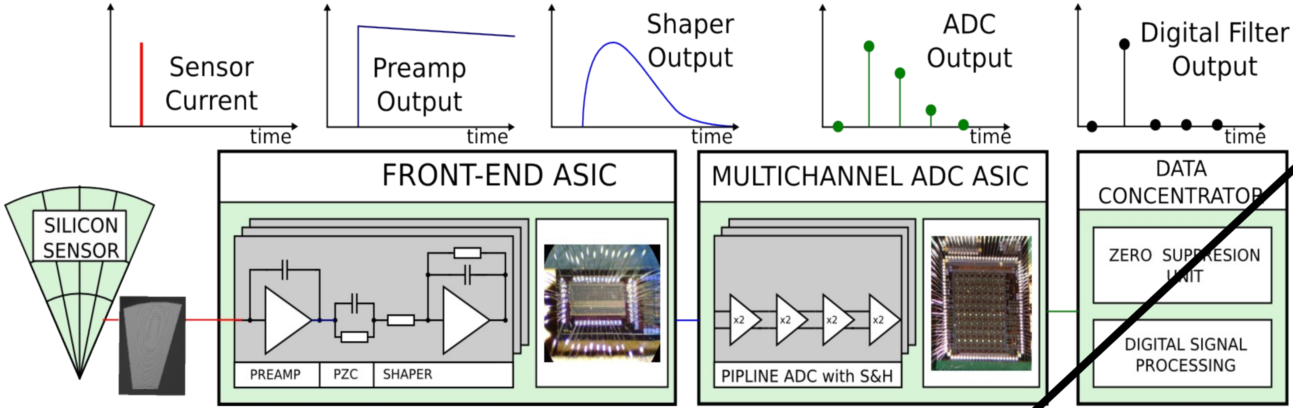
LumiCal

- 2 barrels of silicon-tungsten sandwch calorimeter
- Each barrel - 30 layers
- Silicon detector layer – 48 sectors
- Sector divided into 64 radial pads (5-35pF)
- 92 160 channels in barrel
- Readout SoC dedicated multichannel ASIC - FLAME

Motivation (~2015)
From AMS 350nm to new low power in 130nm

FLAME - main goals:

- Front-end with variable gain and 10-bit ADC in each channel
- CR-RC shaping to allow amplitude&time reconstruction by deconvolution
- 20-40 MS/s sampling with possibility of asynchronous sampling
- Fast data serialization and transmission
- Ultra-low power, 32-channel SoC type chip in 130 nm CMOS



Old LumiCal detector readout comprised:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, 9mW (AMS 0.35um)
- 8 channel pipeline ADC (Tsmp<=25MS/s, 24mW@20MS/s) with ser&fast I/O (AMS 0.35um)
- FPGA based data concentrator and further readout

Motivation
Long term perspective

- FLAME was initially thought as a front-end ASIC for forward calorimeter in International Linear Collider, but because the prospect of Linear Collider construction was always long, its specs were more focused on the requirements from beamtests.
- In parallel, FLAME was also an R&D project on ultra-low power System-on-Chip front-end ASIC. In particular for the design&optimisation of different blocks and signal processing chain:
  – Amplitude&Time reconstruction by deconvolution from a simple CR-CR signal shape
  – Good resolution fast ADC conversion in each channel to allow online DSP.
  – High speed ultra-low power data link

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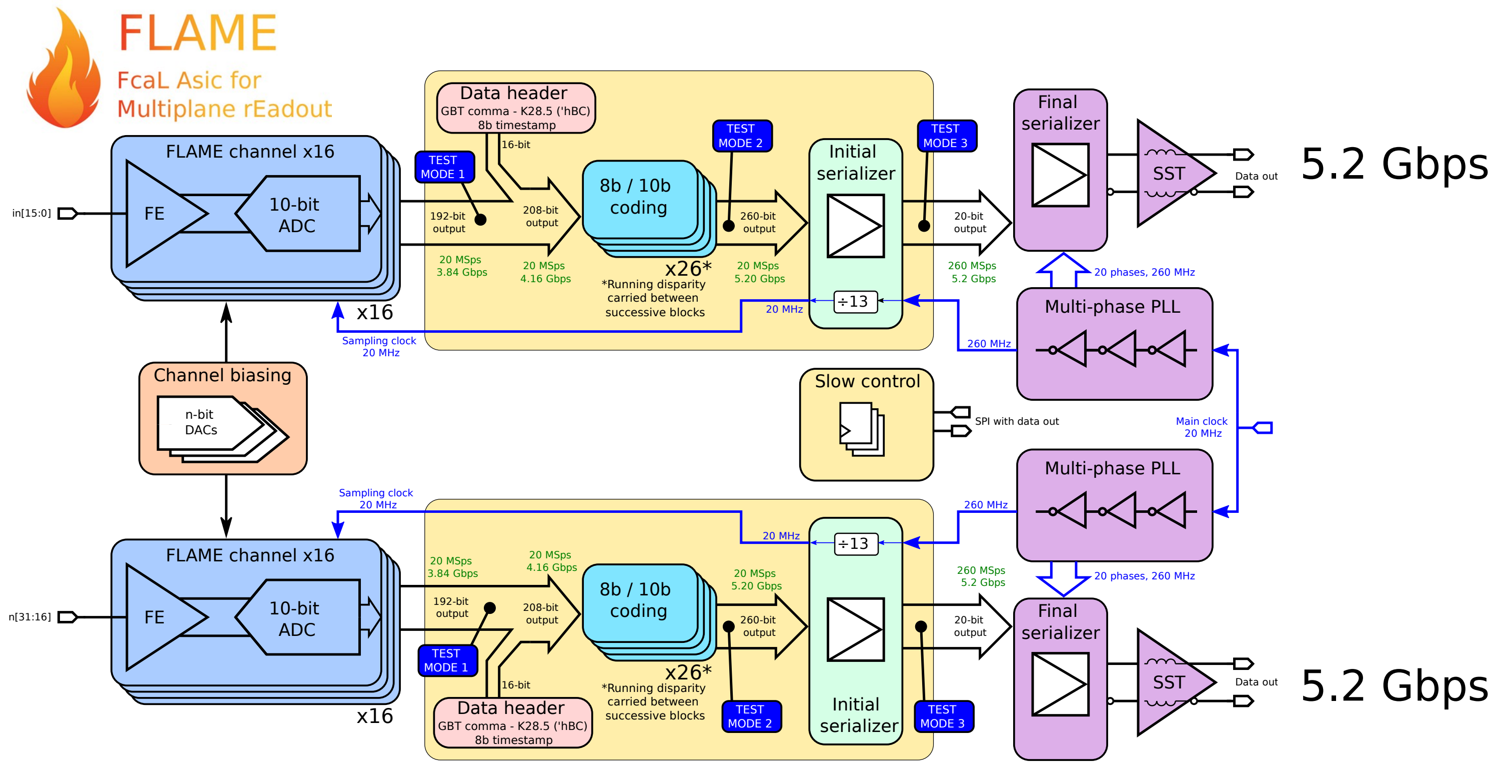
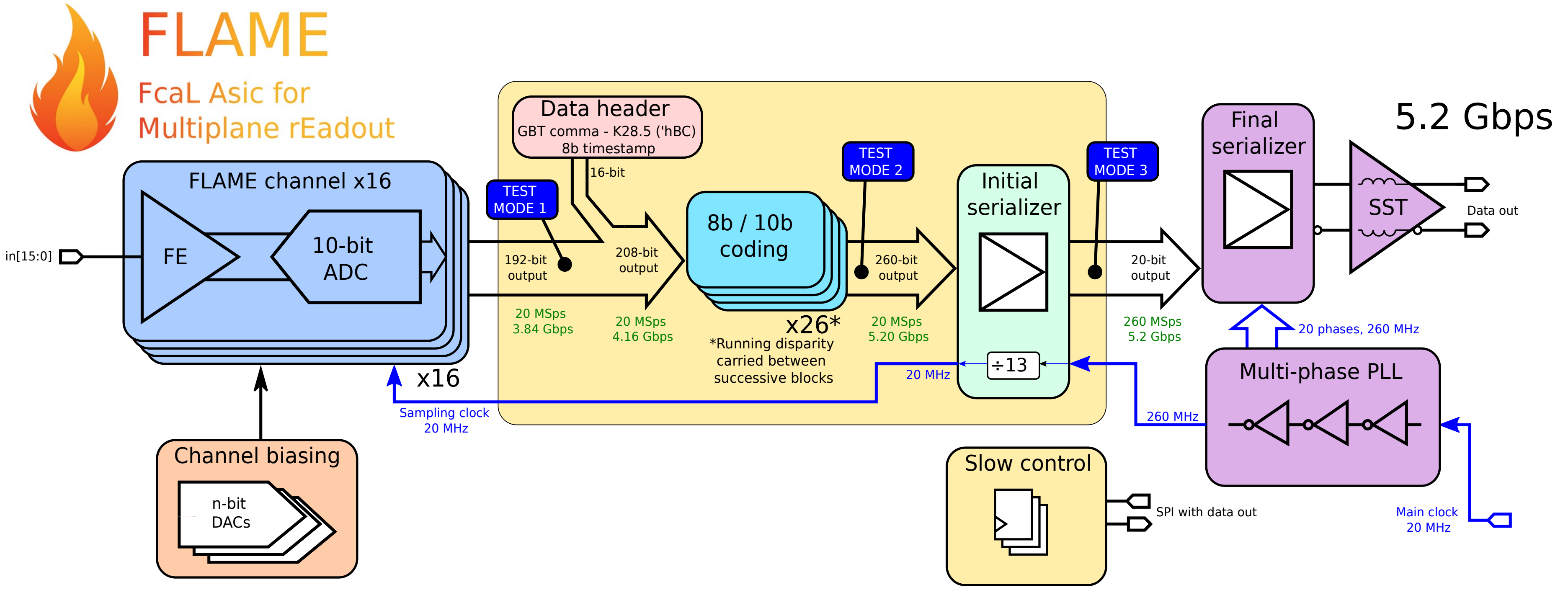
FLAME design Architecture



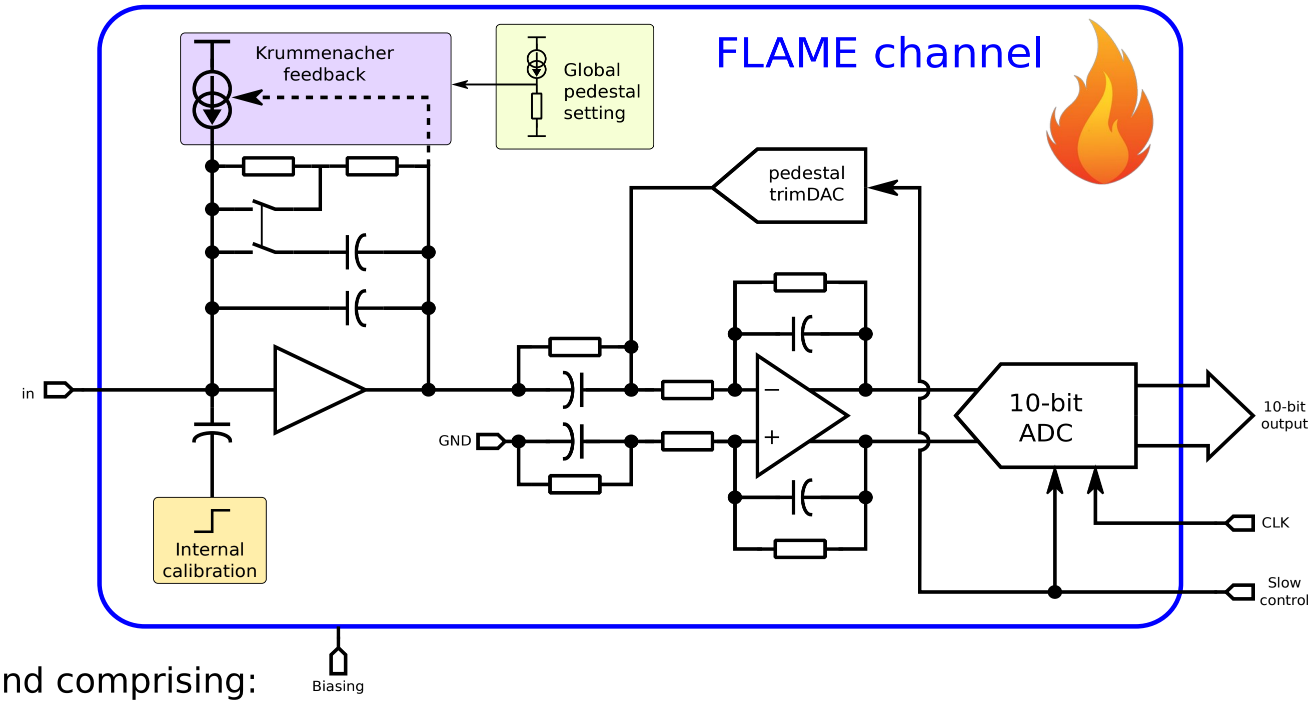
• FLAME is a 32-channel ASIC in CMOS 130nm with analog front-end (T_{peak}~50ns, switched gain), and 10-bit ADC (f_{sample}=20MHz) in each channel, followed by two fast (5.2Gbps) serialisers and data transmitters

FLAME design
Architecture ...



FLAME uses two identical 16-channel blocks with 16x FE&ADC + serialiser + SST. Biasing DACs and Slow Control are common for the chip.

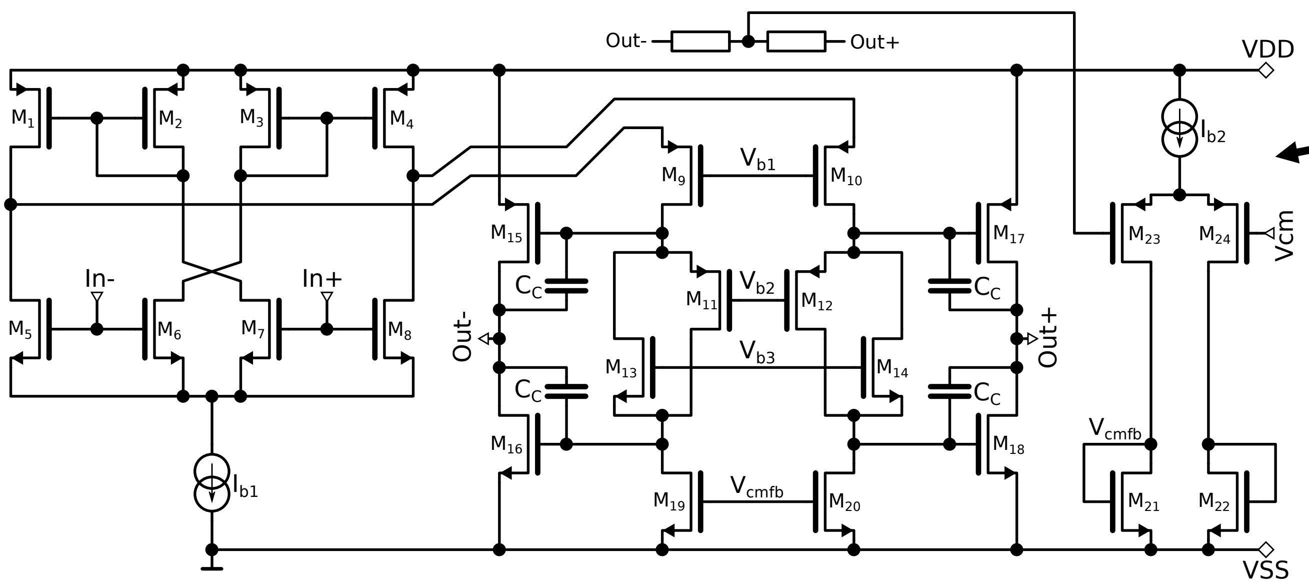
FLAME design
Single channel architecture

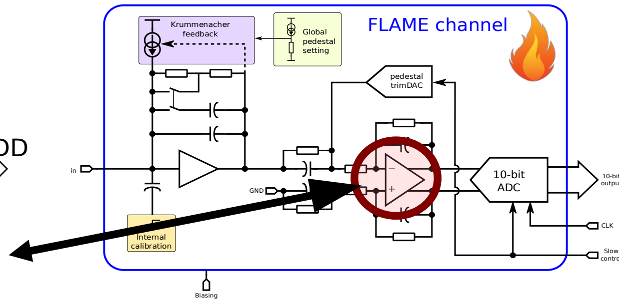


- Analogue front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – for MIP sensitivity (up to ~200fC)
    - Low gain – for shower measurement (up to ~6pC)
  - Default detector capacitance ~20-40pF
  - Differential CR-RC shaper with ~50ns peaking time – **for amplitude and time measurement using deconvolution**
  - Krummenacher feedback
  - Internal calibration and pedestal trimDAC
  - Power consumption ~1.2mW

- 10-bit SAR ADC in each channel
  - Default sampling rate 20MSps (max. up to 50MSps)
  - DNL, INL < 0.5 LSB
  - ENOB > 9.5
  - Ultra low power consumption (~0.7 mW/channel@40 MSps ~0.35mW/channel@20MSps)

FLAME design - single channel
Fully differential shaper amplifier

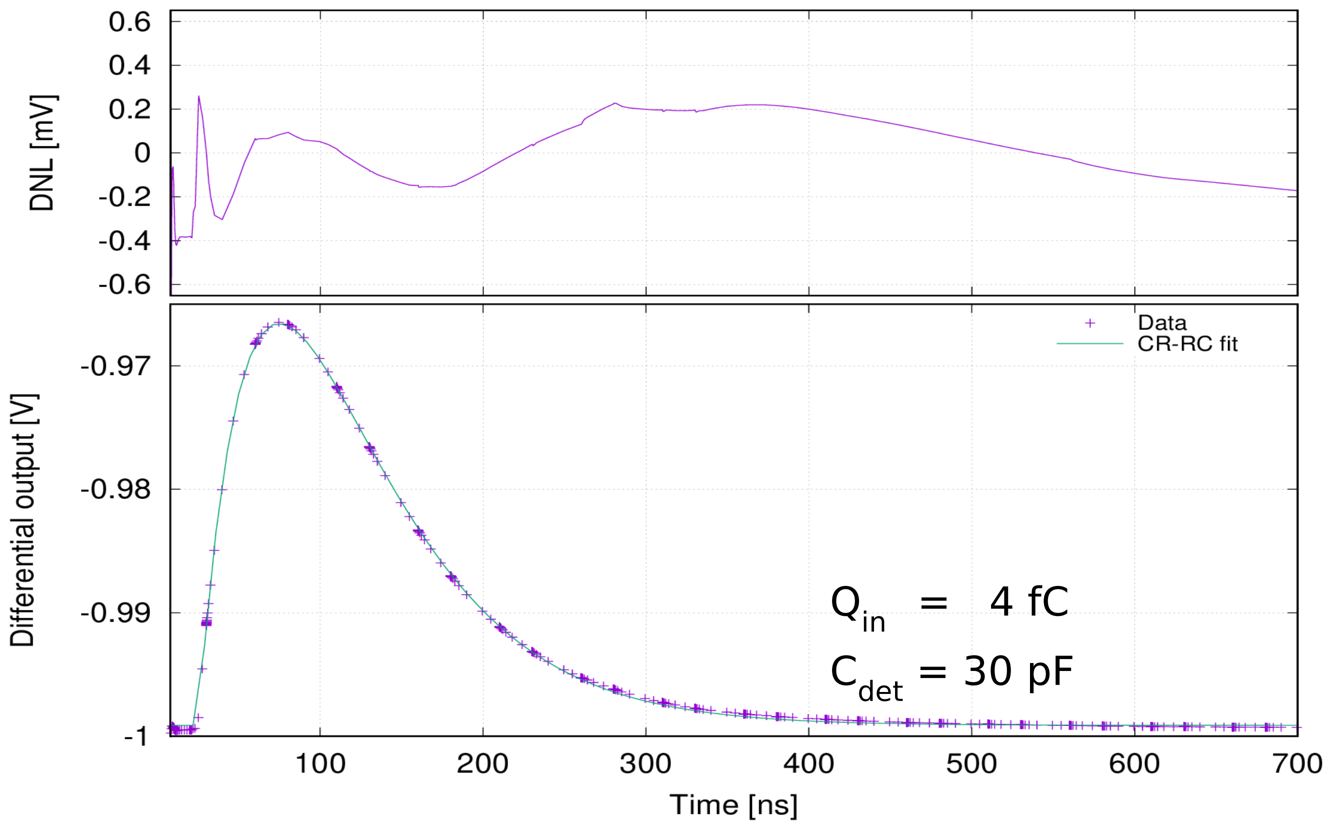




Two-stage amplifier with a recycling folded Cascode (RFC) differential input stage and an AB class rail-to-rail differential output stage. This architecture was chosen for the lowest power consumption at the highest power efficiency and to obtain rail-to-rail output.

FLAME design - single channel CR-RC shaping for deconvolution

Transient simulation of FLAME front-end channel

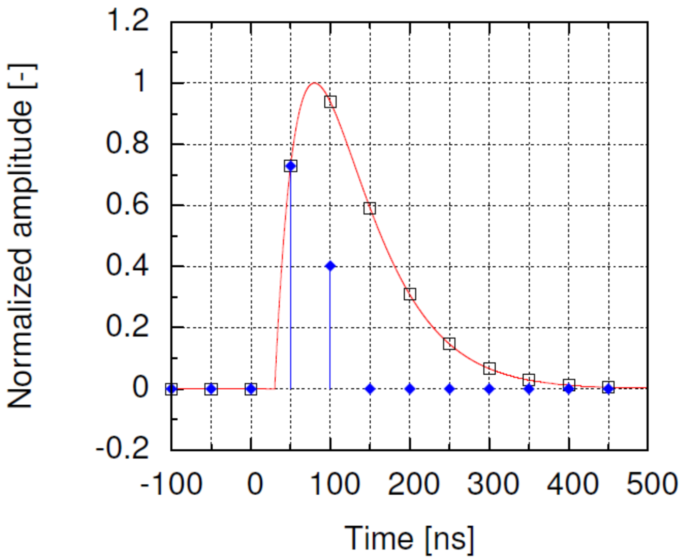


- Simulated analogue response for MIP (4fC) in high gain
- Amplitude ≃ 33 mV (15.5 LSB)
- Excellent agreement with CR-RC pulse – difference (DNL) between data and fitted CR-RC below ±0.5 mV (±0.2 LSB)

Pulse shape is critical for quality of deconvolution which can be applied for synchronous and asynchronous (test-beam) data sampling

FLAME design – CR-RC shaping & deconvolution
Deconvolution procedure

For asynchronously sampled CR-RC pulse the amplitude and time are reconstructed using deconvolution procedure (3-sample FIR filter).



FE pulse

$$V_{FE}(t)=\frac{Q_{\text{in}}}{C}\left(\frac{t}{\tau_{sh}}\right)e^{-\frac{t}{\tau_{sh}}}$$

Samples v_i

Deconvolution d_i

$$d_i=v_i-2e^{-\frac{T_{smp}}{\tau_{sh}}}v_{i-1}+e^{-2\frac{T_{smp}}{\tau_{sh}}}v_{i-2}$$

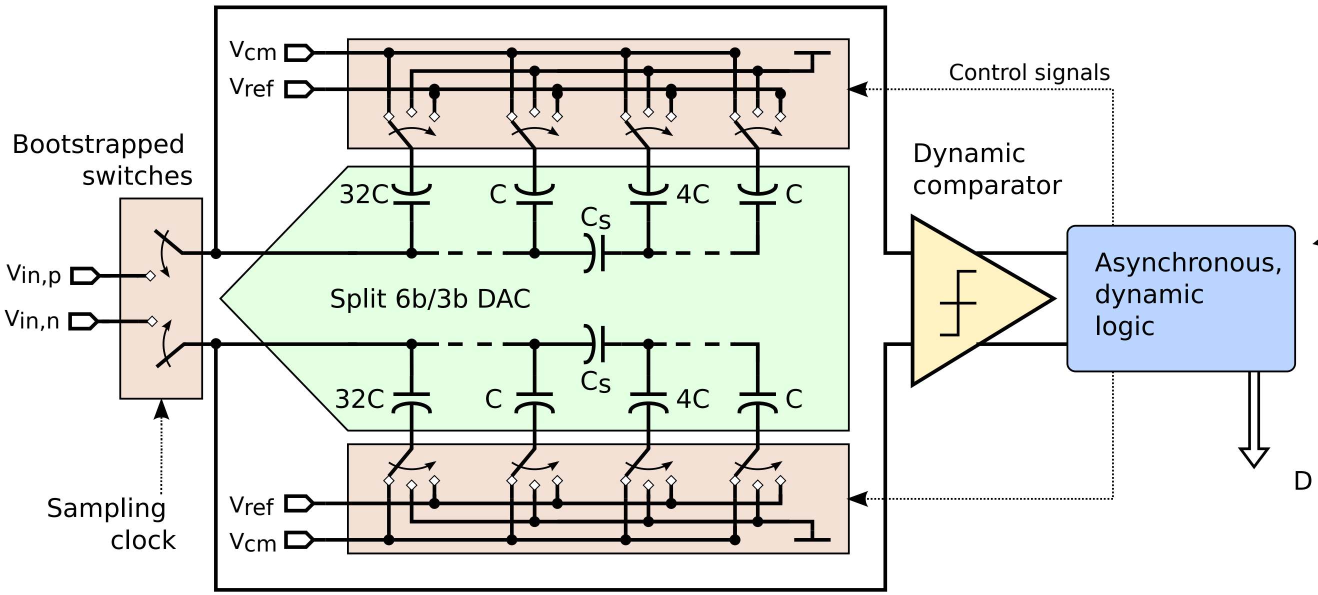
Amplitude and time are reconstructed respectively as weighted sum or weighted ratio of two non-zero d_i samples

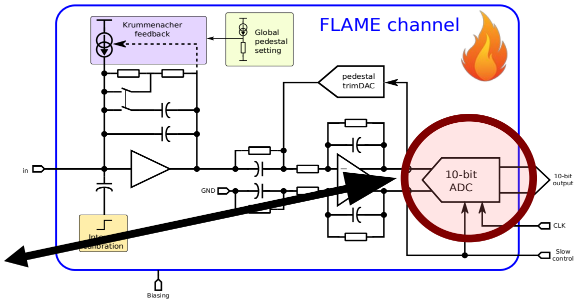
$$A=(d_1+d_2)\left[\frac{\tau_{sh}}{T_{smp}}e^{\frac{T_{smp}-\tau_{sh}}{\tau_{sh}}}\right]\frac{e^{-\frac{t_0}{\tau_{sh}}}}{1-\frac{t_0}{T_{smp}}\left(1-e^{-\frac{T_{smp}}{\tau_{sh}}}\right)}$$

Time dependent correction

$$t_0=\frac{\frac{d_2}{d_1}T_{smp}}{\frac{d_2}{d_1}+e^{-\frac{T_{smp}}{\tau_{sh}}}}$$

FLAME design – single channel 10-bit fast ultra-low power ADC



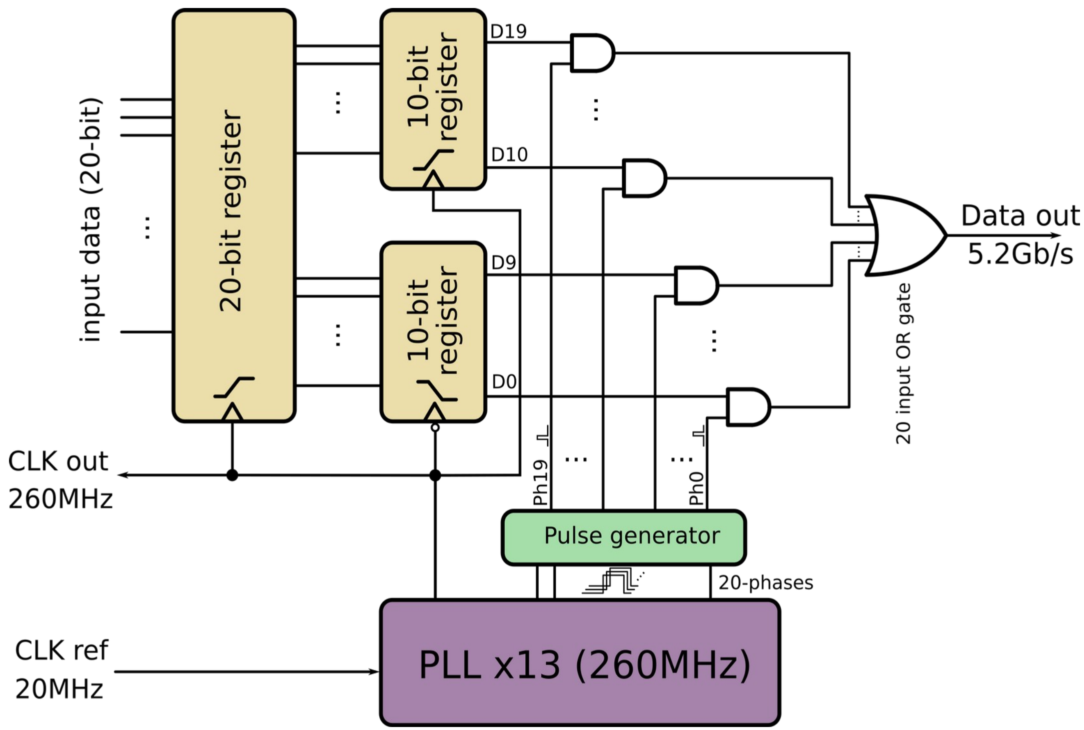


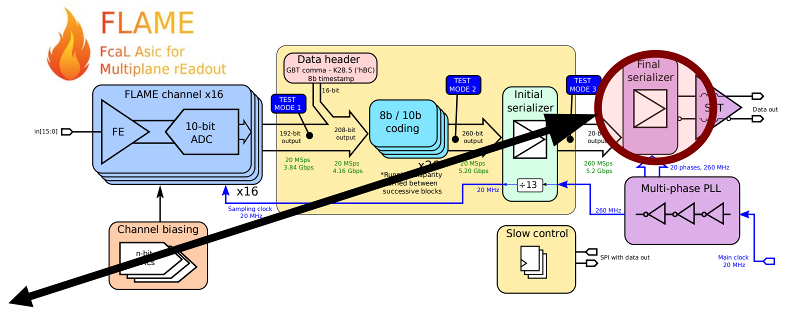
This&other ADCs were discussed in Jakub Moroń talk on ADCs!

Main features:

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption***
- Asynchronous and dynamic logic – no clock tree – ***power saving, allows asynchronous sampling***
- Bootstrapped sampling switch for good linearity
- Works up to >50MS/s (0.85mW@50MS/s)

FLAME design
Fast serialiser architecture



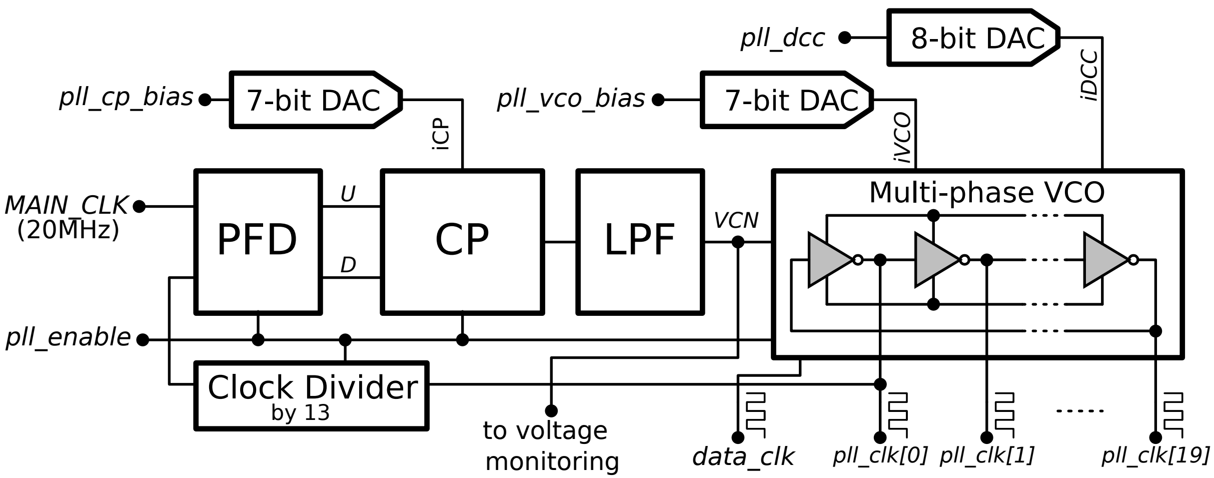


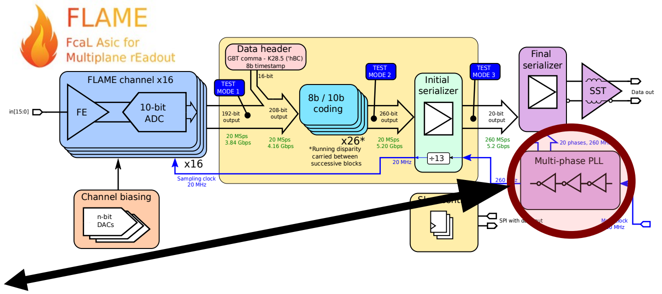
- Serialization based on 20 uniformly distributed phases of PLL clock
- PLL generates 260MHz clocks from 20MHz reference (x13)
- Data muxed by 20 narrow pulses (~200ps) passing data bits through NAND gates
- Two levels of data registers for better time margins
- Single phase 260MHz clock output for initial serializer
- 5.2 Gb/s output data rate

Two identical serialisers are implemented in FLAME, each for 16 channels

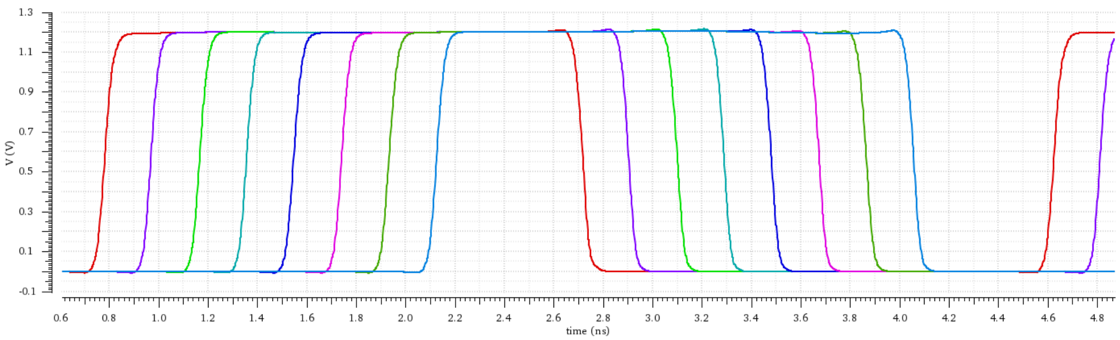
FLAME design
Multi-phase PLL for fast serializer

PLL block diagram



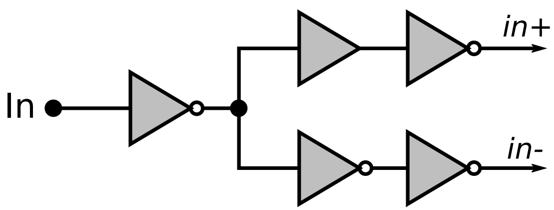


Simulated PLL clock waveforms

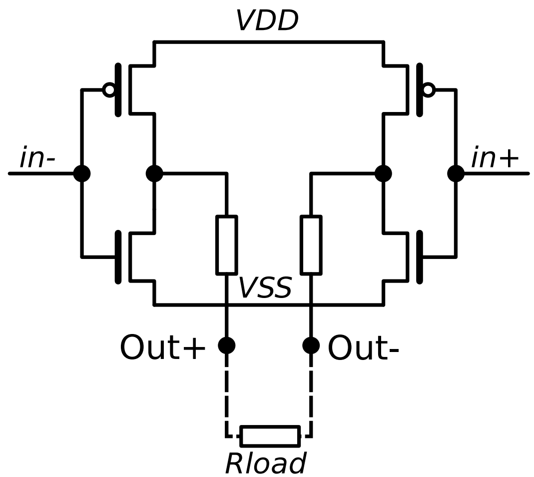


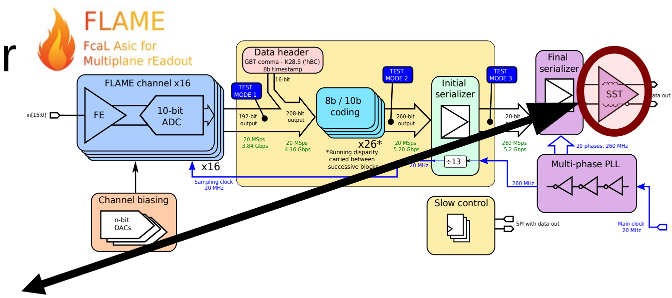
FLAME design
Fast SST (Source-Series Terminated) Driver

Single-ended to differential converter



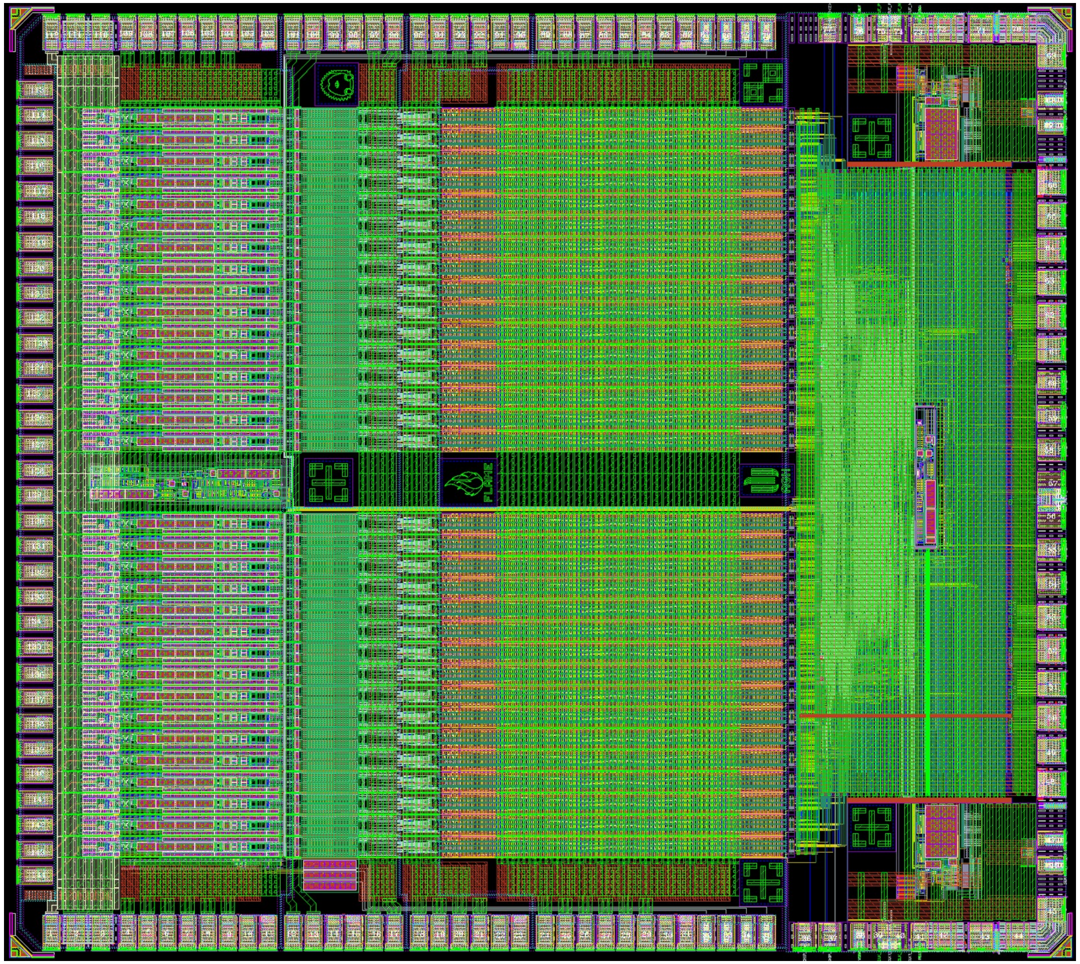
Low impedance 2-inverter Output stage





- Can operate at relatively low power supply,
- Tolerance to common mode noise,
- Ability to work at very high frequency,
- **Consumes about four times less power than CML**

FLAME design
Layout&Submission&Production



Die size 3.7mm x 4.3mm

FLAME was fabricated in 2019

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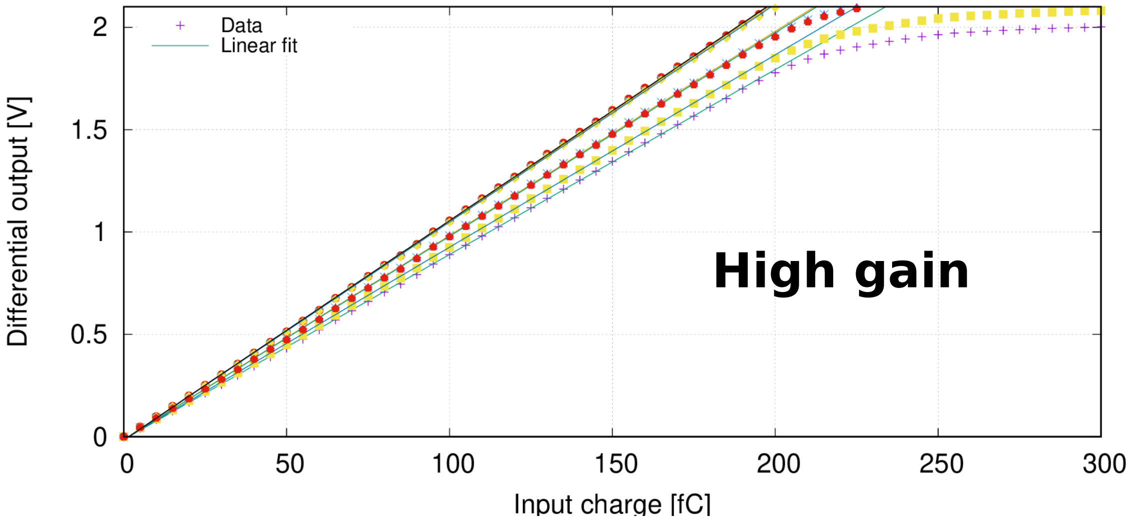
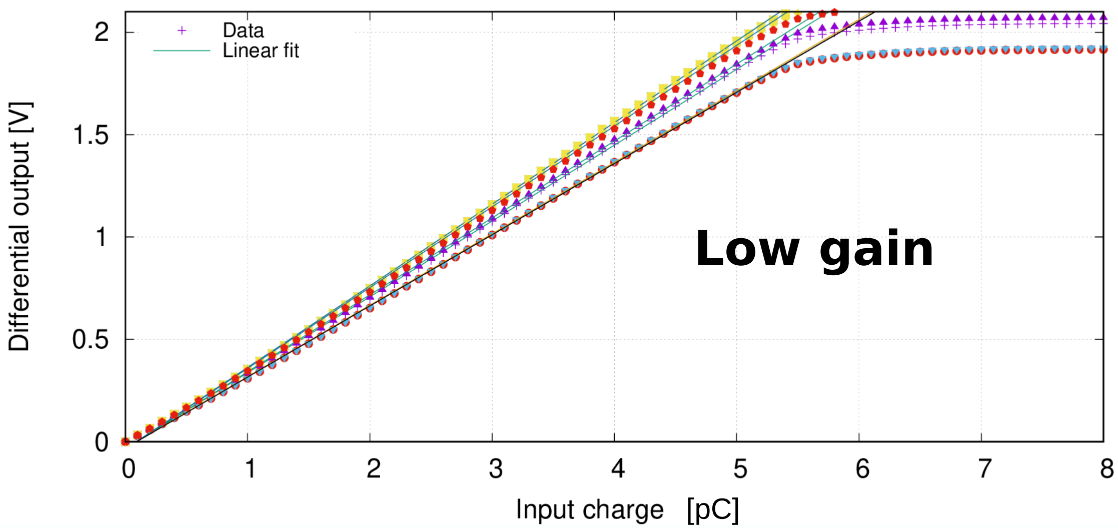
FLAME lab measurements
Analog output - gain



Average gain: 9.23 mV/fC
σ = 0.62 mV/fC

Linear response up to 200 fC (~50 MIPs)



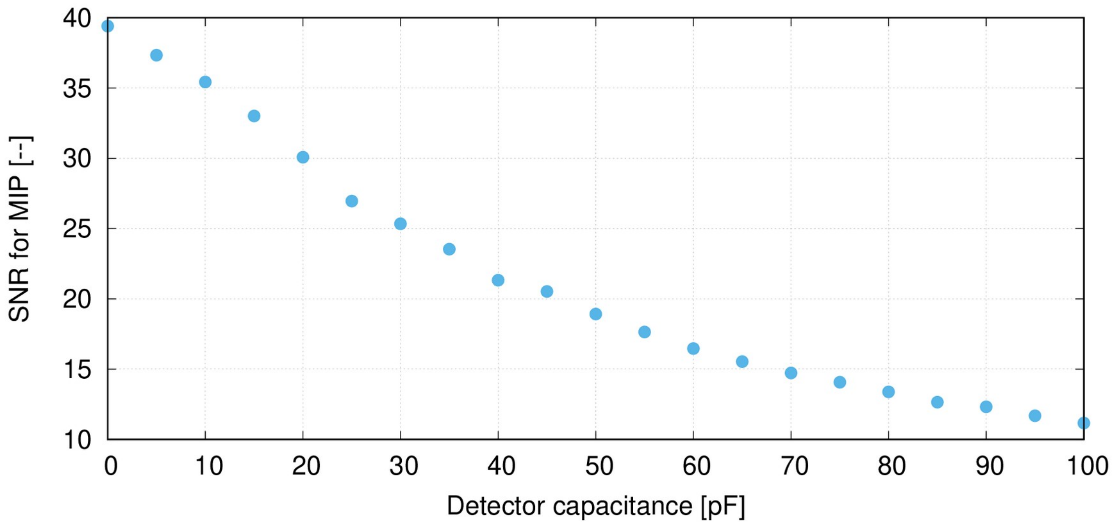
Average gain: 378.69 mV/pC
σ = 21.37 mV/pC

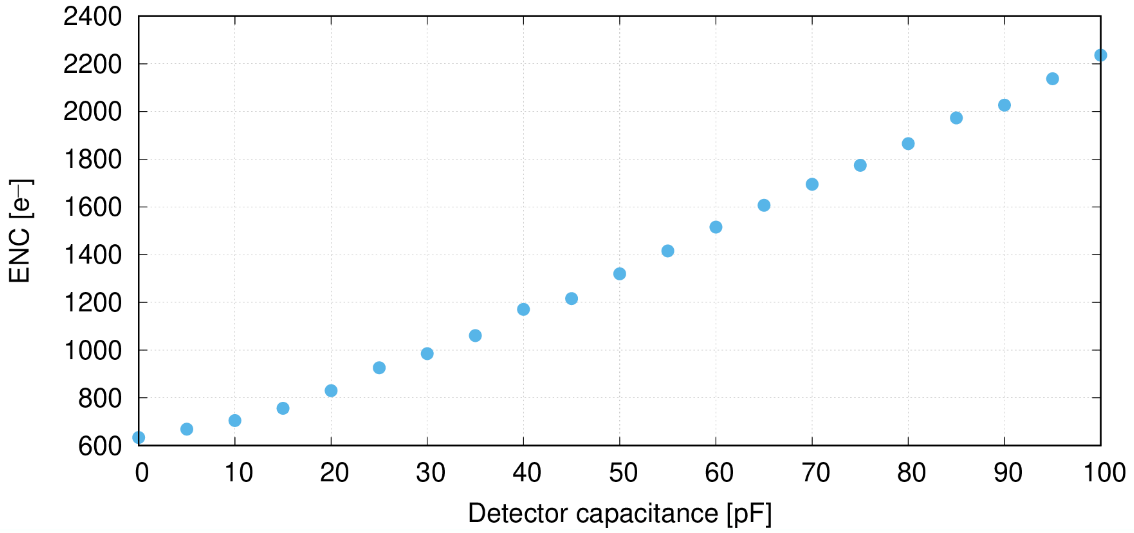
Linear response up to 5.5 pC

FLAME lab measurements
Analog output – noise performance

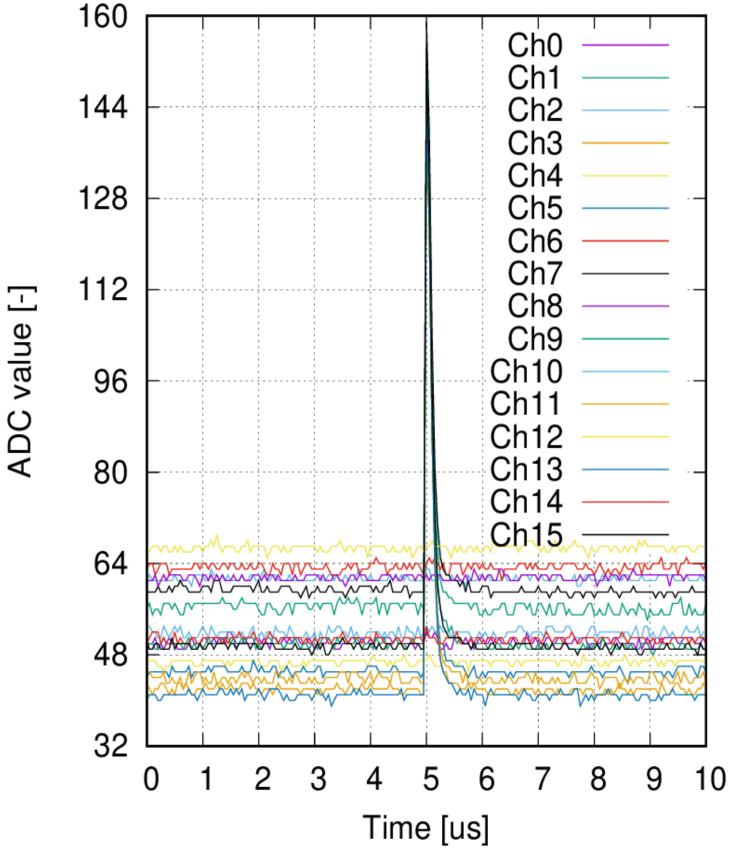
Noise in high gain mode:

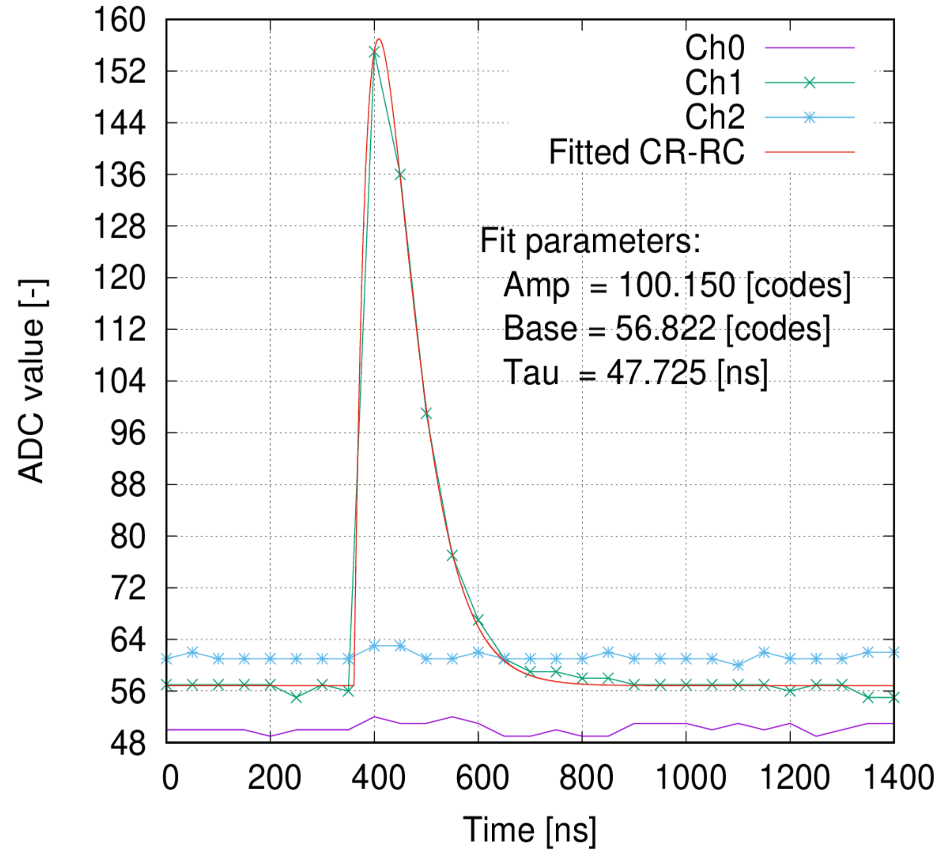
- ENC varies in range **600 – 1400 e$^-$** for expected detector capacitance range of **15 – 50 pF**
- This corresponds to SNR for MIP in range 40 – 20





FLAME lab measurements
Full chain - signal

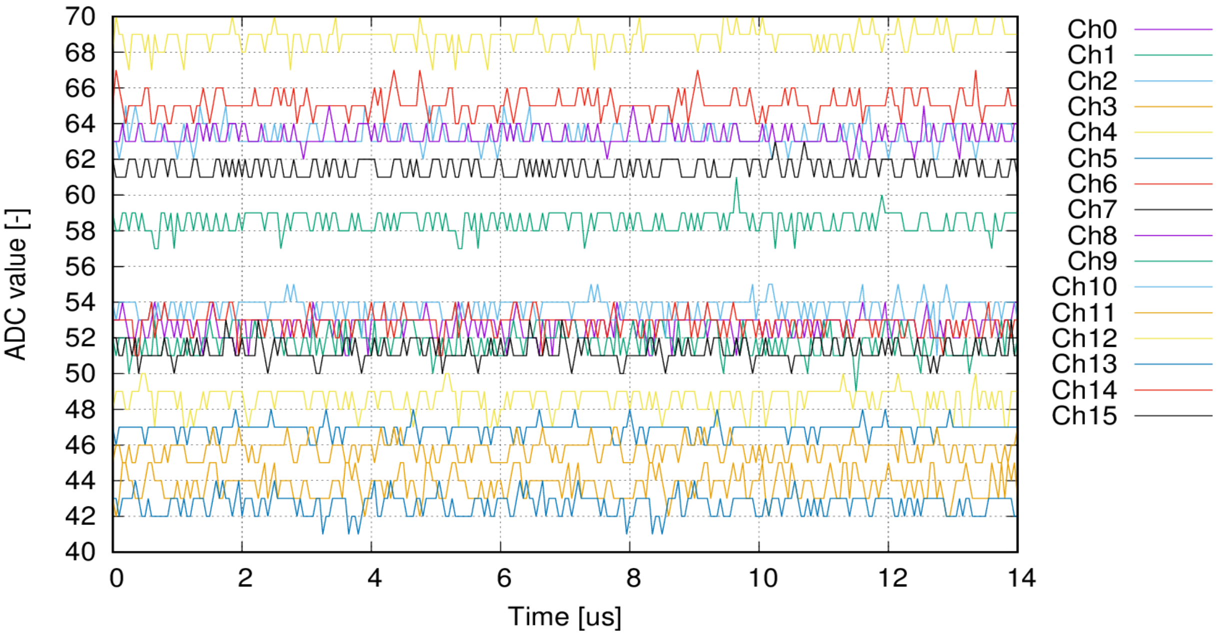




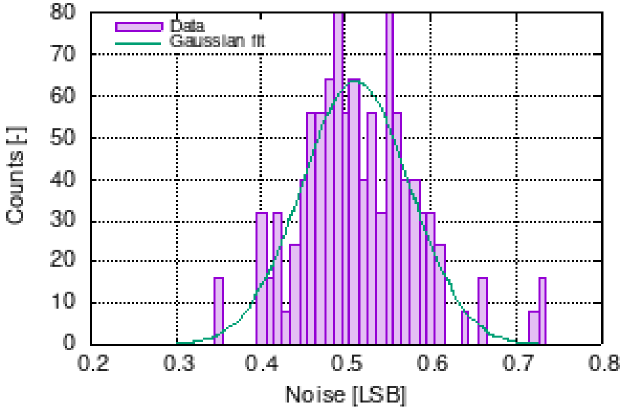
All basic functionalities (comprising fast data transmission) were verified
Very good pulse shape was measured, matching with CR-RC shaping

FLAME lab measurements
Full chain - raw noise – no sensor

Noise in time



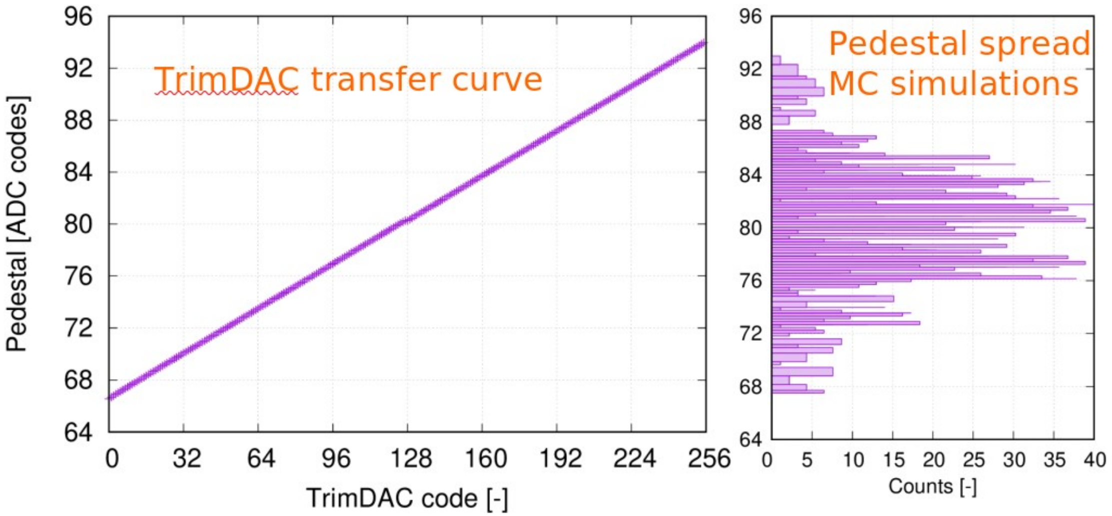
Noise RMS



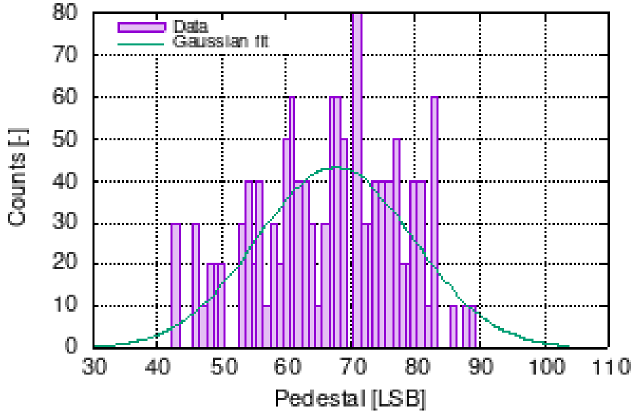
- Significant baseline spread between channels
- Noise RMS ~0.5 LSB

FLAME lab measurements
Pedestal spread – measurement vs simulation

Simulations



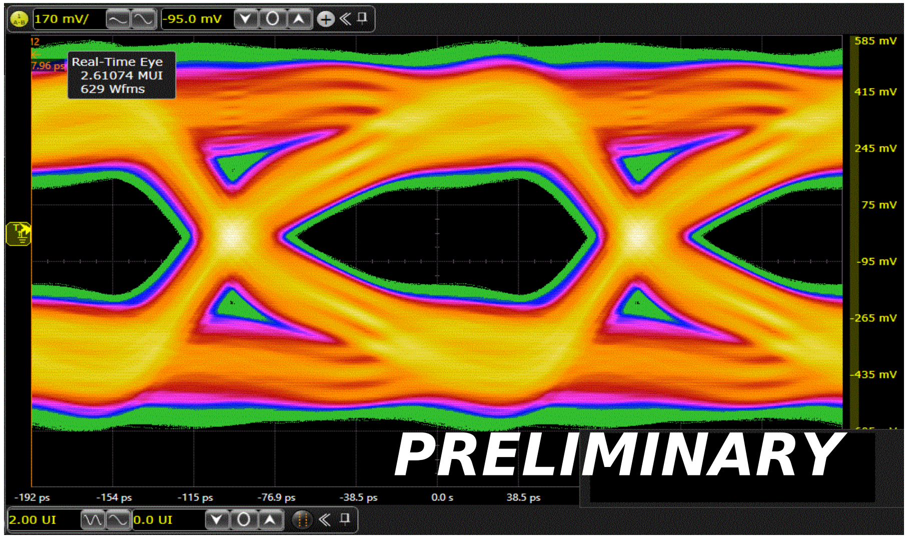
Measured pedestal spread



Pedestal spread from MC simulations does not match the measurements:

- MC: spread from **67** to **93** (26 LSBs),
  μ = 82.1 LSB and σ = 5.45 LSB
- Measurements: spread from **43** up to **101** (58 LSBs),
  μ = 67.7 LSB and σ = 12.1 LSB
- TrimDAC range not sufficient – for the next submision the range was increased

FLAME lab measurements Serialiser&Transmitter



- Preliminary measurement of Eye diagram
- Measurement done by 13GHz active probe and 80GSa/s scope
- Improvements of the test setup ongoing to achieve precise results...

Because FLAME was needed in beam- tests, and due to limited human resources, the characterisation in the lab has not been completed
In fact, we are preparing now the test setup for precise measurements...

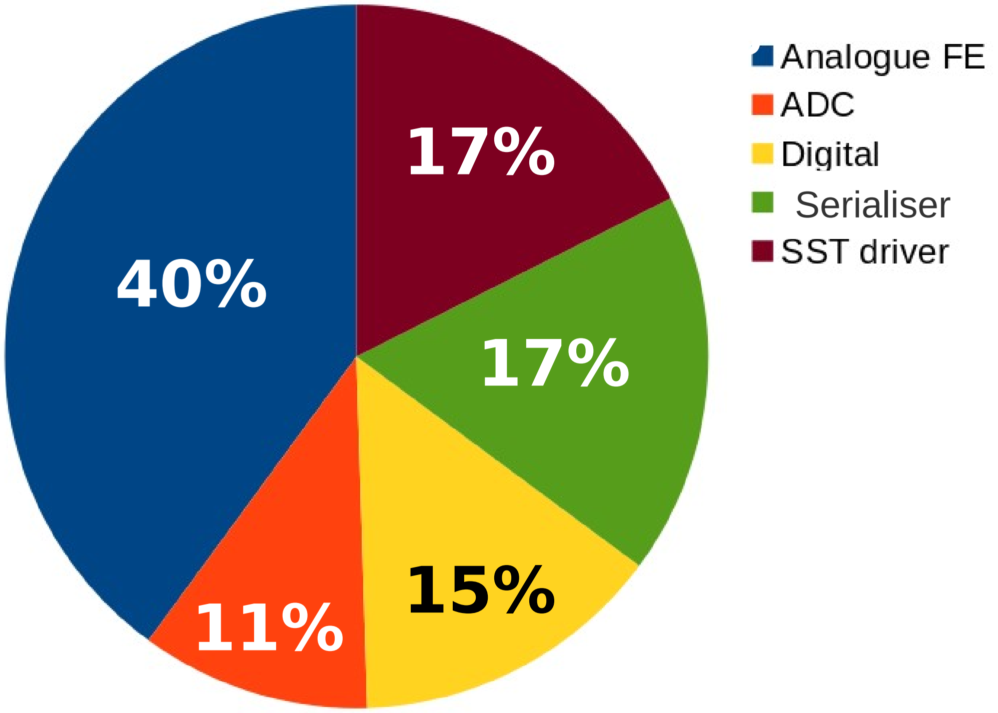
FLAME lab measurements
Power consumption

Average power consumption:
3.13 mW / channel

- Analogue FE : 1.25 mW/chn
- ADC : 0.33 mW/chn
- Digital : 0.45 mW/chn
- Serialiser : 0.55 mW/chn
- SST driver : 0.55 mW/chn

Total ASIC consumption

- Analogue FE : 40.0 mW
- ADC : 10.6 mW
- Digital : 14.4 mW
- Serialiser : 2x 8.8 mW
- SST driver : 2x 8.8 mW
- **Total : 100 mW**



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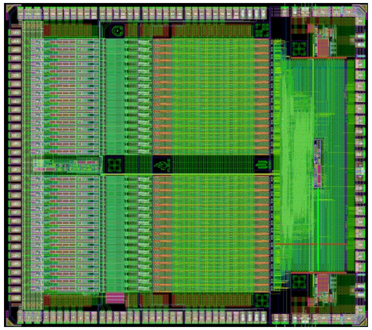
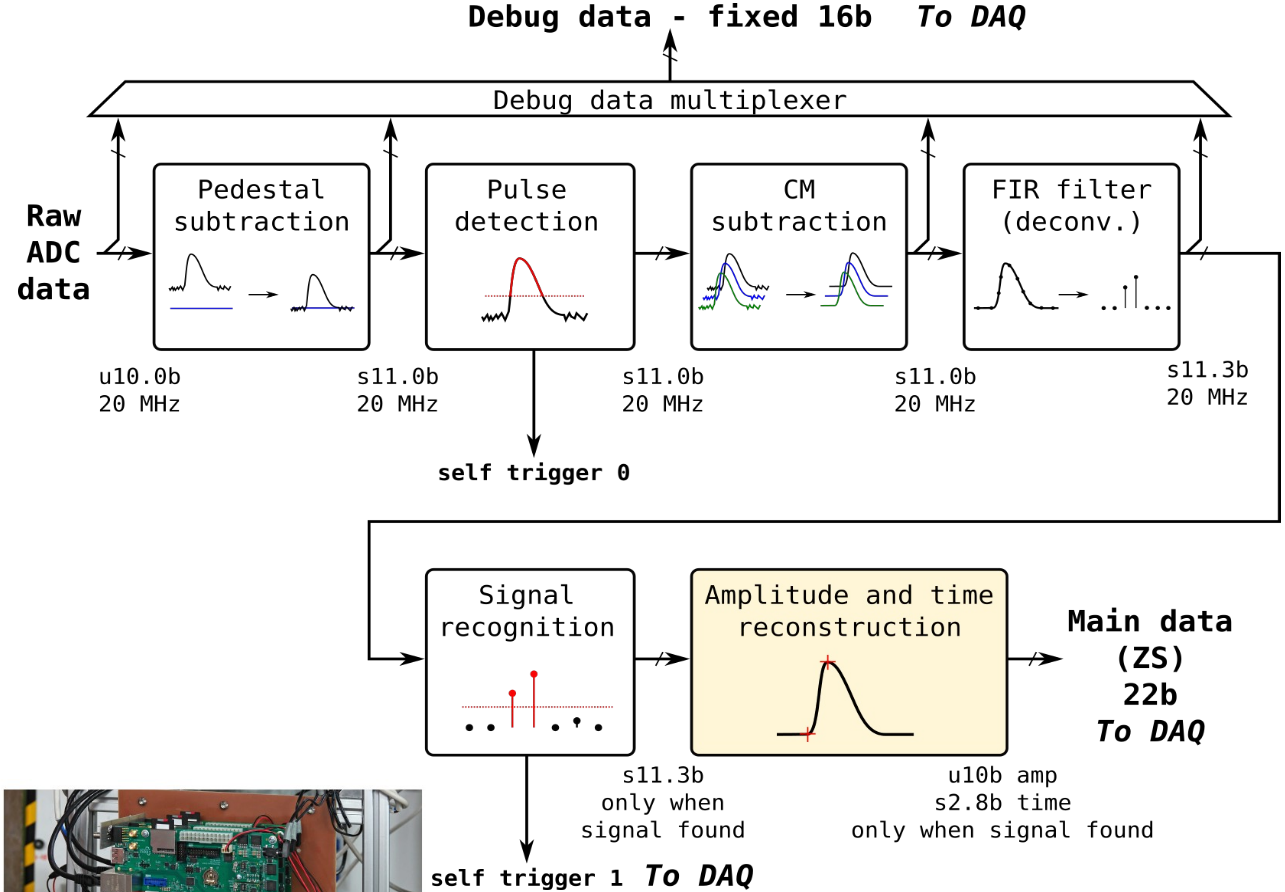
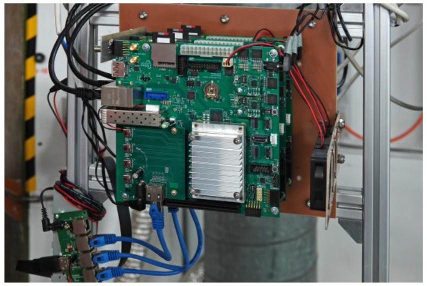
FLAME on testbeams
FPGA-based FLAME Readout



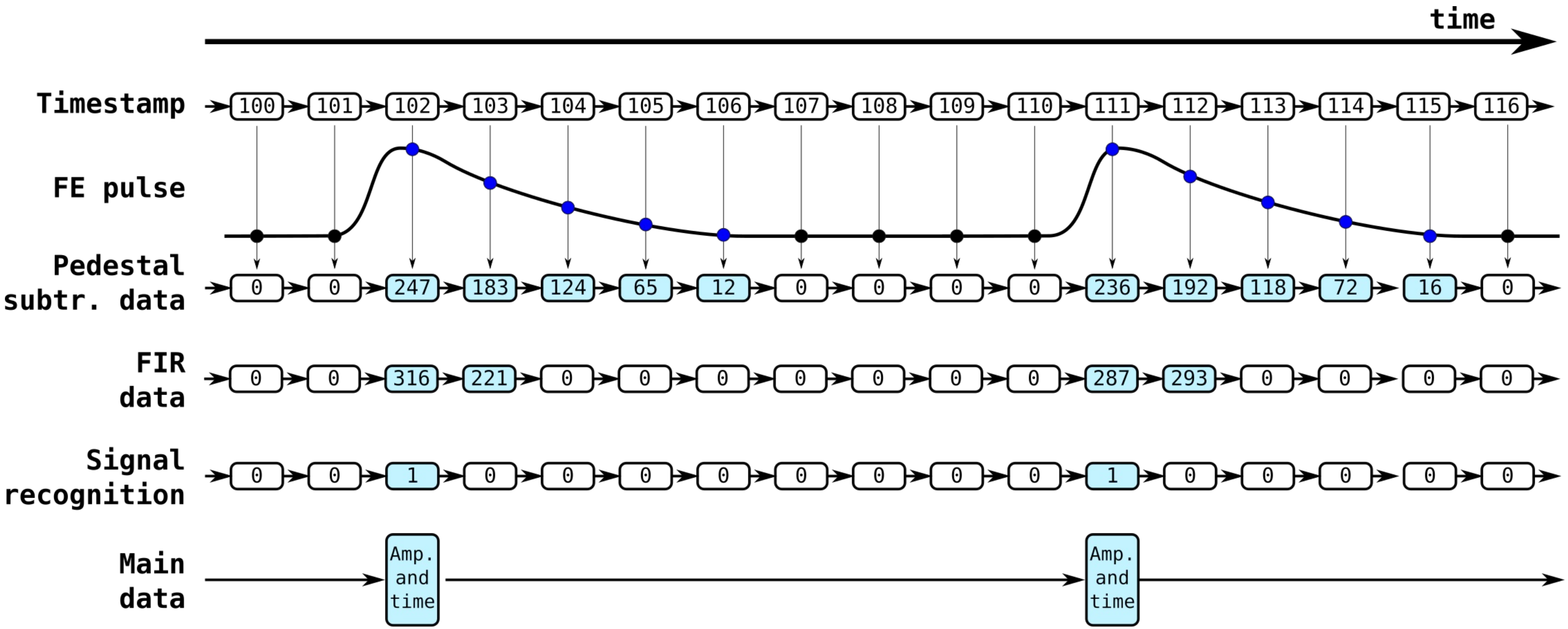
FLAME serialisers send data to GTH transceivers of Zynq UltraScale FPGA for online processing





Reconstructed amplitude (10-bit) and time of arrival information of detected pulses are sent to DAQ system

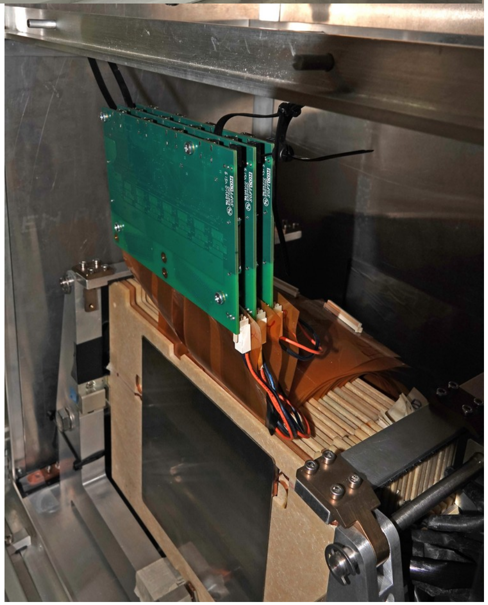
FPGA-based FLAME Readout
DSP online processing

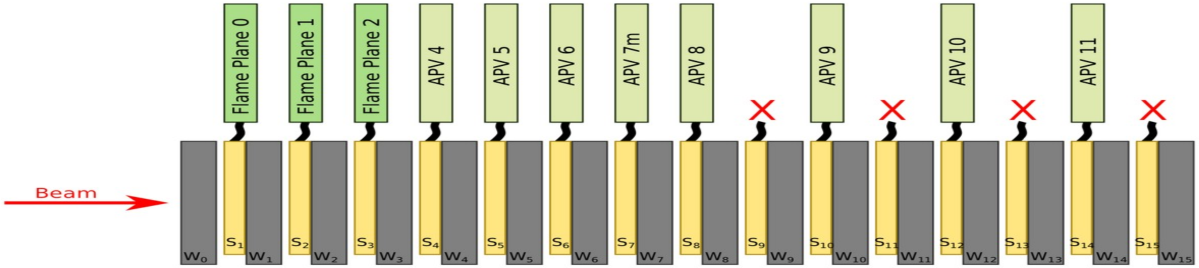


FLAME can work asynchronously to the beam, and such scheme is used in FCAL test-beams. By default deconvolution DSP is applied to data. Raw data with ADC values can also be taken.

FLAME in testbeam 2020
Test-beam Setup

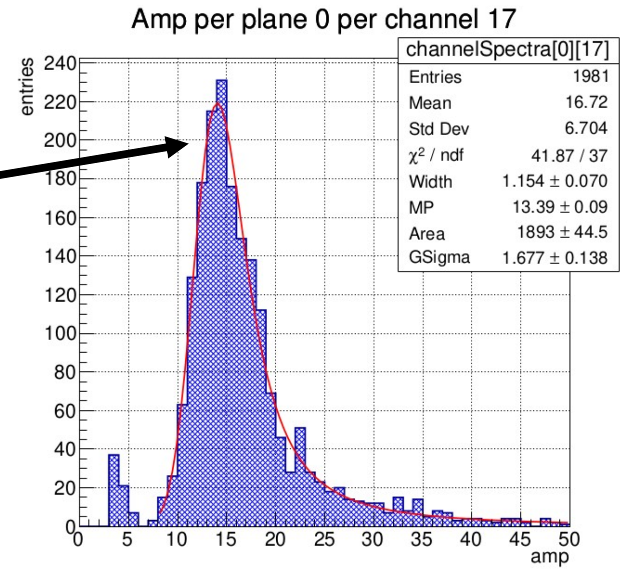
- Two weeks campaign on March 2020 at DESY
- Setup built of 16 Tungsten plates and silicon sensors
- Available readout:
  - 3 readout boards with FLAME chip
    First test-beam with FLAME readout !
  - 8 SRS readout boards with APV25 chip
- 5 ALPIDE planes for tracking
- Data acquired for:
  - different beam energies (1-5 GeV)
  - impact position scans
  - different incident angles
  - different readout board configuration (position in the stack)

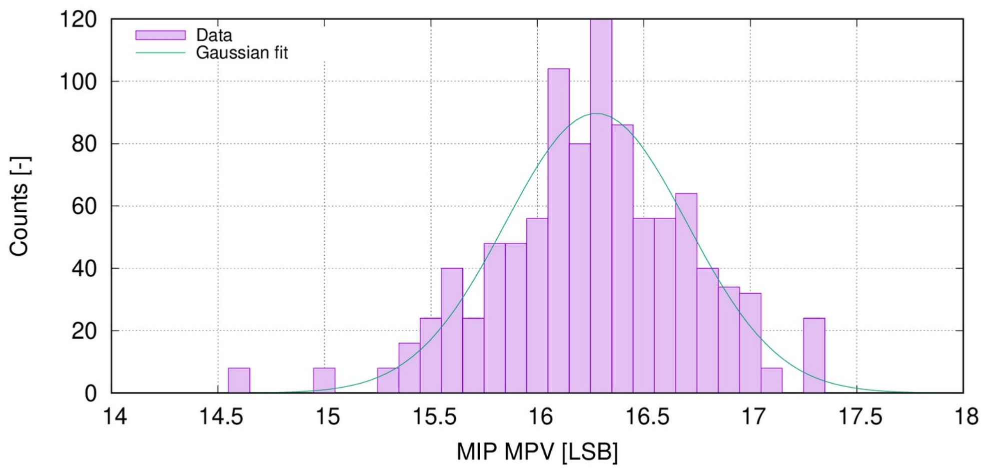




FLAME in testbeam 2020
Deconvoluted signal with 320um Si sensor
Gain calibration

Channels calibration obtained from the MIP depositions in 320 µm thick Si sensor (4 fC) using Landau–Gaussian convolution fit

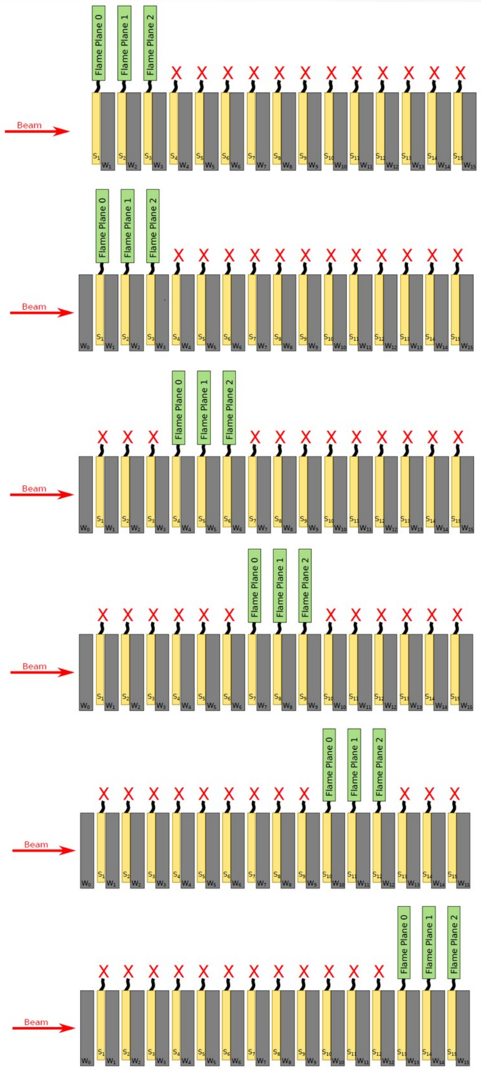




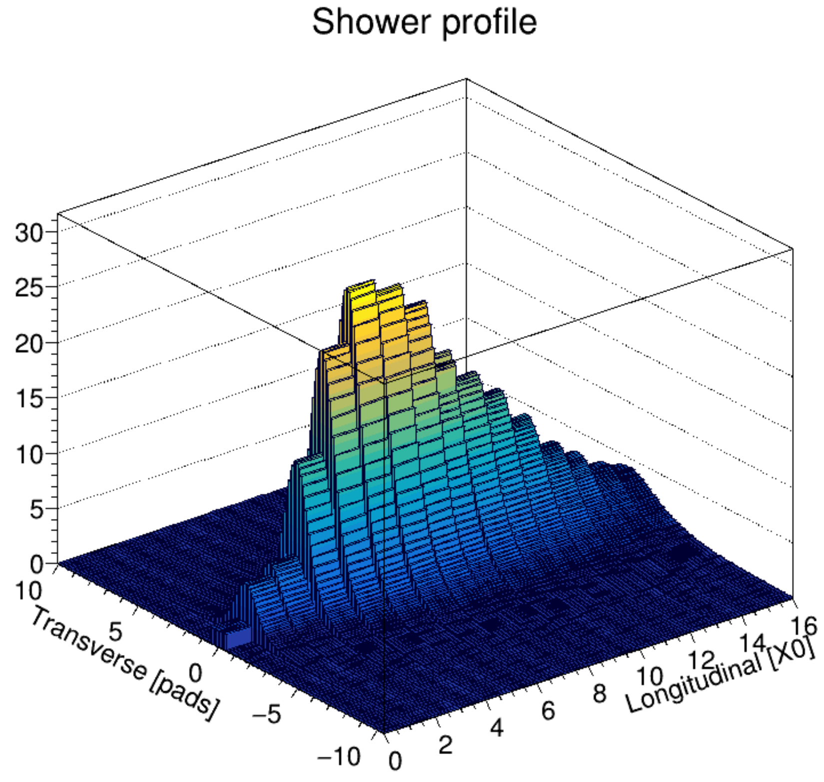
μ = 16.28 LSB → 4.07 LSB / fC
σ = 0.43 LSB

Gain = 4.01 LSB/fC from analogue pulse fit measurements

FLAME in testbeam 2020
Readout configurations – shower measuremen

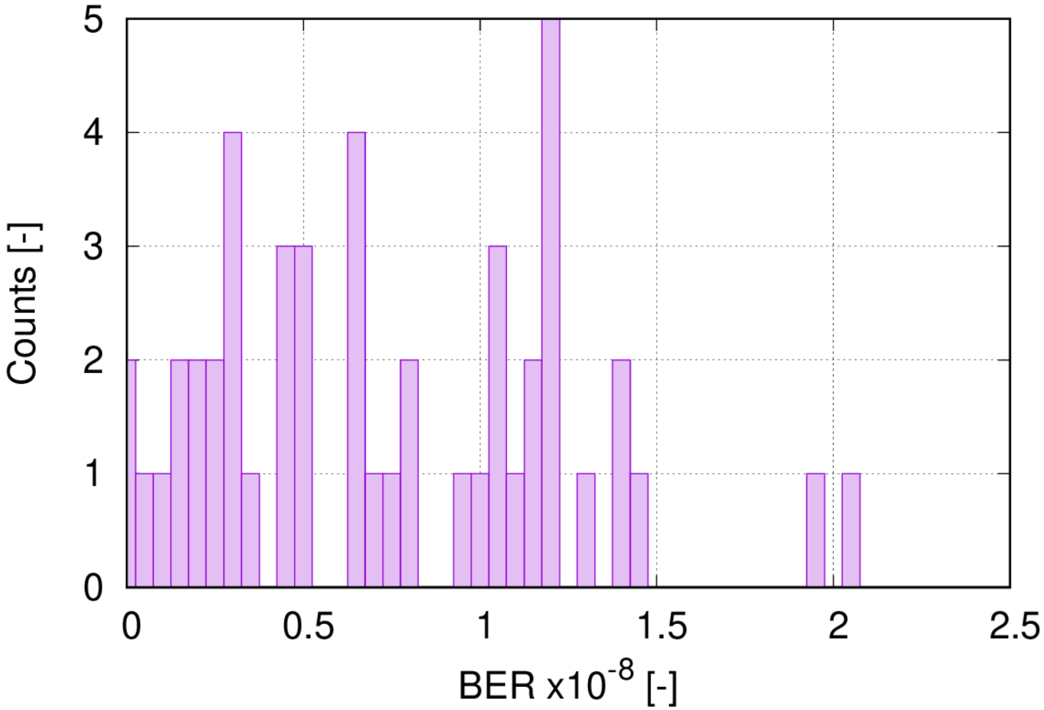


- To study the shower development in the entire calorimeter stack with 3 FLAME boards, the boards were successively connected to the next sensor layers
- Shower development reconstruction in the whole stack was done offline by merging data from different configurations



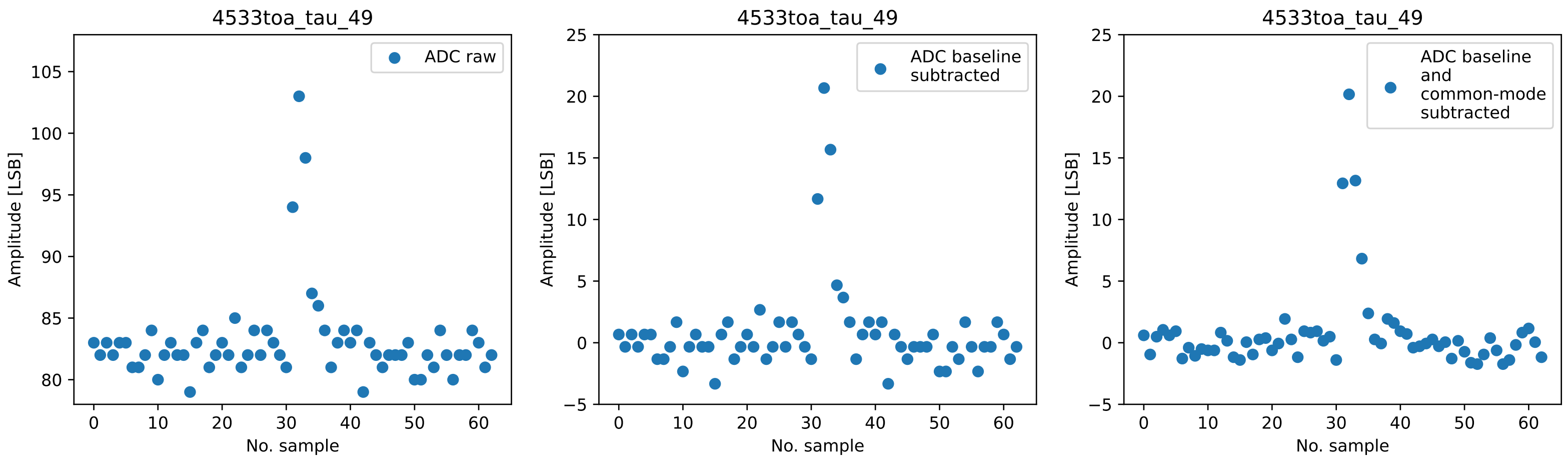
FLAME in testbeam 2022
High speed link performance

- BER is estimated by number of flipped bits detected by 8/10b decoder to total number of bits
- Average BER = **7.64 x10^{-9}**



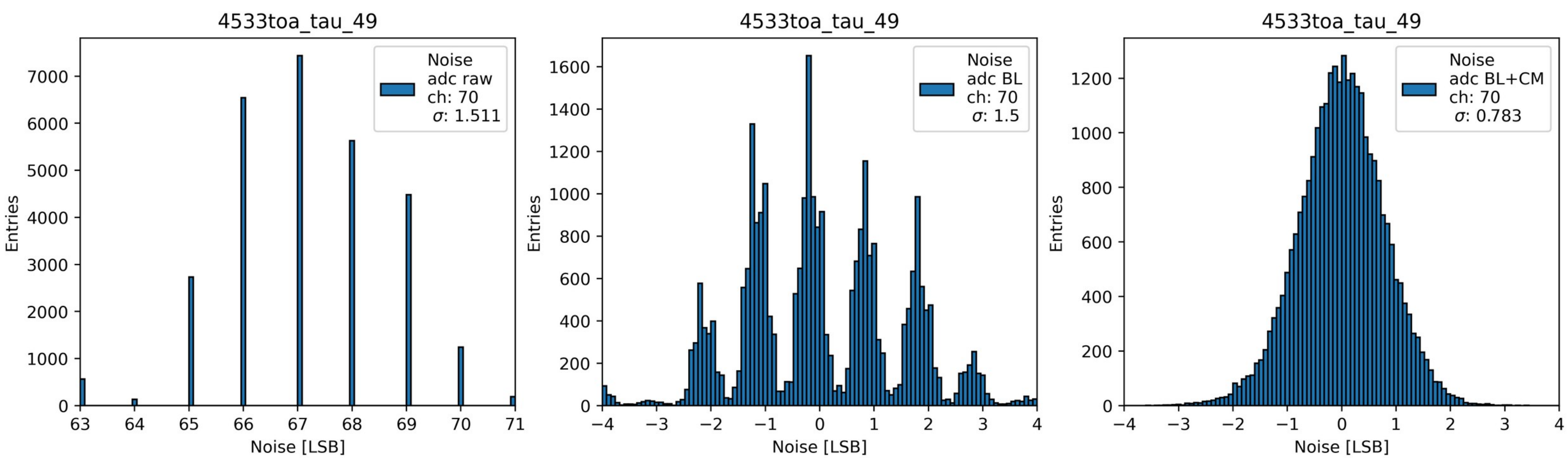
FLAME in testbeam 2022
Signal and Noise with 500um Calice Si sensor

Signal



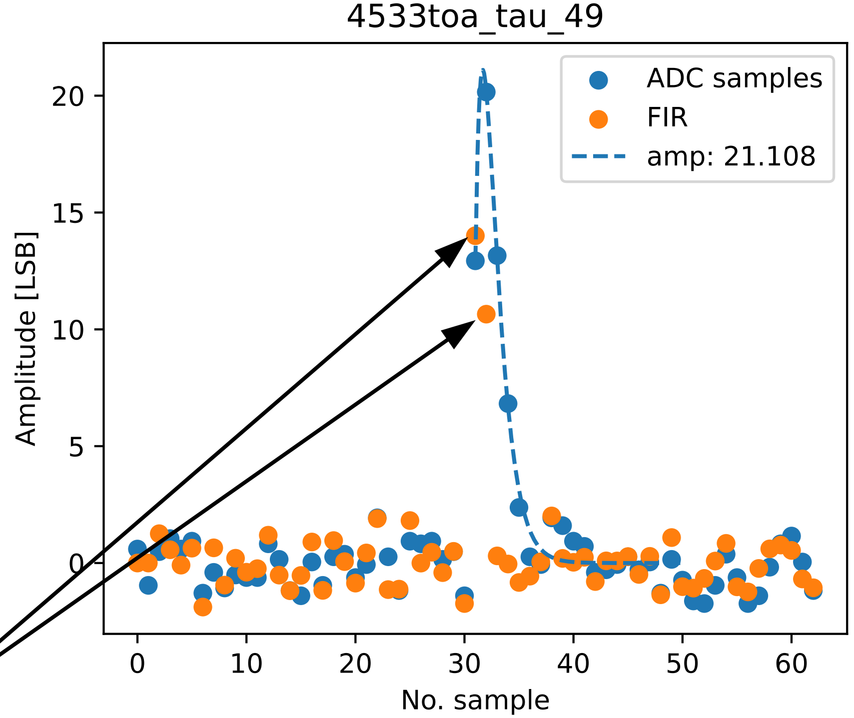
Raw data | Baseline subtracted | Baseline&CM subtracted

Noise



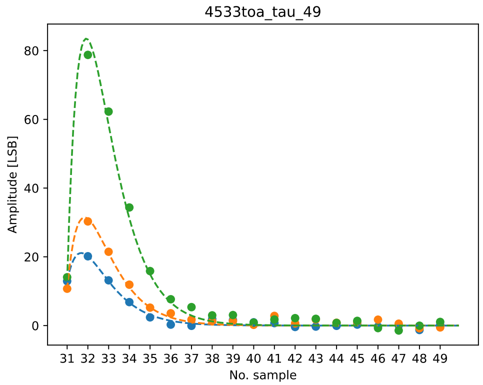
FLAME in testbeam 2022
Signal with 500um Calice Si sensor
Fitting raw ADC values vs deconvolution

Comparison of results obtained fitting ADC samples and from deconvolution in progress...



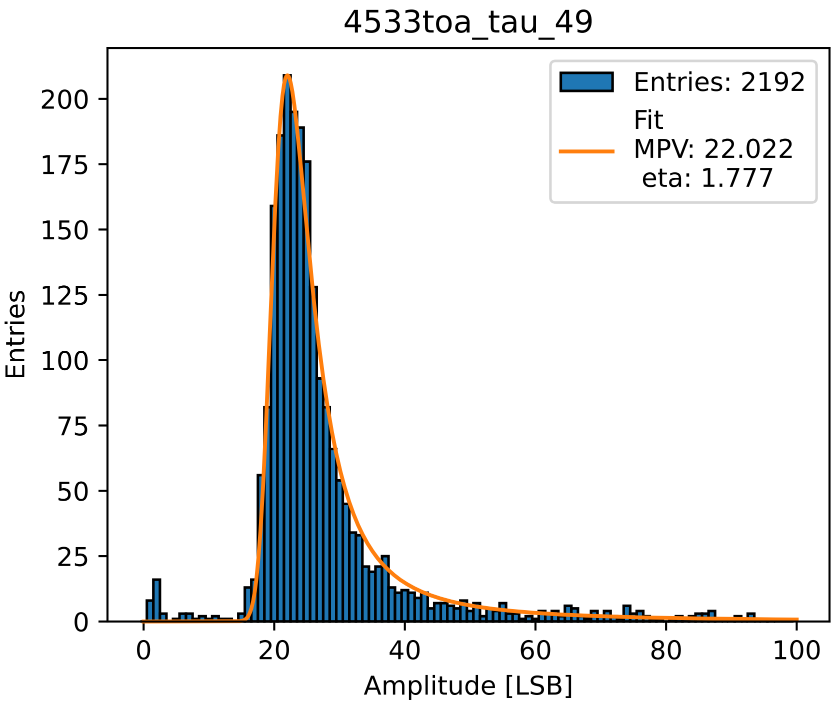
To get amplitude and time from 2 non-zero FIR samples (orange) deconvolution formulas are applied

Few more fitting examples

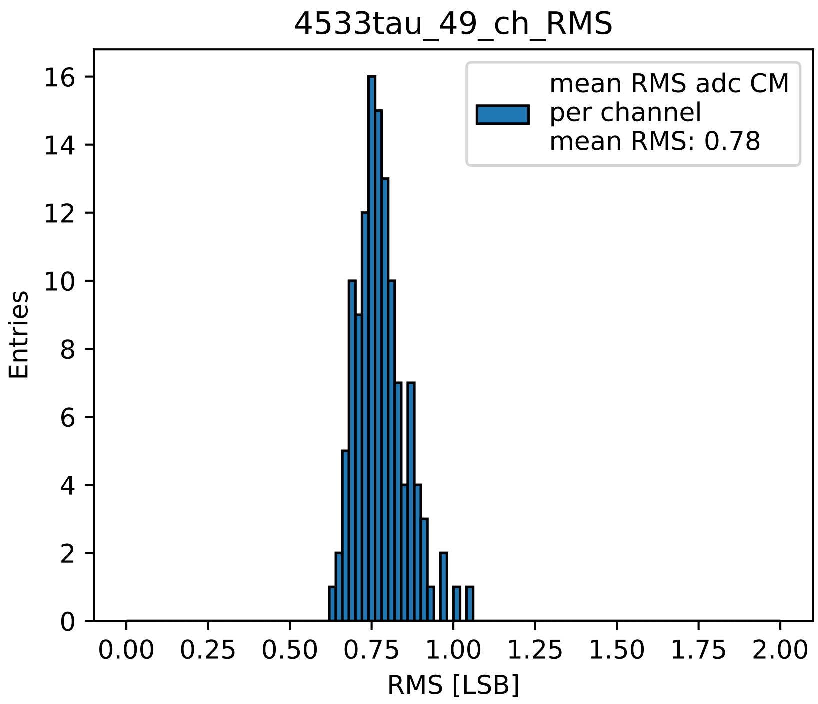


FLAME in testbeam 2022
Signal and Noise with 500um Calice Si sensor
Raw ADC values

Signal (MIP from Landau–Gaussian fit)



Noise



MIP = 22.022 LSB

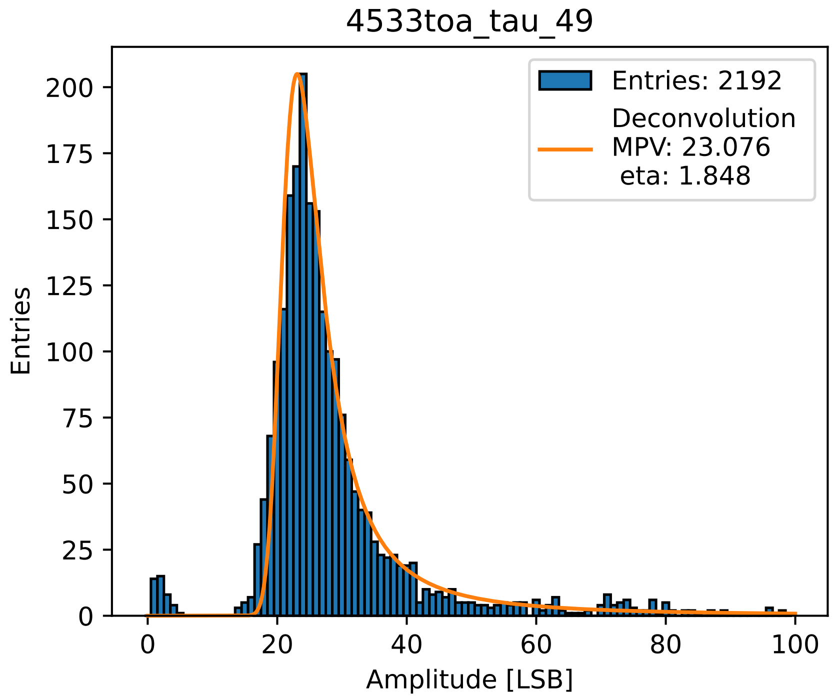
RMS = 0.78 LSB

SNR= 28.2

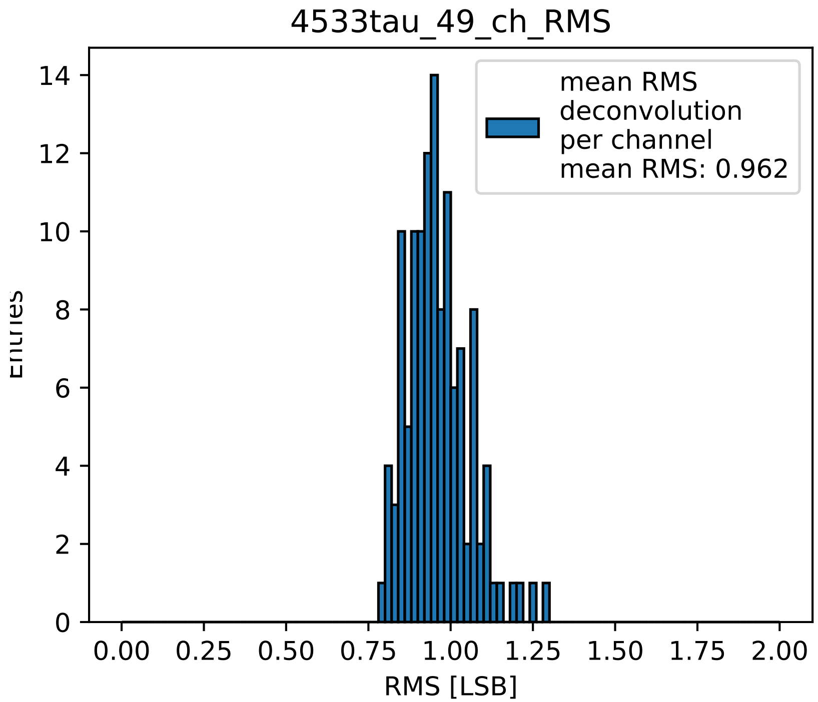
ENC~1400 el.

FLAME in testbeam 2022
Signal and Noise with 500um Calice Si sensor
Deconvolution

Signal (MIP from Landau–Gaussian fit)



Noise



MIP = 23.076 LSB

RMS = 0.96 LSB

SNR= 23.99

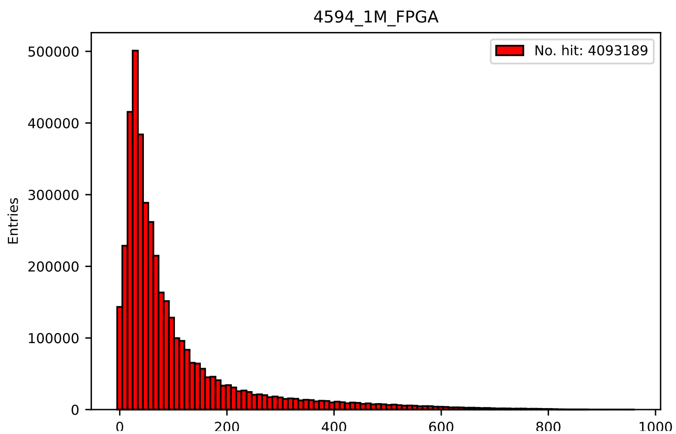
ENC~1700 el.

After deconvolution SNR is about 15% lower than from ADC fitting

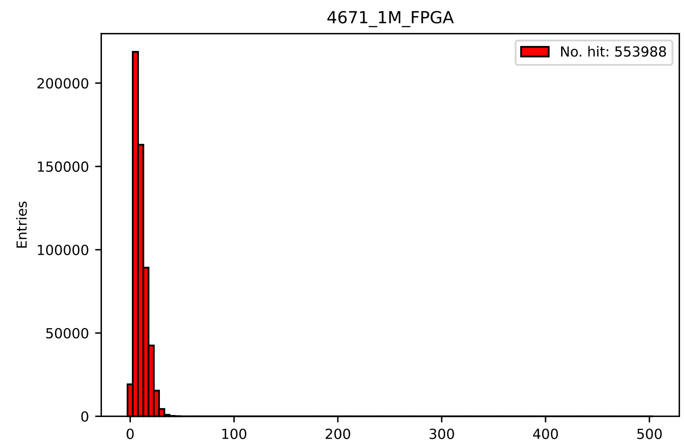
FLAME in testbeam 2022
Signals in shower peak (5 X0 tungsten)

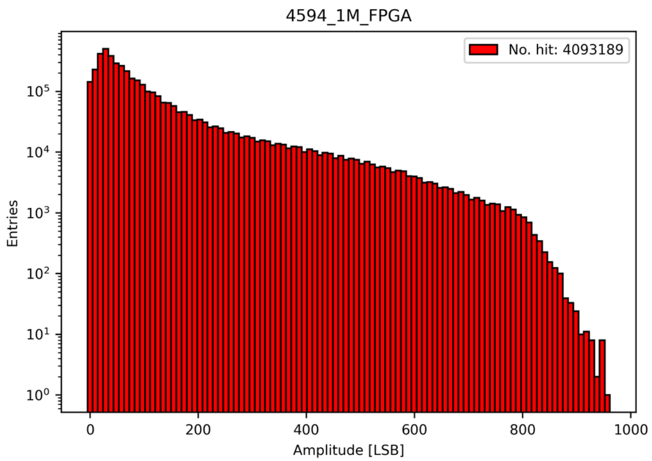
High gain

Low gain

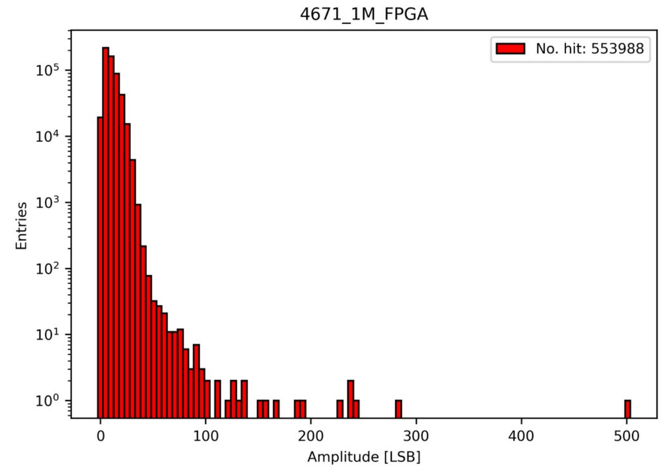


Linear Scale





Log scale

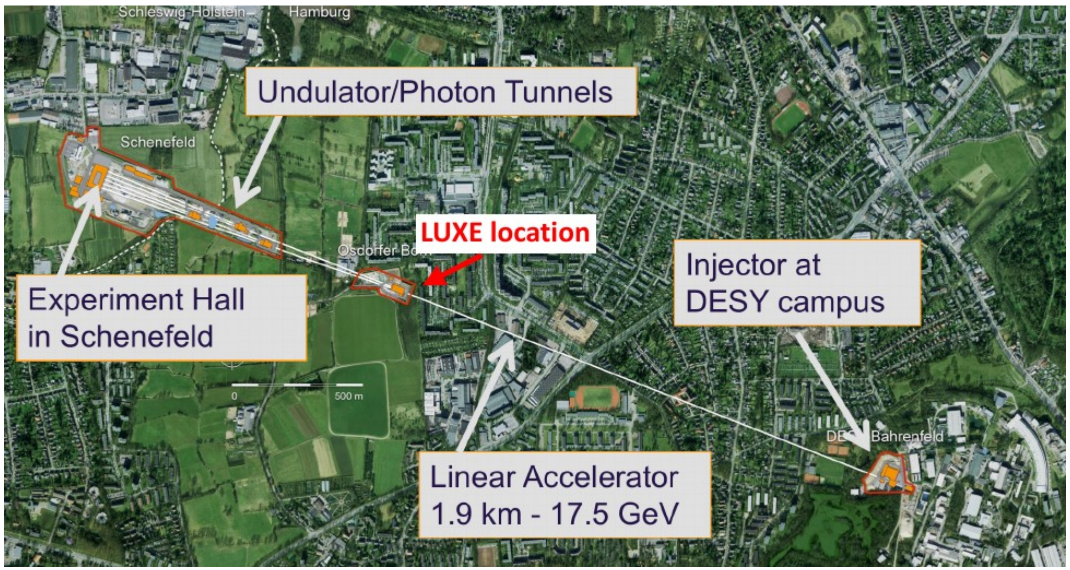


Outline

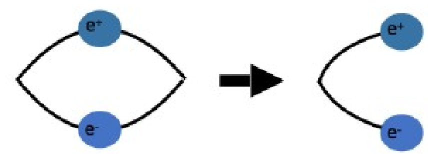
- Motivation
- FLAME design
- FLAME lab measurements
- FLAME on testbeams
- **FLAXE ASIC for LUXE experiment**
- To do / New developments and Plans

FLAXE ASIC for LUXE experiment
Motivation

LUXE experiment at the European XFEL



LUXE will study non-perturbative and non-linear QED phenomena in the strong-field regime



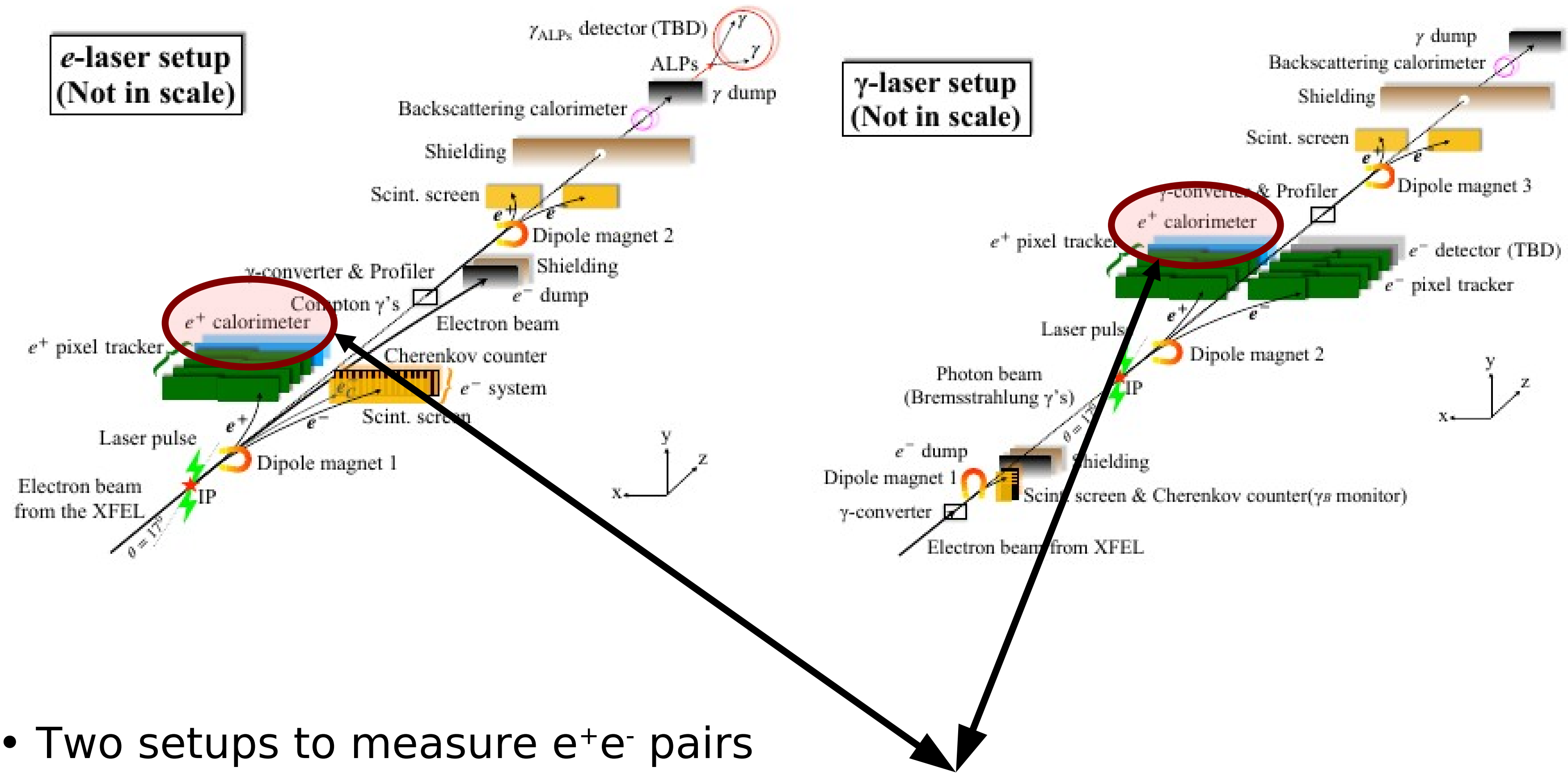
$E_{\text{field}} < 2m_e$ $\quad$ $E_{\text{field}} > 2m_e$

$$E_{field} = \frac{\varepsilon}{m_e}$$

$$\varepsilon_{crit} = \frac{m_e^2 c^3}{\hbar e} \simeq 1.3 \cdot 10^{18}\ \mathrm{V/m}$$

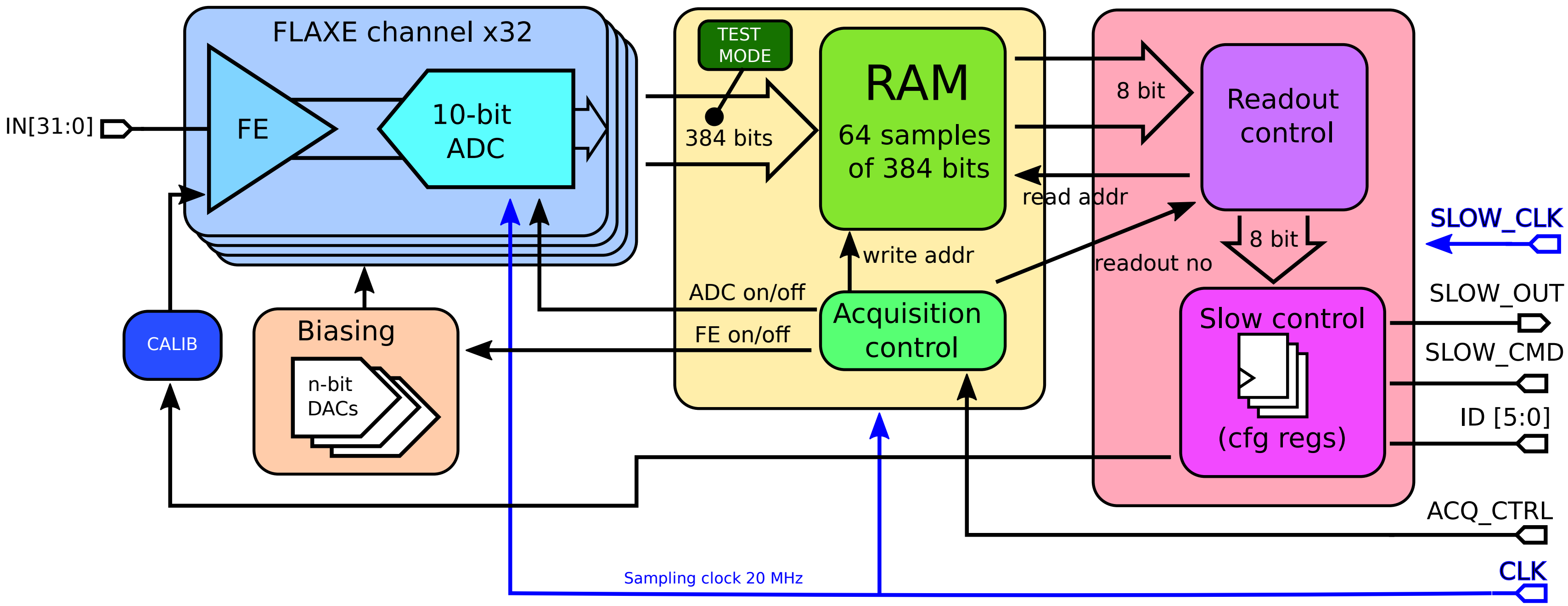
Vacuum boils if the field is large enough to create real e^+e^- pairs (above Schwinger-Limit)

FLAXE ASIC for LUXE experiment
LUXE setups



- Two setups to measure e^+e^- pairs
- ECALp will be build based on compact LumiCal developed by FCAL
- ECALp will use FLAXE readout

FLAXE ASIC for LUXE experiment
FLAXE architecture



- FLAXE is a modified 32-channel FLAME in CMOS 130nm without high speed serialisers&transmitters – readout rate in LUXE ~10 Hz
- About 1000 FLAXE chips is just being produced...

Outline

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FLAME & FLAXE
To do...

- Precise lab measurements of FLAME parameters still needed
- Setup for accurate measurement of high speed link performance under preparation...
- Quantitative comparison ADCsamples+fitting vs deconvolution in progress...
- Precision of timing measurements, in particular using deconvolution, needs to be quantitatively understood, in progress...

FLAME & FLAXE
New developments and Plans

FLAME is still an R&D project and we would like to improve some features in the future:

- ADC with internal threshold – we think about adding internal threshold in the ADC design, in order to stop the conversion (save power) in case of no hit, in progress...
- 12-bit ADC - for calorimetry 10-bit resolution is rather low. We have already designed and fabricated 12-bit ADC prototype, which is waiting for tests since long time...
- Few years ago we have started collaboration with Omega group (Christophe de la Taille, Damien Thienpont,...) on HGCROC chip for HGCAL in CMS. This collaboration continues and may affect future plans...

Thank you for attention

Back-up