The cryogenic ALCOR ASIC for SiPM readout

XII Front-End Electronics Workshop, June 12-16, 2023, Torino

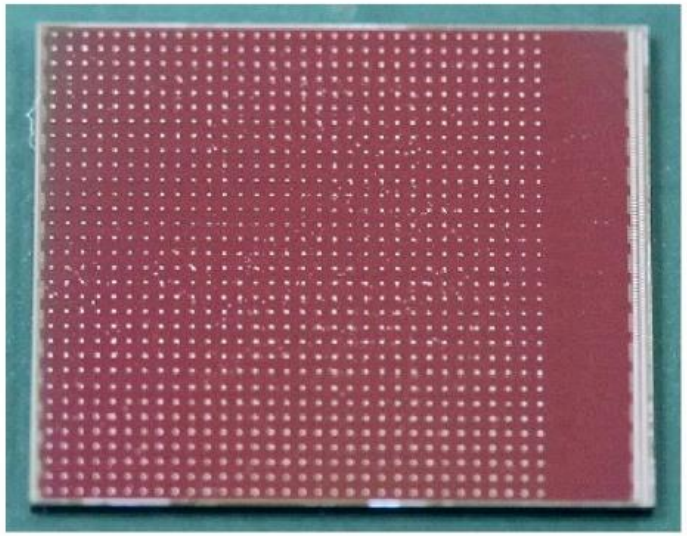
Giulio Dellacasa giulio.dellacasa@to.infn.it

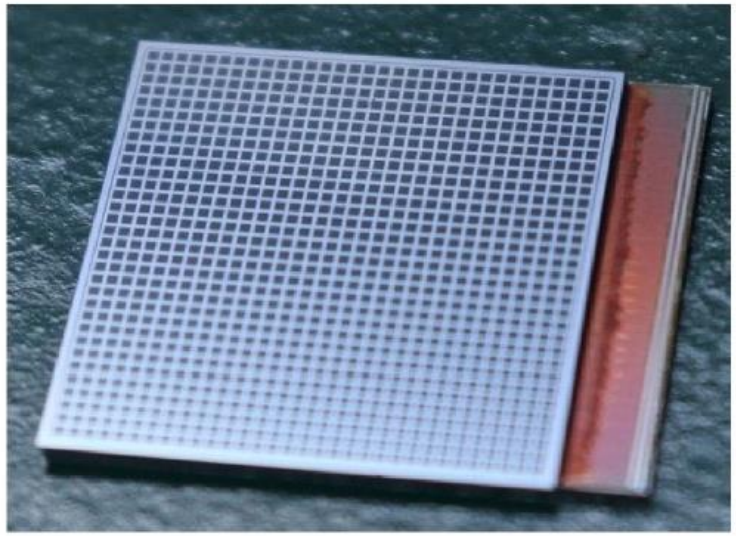
The ALCOR group:
INFN Torino: F. Cossio, M. Da Rocha Rolo, G. Dellacasa, M. Mignone, A. Rivetti, R. Wheadon
INFN Bologna: P. Antonioli, D. Falchieri, R. Preghenella, N. Tosi, L. Rignanese, N. Rubini,

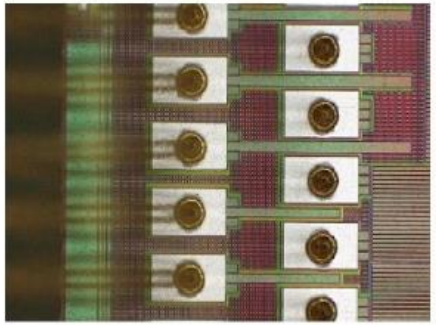
ALCOR

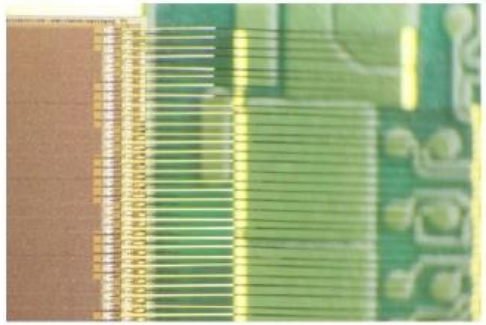
- A Low-power Circuit for Optical Readout
- 32 channels pixel style matrix mixed-signal ASIC for SiPM readout (towards the implementation of a 3D SiPM readout)
- CMOS 110 nm technology (UMC)
- Developed by INFN (CSN2) for the readout of SiPM at 77K, in the framework of Darkside
- The chip performs signal amplification, conditioning and event digitization
- Each pixel features:
  - Dual-polarity front-end amplifier with low input impedance (10-20 Ω) and 4 programmable gain settings
  - 2 leading edge discriminators for events selection
  - 4 TDCs based on analogue interpolation: time binning ≈ 25 or 50ps (programmable option, 320 MHz clock frequency)
- Single photon time tagging: Time-of-Arrival or Time-over-Threshold modes
- Fully digital output (4 LVDS TX data links)
  - Theoretical bandwidth limitation: 4 links up to 640 Mb/s
  - 640 / 40 bits / 8 pixels => 2 MHz/pixel (1 MHz TOT mode)
  - Now 500 kHz / pixel due to some limitations in the EoC readout
  - TX data links successfully tested up to 780 Mb/s (390 MHz clock frequency)

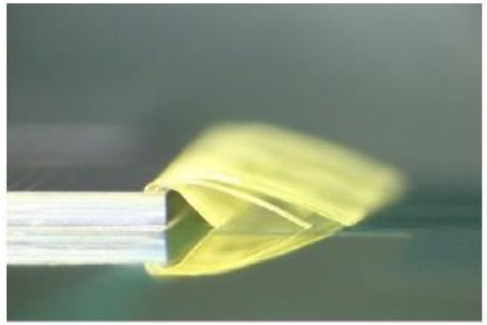
The pioneer: ASIC for industrial application







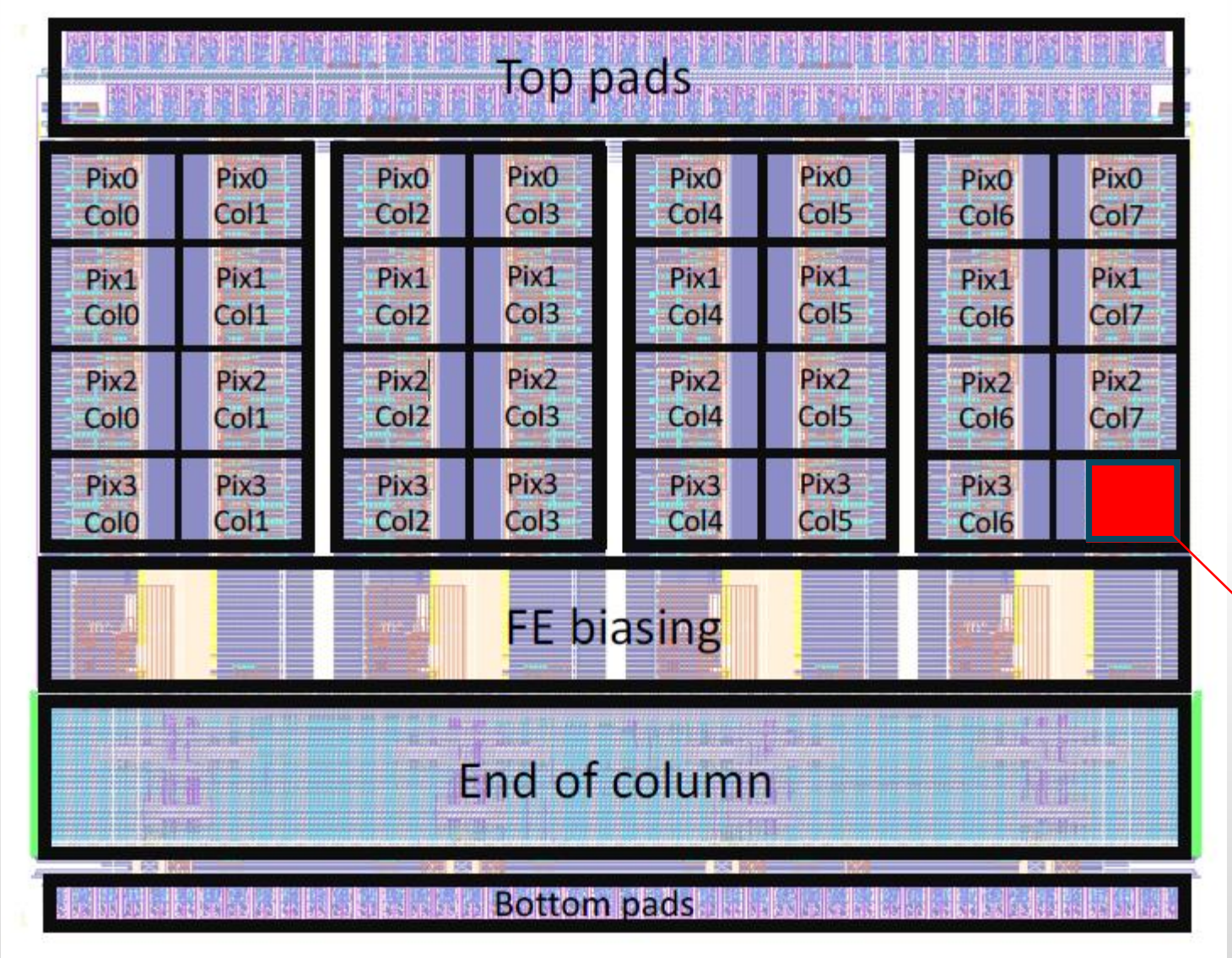




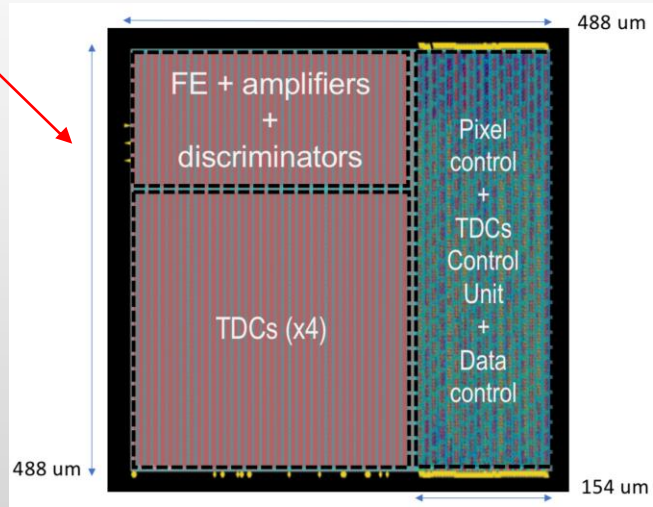
- 1024-pixel readout ASIC for fast timing application developed at INFN-TO
- CMOS 110 nm, pixel size 440 x 440 μm^2
- 32x32 matrix, appr. 250 mm^2
- Flip-chip mounted to a silicon detector
- Performs 30 ps r.m.s. time resolution up to 100 MHz / cm^2

From this project came up with the idea to realize a SiPM readout chip in a “pixel style” configuration to maintain channel scalability and the possibility to make a direct bump bonding with mini SiPM sensors in future releases

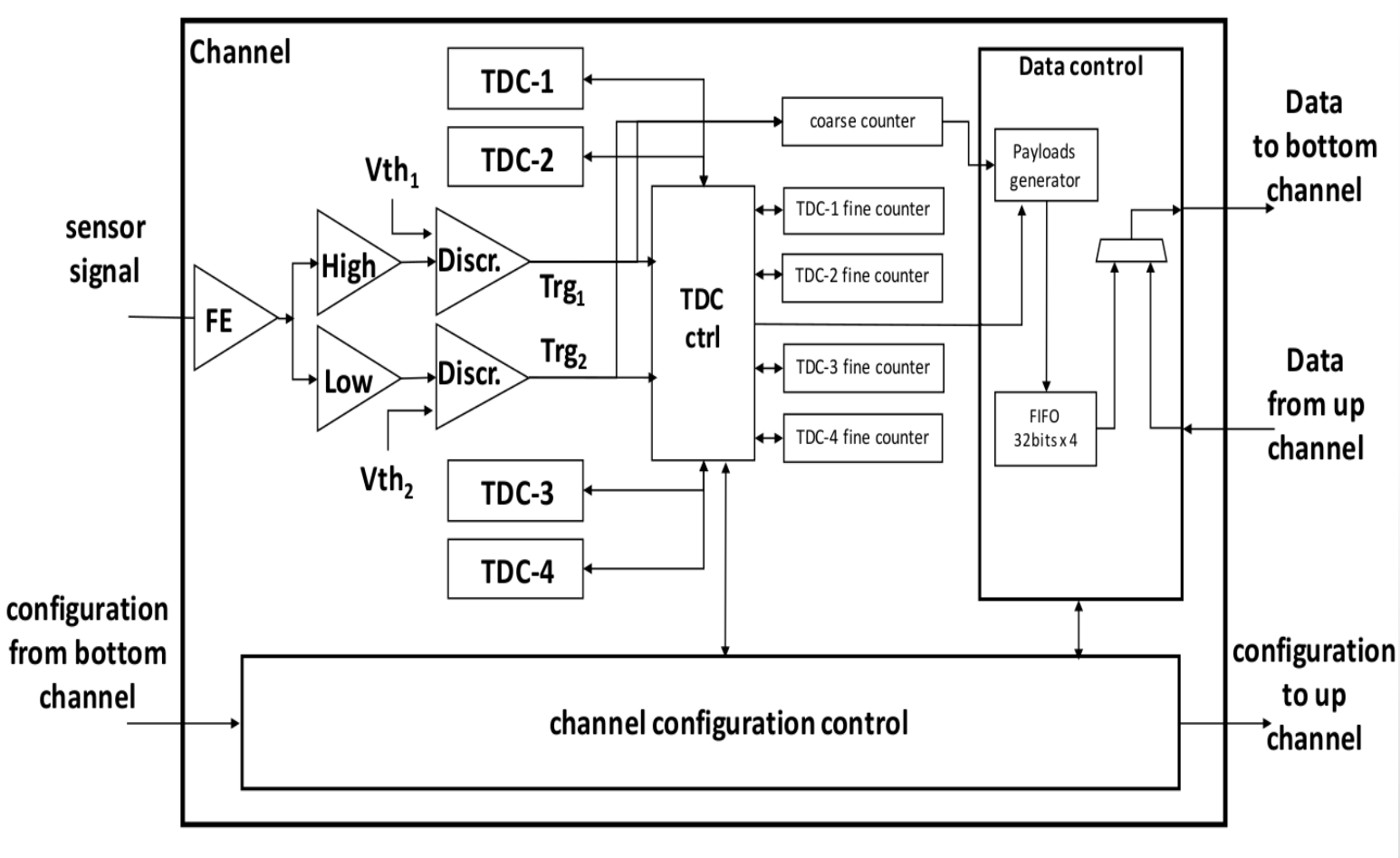
ALCOR layout and architecture



- 32 channels 4x8 pixels array
- pixel size 440 x 440 μm^2
- SiPM connection through wire bonding pads (top side)
- End of Column performs readout and SPI configuration
- 4 LVDS serializers (one every two columns) for data transmission
- Analogue I/O on the top side
- Digital I/O on the bottom side

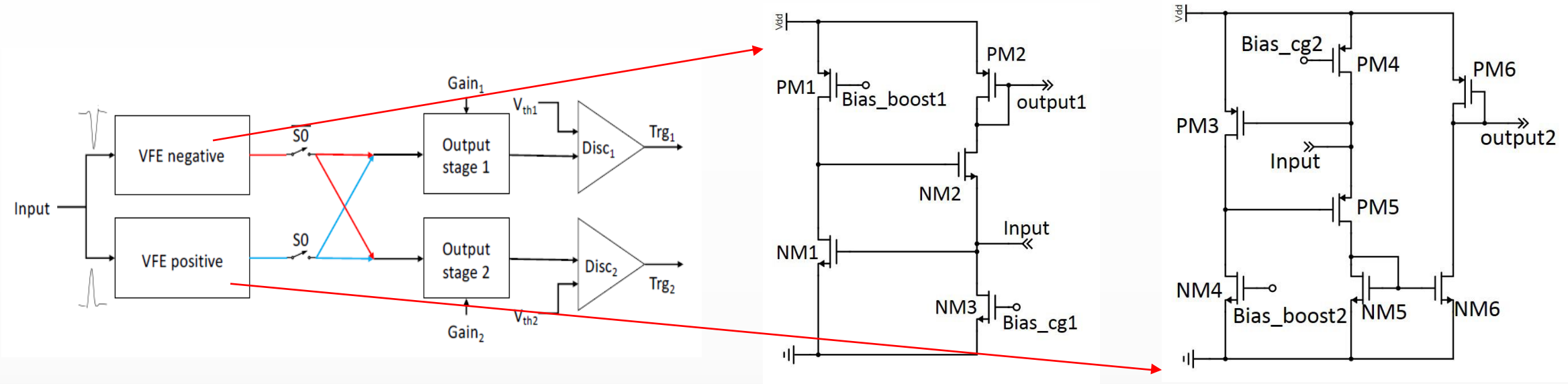


Channel diagram



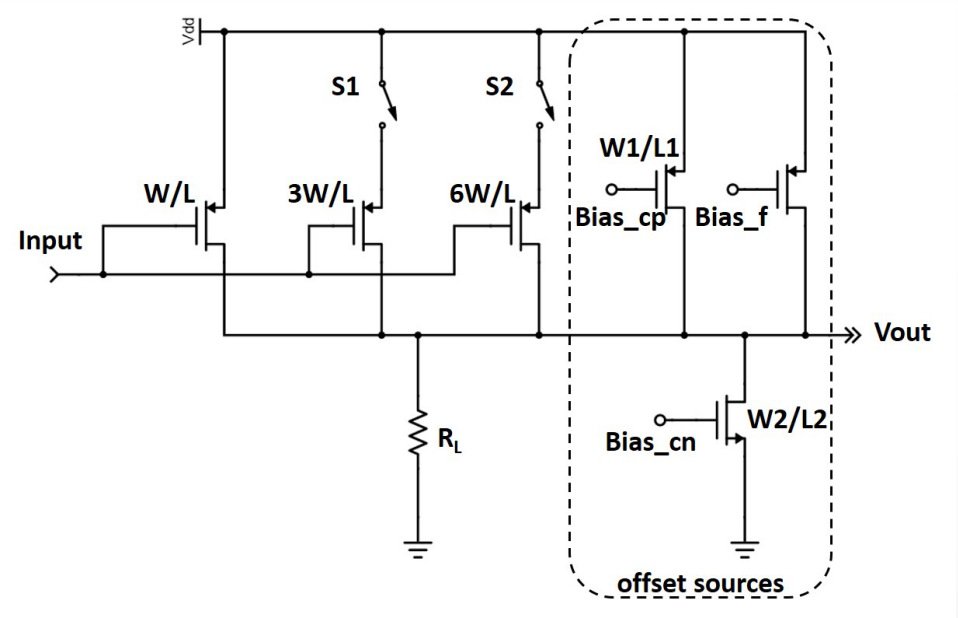
- **RCG**-based preamplifier
- High bandwidth (220 MHz down to 58 MHz with Cin 0 to 5 nF)
- Low input impedance (10-20 ohm)
- **dual-polarity** to readout either the anode or cathode signal
- 2 independent TIA branches
- **4 gain** settings
- followed by **LE discriminator** with independent threshold (6-bit DAC)
- **Time measurement** from 4 **TDCs** based on analogue interpolation
- **Pixel** control **logic** handles TDCs operation, pixel configuration and data transmission

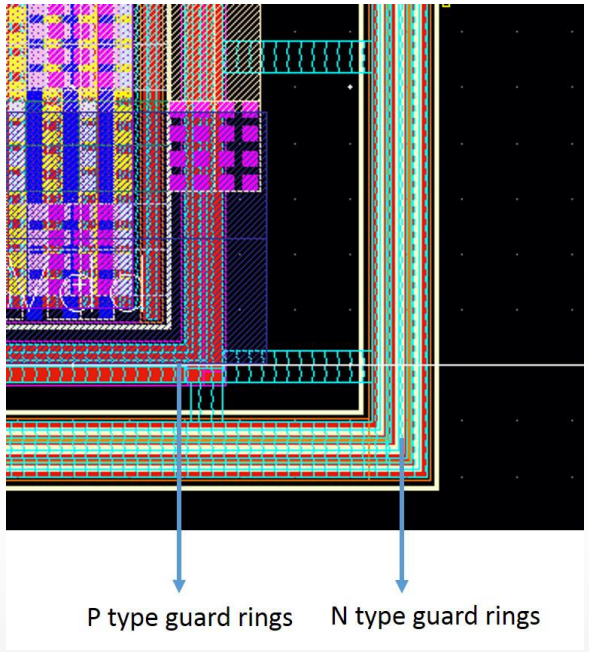
Very Front End



- RCGs both for anode or cathode signal readout (selectable)
- Programmable bias currents by 5-bit DAC
- Programmable Vth between 550 – 878 mV

Very Front End

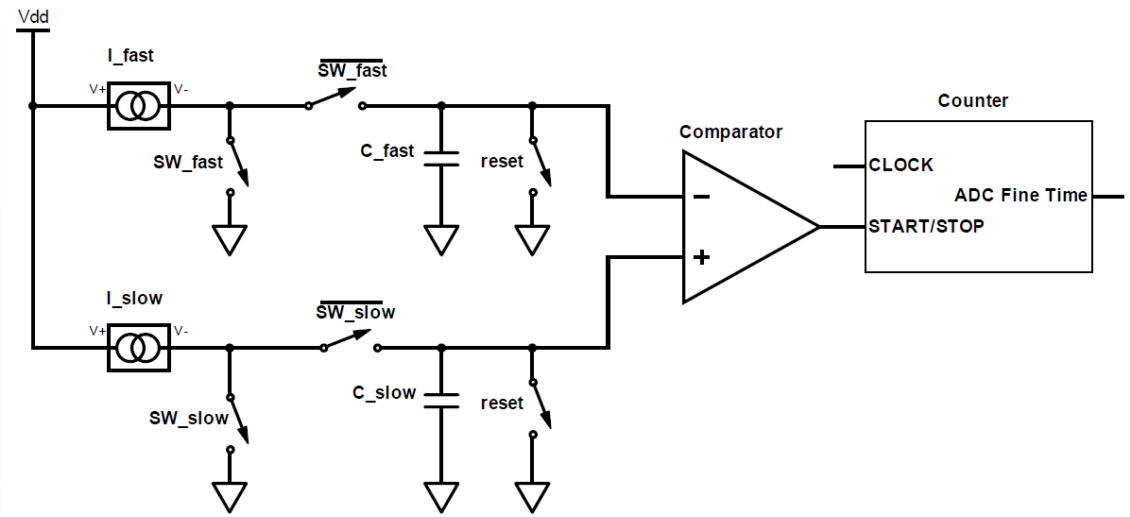


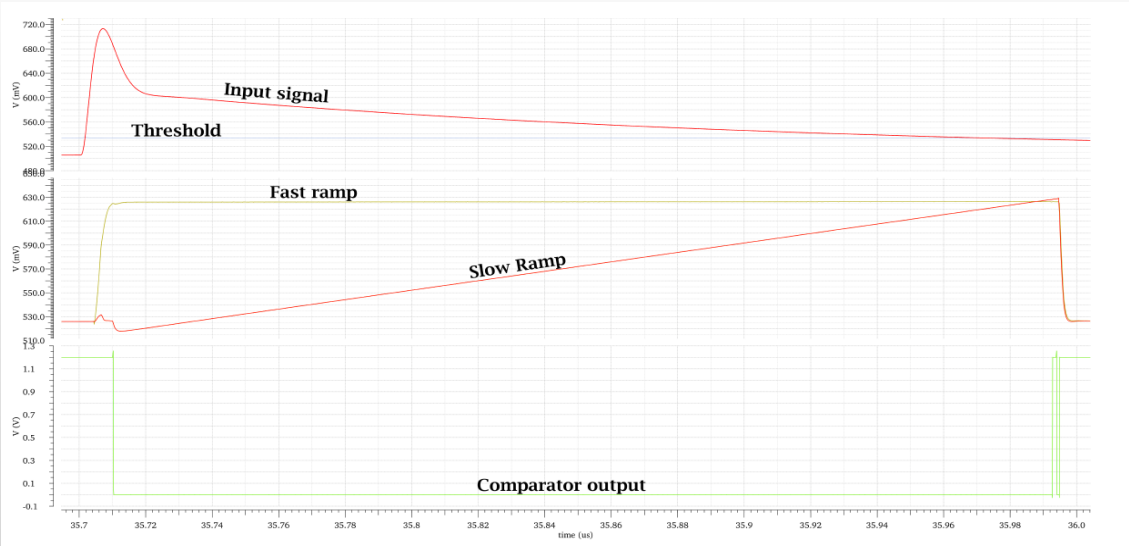


- TIA amplifier is adopted to transfer the current to voltage signal
- I/V conversion through 2.7 kohm resistor
- Each branch has 4 programmable gains: 1/3, 4/3, 7/3, 10/3
- Baseline offset adjustment 150-200 mV range by 3-bit DAC
- Cross talk between A/D blocks through the substrate has been mitigated by means of:
  - NMOS transistors with independent substrate
  - A/D blocks separated to keep a long distance in the layout
  - Guard rings around key transistors
  - Multiple guard rings around each module

Time to Digital Conversion

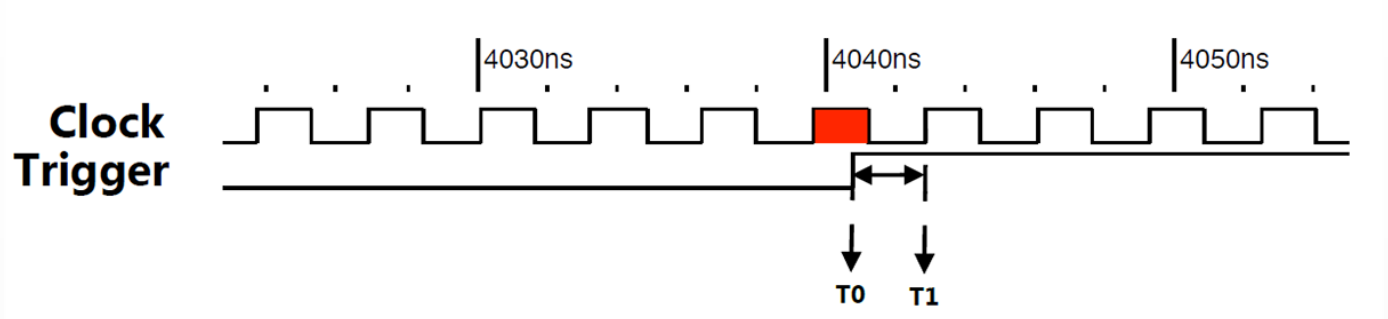
- Coarse time: 15-bit clock counter
- Time conversion performed by 4 TDC per pixel
- 9-bit fine time
- TDC are based on an analogue interpolation:
  - Idle state: current flows to ground in both branches
  - Fast ramp: C_fast charged to measure the phase between the event trigger and the clock
  - Slow ramp: counts the clock cycles to measure the fine time until C_slow and C_fast voltages are equal
- I.F. Interpolation Factor 64 or 128 (programmable)
- $I_{fast} = I.F. \cdot I_{slow}$
- LSB = CLKperiod / I.F.
  - ~ 50 – 100 ps @160 MHz
  - ~ 25 – 50 ps @320 MHz



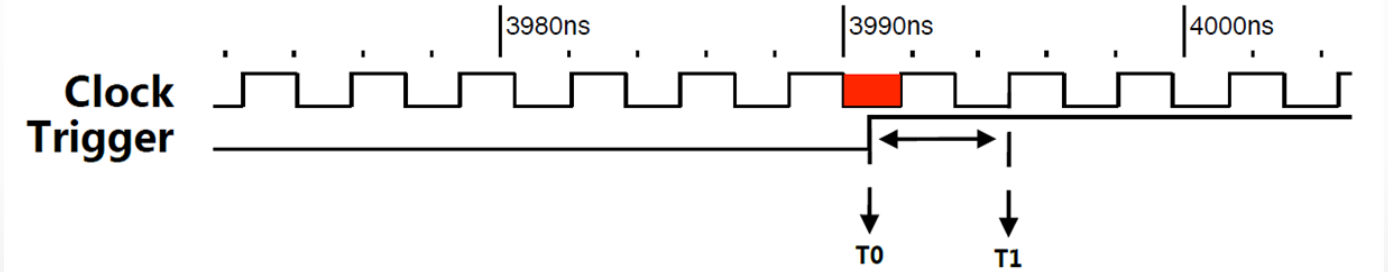


TDC principle of operation

1



2

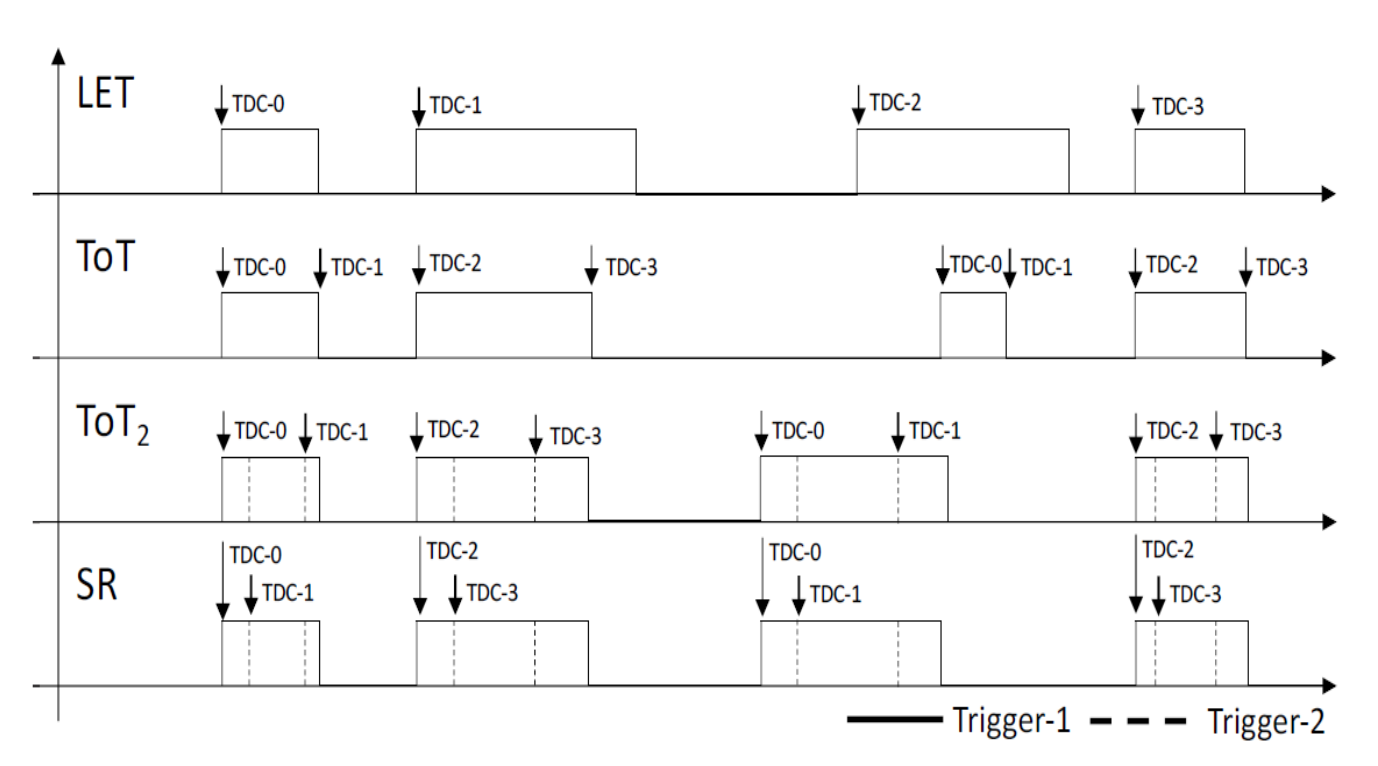


$$T = \begin{cases} (T_{coarse} \cdot \tau_{clk}) - (T_{fine} - MIN) \cdot LSB & \text{if} \quad T_{fine} \leq CUT \\ (T_{coarse} \cdot \tau_{clk}) - (T_{fine} - MIN) \cdot LSB + \tau_{clk} & \text{if} \quad T_{fine} > CUT \end{cases}$$

$$CUT = \frac{MIN + MAX}{2}$$

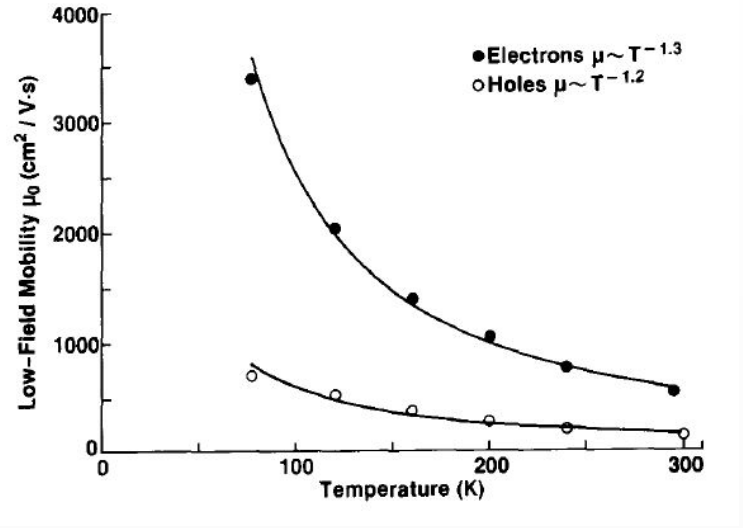
- To avoid metastability issues:
  1. If the trigger occurs BEFORE clock falling edge the fine time measurement ends at the next clock rising edge
  2. If the trigger occurs AFTER clock falling edge the fine time measurement ends at the second clock rising edge
- TDC time bin: $LSB = \frac{\tau clk}{MAX - MIN}$ where MIN and MAX are the TDC minimum and maximum values

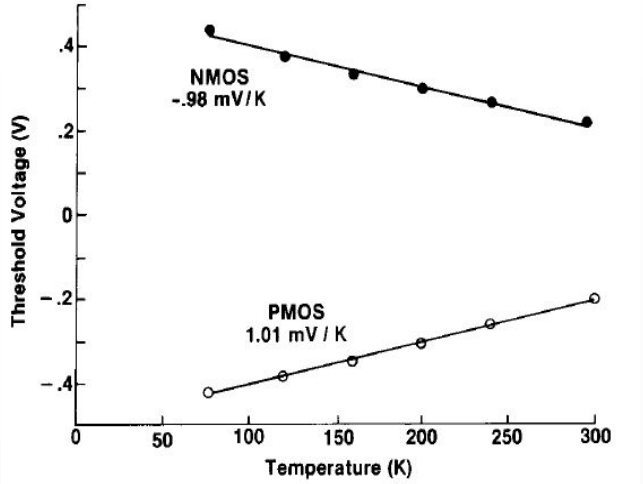
ALCOR pixel operating modes



- 4 operating modes:
- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators. Triggers are generated from amplifiers with different gains to reduce jitter due to long tail signals
- **SR**: slew-rate measurement using both discriminators
- Each mode can be set to:
  - **FE**: normal operation mode
  - **FE_TP**: send test-pulse to analogue front-end
  - **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)
  - Each pixel can also be **disabled**

Cold CMOS electronics

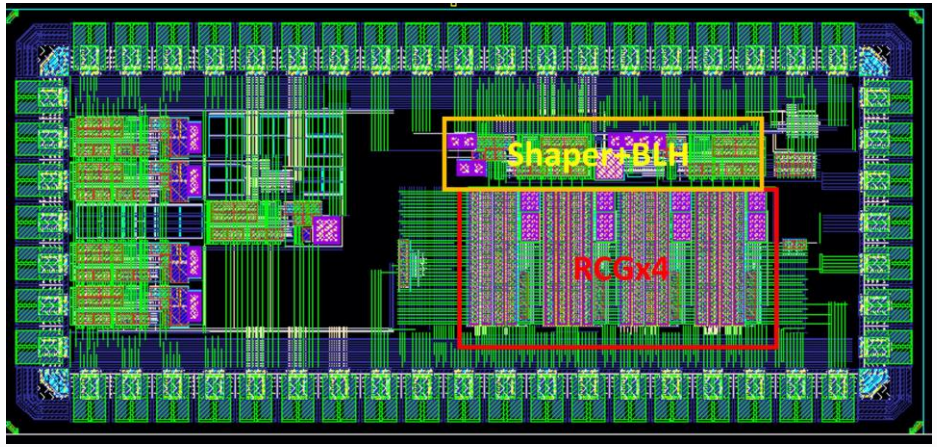


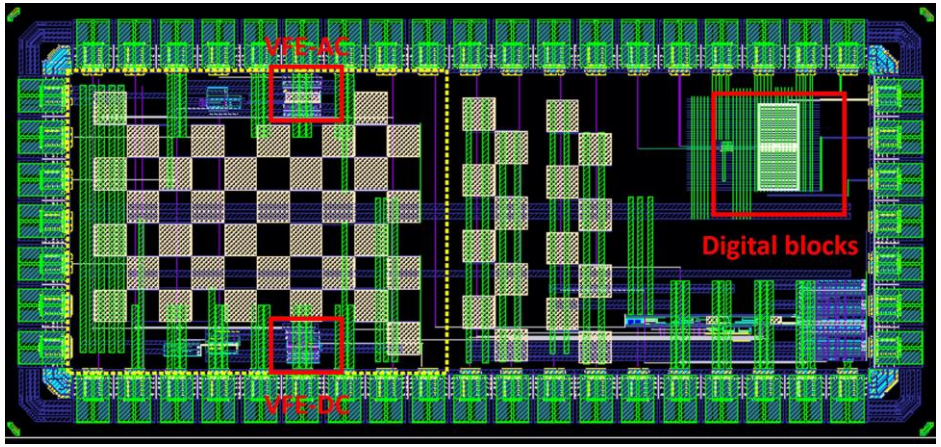


- CMOS technologies show strong dependence on temperature, as reported in literature:
  - Mobility increase 4-6 times from 300 K to 77 K (*). Improved gm
  - Parasitic resistance decrease one order on magnitude from 300 K to 77 K
  - Junction capacitance decreases
  - Threshold voltage increase with a linear trend 1 mV/K – 2 mV/K (*)
  - Noise reduction (more on PMOS devices)
  - Hot carrier effects increase (higher degradation on NMOS devices (**))
- Simple recommendations: use PMOS for key transistor (if possible). Avoid min width devices
- PDK models are accurate at temperatures down to -40 C
- Analogue simulations at 77 K are possible with some extrapolation, but should be verified for each technology

(*) William F Clark et al. “Low temperature CMOS-a brief review”. In: *IEEE Transactions on Components Hybrids and manufacturing Technology* 15.3 (1992), pp. 397–404
(**) Shaorui Li et al. “LAr TPC electronics CMOS lifetime at 300 K and 77 K and reliability under thermal cycling”. In: *IEEE Transactions on Nuclear Science* 60.6 (2013), pp. 4737–4743

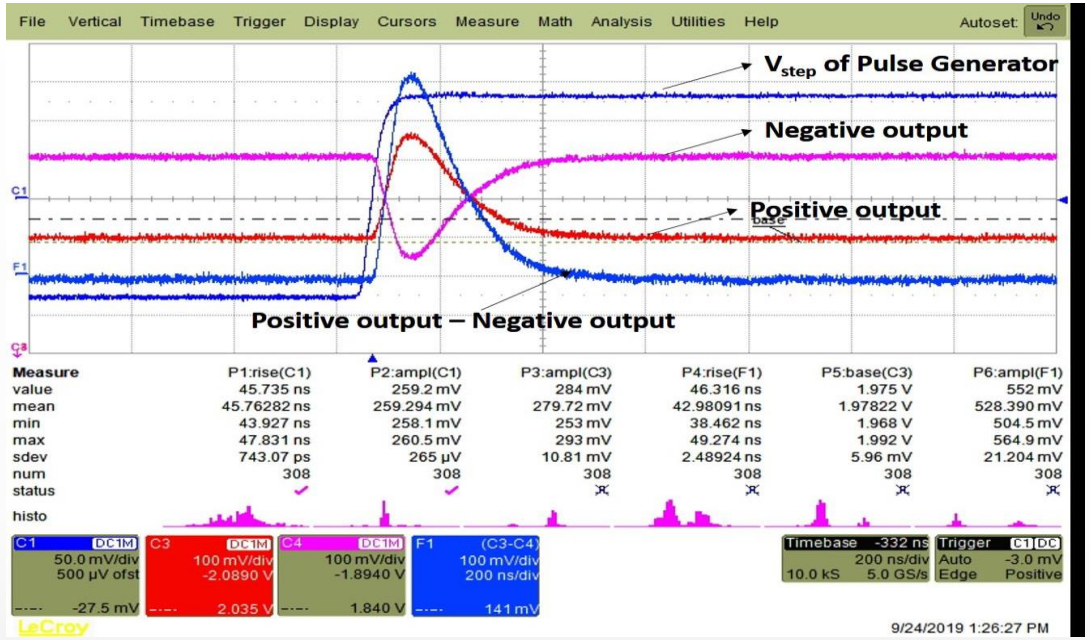
Test chips

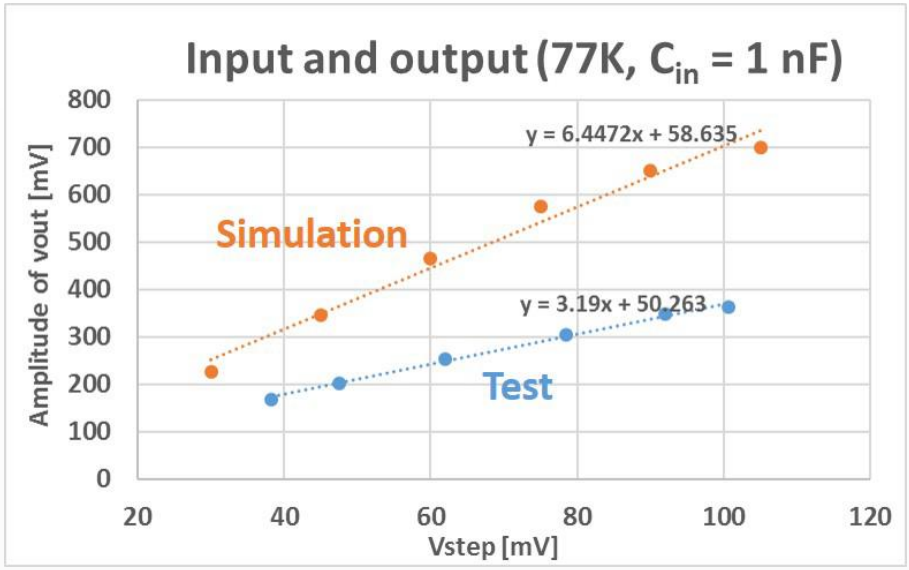


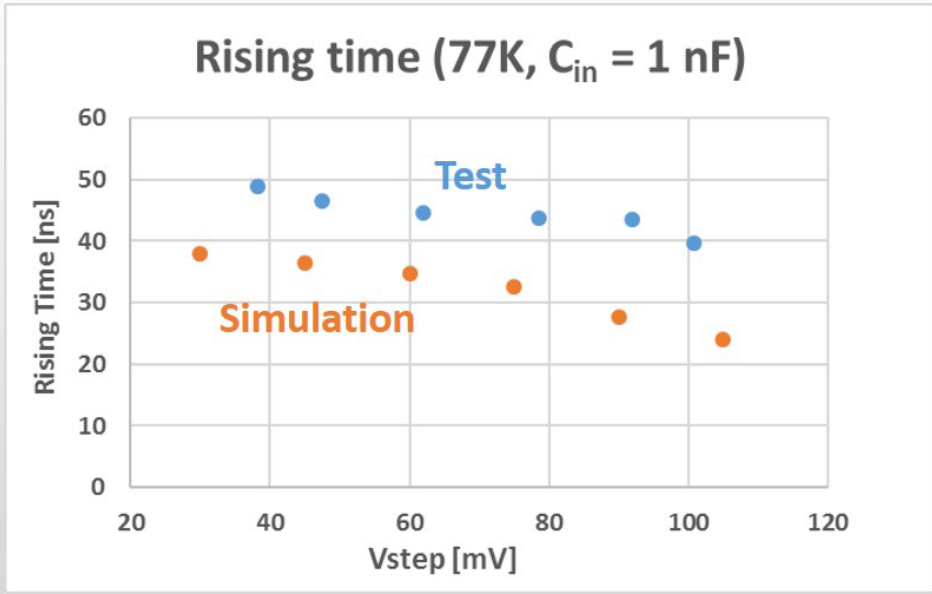


- Two test chips have been done and tested at 77 K before to design the ALCOR chip
- Both analogue and digital modules have been implemented:
  - VFE based on RCG with DC or AC coupling
  - CR-RC shaper used as TIA stage
  - Baseline holder
  - Digital synchronizer flip-flop chain
  - LVDS driver

Test chips 77K analogue results

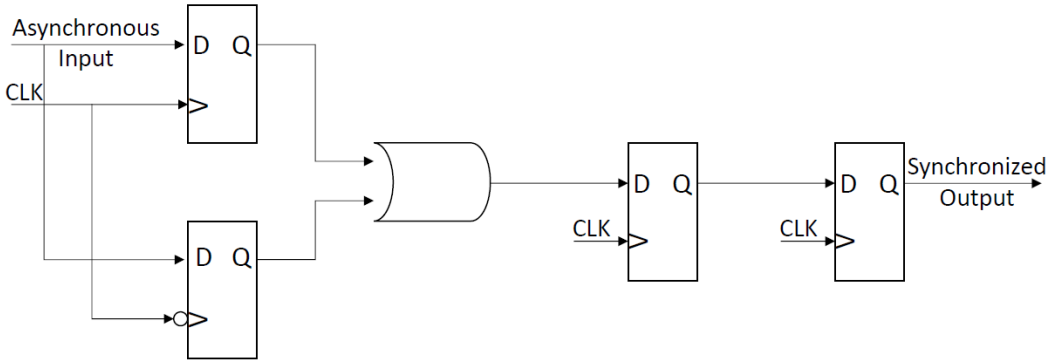


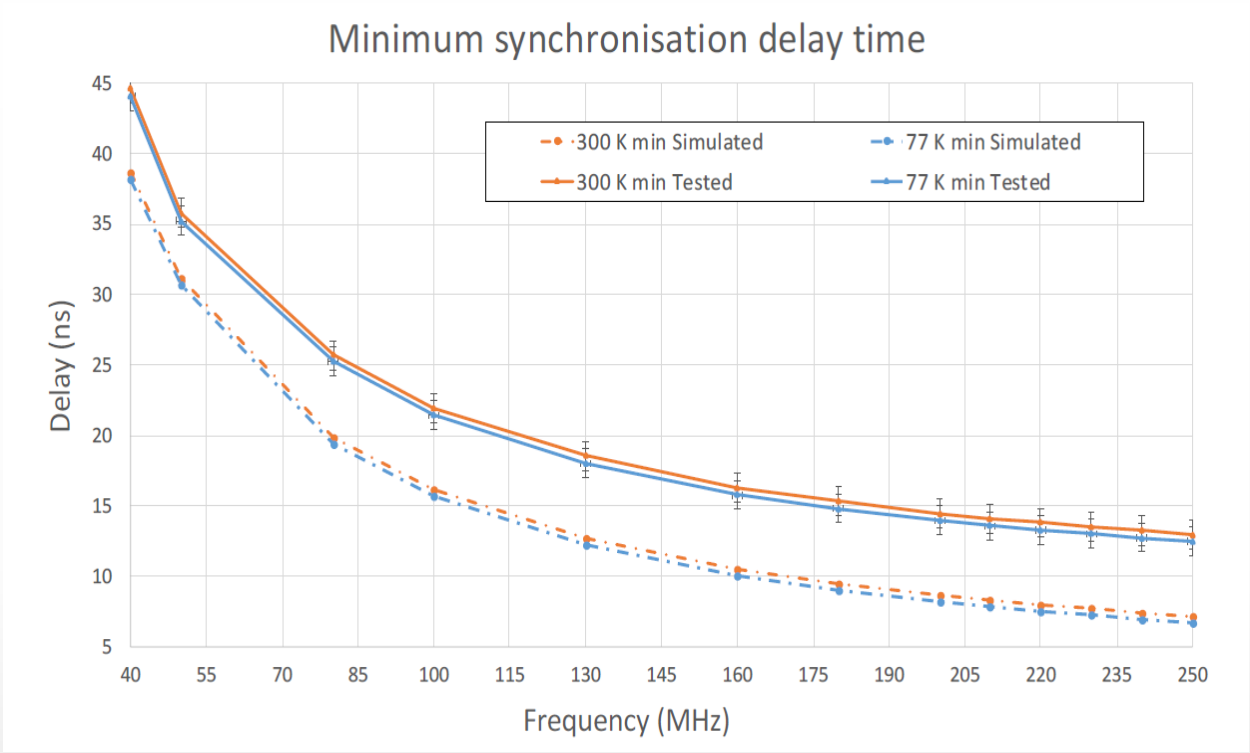




- RCG FE fully working with DC coupling
- AC didn't work properly. ALCOR VFE is DC coupled
- Observed an oscillation on CR-RC shaper due to a lack of phase margin. In ALCOR replaced by a non-inverted voltage amplifier
- Simulations/test mismatches: gain -50%, noise -45%, ENC 9.7%, rising time 34.8%
- Different performances 300K / 77K: gain improved 25%, ENC decreased 25%, rising time decreased 45%

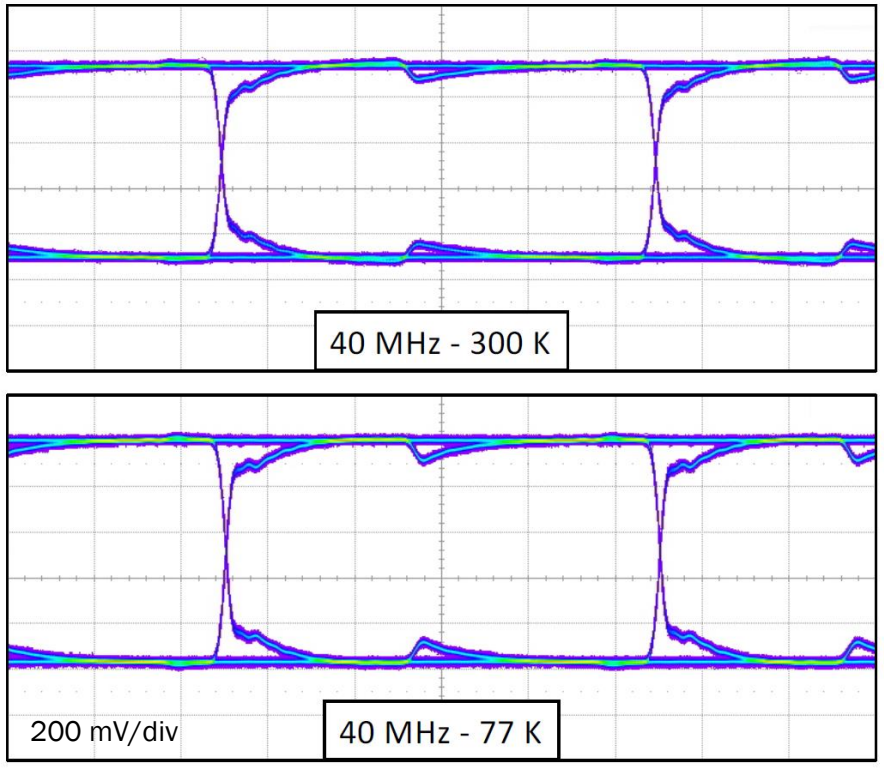
Test chips 77K digital results

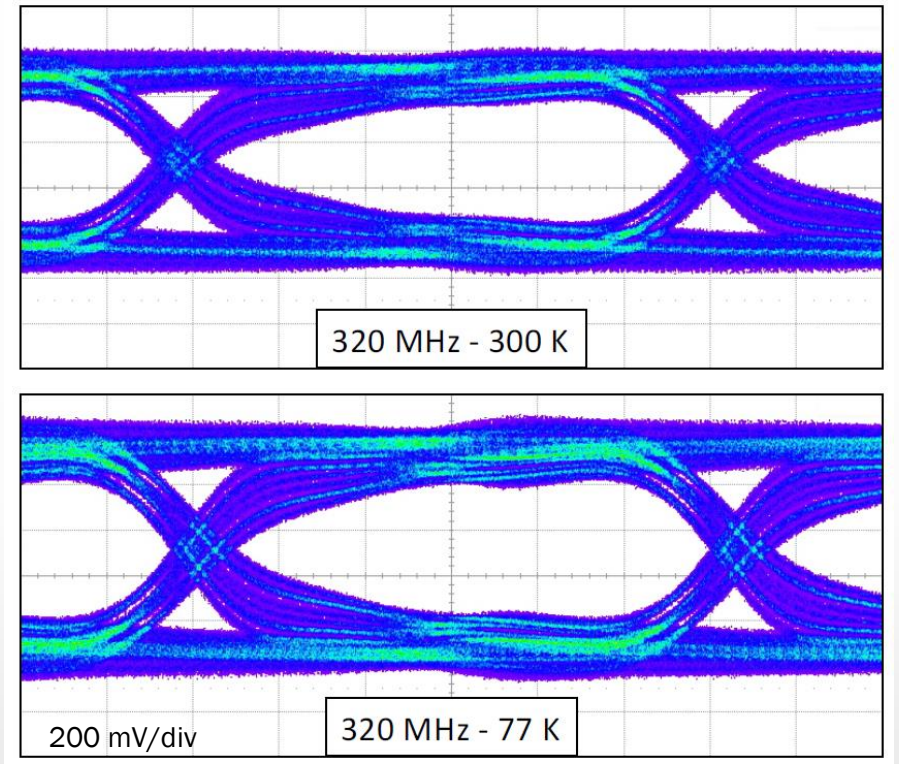




- Synchronizer circuit
  - Delay time measured at different clock frequencies, from the asynchronous arrival time to the synchronized output
  - Systematic offset due to the cables ~5 ns
  - Extrapolated SPICE models at 77K are valid
  - Expected min synch delay time: 1.5 clock cycles + propagation delays through FFs and gates
  - Time difference between measurements at 300 K and 77 K: ~450 ps
- For reference, standard cell CKBUFM32LM model shows the following delays at different corners: TYP 108 ps, MIN 71 ps (-34%), MAX 195 ps (+80%)

Test chips 77K digital results



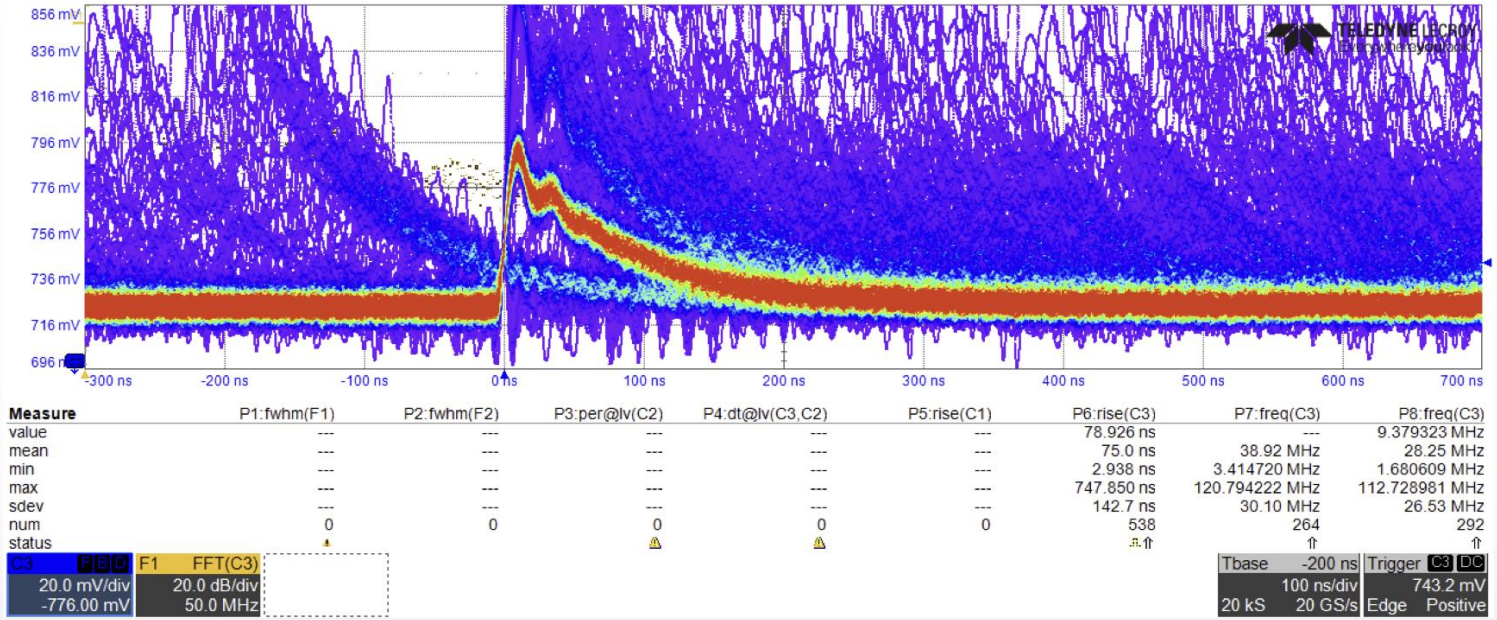


- LVDS drivers worked up to their nominal frequency of 320 MHz without any issue

ALCOR results

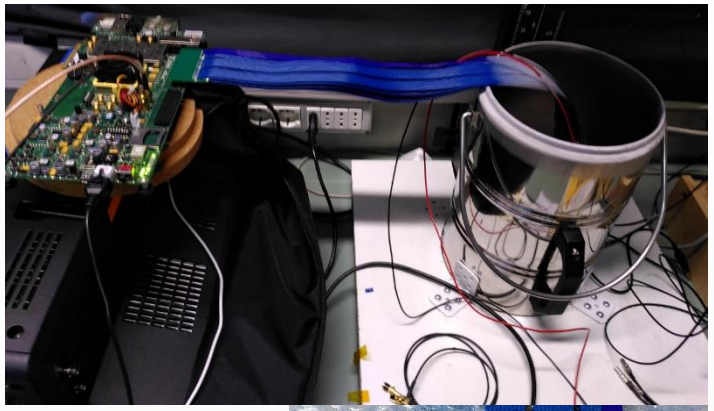
- The purpose of this development was a research programme of INFN CSN2, to characterise the CMOS technology at very low temperature (77K)
- DUNE experiment have expressed interest to this ASIC and the chip is under test at cryogenic temperatures
- With the years it became also the main choice for non-cryogenic temperatures experiments:
  - FE readout for dIRICH EPIC detector at Electron-Ion Collider (EIC)
  - PRIN project to study the squeezed states of the light
  - Fast Silicon Detectors (with a different VFE)
- The results obtained so far are mostly collected within EPIC programme
- The first version of the chip has been extensively used in the last two years, both in laboratory and in two different test beams
- A new revision of the chip has been submitted to solve some bug in the digital logic and to adapt the FE to the chosen model of SiPM

ALCOR in liquid nitrogen



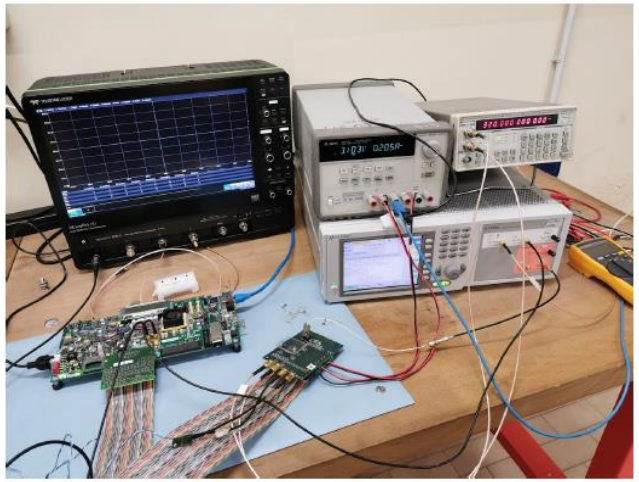
Measure	P1:fwhm(F1)	P2:fwhm(F2)	P3:per@lv(C2)	P4:dt@lv(C3,C2)	P5:rise(C1)	P6:rise(C3)	P7:freq(C3)	P8:freq(C3)
value	---	---	---	---	---	78.926 ns	---	9.379323 MHz
mean	---	---	---	---	---	75.0 ns	38.92 MHz	28.25 MHz
min	---	---	---	---	---	2.938 ns	3.414720 MHz	1.680609 MHz
max	---	---	---	---	---	747.850 ns	120.794222 MHz	112.728981 MHz
sdev	---	---	---	---	---	142.7 ns	30.10 MHz	26.53 MHz
num	0	0	0	0	0	538	264	292
status								

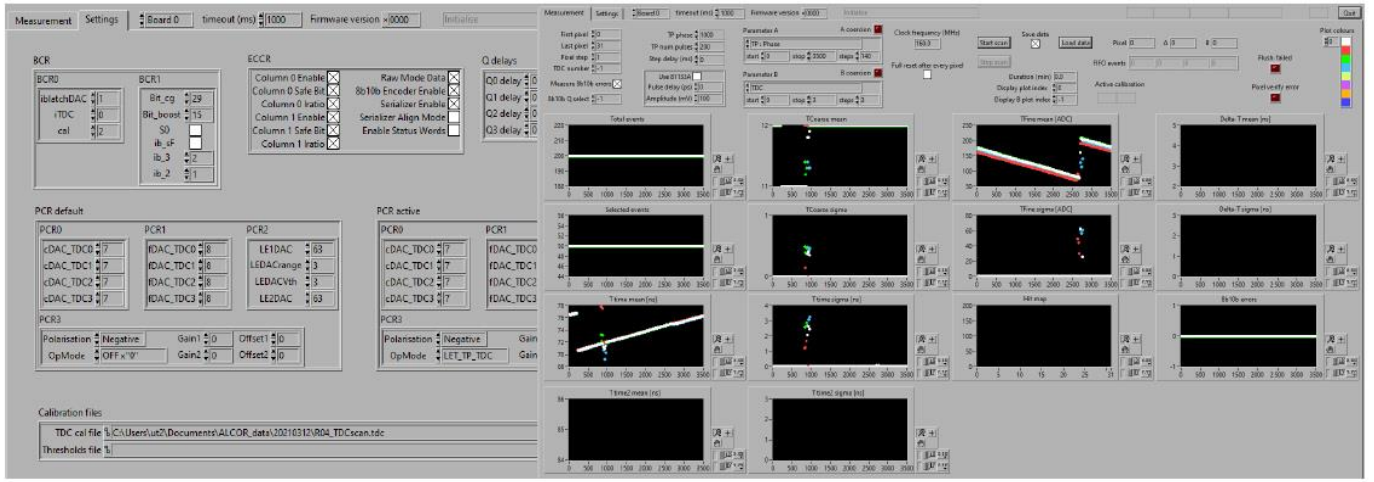
C3 20.0 mV/div -776.00 mV | F1 FFT(C3) 20.0 dB/div 50.0 MHz | Tbase -200 ns 100 ns/div 20 kS 20 GS/s | Trigger C3 DC 743.2 mV Edge Positive

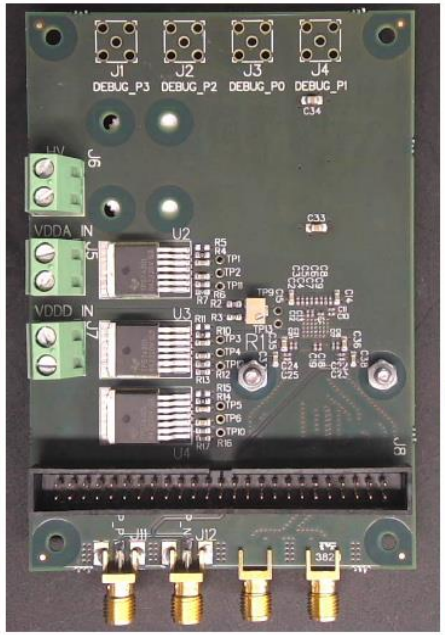


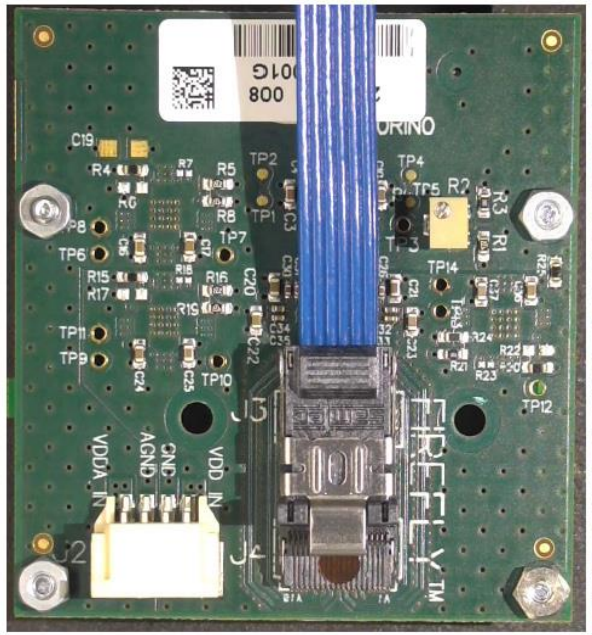
- The DUNE collaboration at INFN-BO is working on the characterization of the chip at 77 K
- 8 ALCOR ASICS are coupled to Hamamatsu SiPM S14161-3050HS-08 for a total of 256 channels
- Digital circuits are working without any issue
- Analog frontend works as expected
- More measurements are ongoing

LAB test environment and FEB



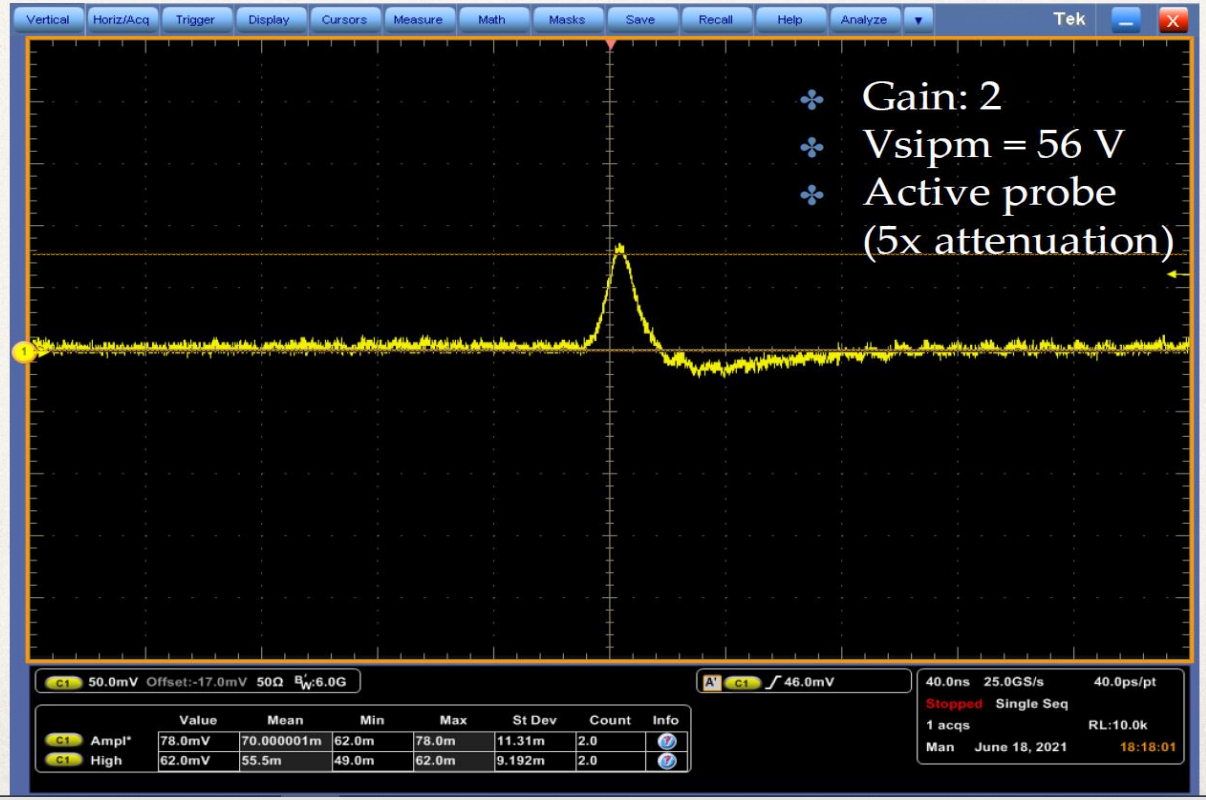






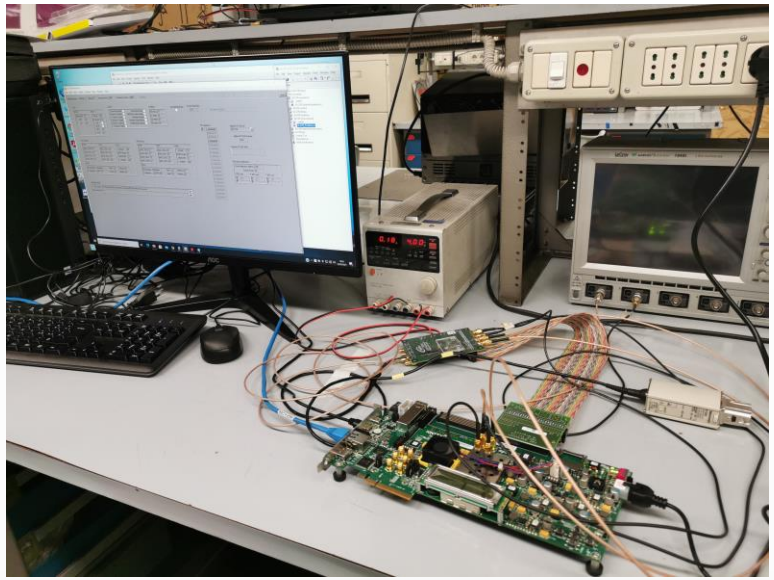
Dark count measurements with Hamamatsu S13360 3050VS

ALCOR Ch0: SiPM1 = HAMA1 (S13360 3050VS)
Vbr = 53+-5V ; Operating V = Vbr+3

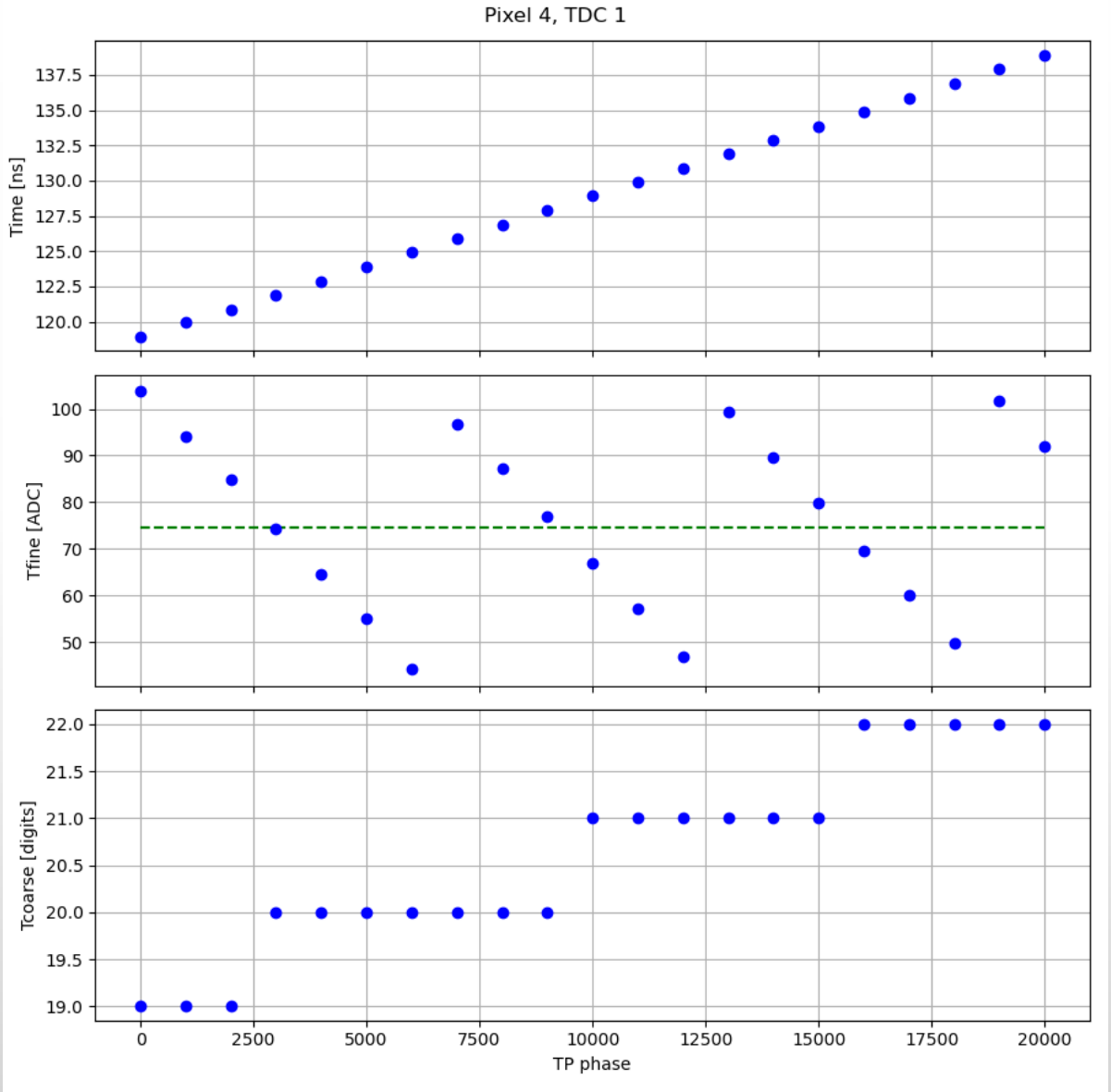


Full chip power consumption @320 MHz (analogue + digital):
Core: 246 mW – 366 mW depending on the bias settings
LVDS drivers: 26 mW
8 mW – 12 mW per channel including everything

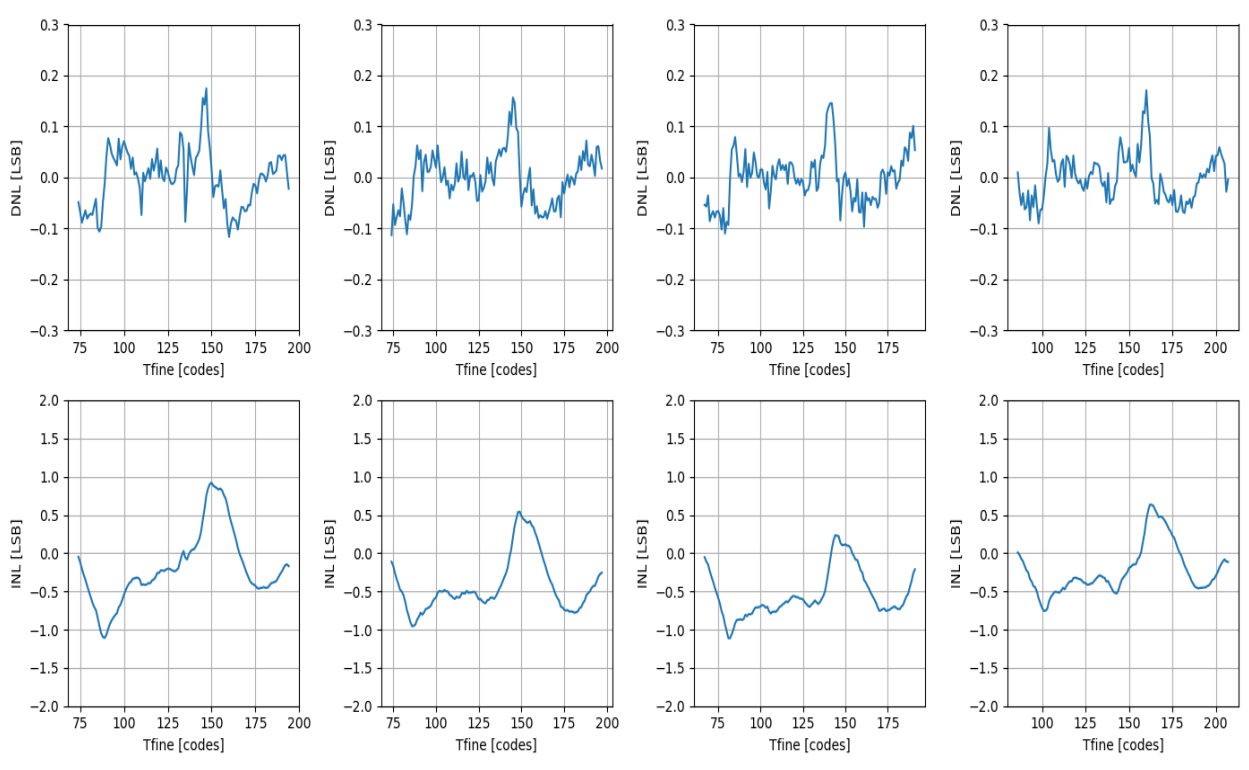
TDC calibration with Test Pulse

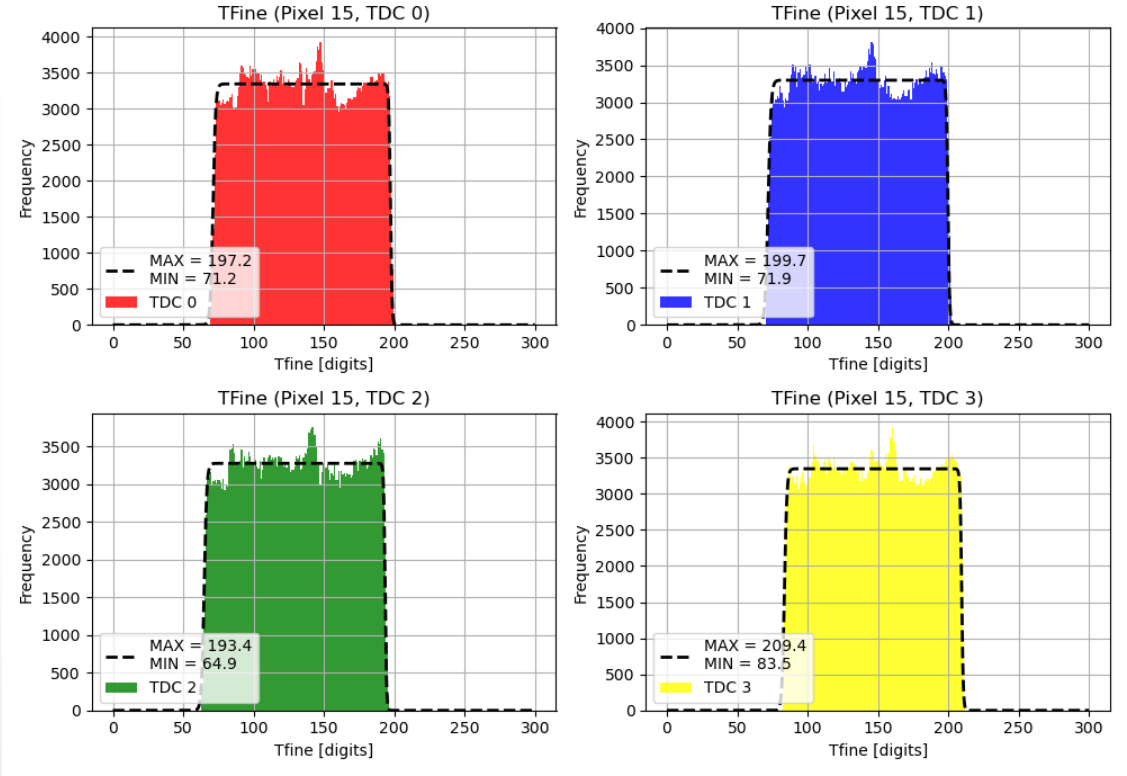


- Digital test-pulse phase scan from FPGA
- Extract Tfine MIN and MAX for each TDC of each pixel, save (32 pixels x 4 TDCs) 128 entries LUT
- Interpolation Factor (I.F.) = MAX - MIN
- LSB = clk_period / I.F. ≈ 25 or 50 ps



TDC calibration with dark count

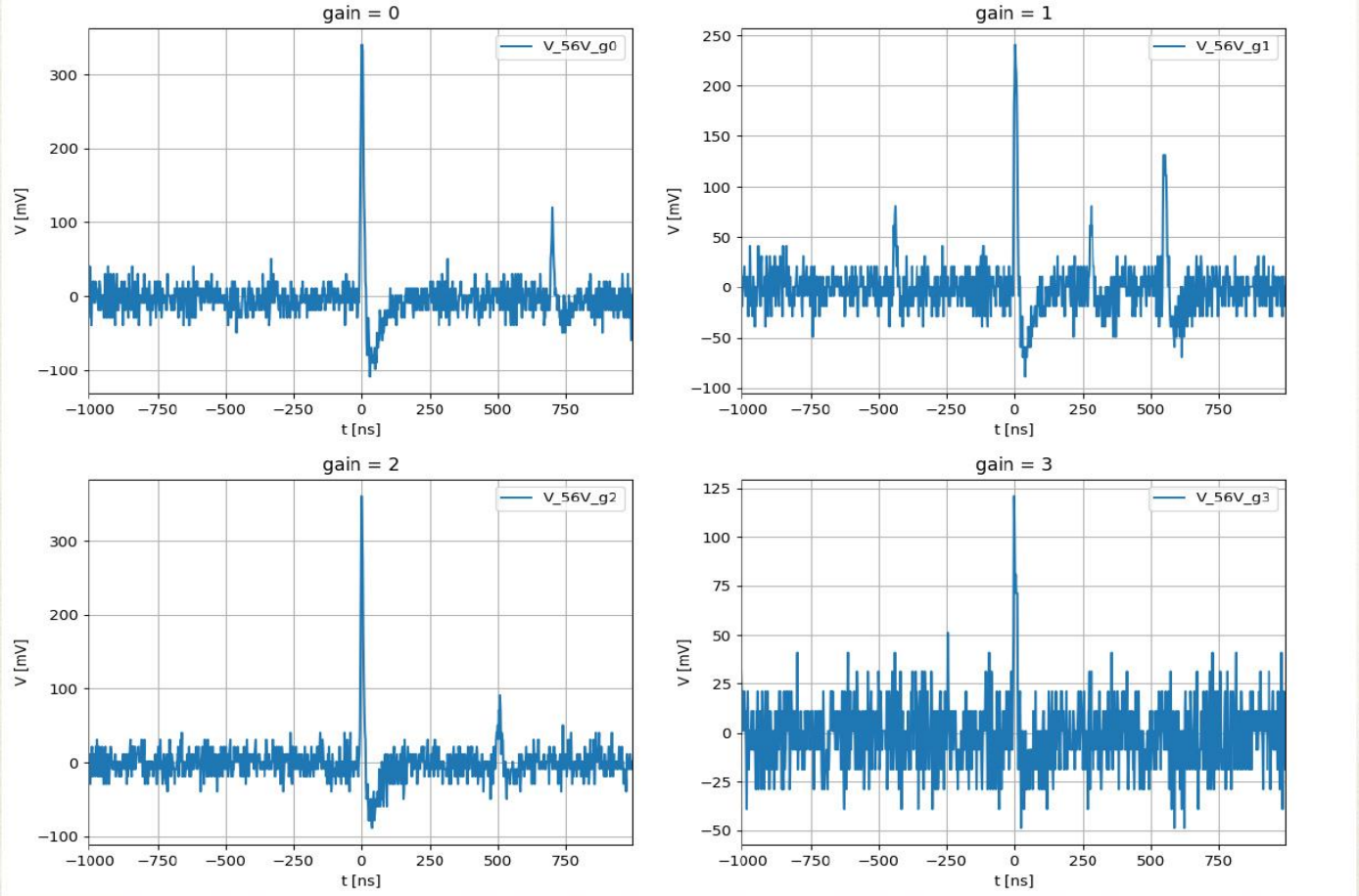




- SiPM Hamamatsu S13360 3050VS at room temperature
- Tfine MIN and MAX limits are as expected
- Corrupted data due to some bug in the logic readout can have affected these measurements
- The new version of the chip will fix these errors in the digital logic (already shipped!)

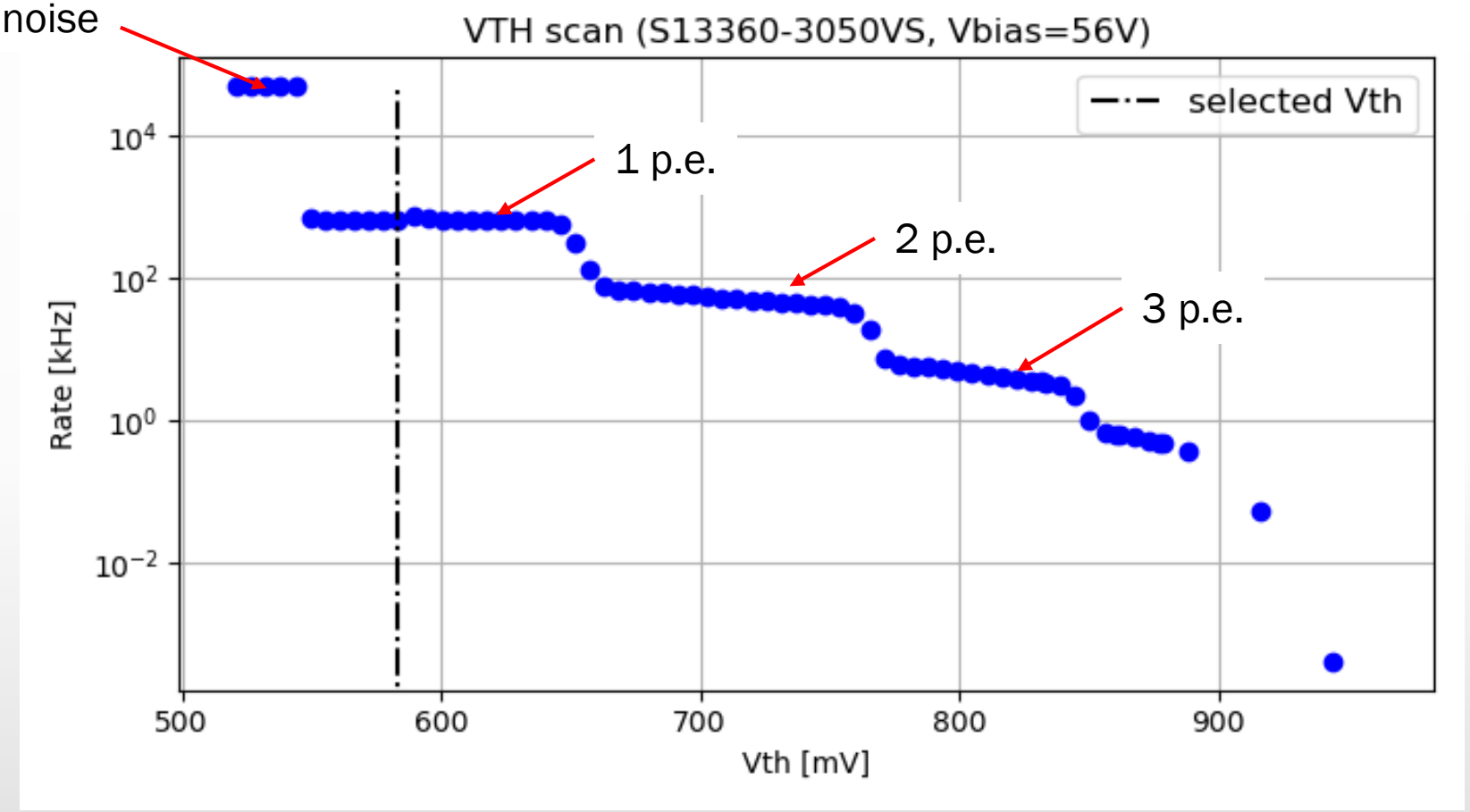
Dark count measurements with Hamamatsu S13360 3050VS

ALCOR Ch0: SiPM1 = HAMA1 (S13360 3050VS)
Vbr = 53+-5V ; Operating V = Vbr+3



- Active probe
- Gain scan
- Vsipm: 56V

Dark count measurements with Hamamatsu S13360 3050VS

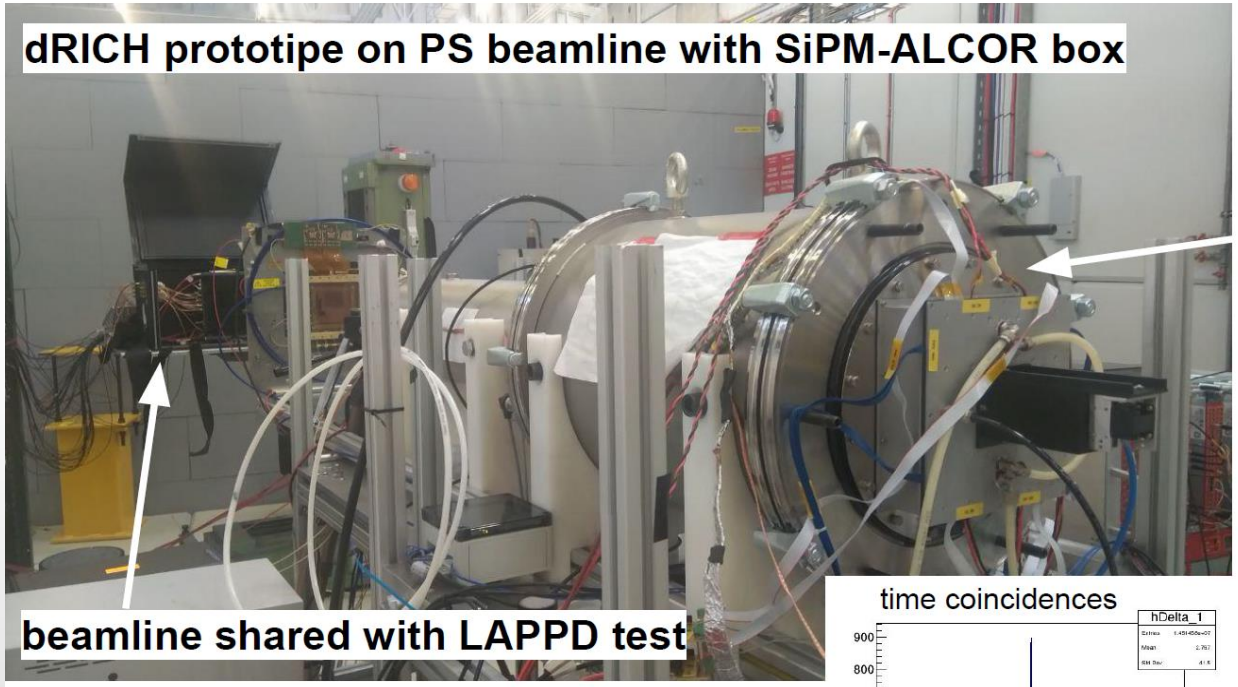


Threshold scan:
Dark-count rate *vs* threshold → “staircase” plot
Room temperature

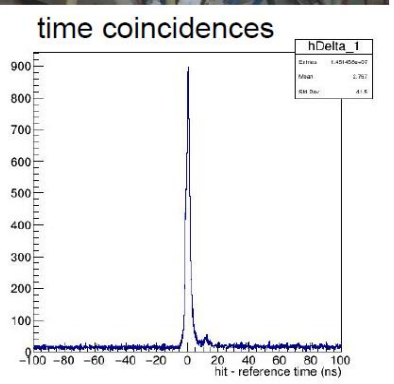
The 2022 test beam (EPIC dRICH)

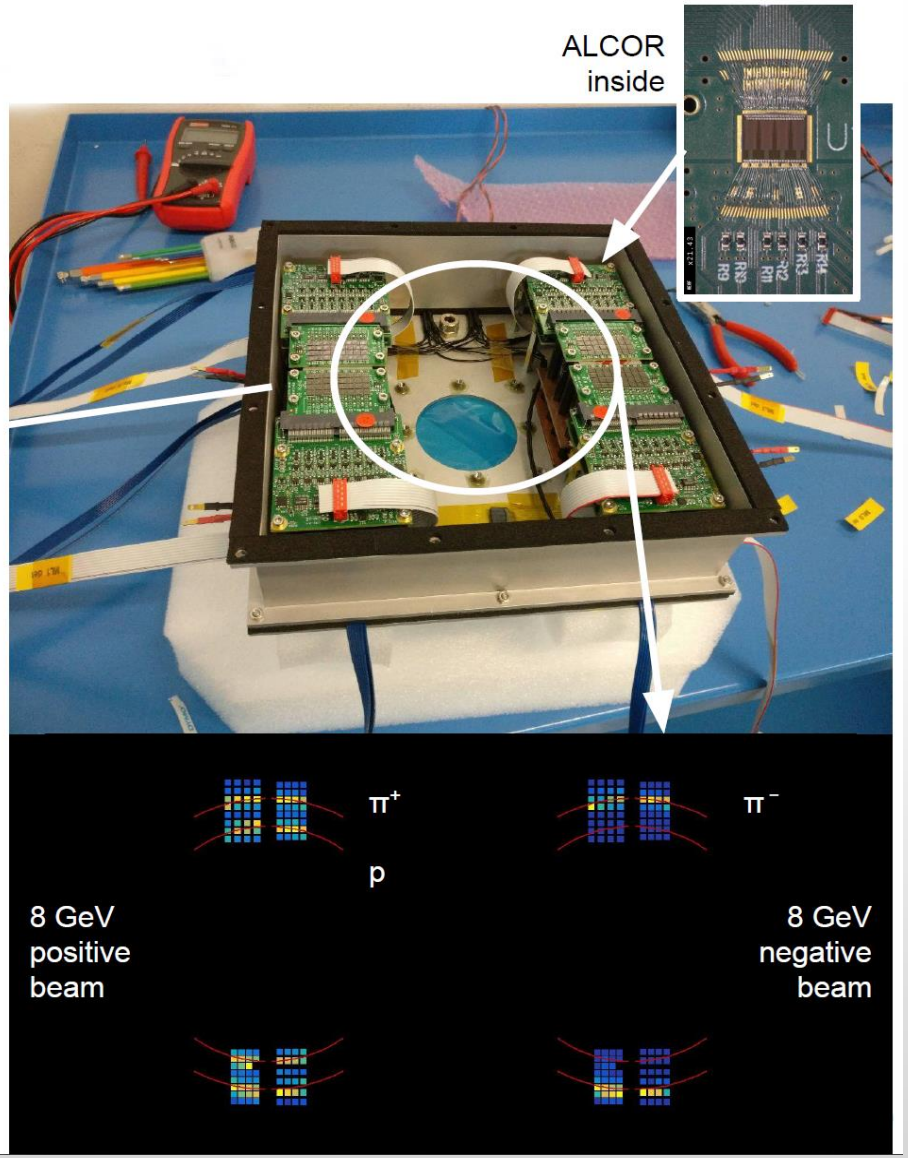
operating at -30°C

successful operation of SiPM with complete readout chain



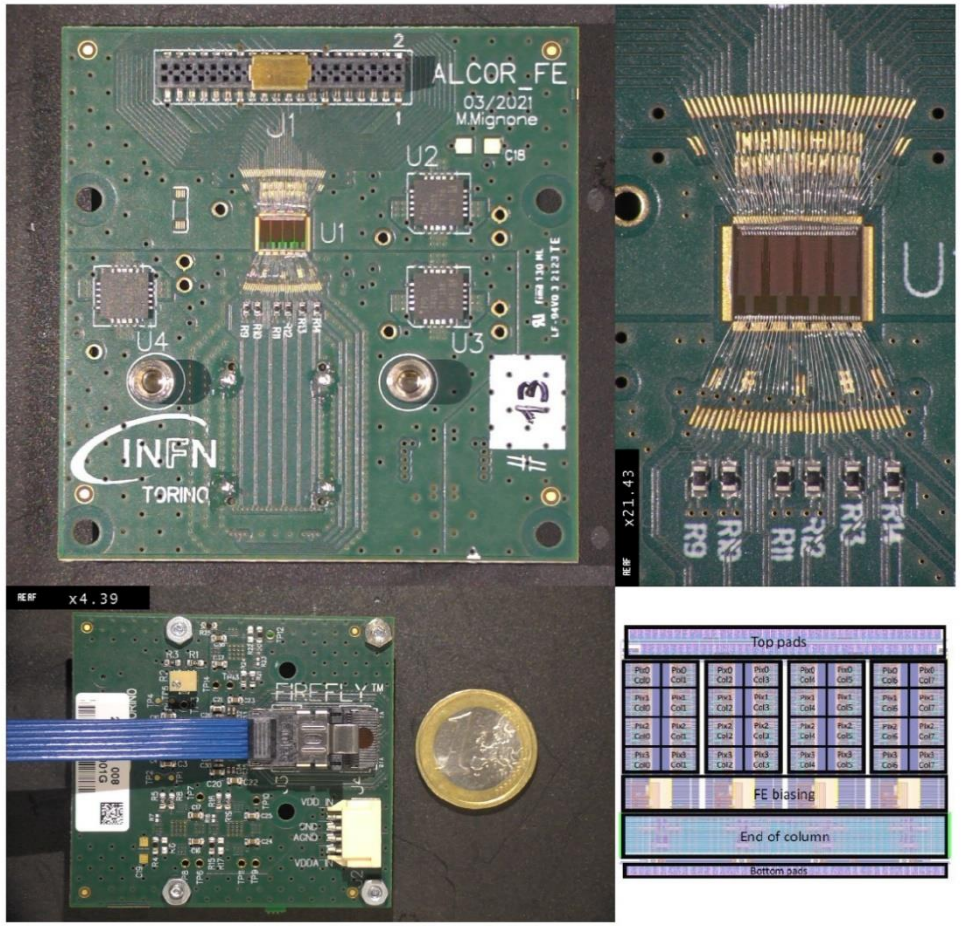
SiPM sensors were **irradiated** (up to 10^{10}) and **annealed** (150 hours at T = 150 C)

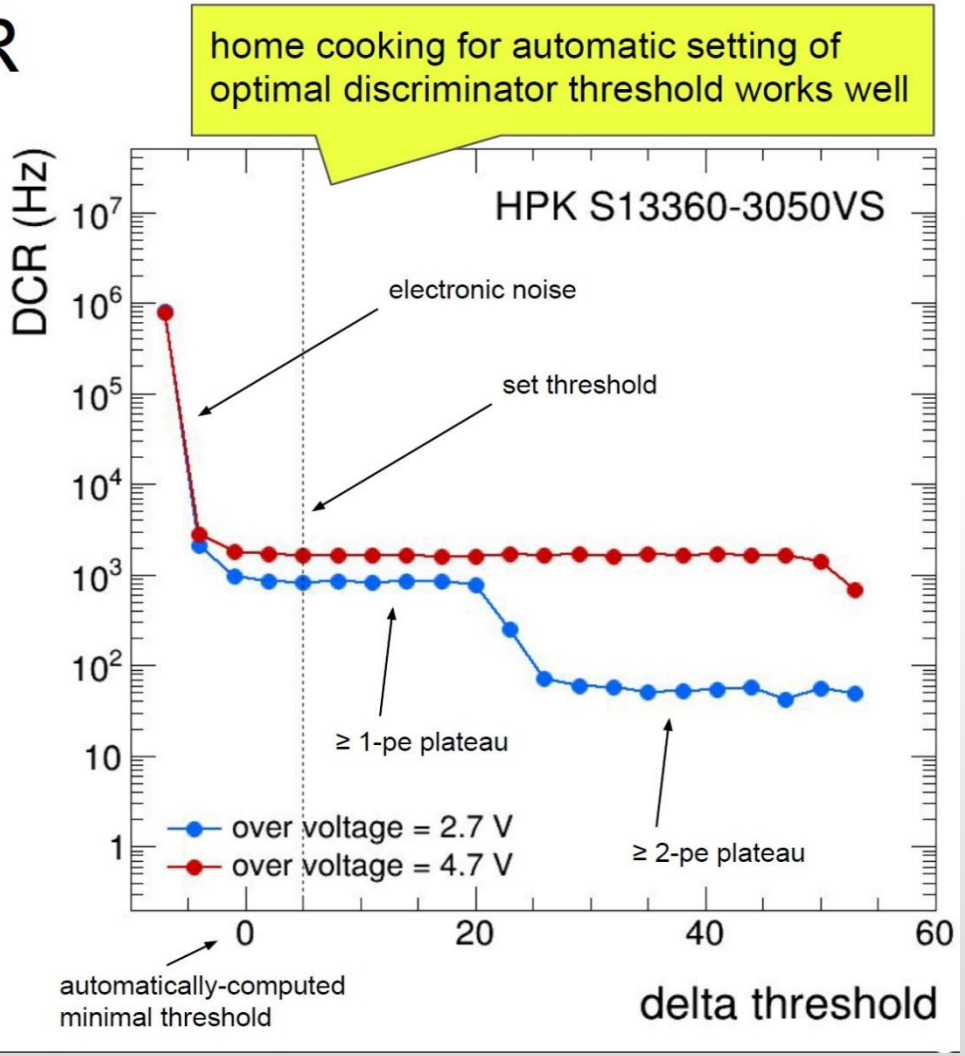




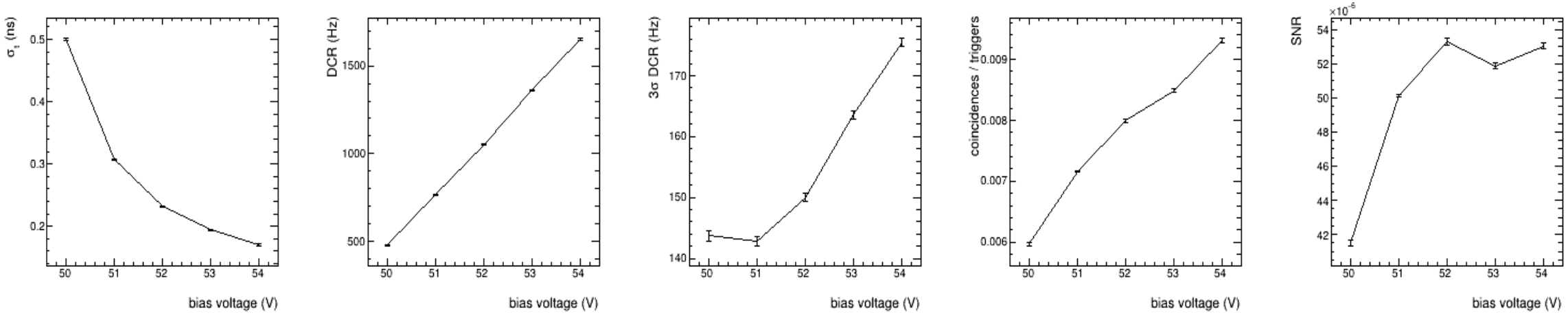
The 2022 test beam (EPIC dRICH)

Photon counting with ALCOR

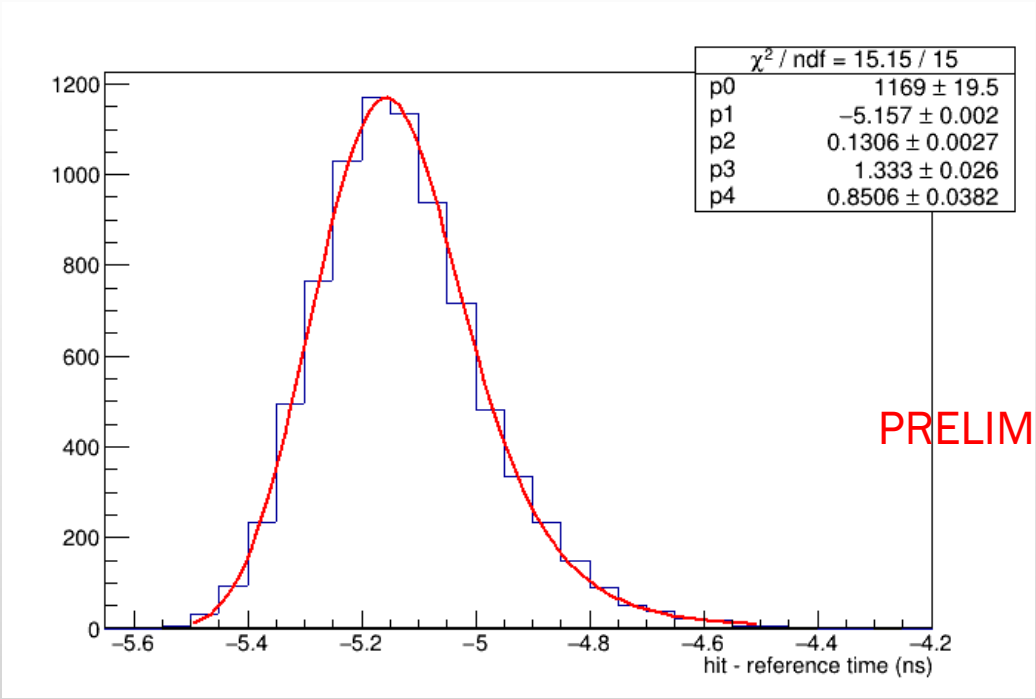




Measurements with LASER



- Operating at -30 °C
- SiPM Hamamatsu S13360 3050VS
- Laser specifications:
  - picosecond pulsed laser
  - 401.4 nm
  - 25 ps FWHM pulse width
  - < 4 ps synchronization jitter
- Measured PDE and SNR increase with Vbias
- TDC LSB 50 ps
- Preliminary time resolution ~130 ps r.m.s.



PRELIMINARY

Summary

- The first version of ALCOR has been tested intensively giving good preliminary results and detecting minor problems to fix
- More measurements will be done at 77K thanks to the DUNE collaboration
- ALCOR v2 shipped few days ago (MPW run)
- ALCOR v2.1 will be delivered this summer (INFN engineering run)
- ALCOR 2.1 adds more corrections to ALCOR v2
- The programme for EIC/EPIC establishes:
  - October 2023: test beam to equip 6 readout unit (48 ALCOR, 1536 channels)
  - 2024: development of the new chip with improved capabilities, 64 channels and packaging (flip-chip BGA)
- The DUNE programme aims to develop a new version of ALCOR with 1024 channels in package operating at 77K