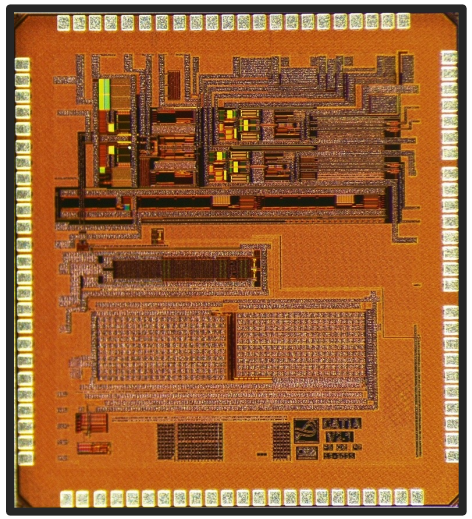
CATIA

Large dynamic range preamplifier for the CMS ECAL upgrade



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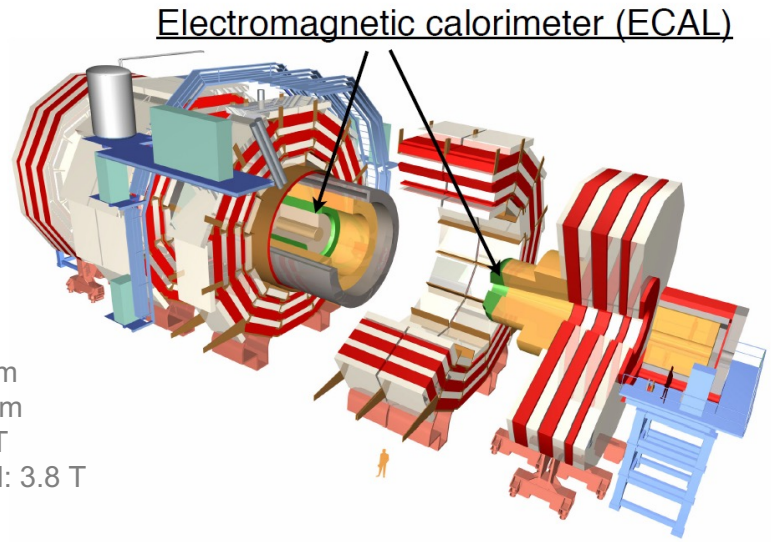
Outline

1. CMS ECAL barrel detector
2. Architecture of the new VFE for the upgrade phase II
3. CATIA
4. Measurements Results
5. Summary

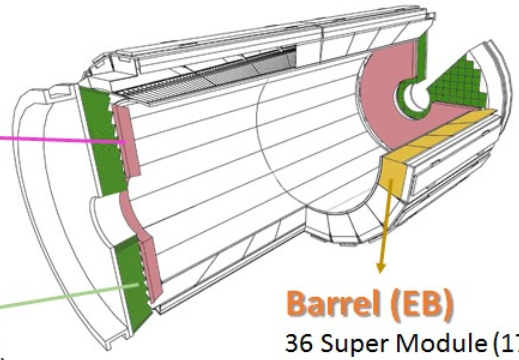
CMS ECAL barrel detector



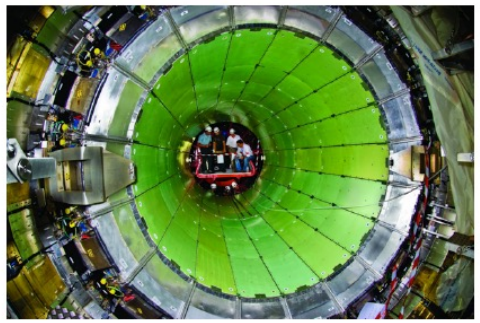
CMS:
Length: 21.5 m
Diameter: 15 m
Weight: 14 KT
Magnetic field: 3.8 T

Preshower (ES)
4 half-disk Dees
2 Pb/Si planes
Total of 137216 Si strips
Coverage: $1.65<|\eta|<2.6$

Endcap (EE)
4 half-disk Dees (3662 crystals)
Total of 14648 $PbWO_4$ crystals
Coverage: $1.48<|\eta|<3.0$

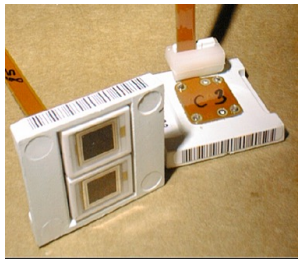


Barrel (EB)
36 Super Module (1700 crystals)
Total of 61200 $PbWO_4$ crystals
Coverage: $|\eta|<1.48$



Barrel (EB)

Endcap (EE)



Barrel
2x **A**valanche **P**hoto-**D**iodes

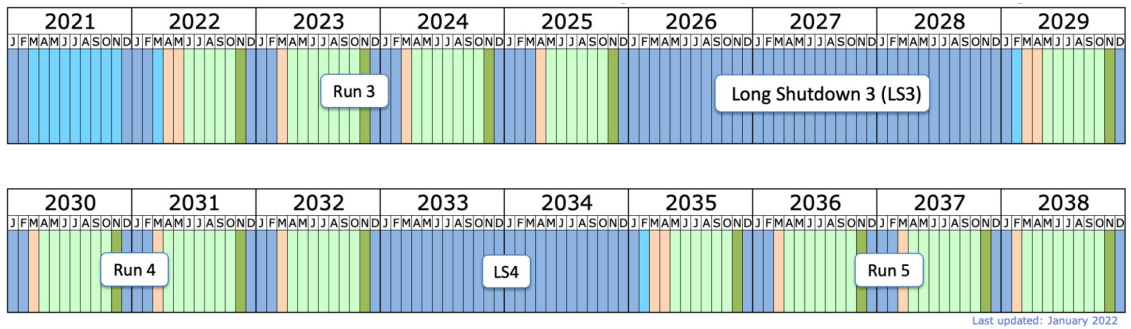
Endcap
1x **V**acuum **P**hoto-**T**riodes

- The current **CMS Electromagnetic Calorimeter** (ECAL) is a hermetic system organized into a barrel and two endcap detectors using scintillating lead tungstate crystals.

ECAL Barrel Phase II upgrade

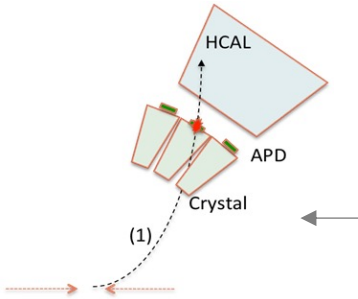
Aim at collecting 3000/fb by the end of the 2030's

- Up to 200 PU per beam-crossing w/r to 40-50 in phase I
- Detectors have to support a large radiation dose (increased noise)

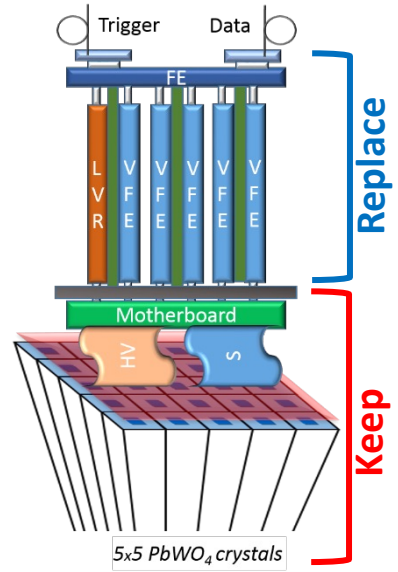


New endcap calorimeter with new technologies

BCAL : electronics upgrade mandatory to meet HL-LHC L1 trigger requirements



- New Trigger
  - Provide crystal by crystal information at L1 trigger (currently 5 x 5 crystals granularity)
  - Improvement of "Spike" rejection (it would dominate L1 trigger if unsuppressed)
    - Hadrons interacting directly with APDs causing anomalous high E deposits
- Keep current energy resolution
  - Cooling of crystals and photodetectors from 18 °C to 9 °C to mitigate APD dark current increase
- New precision timing
  - 30 ps time resolution for deposits with E > 50 GeV (photons from H → γ γ decay) for pile-up mitigation

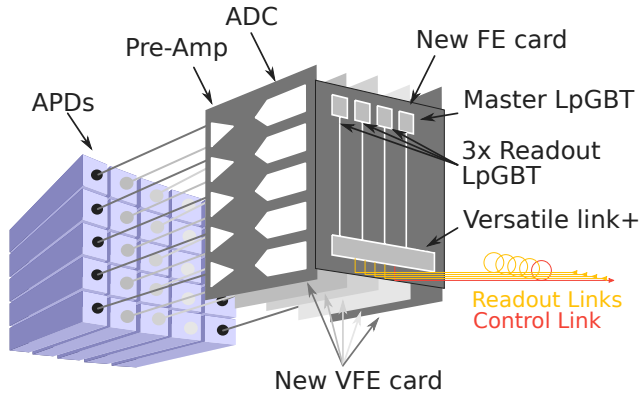


Replace all active on-detector electronic components

VFE electronic: TIA + Fast ADC

New VFE to improve spike rejection and timing measurement

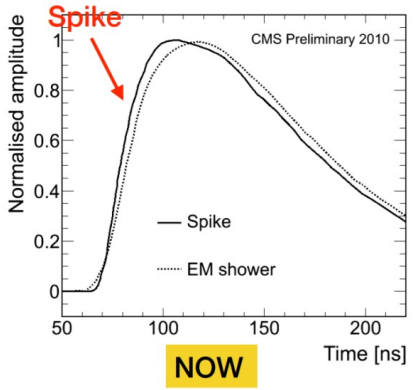
- Dual gain Trans-Impedance Amplifier (TIA) with a 50 MHz bandwidth
- 12-bit ADC: 2 channels at 160 MHz sampling including data compression



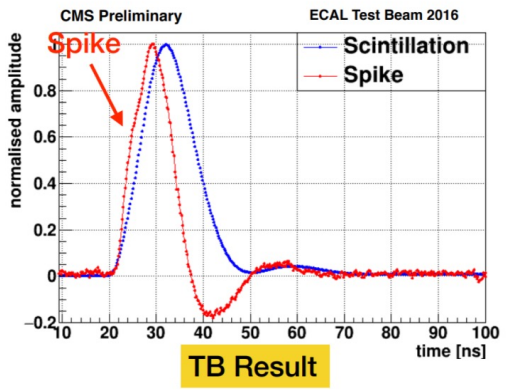
Lead-Tungstate crystal

Spike rejection

- TIA solution preserves fast signals
- On-line spike tagging by shape analysis (HWHM)



NOW

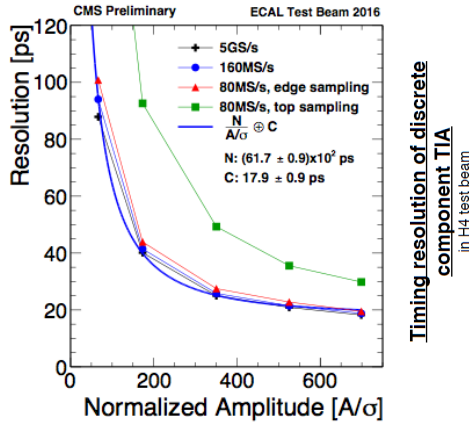


TB Result

Time resolution

- Needs 160 MHz sampling to have 30 ps @ 50 GeV (HL-LHC start)

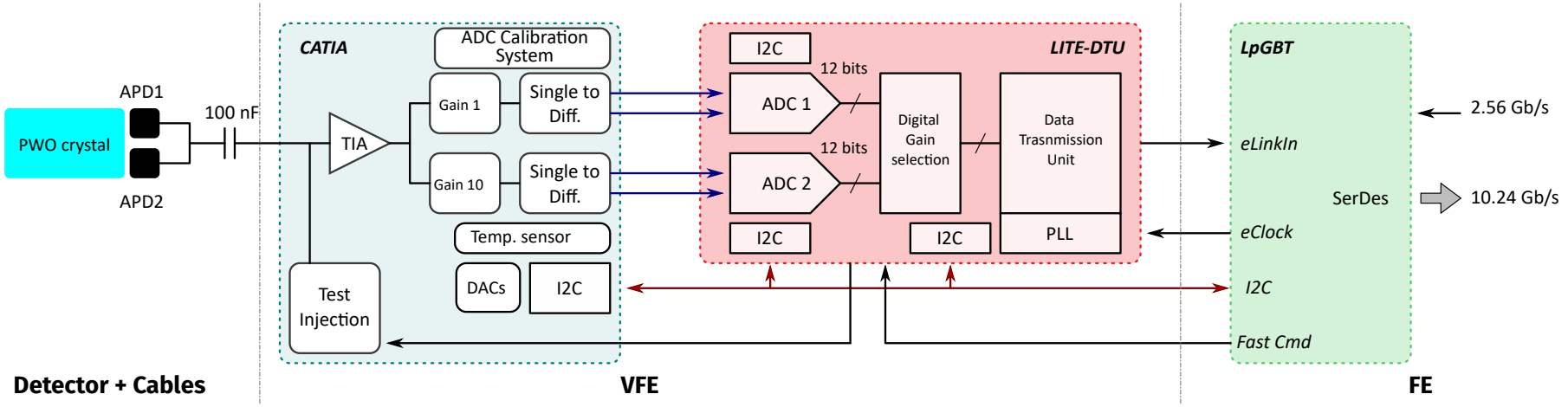
Crystal + TIA + ADC



18 ps constant term

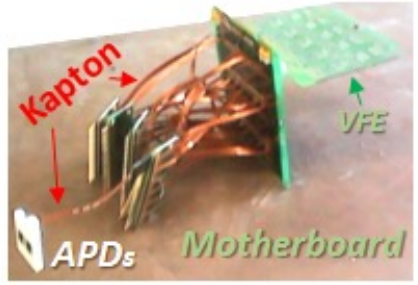
61200 readout channels of the barrel will be replaced

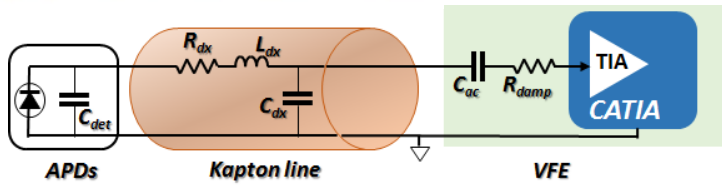
On detector Electronics



CATIA Requirements

- Input signals
  - Polarity : negative
  - Dynamic : 3(0.3) mA max. for Gain1(10)
    [43.4 pC @ 2 TeV, HL-LHC & η = 0]
- Linearity : ±1‰ INL full scale
- Energy resolution : 80 MeV intrinsic (480 µV RMS)
- Time resolution : 30 ps @ 50 GeV (full chain)
- Radiation hardness:
  - TID < 10 Mrad (with safety factor of 10)
  - NIEL < 5 10^{14} n_{eq}/cm^2 (with safety factor of 5)

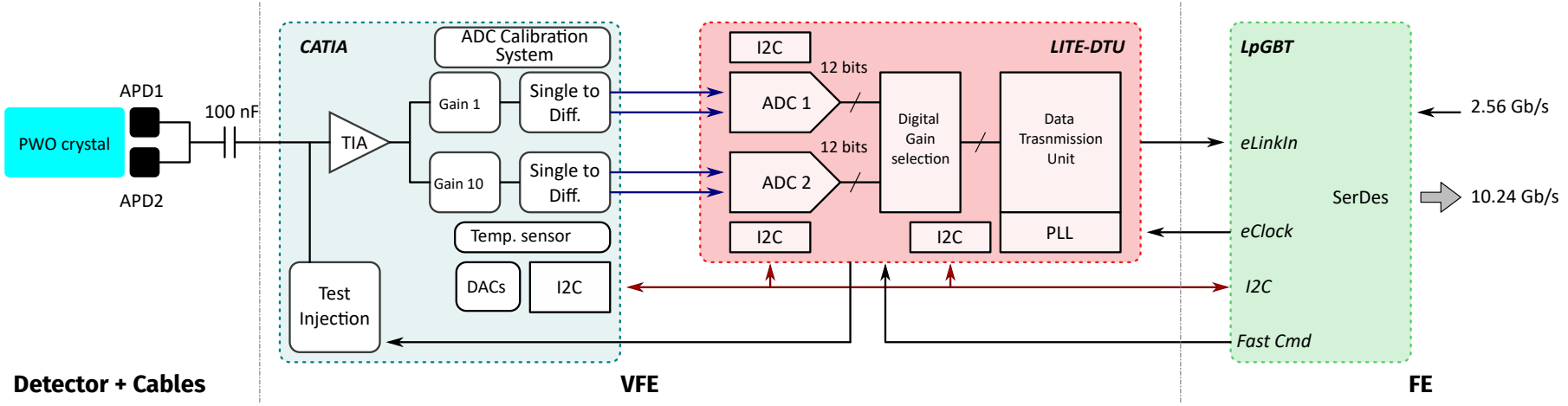




Kapton line parameters:
R_{dx} = 0.05 Ω / cm
L_{dx} = 3.75 nH / cm
C_{dx} = 2.4 pF / cm
Length: ≈ 20 cm

R serie = 20 Ω

On detector Electronics



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Control and ancillaries

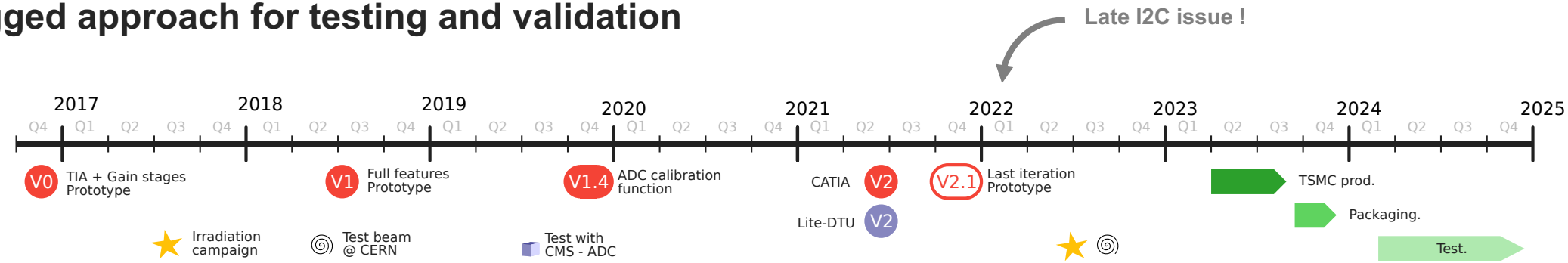
- Test pulse : Online control of gain stability and linearity
- Pedestal tuning : Optimize ADC dynamic range
- Monitoring temperature sensor
- Comply with lpGBT I2C protocol

Extra (new) features

- Provide reference voltages for ADC calibration

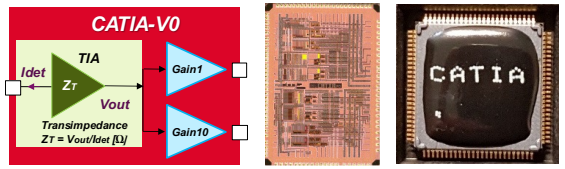
CATIA development time line

Stagged approach for testing and validation



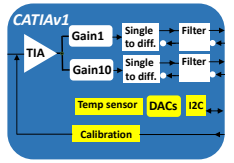
V0 : Feasibility study

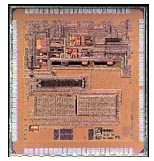
- Validate 130 nm technology, thick oxide transistors (2.5V power supply)



V1 : Full feature prototype

- V1.4 : Add Analog multiplexers on output pins to present calibration voltages for ADC calibrations





V2 : Large production (600 dies) for large scale test

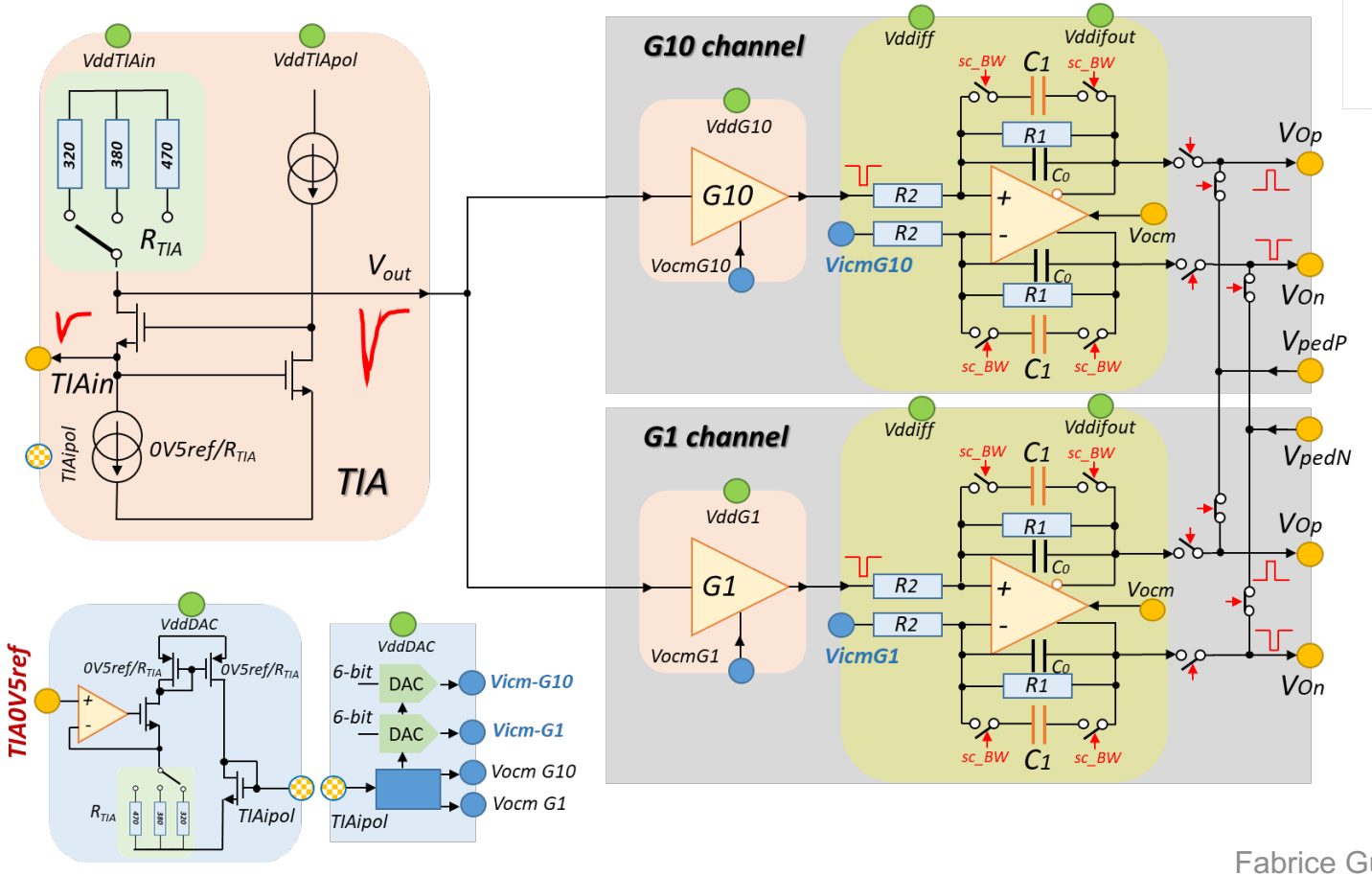
- Almost 100% Yield (1 bad chip)
- Parameter shift : the incident (never seen before, never happen after)

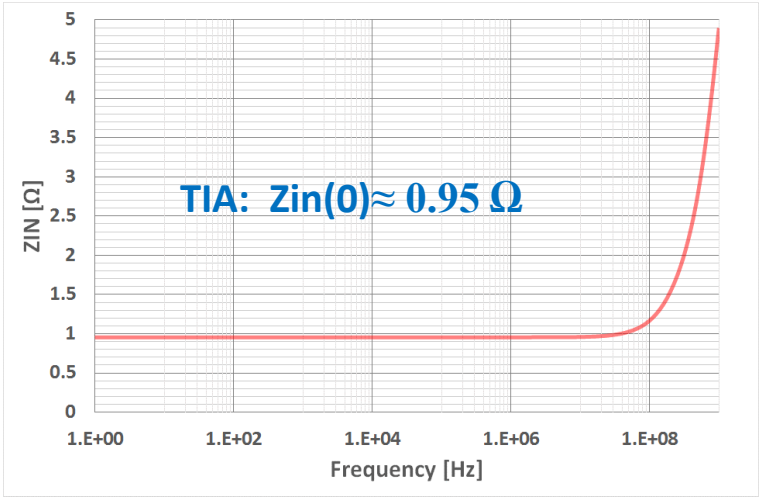
V2.2 : Production ASIC

CATIA Analogue channel

TIA: Regulated Common-Gate (RCG)

- Low input impedance compatible with $C_{det} \approx 200$ pF
- 3 gains via R_{TIA} = 320 Ω, 380 Ω or 470 Ω





G1 output

Luminosity	ileak	Resolution η = 0	ileak	Resolution η = 1.45
300 fb-1	5 µA	**196 MeV**	10 µA	**242 MeV**
4500 fb-1	80 µA	**552 MeV**	140 µA	**1223 MeV**

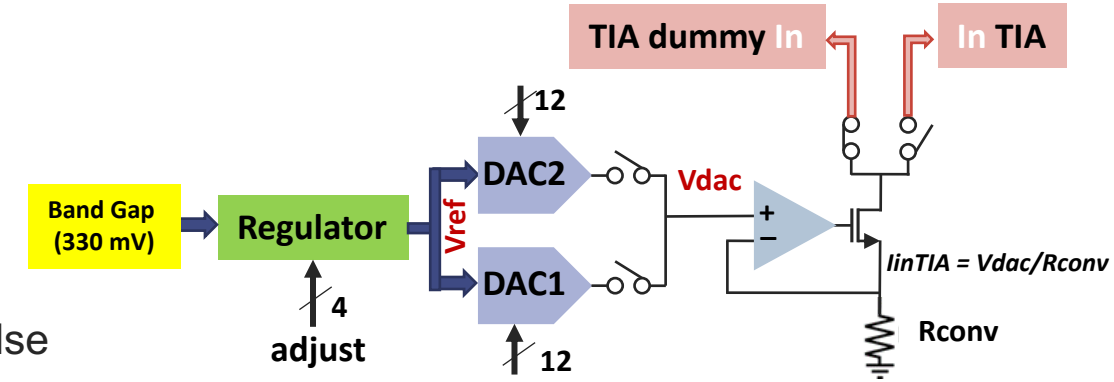
G10 output

Luminosity	ileak	Resolution η = 0	ileak	Resolution η = 1.45
300 fb-1	5 µA	**107 MeV**	10 µA	**142 MeV**
4500 fb-1	80 µA	**446 MeV**	140 µA	**1061 MeV**

CATIA internal calibration and monitoring

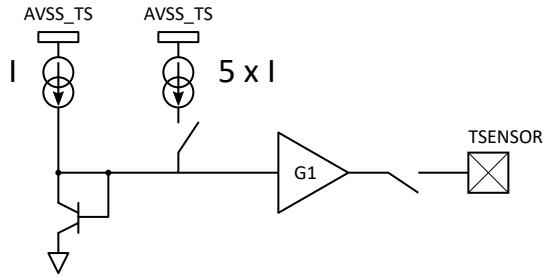
Internal Test pulse

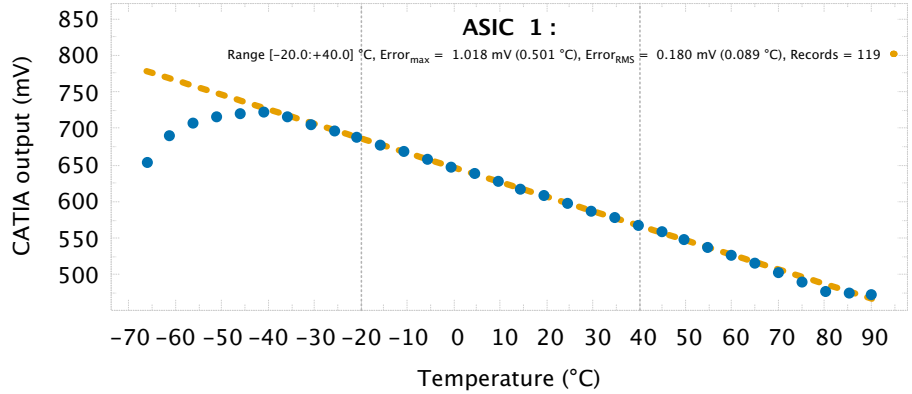
- Current source from 12 bit DACs (I_{max} = 4.2 mA; LSB = 1 µA) set by I2C.
- Current injection : INL far better than ±1‰ (0.3 ‰ from sim.)
- CATIA requires LVCMOS12 trigger to generate internal test-pulse
  - Should be synchronous signal to be interleaved in LHC data taking
  - Use Fast command (Decoding and trigger generation in LiTE-DTU)
  - Test pulse width tuned by I2C in LiTE-DTU



Temperature sensor

- Current source from bandgap
- Measured Error :
  - 0.5°C with offset calibration





I2C (“event. Driven”, no external clock)

CATIA for LiTE-DTU calibration

Requirements

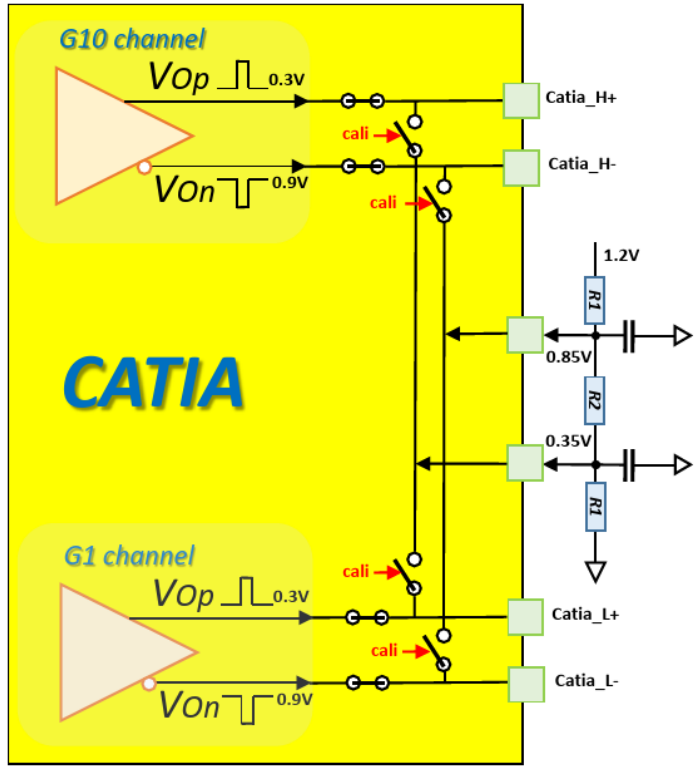
- ADC requires 2 stable DC voltages at 350 mV and 850 mV during calibration process
-

CATIA (≥ V1.4) implements 2 scenarios

- ~~Enhanced pedestal setting range up to 350/850 mV~~
- Analogue multiplexer on CATIA output stage to present externally built calibration voltages.

Calibration voltages built from CATIA internal BandGap

- Vref on chip level tuning possible with I2C
- Vref on (existing) temperature sensor line
- Use lpGBT ADC to check value/stability



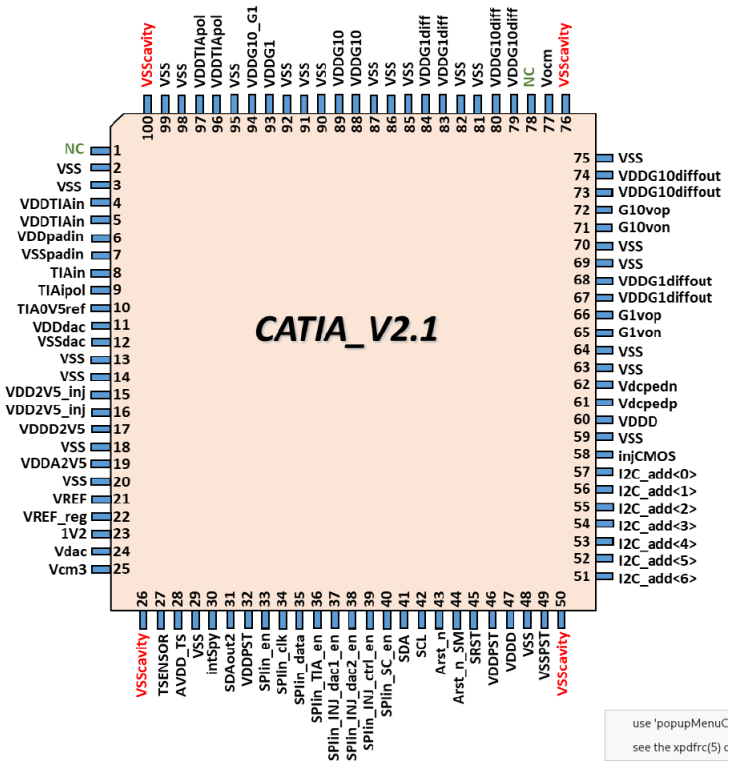
CATIA power and packaging

Power consumption

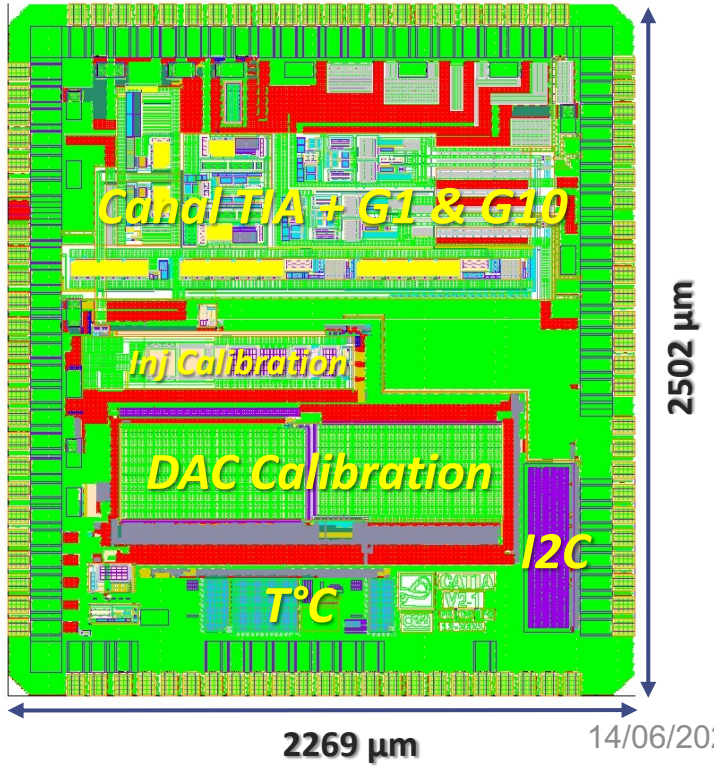
Description	Current @ 2.5V	Current @ 1.2V
TIA	19 mA	
G1	14.2 mA	13.4 mA
G10	14.2 mA	13.4 mA
T° & Calibration	2 mA	270 µA
Total	**49.4 mA; 123.5 mW**	**27 mA; 32.5 mW**

Packaging

- 100-pin LQFP:
  - 14 mm x 14 mm
  - 0.5mm of pitch



Layout V2.1



CATIA standalone results

APD stimulation with a laser

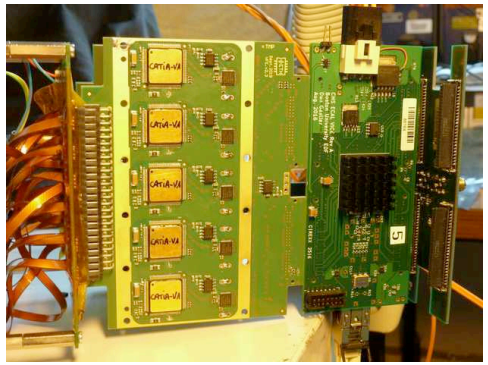
- Measured bandwidth = 35 MHz
- Rise time (10-90 %) = 6.25 ns

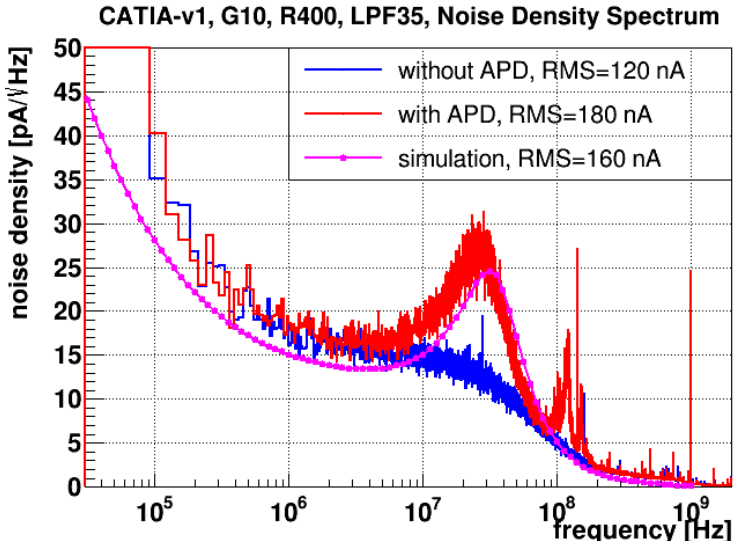
Linearity with internal TP

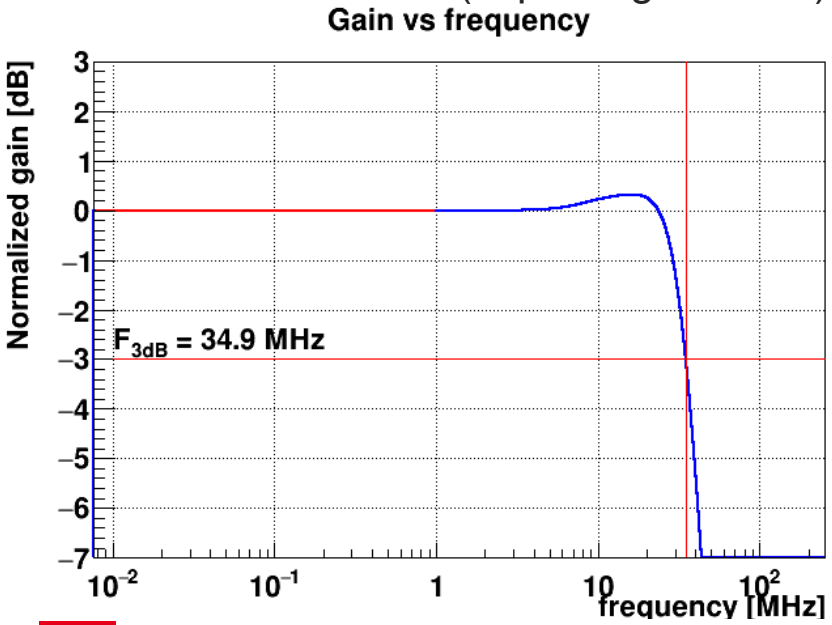
- INL < +/- 1/1000

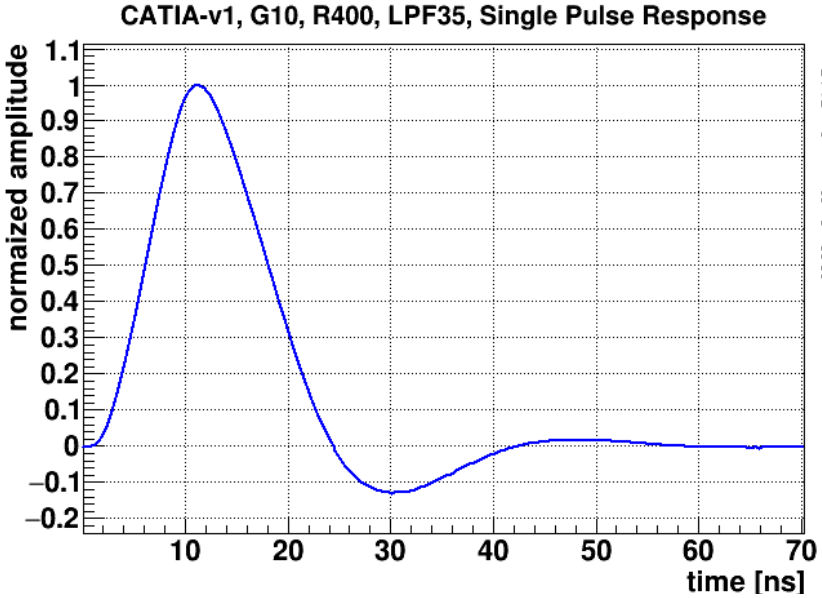
Noise

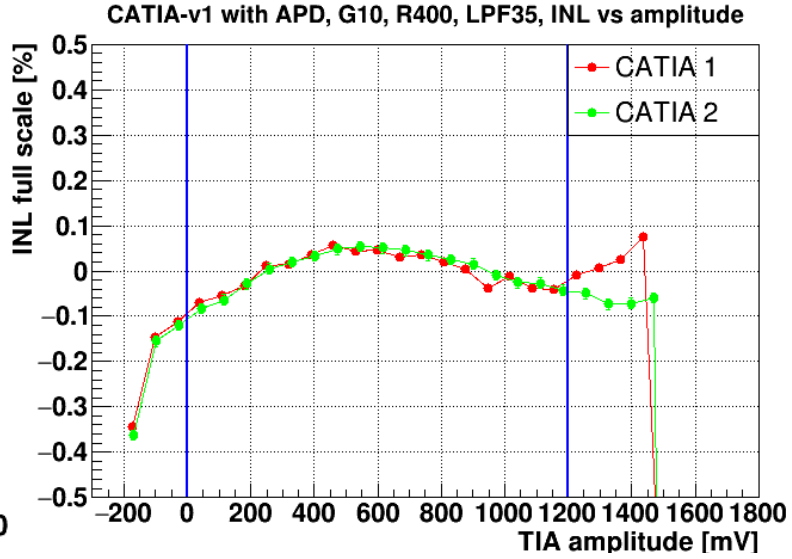
- RMS: 180 nA (expecting: 170 nA)











CATIA irradiation tests

TID hardness (photons) studied at Saclay (Pagure*) on Feb 2020

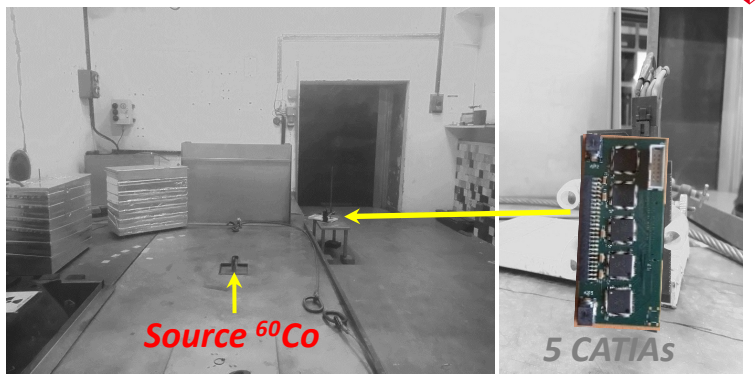
- Dose up to 140 kGy (14 Mrad)
- Every thing stable except Temperature Sensor (-0.5°C/Mrad)

Neutron hardness studied at Ljubljana

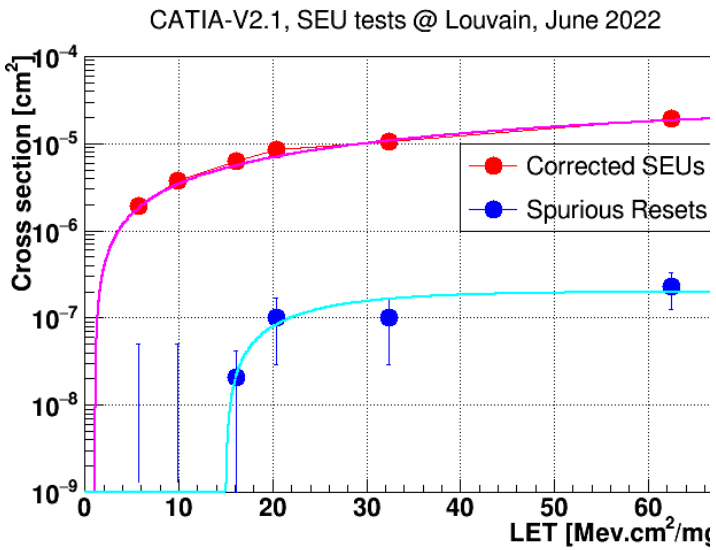
- April 2021: up to $5x10^{14}$ n_{eq}/cm^2 ➔ No significative change measured
- June 2022: up to $5x10^{16}$ n_{eq}/cm^2 ➔ Every thing stable except Temperature Sensor

SEU hardness studied

- HIF Louvain (September 2019 – June 2022)
  - Up to 70 MeV/(mg/cm2), no SEL seen
  - No register corruption seen, SEU correction by triplication works well, spurious reset SET →
- Proton (60 MeV) irradiation at Nantes (Arronax) (09 and 10/2022)
  - Corrected SEUs seen as expected, no register corruption
  - First run : No reset seen with 5 hours-equivalent of HL-LHC on whole ECAL (η=1.5)
  - Second run : 2 resets seen with 21 hours-equivalent of HL-LHC on whole ECAL



14 Mrad (140 kGy) in 3 weeks

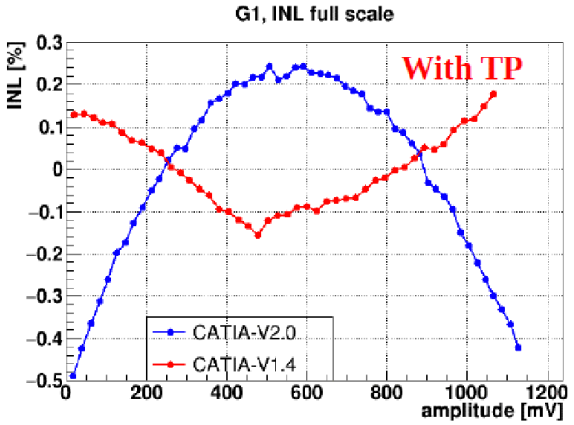


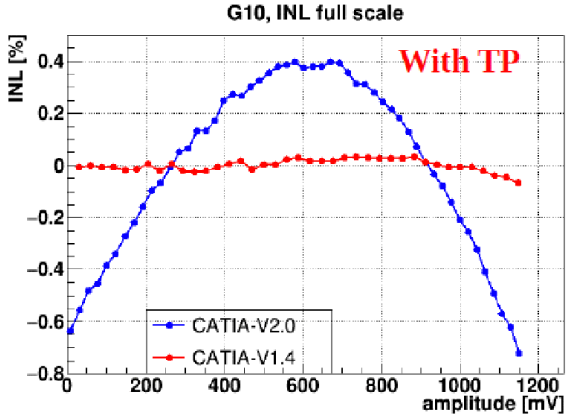
CATIA V2.0 anomalies

Problem description (measurements of all 600 chips):

- Current over-consumption greater than + 20 mA
- Signal shape changed
- Worst linearity for both gains

	SIMU	V1.4	V2.0	V2.1
TIAin	521 mV	534 mV	295 mV	518 mV
TIAipol	947 mV	862 mV	690 mV	933 mV

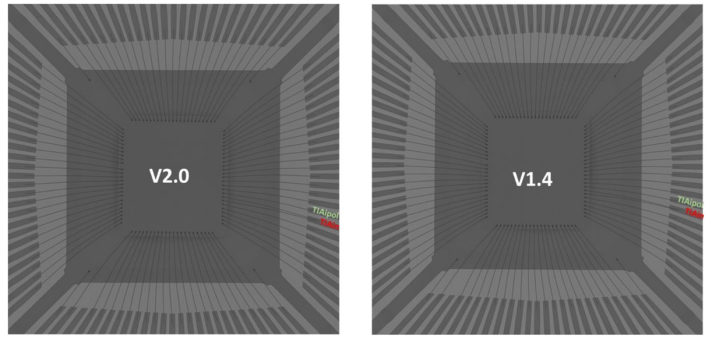




** TP: Test Pulser*

Outlook hypothesis

- First Hypothesis: process parameters
  - This abnormal behavior cannot be confirmed by a simulation (Worst case analysis 78 mA to 101 mA (mean: 88 mA))
  - We analyzed the measured parameters of TSMC for this run compared to those of the V1.4 run
    - The only difference concerns the resistance values which are much lower in this run
- Second Hypothesis: functionality problem
  - The X-ray analysis of the package did not detect any failure in the bonding
- Third Hypothesis: oxide thickness



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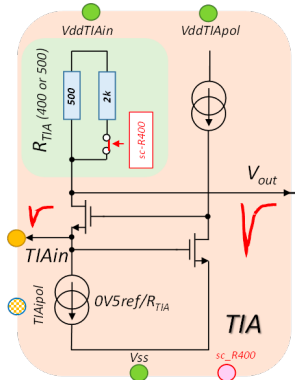
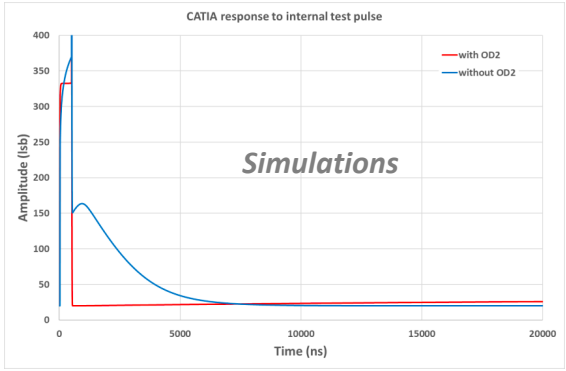
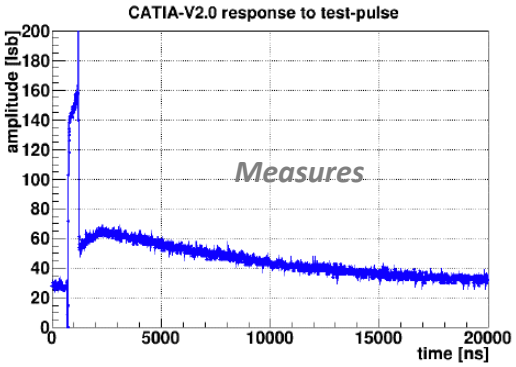


- Third Hypothesis: The hypothesis is to consider that the technological mask OD2 (No. 132) defining the thick oxide is missing.

	SIMU with OD2	SIMU without OD2	V2.0
TIAin	521 mV	355 mV	295 mV
TIAipol	947 mV	603 mV	690 mV

Without OD2, DC points from simulations are closer to measurements





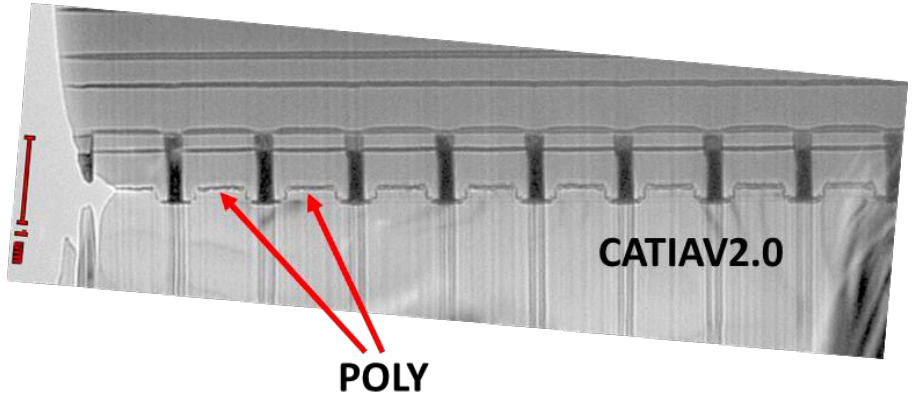
Without OD2, signal shape is reproduced

Oxide thickness measurement by Transmission Electron Microscopy analysis

- 2 slices position (NMOS and PMOS transistors)
  + 2 ASIC versions

	Slice 1 (nm)						Expected Slice 1 (nm) NMOS standard Vt
V1.4	5.7	5.7	5.6	5.6	5.5	5.6	5.83 +/- 0.15 (thick oxide)
V2.0	5.3	5.3	5.2	5.3	5.2	5.2	Hypothesis: 2.81 +/- 0.019 (thin oxide)

  - This analysis does not confirm the hypothesis of mask missing



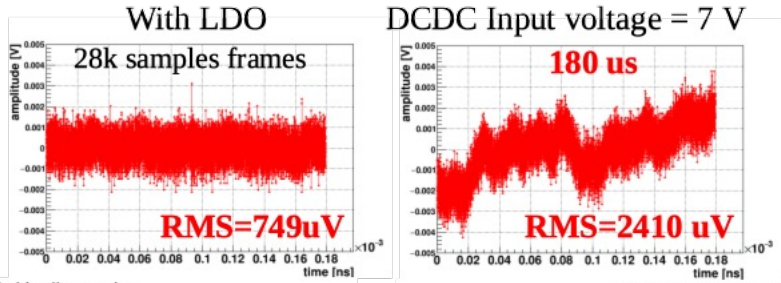
CERN consulted for expert reviews

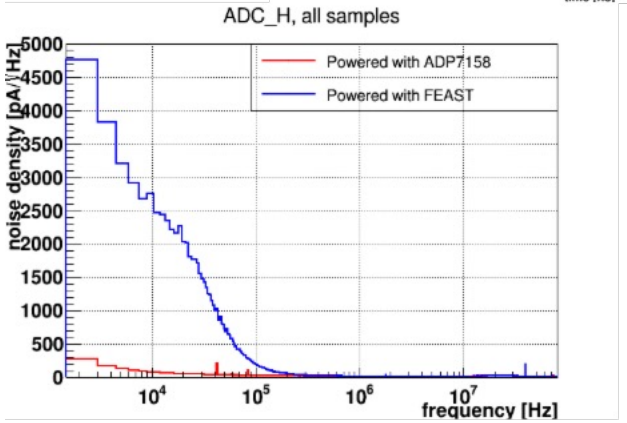
- Other hypothesis investigated do not give an answer. Only one difference remains: CATIA V2.0 was manufactured at FAB 14

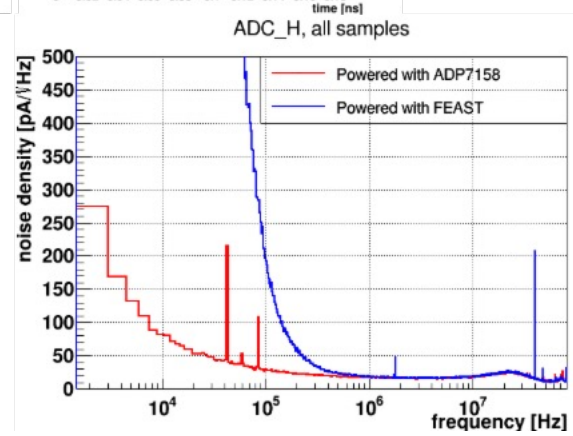
CATIA-V2.1 + LiTE-DTU-V2.0 : PSRR 1/2

Impact of full system

- VFE powered with LDO
- VFE powered with FEAST (DCDC)

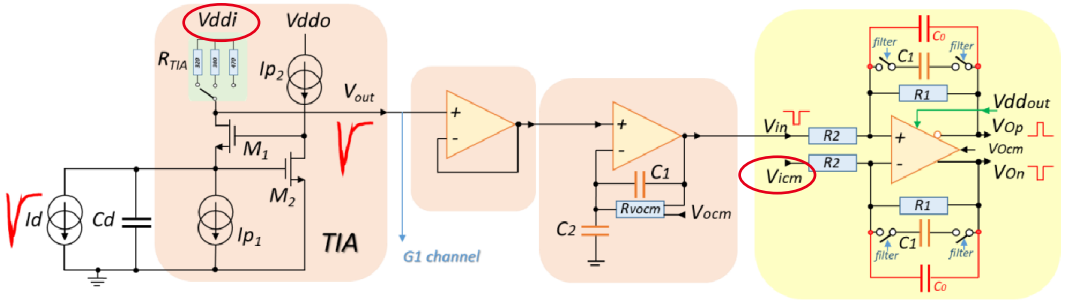






Weak point identification

- TIA power supply



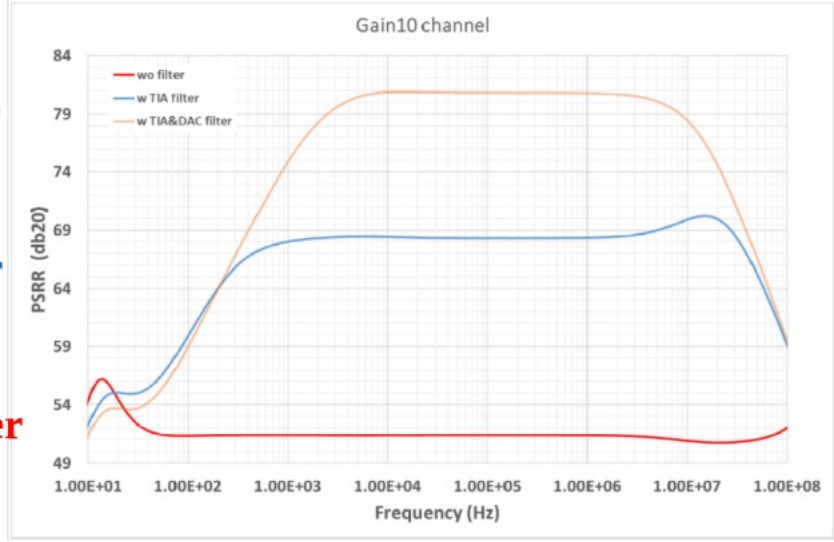
From simulation

- Extra filtering needed !

Plus VDD_{DAC} filter

With VDD_{TIA} filter

Without extra filter



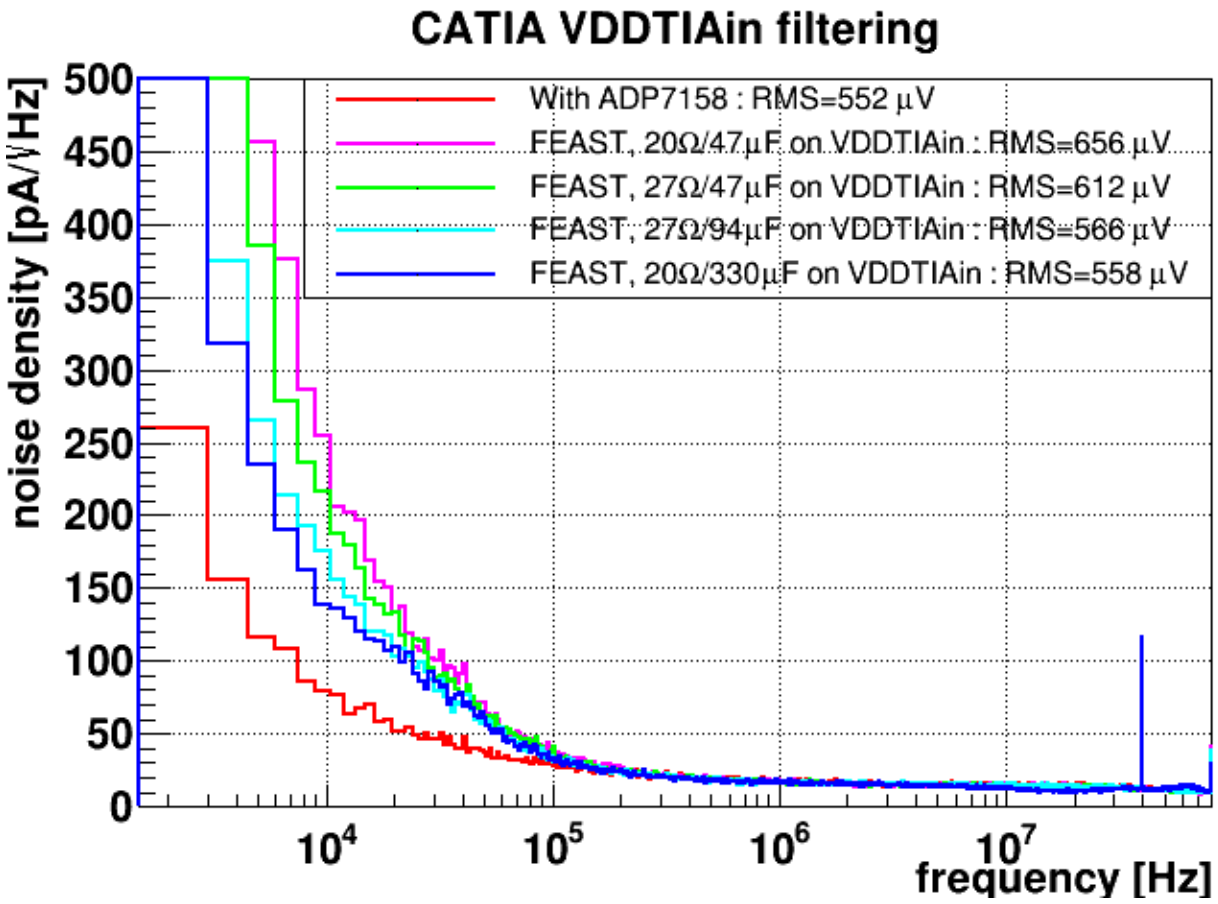
CATIA-V2.1 + LiTE-DTU-V2.0 : PSRR 2/2

Optimize filter on CATIA and LiTE-DTU power pins

- With 10 Ω/22 µF on LiTE-DTU VDDref_H/L
- With 5 Ω/47 µF on CATIA VDD_{DAC}
- With 47 Ω/ 2x47 µF on CATIA VDD_{TIA}

LDO :
RMS = 552 µV

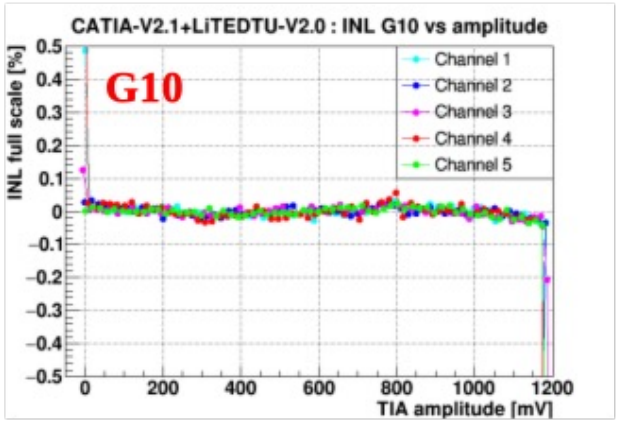
DCDC + filtering :
RMS = 558 µV

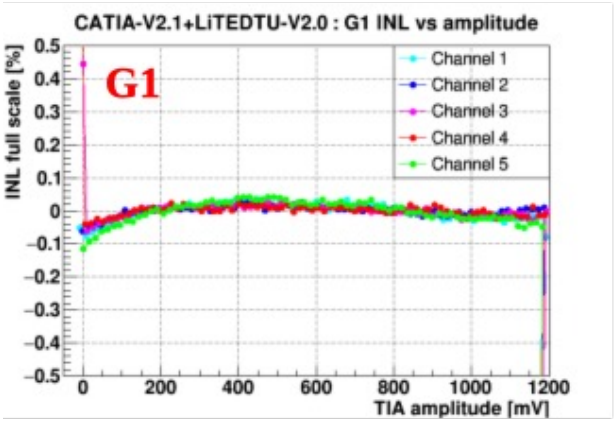


CATIA-V2.1 + LiTE-DTU-V2.0 : Linearity and Distortion

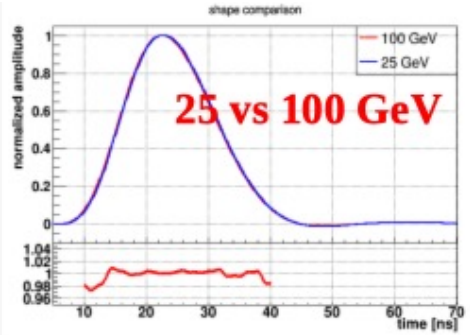
Pulse shape stability mandatory for “template fit” algorithm

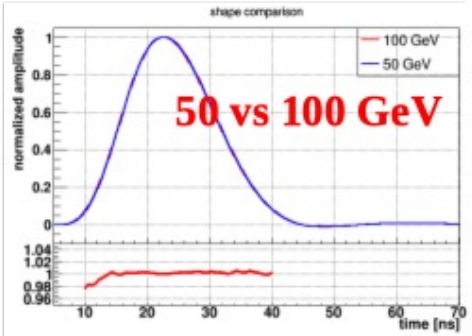
Good linearity mandatory for physics analysis

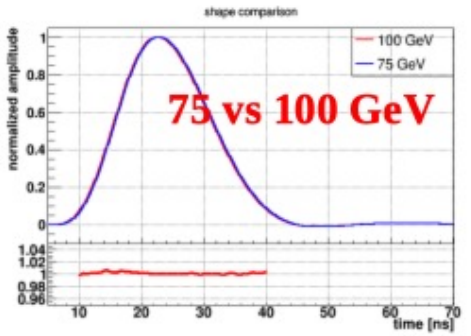


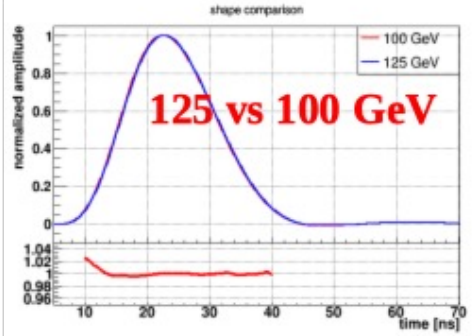


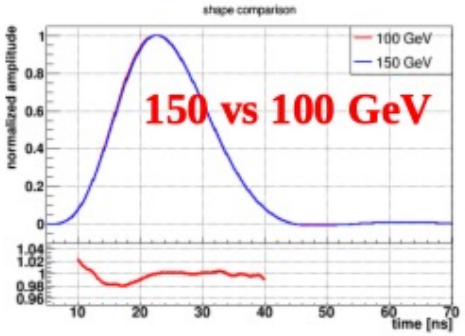
CATIA-V1.1@TB





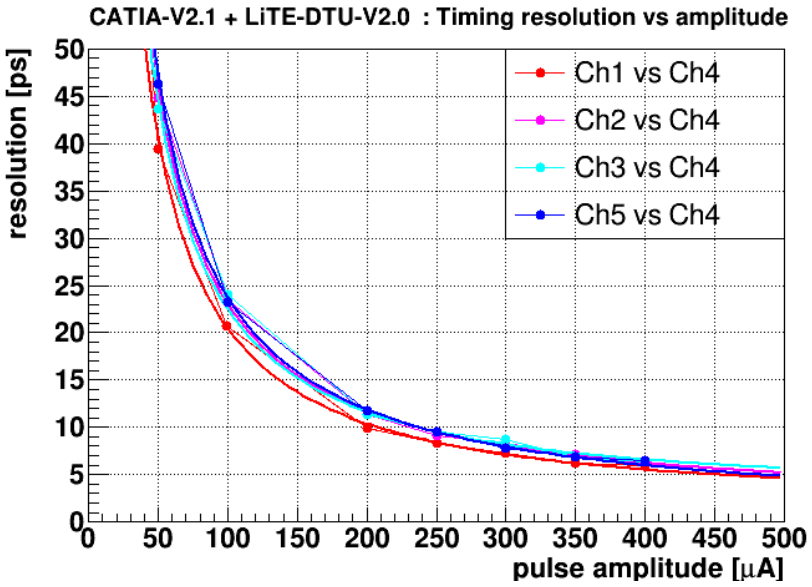




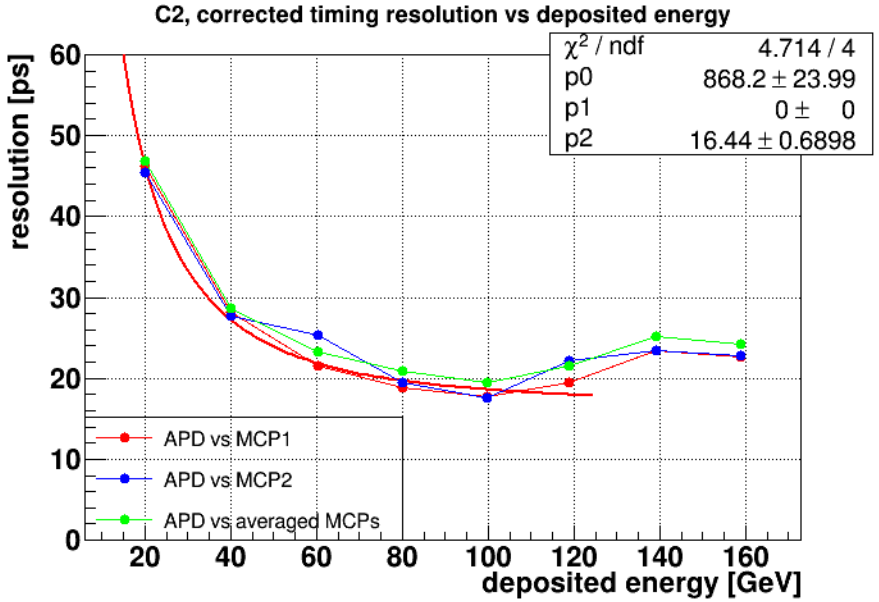


CATIA-V2.1 + LiTE-DTU-V2.0 : Intrinsic Timing Performances

Lab timing resolution vs energy



Overall timing resolution vs energy



Summary

End of long sequence of developments, tests and improvements

- Version 2.1 is THE candidate for final production
  - No major changes foreseen
  - Fine tuning of resistor values to increase Vref setting precision (no design change)

- All parameters and performances conform to requirements and specifications
  - Gain, linearity, noise, bandwidth, radiation hardness

- Remaining weak point
  - V2.0 incident

Ready for production

- Engineering run with RAFAEL in ~~03/2023~~ → 05/2023


Merci

CATIA V2.0 anomalies

Oxide thickness measurement by TEM analysis: Slice 1