The HGCROC for CMS high granularity calorimeter

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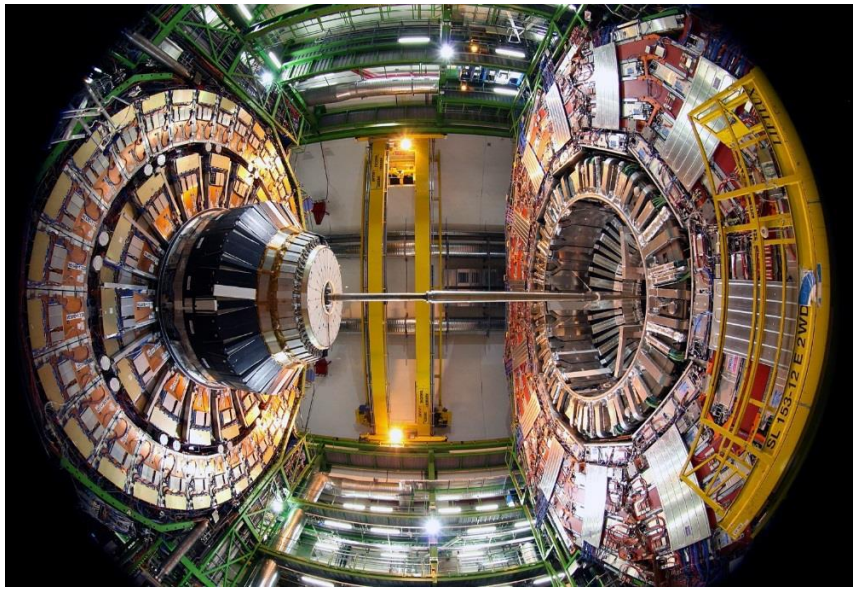
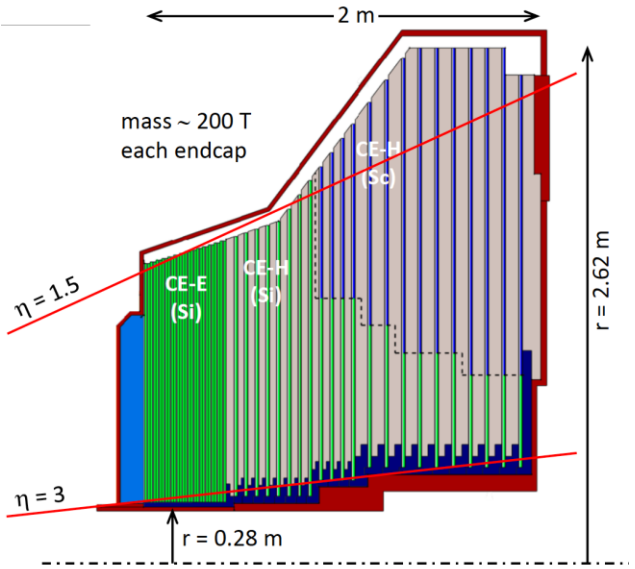
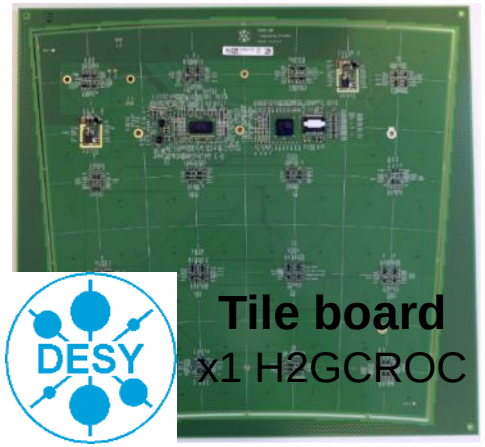
Organization for Micro-Electronics desiGn and Applications

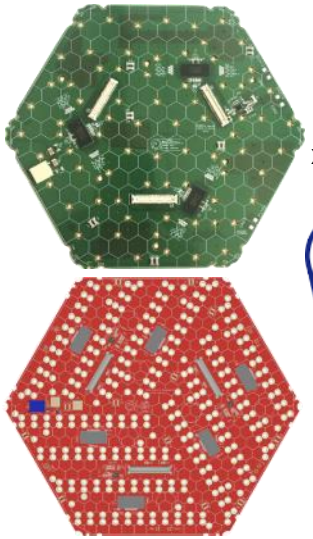
HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade

- **HGCAL covers 1.5 < eta < 3.0**
- Full system maintained at -30°C
  - ~ 640 m² of silicon sensors, 6.1M Si channels, 0.5 or 1.1 cm² cell size
  - ~ 370 m² of scintillators, 240k scint-tile channels
- Data readout from all layers
- Trigger readout from alternate layers in CE-E and all in CE-H
- Active Elements
  - Electromagnetic calorimeter (CE-E): Si, Cu/CuW/Pb absorbers
  - Hadronic calorimeter (CE-H): Si & scintillator, steel absorber
- New Front-end electronics
  - Two versions: Silicon and SiPM
  - Rad.tolerant (200 Mrad, 1.1016 neq / cm²)
  - Power consumption: 15 mW per channel
  - Noise: 0.4 fC
  - Charge: 0.2 fC to 10 pC
  - Pileup mitigation: Fast shaping (peak < 25 ns), precise timing capability (25 ps)





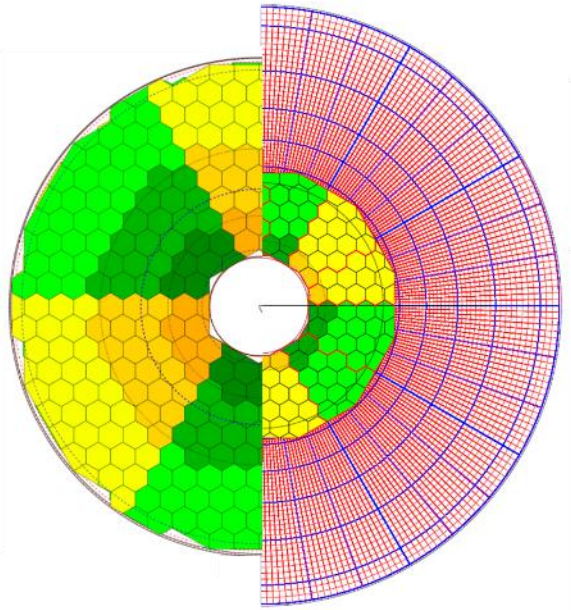




LD HB
x3 HGCROC

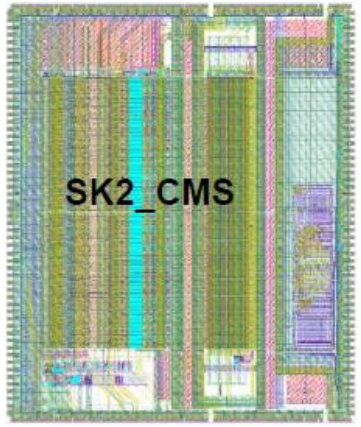
CERN

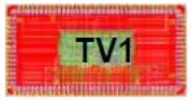
HD HB
x6 HGCROC

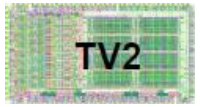


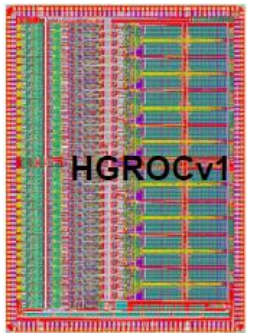
Development history

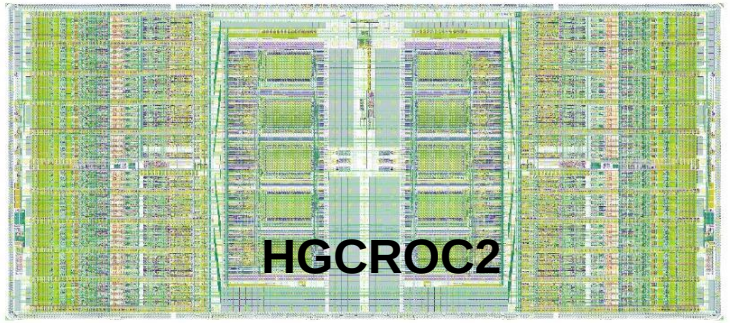
- Jan 16: SKIROC2_CMS [TWEPP 2016]
  - SiGe 350 nm 7x9 mm²
  - Dedicated to test beam and analog architecture (TOT)
- May 16: 1st test vehicle TV1
  - CMOS 130 nm 2x1 mm²
  - Dedicated to preamplifier studies
- Dec 16: 2nd test vehicle TV2 [TWEPP 2017]
  - CMOS 130 nm 4x2 mm²
  - Dedicated to technical proposal analog channel study
- July 17: HGCROCv1 [TWEPP 2018]
  - CMOS 130 nm 5x7 mm²
  - **Wire bonds**
  - All analog and mixed blocks; large part of digital blocks
- Feb 19: HGCROC2 [CHEF 2019, IEEE 2020, TIPP 2021]
  - CMOS 130 nm 15x6 mm²
  - **Bump bonds**
  - Silicon and SiPM versions (for both 2 and 2A)
  - Final size, packaging and I/Os
- Dec 20: HGCROC3 [TWEPP 2021, IEEE 2021]
  - CMOS 130 nm 15x6 mm²
  - **Bump bonds**
  - Silicon and SiPM versions
- June 23: HGCROC3b
  - CMOS 130 nm 15x6 mm²
  - Pre-production

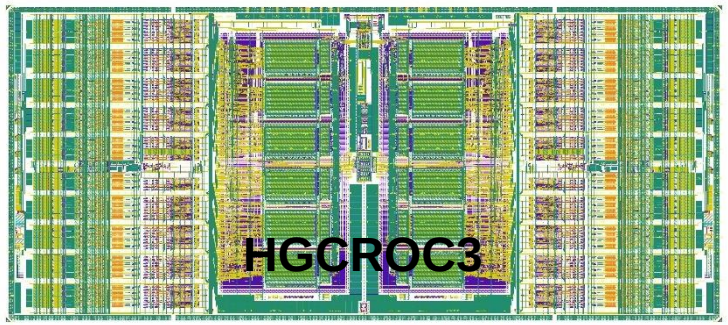


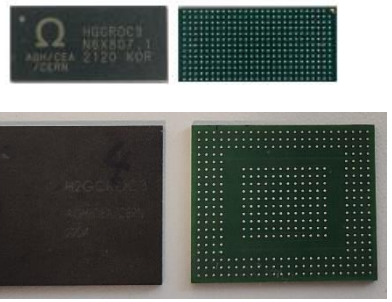












High Density (HD) and Low Density (LD) packages

HGCROC3 overview

Overall chip divided in two symmetrical parts

- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

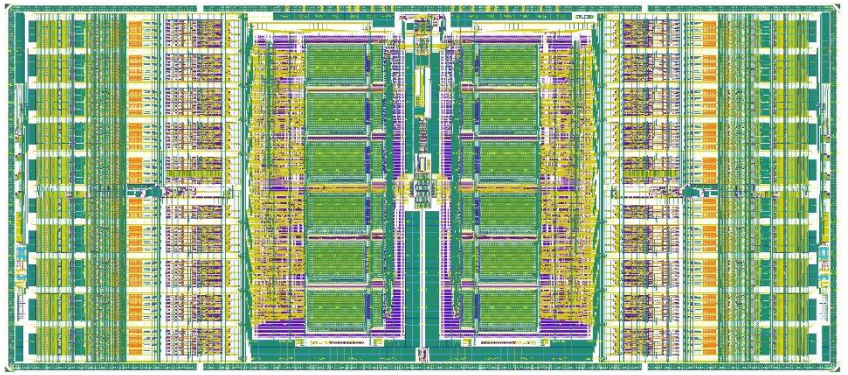
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links

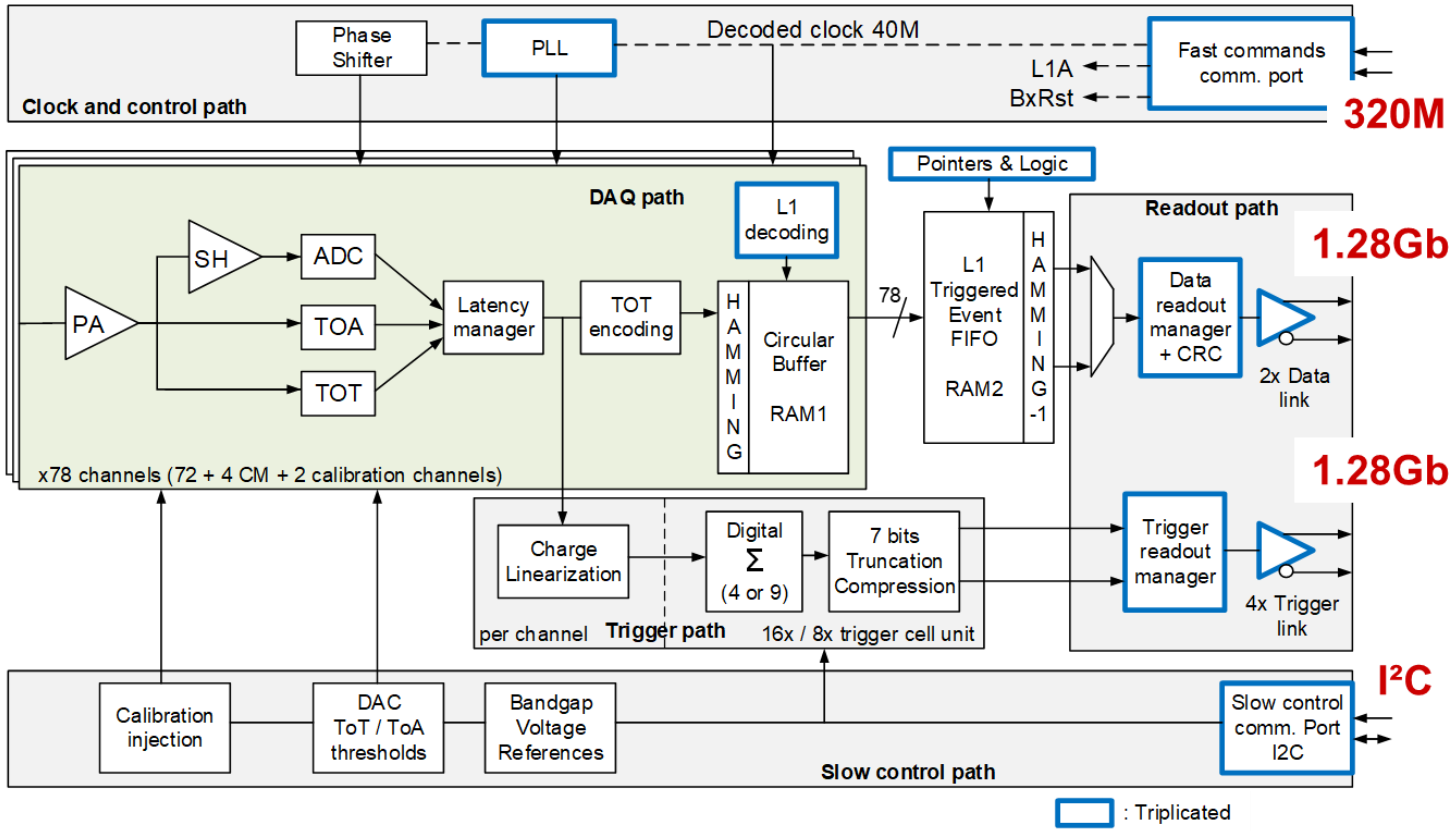
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

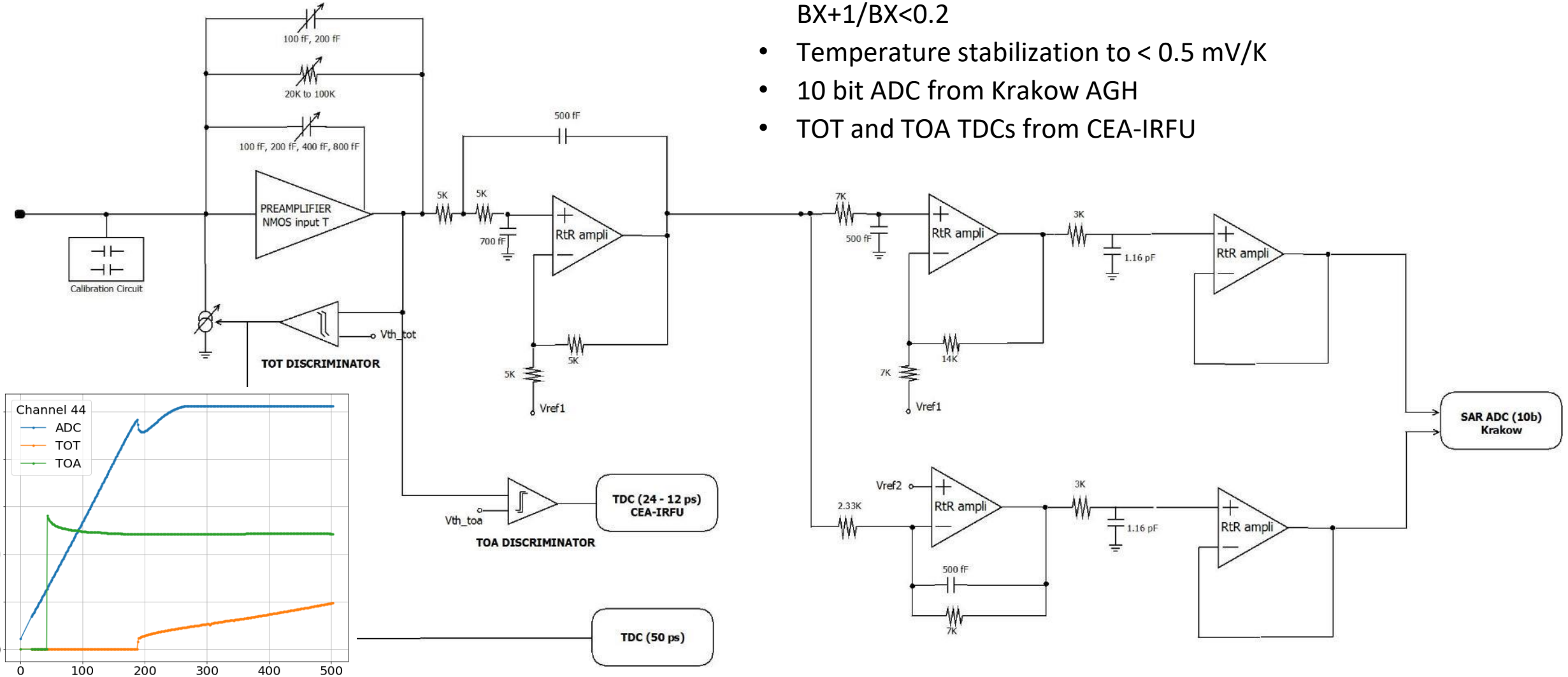
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain





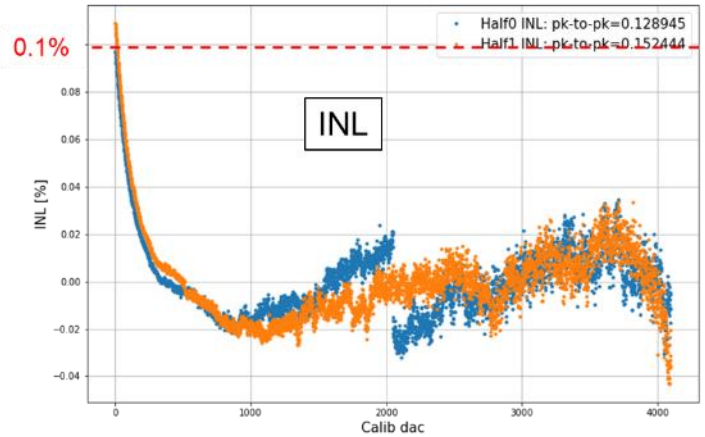
Analog Channel Overview (Silicon version)

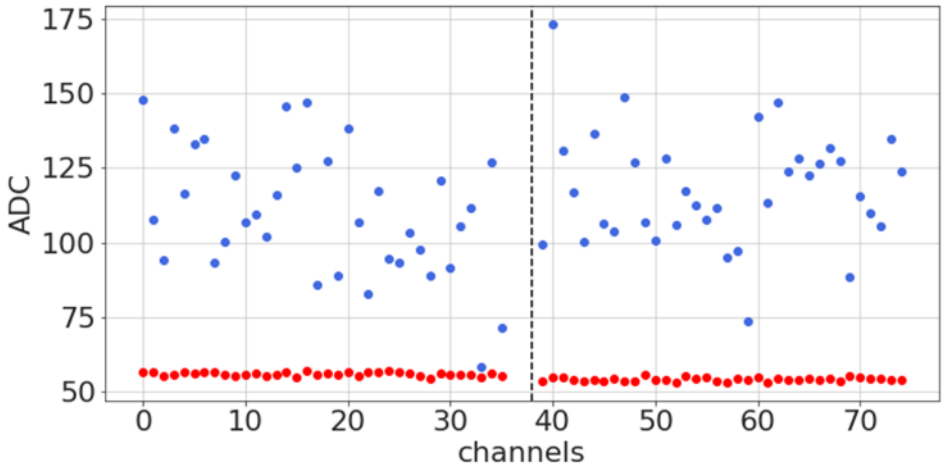
- Calibration pulser, 0.5pF and 10 pF calibration cap.
- Preamp : adjustable gains for 80, 160 and 320 fC ranges
- Tunable TOT over 5 bits
- Compensation for the leakage current, 50 µA max. (not shown in the figure)
- Sallen Key shaper RC4, tp<25 ns, tunable (~20%) with 2 bits, BX+1/BX<0.2
- Temperature stabilization to < 0.5 mV/K
- 10 bit ADC from Krakow AGH
- TOT and TOA TDCs from CEA-IRFU

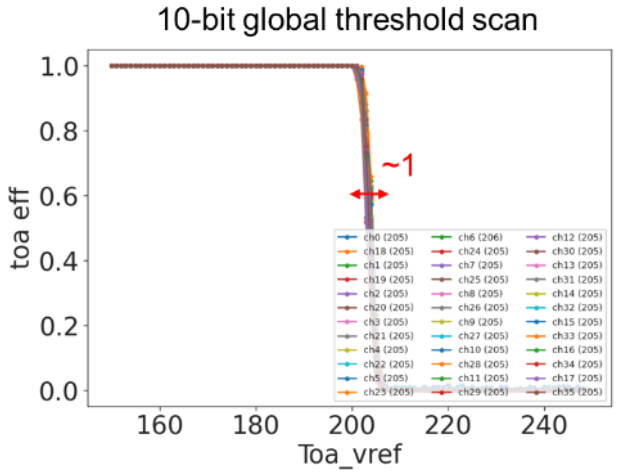


DACs & trimming

- 12 bits calibration DAC
  - ~ 2-3 mV offset due to leakage current (1 – 1.5 fC)
  - < 0.1 % linearity, temperature sensitivity: 60 ppm/K, stable after 350 Mrad
- Four 10-bit DACs to set pedestals, TOA & TOT thresholds + 3 channel-wise 6-bit DACs to reduce dispersion per channel
  - Pedestals: ~ 3 ADC counts dispersion after trimming, TOA & TOT thresholds: 1-2 DAC counts after trimming
- 8-bit input DAC to compensate for the leakage current up to 45µA
  - Additional noise as expected from simulation

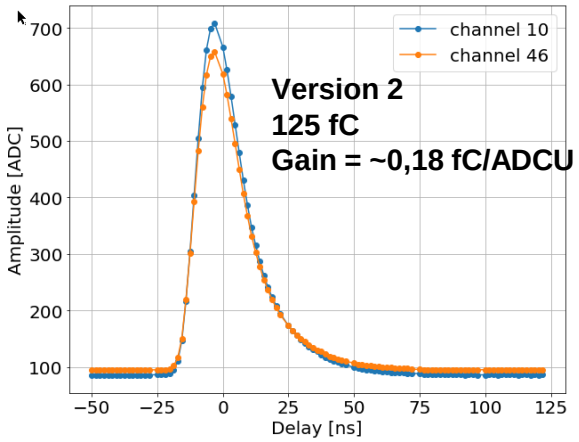




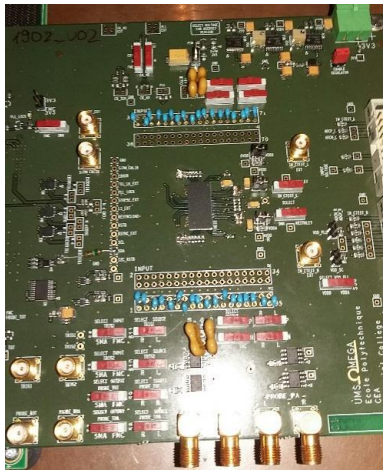


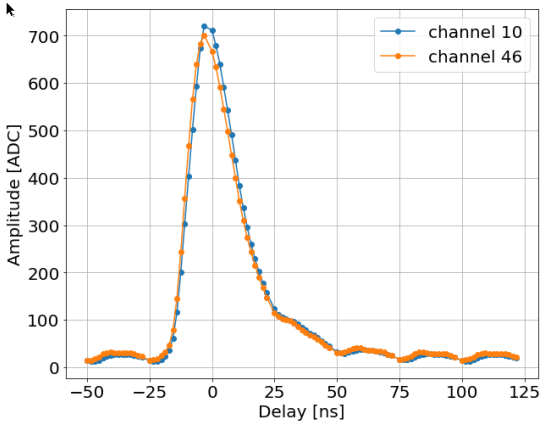
Test boards and signal

Flip-Chip on mezzanine

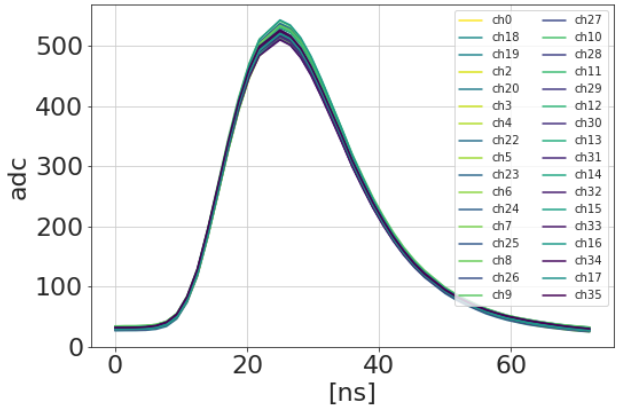


HD BGA board





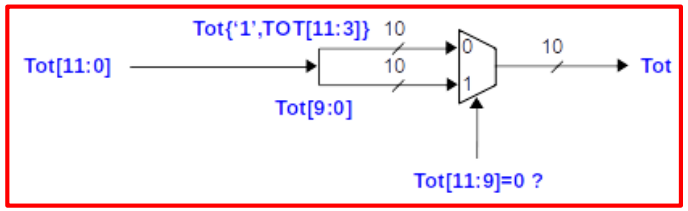
HD BGA on mezzanine

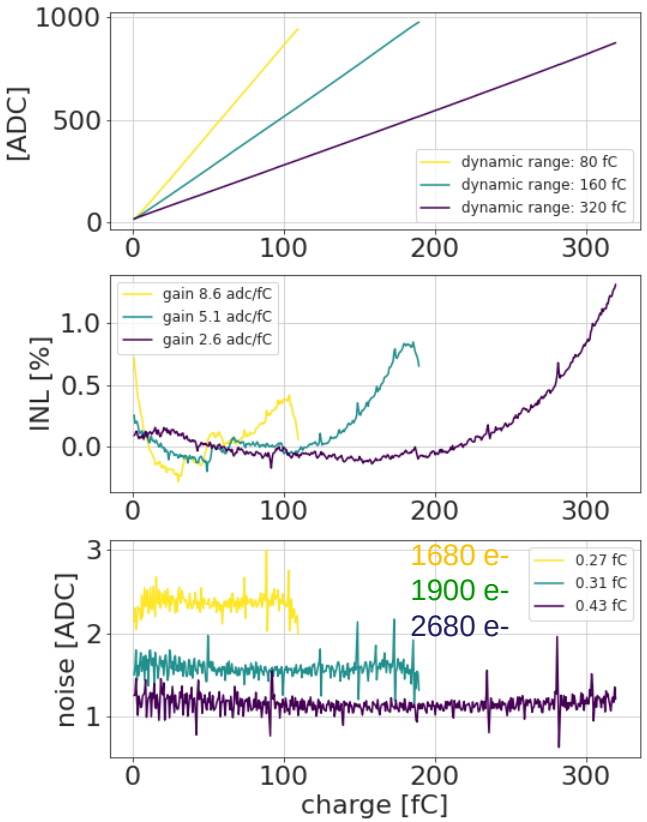


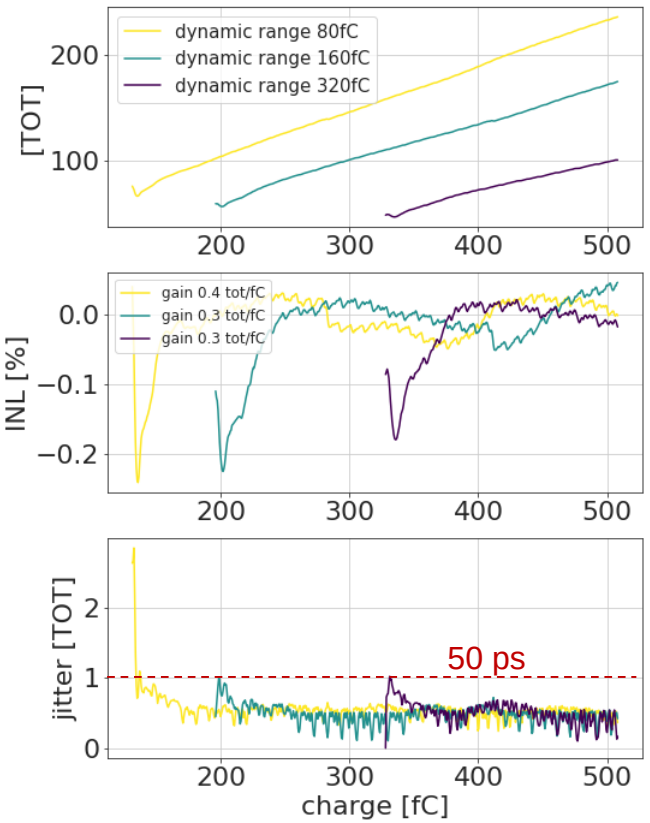
- Separates effects from the BGA substrate and PCB
- Rising time (10-90 %): ~ 15 ns
- Falling time (10-90 %): ~ 30 ns, < 20 % at BX+1
- Good uniformity over the channels
- Digital 40 MHz clock coupling on the analog inputs

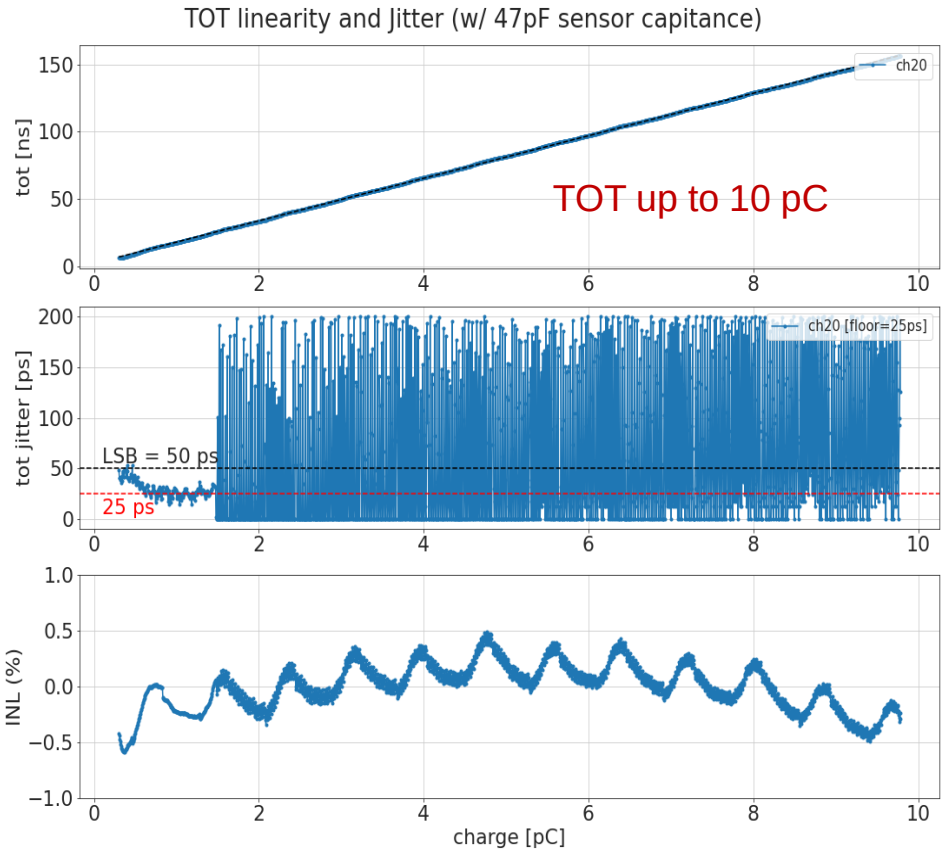
Charge

- ADC range
  - Linearity in +/- 0.5 %
- TOT range
  - Linearity in +/- 0.5 %
  - Jitter around 25 ps (50 ps binning)
  - TOT 12-to-10 compression visible on the jitter
- Crosstalk: ~ 1-2% with internal injection (positive), < 0,2% with external injection from pulse (negative)









Noise

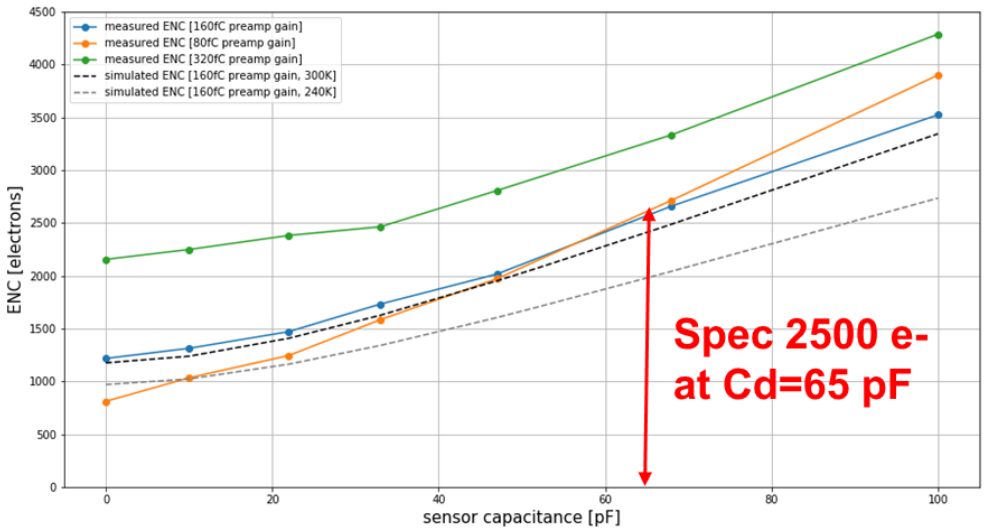
- Measured noise with 50 pF input cap: < 0.3 fC (< 2000 electrons)

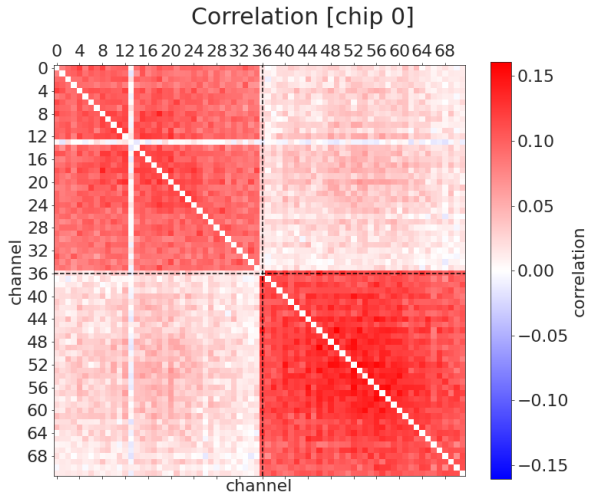
$$ENC^2(C_d) - ENC^2(0) = \sim 3E^4 * e_n^2 \frac{(C_d^2 + C_d * C_{pa})}{t_p} \quad (t_p = 18\,ns)$$

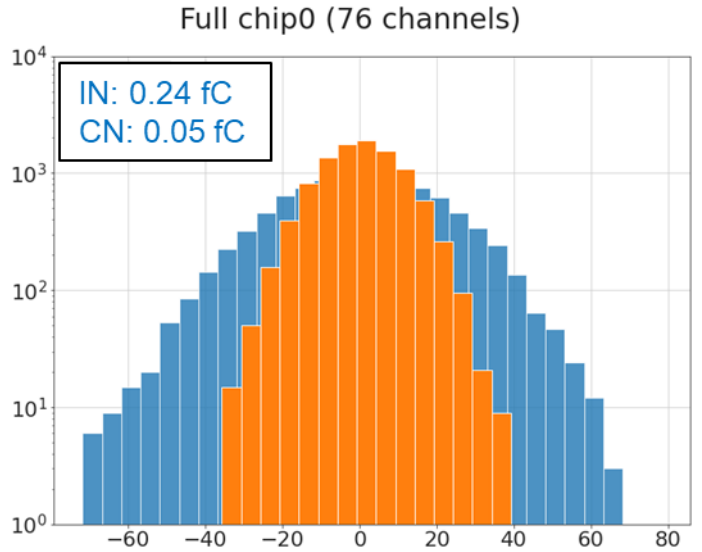
  - Series noise extracted as e_n = 0.79 nV/√Hz and C_{PA} = 12.6 pF (simulation gives 0,75 nV/√Hz and 11 pF)
  - Preamp contributes to ~75% to total noise
- Very low correlated noise contribution: ~ 0.05 fC
- Coherent noise extracted by comparing direct and alternate sums on n channels (n = 72):

$$DS = \sum ped[i]\,;\, AS = \sum(-1^i)ped[i]$$

  - Incoherent noise $IN = rms(AS)/\sqrt{n}$
  - Coherent noise $\mathrm{CN} = \sqrt{var(DS) - var(AS)}/n$







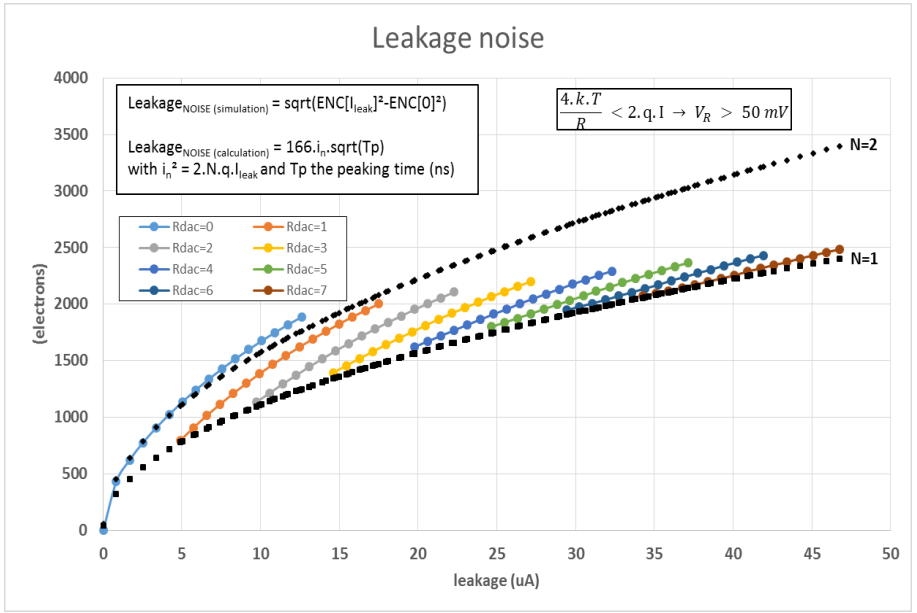
Coherent noise extracted by comparing Direct and Alternate Sums on n channels :

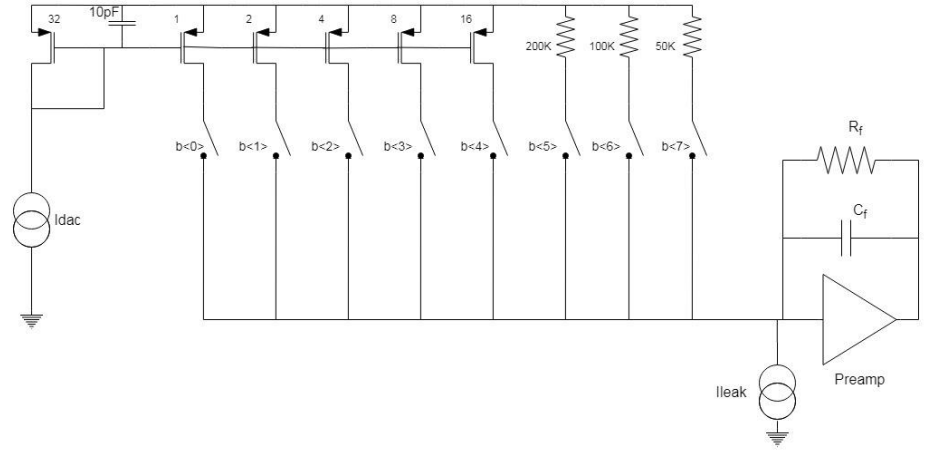
$DS = \sum ped[i]$ and $AS = \sum(-1^i)ped[i]$

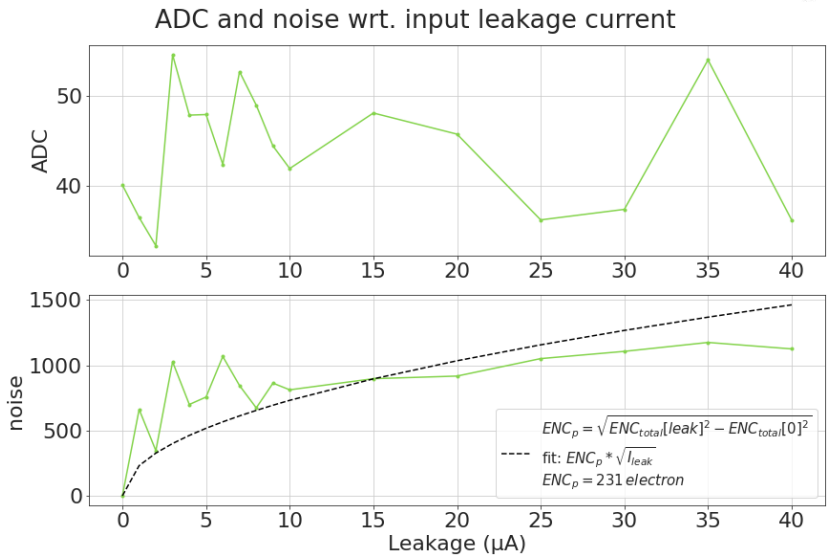
$\mathrm{IN} = \frac{rms(AS)}{\sqrt{n}}$ and $\mathrm{CN} = \frac{\sqrt{(var(DS) - var(AS)}}{n}$

Extra noise due to Leakage current

- After irradiation, the sensor cell is expected to leak up to 50 µA
- Need to compensate for maintaining full dynamic range
  - I-Dacs: $ENC^2 = A*2*I_{leak}$
  - R-dacs: $ENC^2 = A*I_{leak} + A*4kt/R$
    - At 10 µA leakage, 1550 electrons vs. 1000 electrons



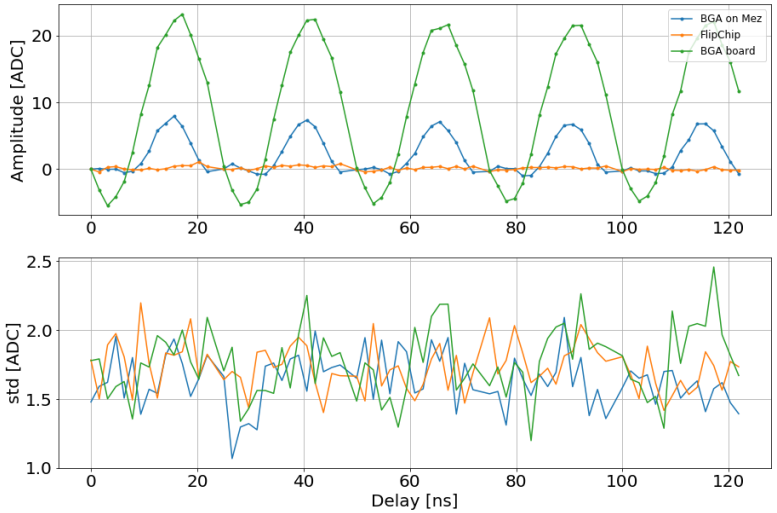


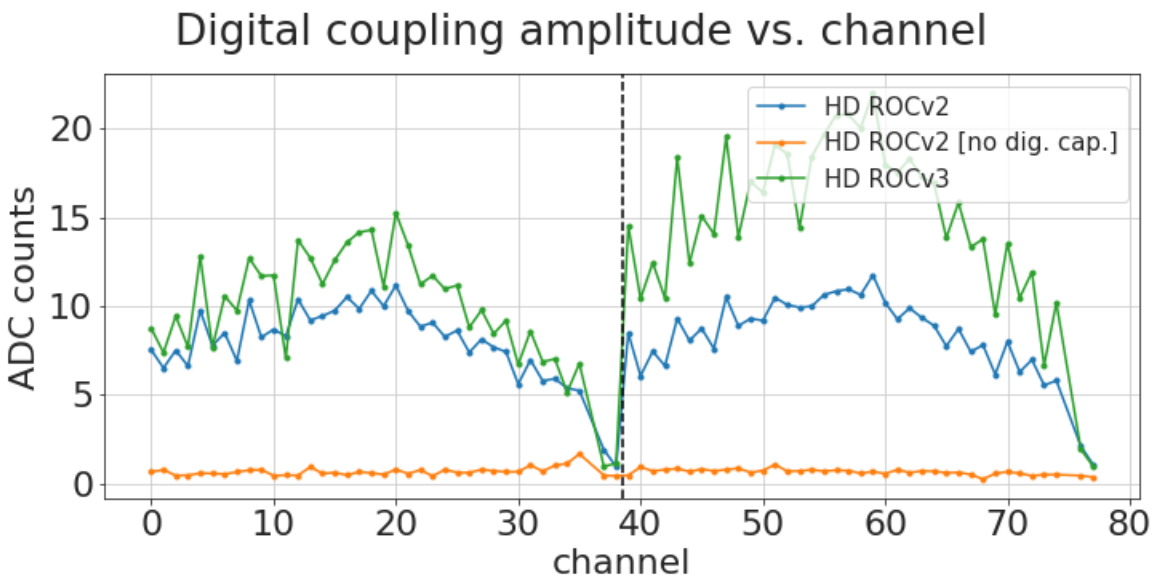


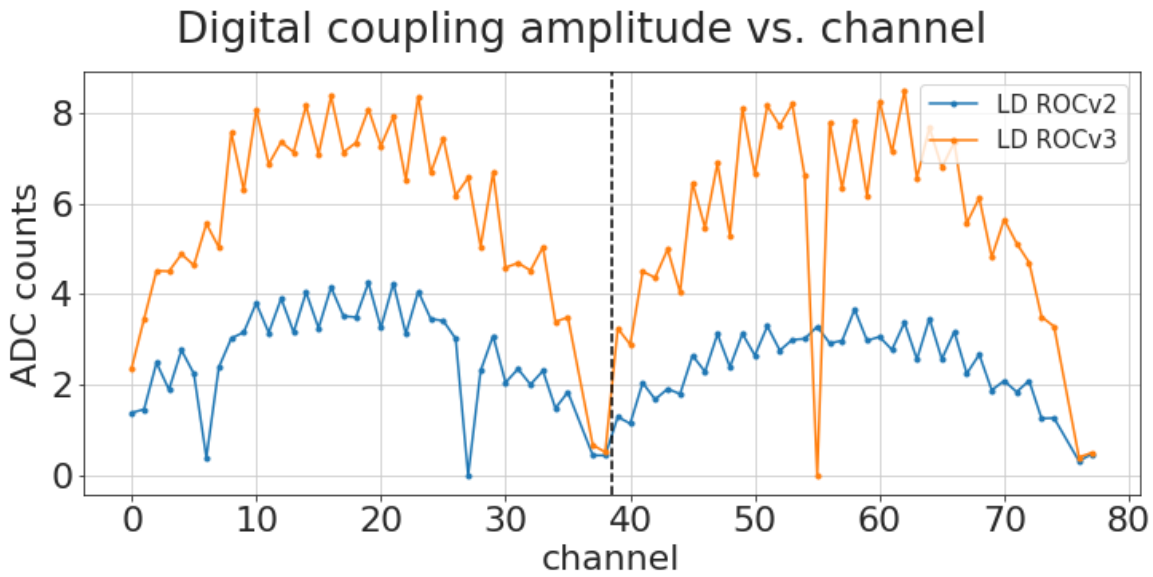
Digital modulation on mezzanine

- Analog front-end very sensitive to the ground and BV
  - gain = C_{det}/C_{f_pa} > 100 , 1 ADC count = ~ 10 µV on ground
  - Ground: very low impedance ➔ planes above and below the inputs layer

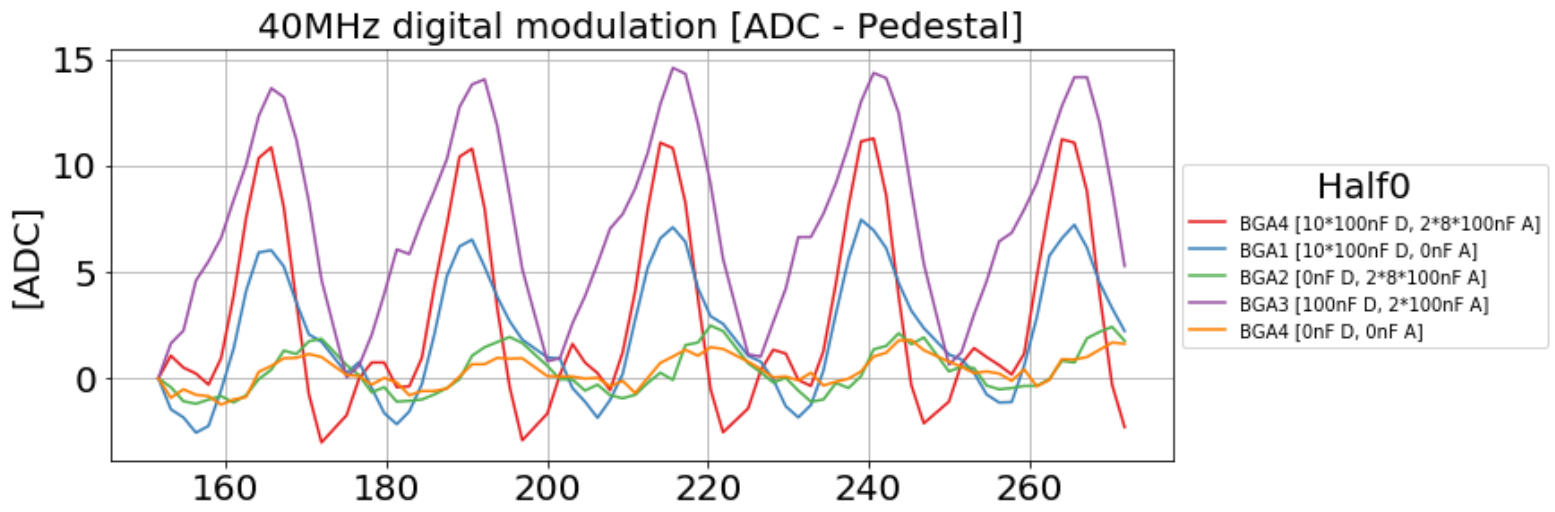
- Capacitors inside the chip for decoupling VDDD
  - 2nF in HGCROC3, 16nF in HGCROC3A
  - No obvious difference observed

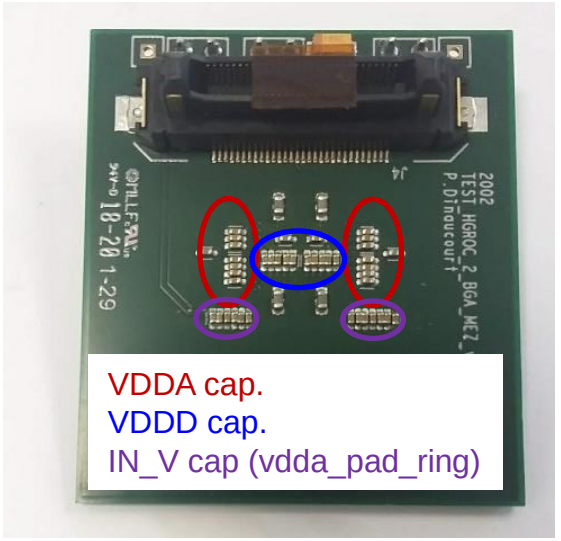


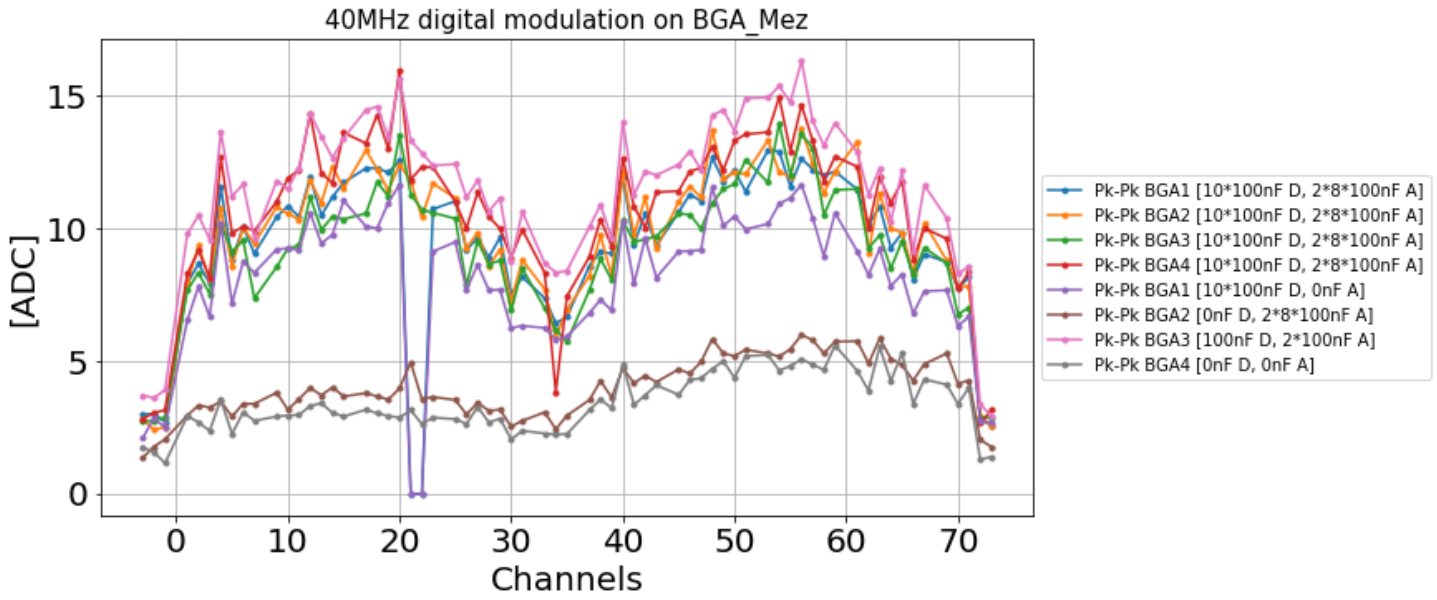


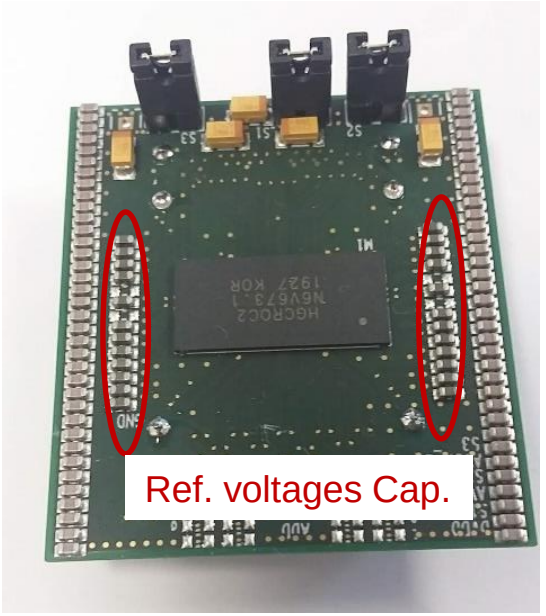


HD package: 40 MHz coupling with the HD BGA on a Mezzanine



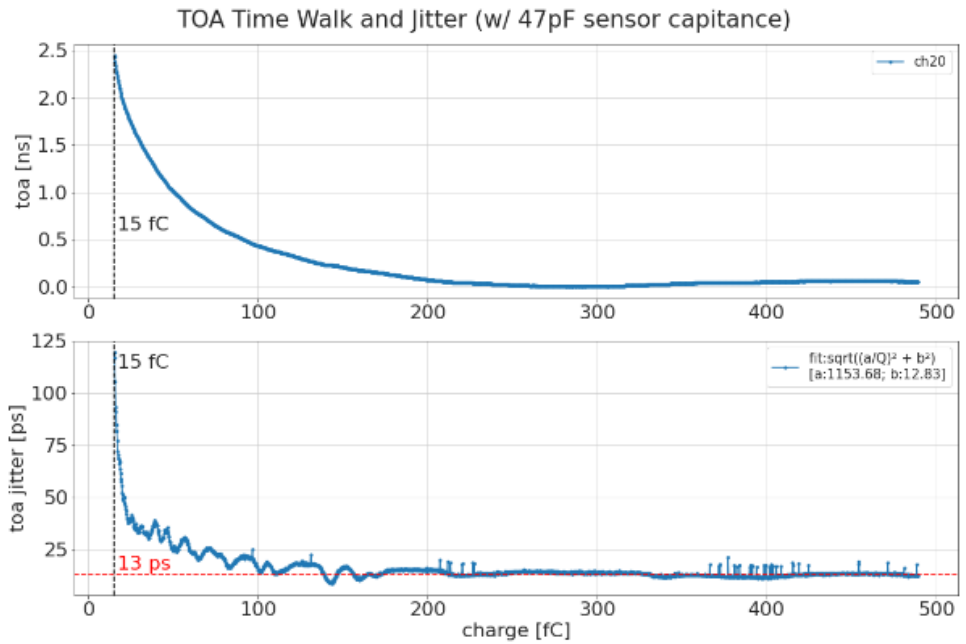


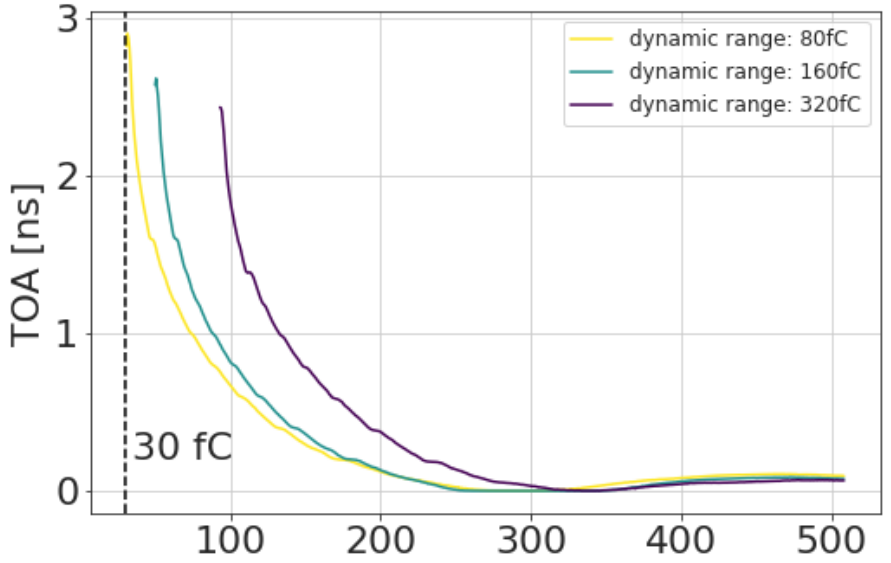


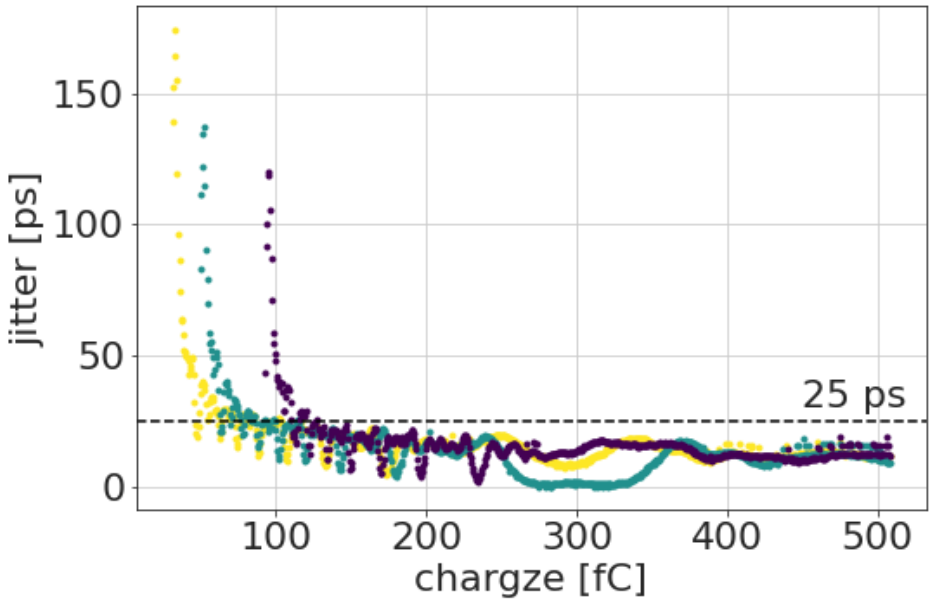


Time

- Minimum threshold setting
  - Depending on the board, limited by digital modulation on pedestals
  - Min. achieved is 15 fC on characterization board
- Time walk
  - 2.5 ns
- Jitter
  - 1.15 ns/Q(fC)
  - 13 ps floor

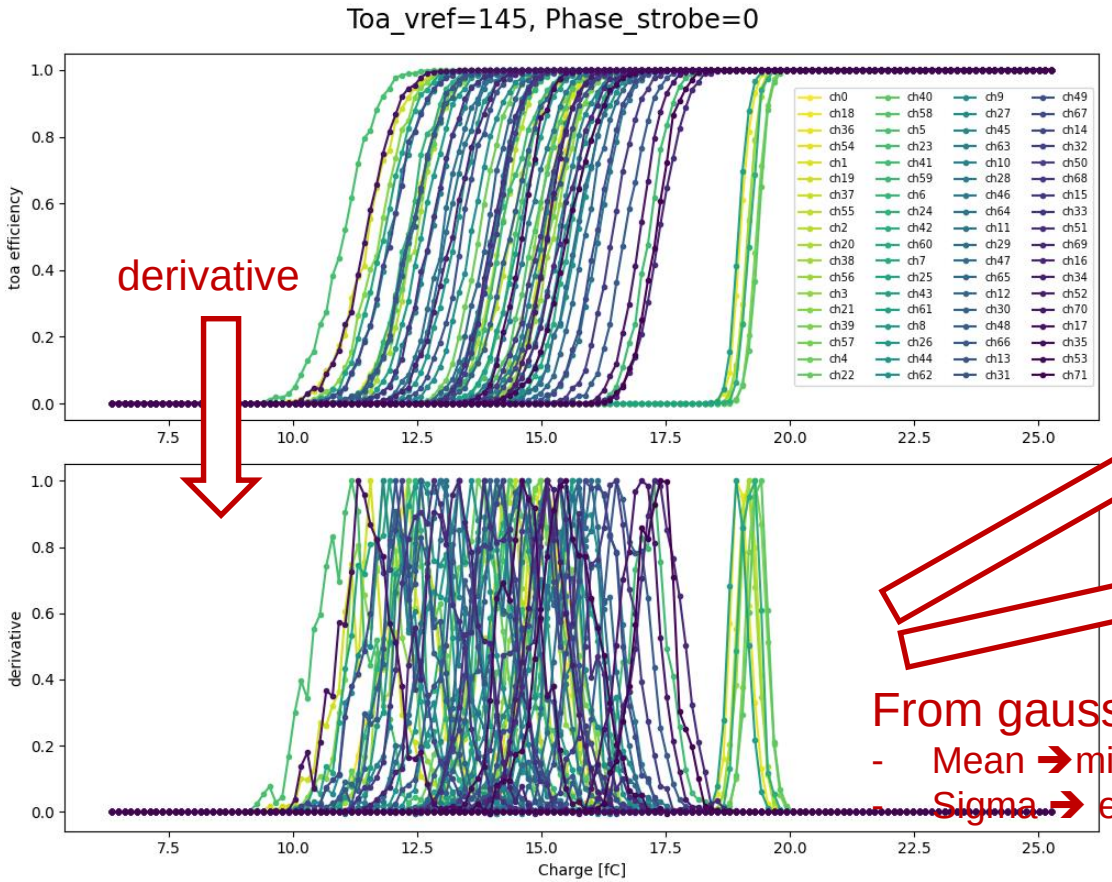


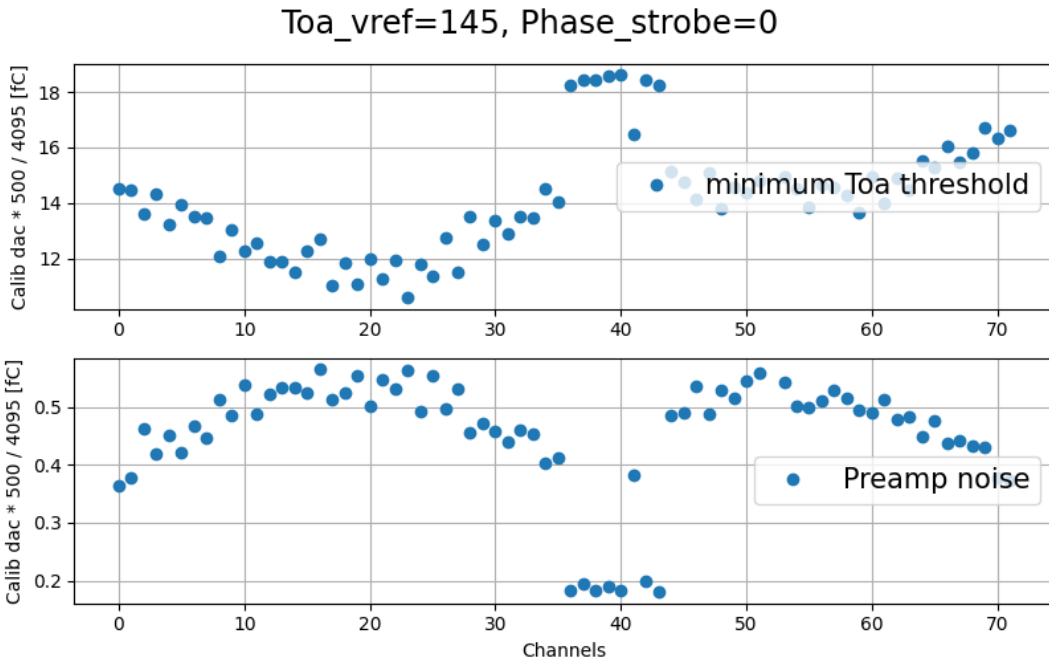




How to extract minimum toa and preamp noise?

S-curves: Toa efficiency as a function of the injected charge



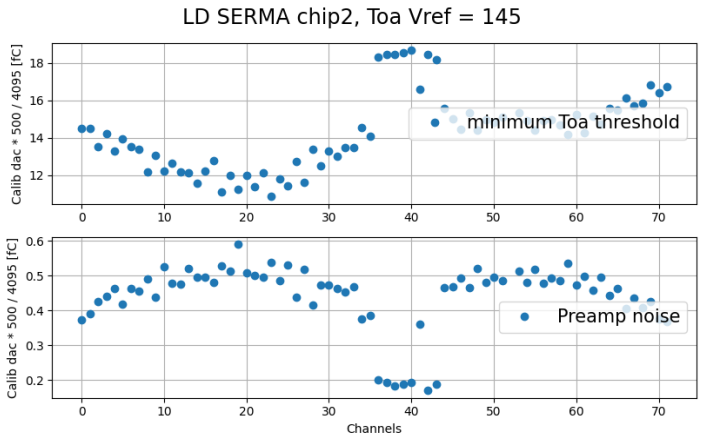


From gaussian fit

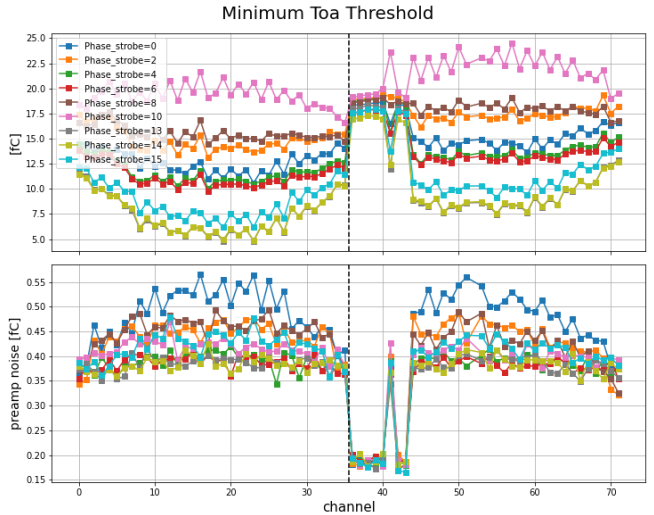
- Mean ➔minimum toa threshold
- Sigma ➔ electronics noise at the preamp output

- 0,5 fC electronics noise at the preamp output ➔ minimum Toa threshold should be just higher than 2,5 fC
- 12 fC is the best we achieved

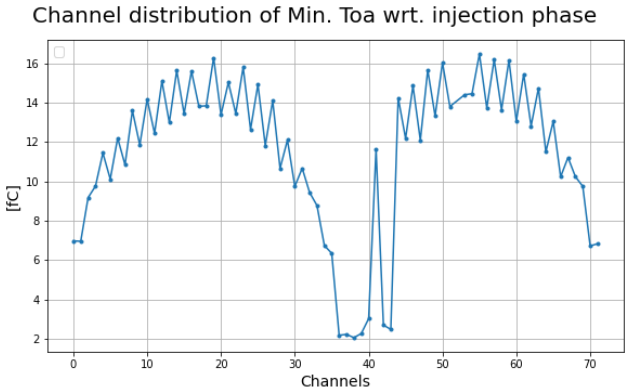
Digital noise: Preamp output vs. Shaper output

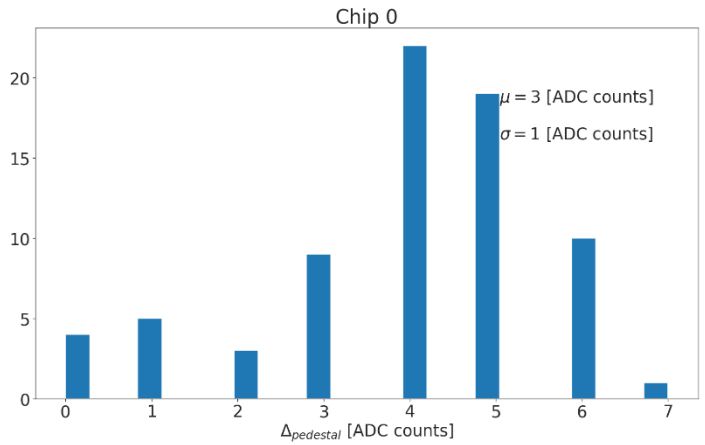


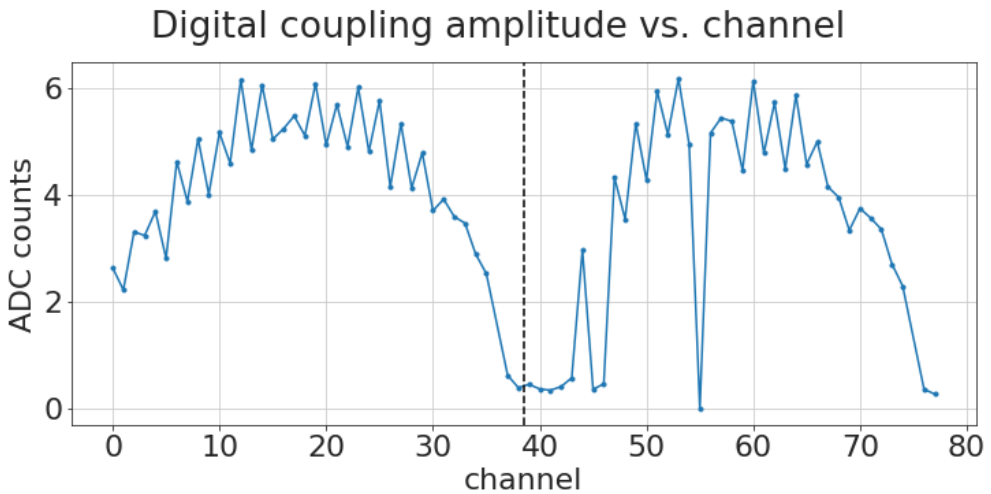
Injection phase = 0



Injection phase = 0 .. 15





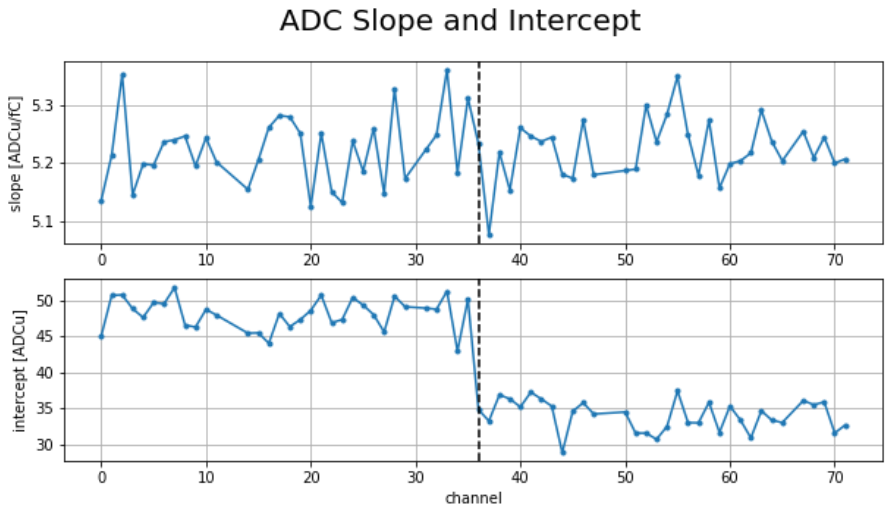


Delta pedestal

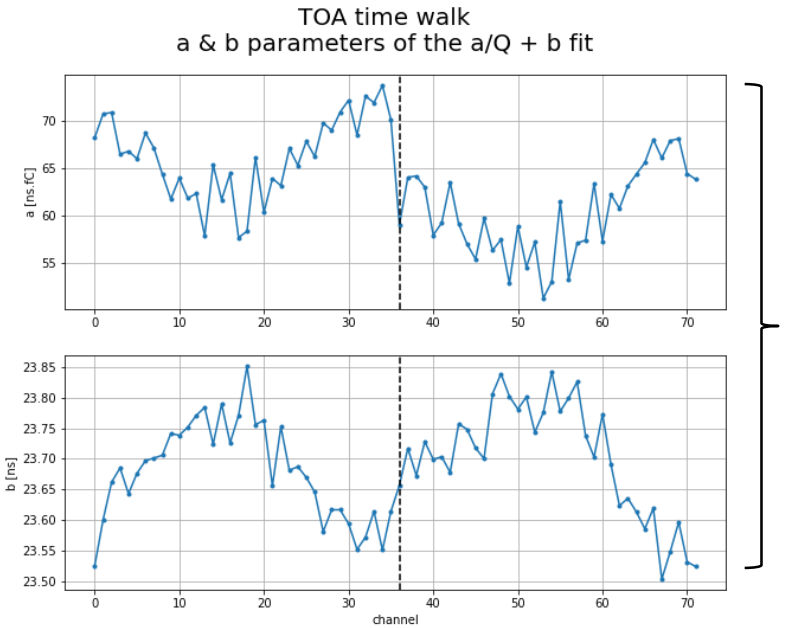
Shaper output:
- Gain = 0,2 fC/ADC
- Delta ped = 2 – 6 ADCs
- Delta_ped = 0,4 – 1,2 fC

Preamp Output
- Delta ped = 5 – 20 fC

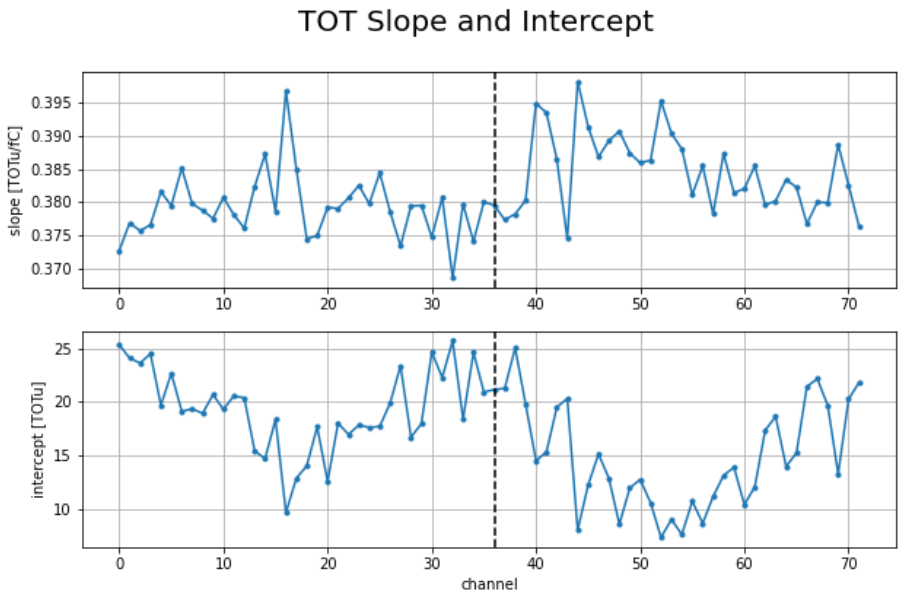
Charge and time uniformity



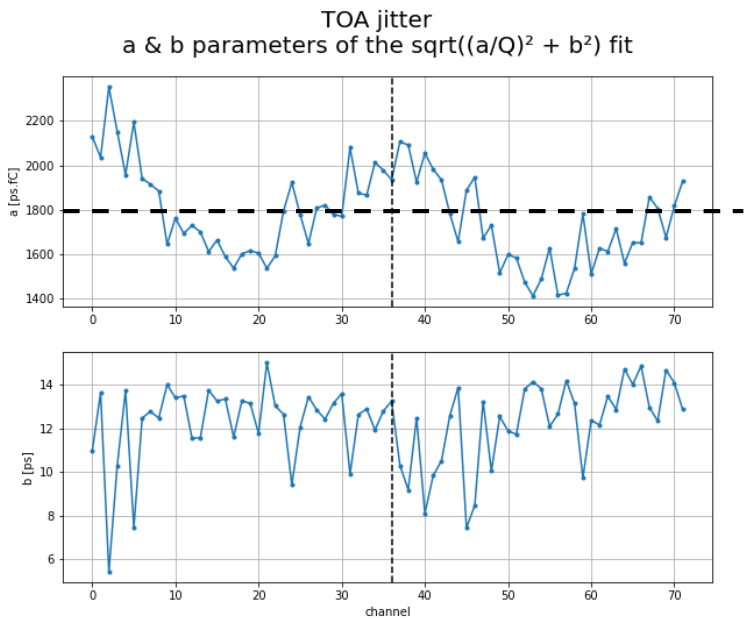
5.2 ADCu / ch
(+/- 2%)



Clock distribution from the middle of each half visible on the time walk distribution



0.38 TOTu / ch
(+/- 3 %)

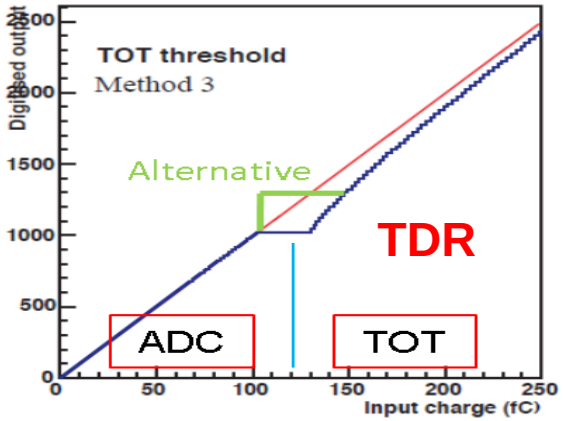


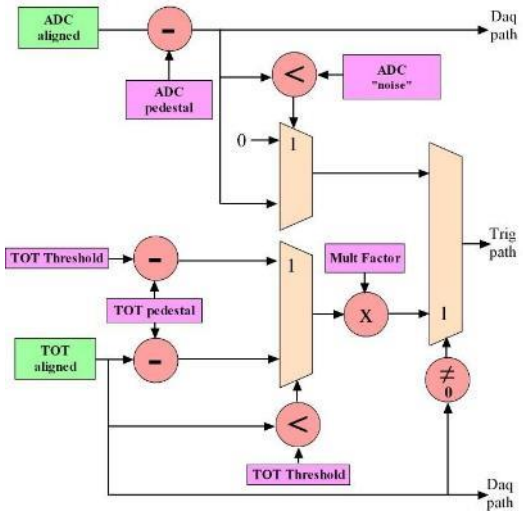
1.8 ns / Q(fC)

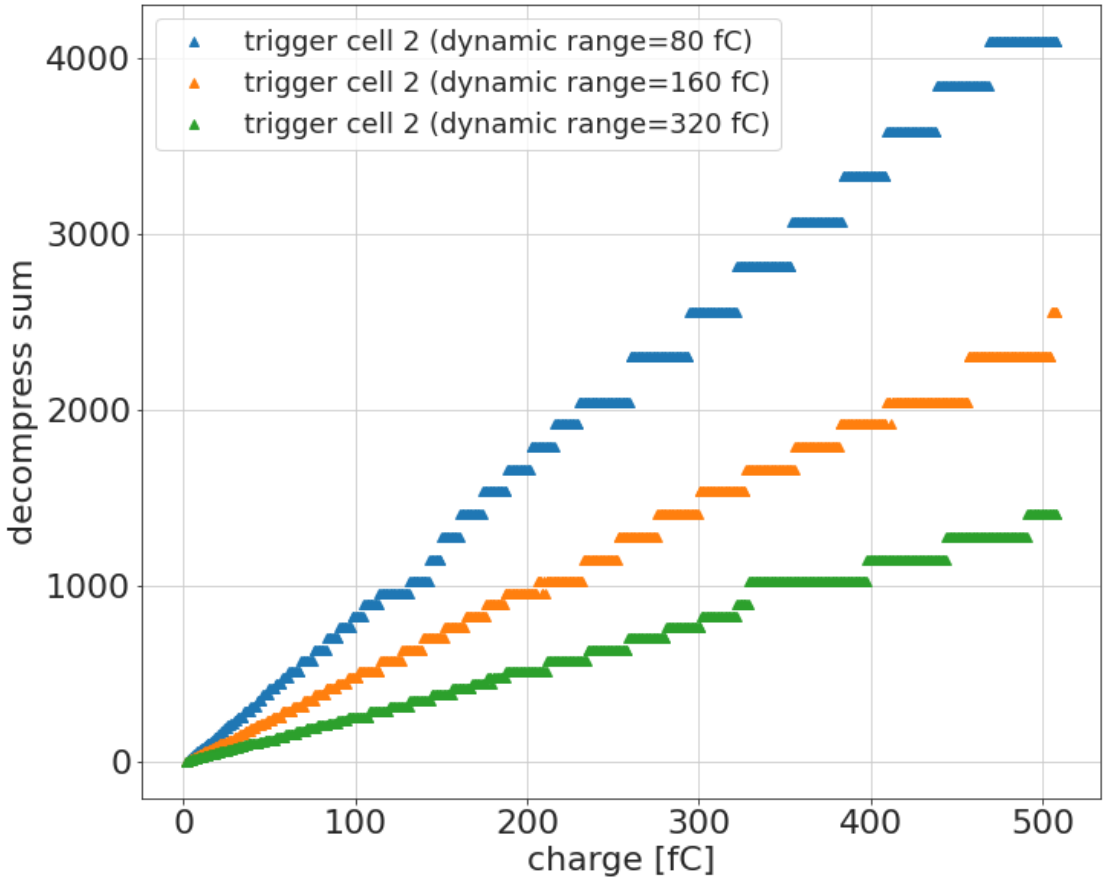
13 ps rms

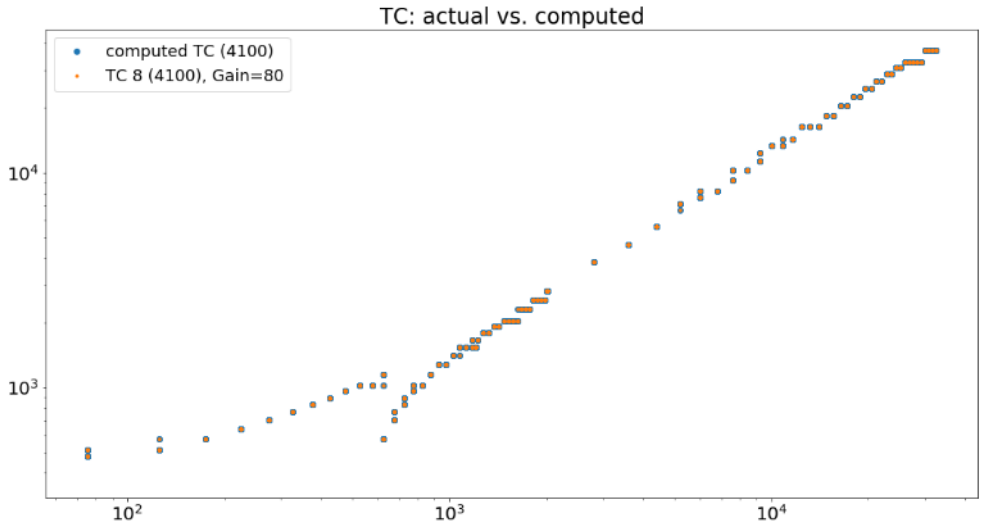
Trigger path

- Charge linearization over ADC and TOT range
- Sum by 4 / 9 (19b / 21b)
- Compression: 4b exponent + 3b mantissa









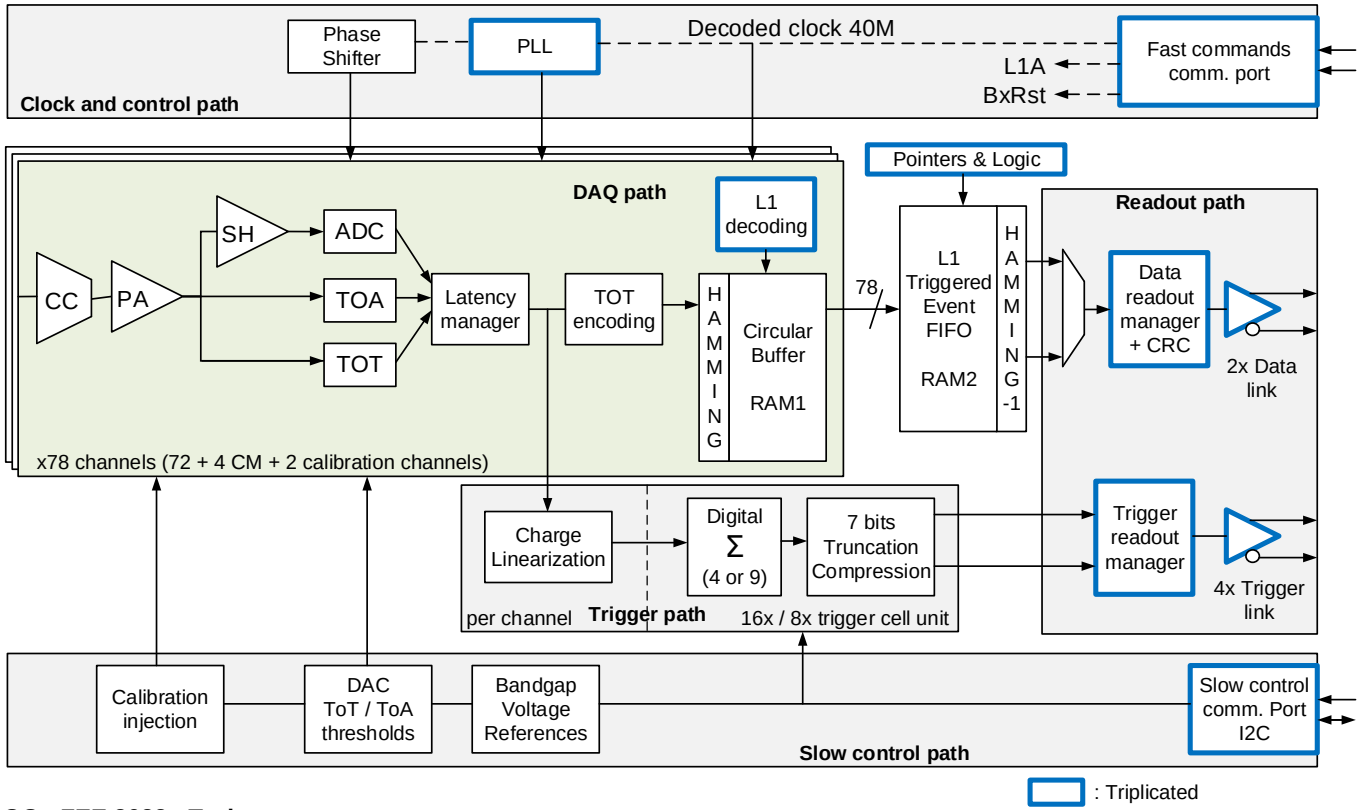
H2GCROC3: the SiPM version of HGCROC3

Differences on H2GCROC3

- 2,5 V power supply for the very front-end to cope with SiPM bias voltage
- Dynamic charge: **160 fC to 320 pC**
- Input DAC to tune the input voltage in order to compensate for breakdown voltage fluctuation
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**

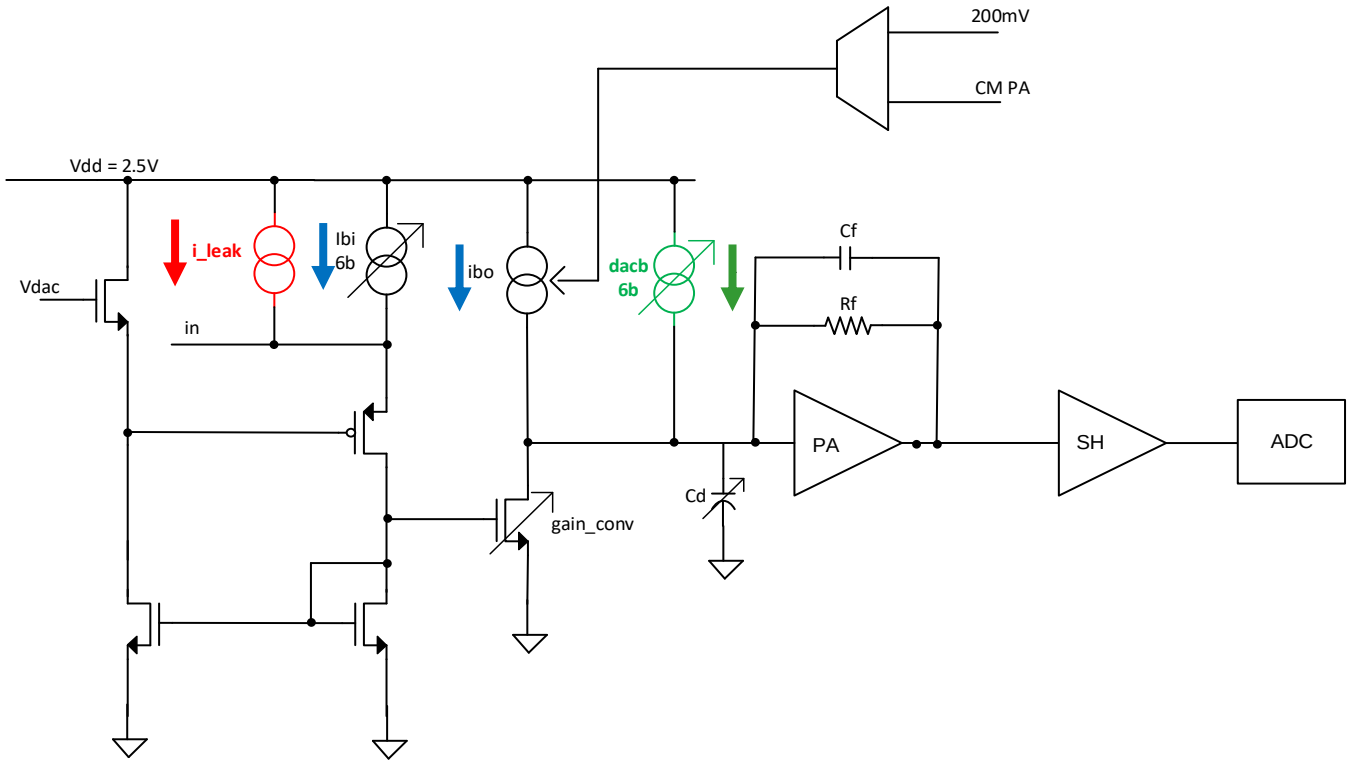
Current Conveyor
based on KLAUS chip from Heidelberg UNI.

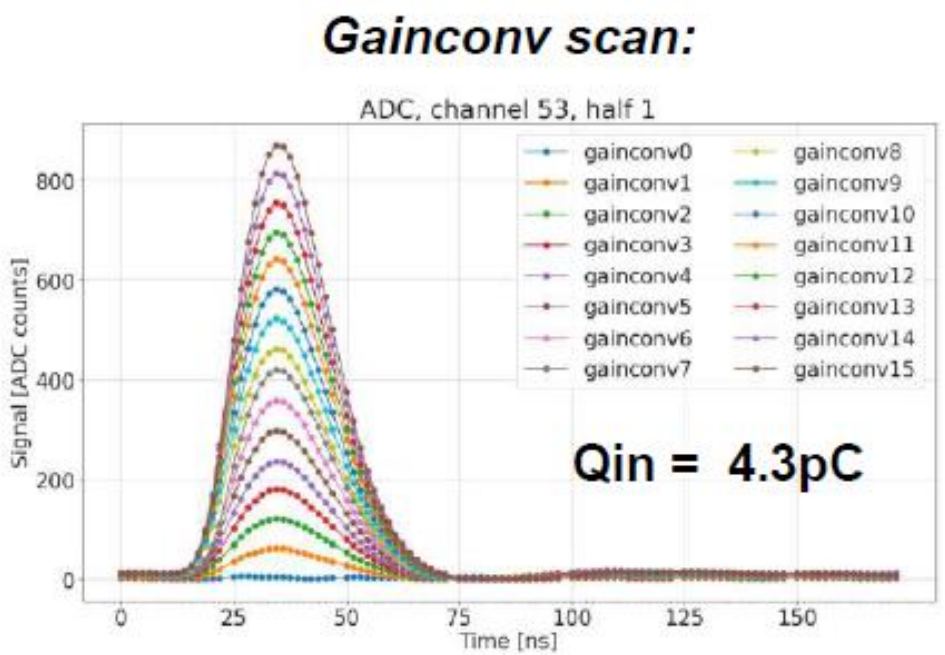
Attenuates the current at the input with 4 bits.
Gain: 0,025 to 0,375 (step 0,025)



H2GCROC: the current conveyor

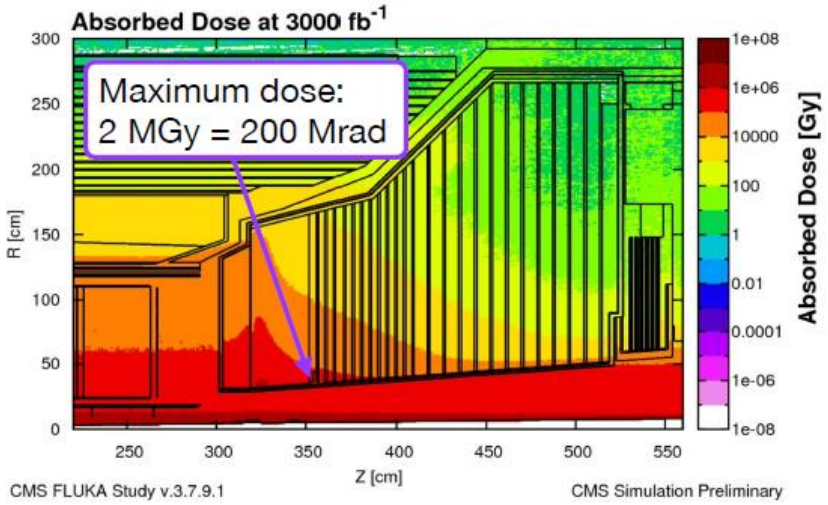
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**



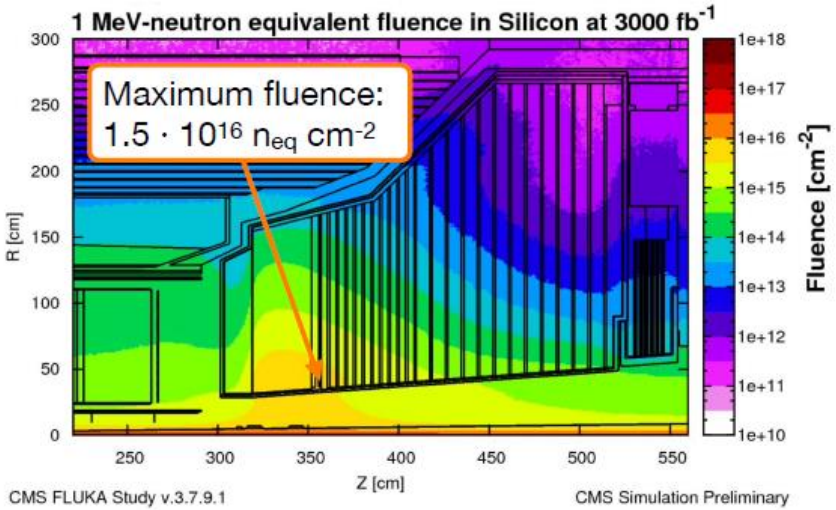


Radiation hardness

- According to FLUKA simulations, the CMS forward region will be exposed to a total integrated dose of up to ~ 200 Mrad and a hadron fluence up to $1,5.10^{16}$ n_{eq} cm^{-2}
- Irradiation campaigns required to demonstrate that HGCROC3 withstands such harsh radiation environments



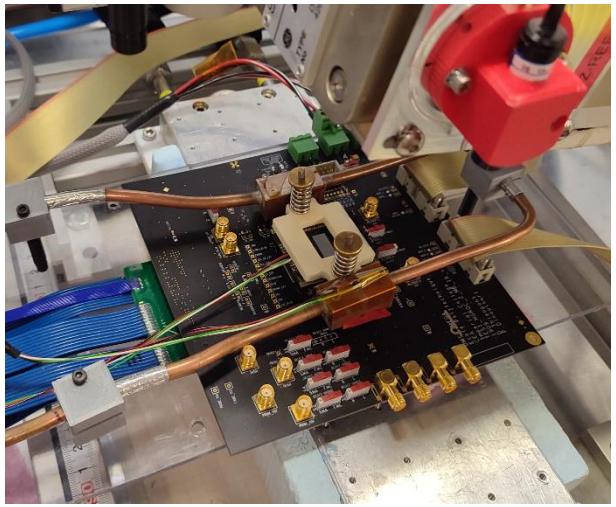
Total Ionising Dose (TID): test the cumulative damage of ionising particles

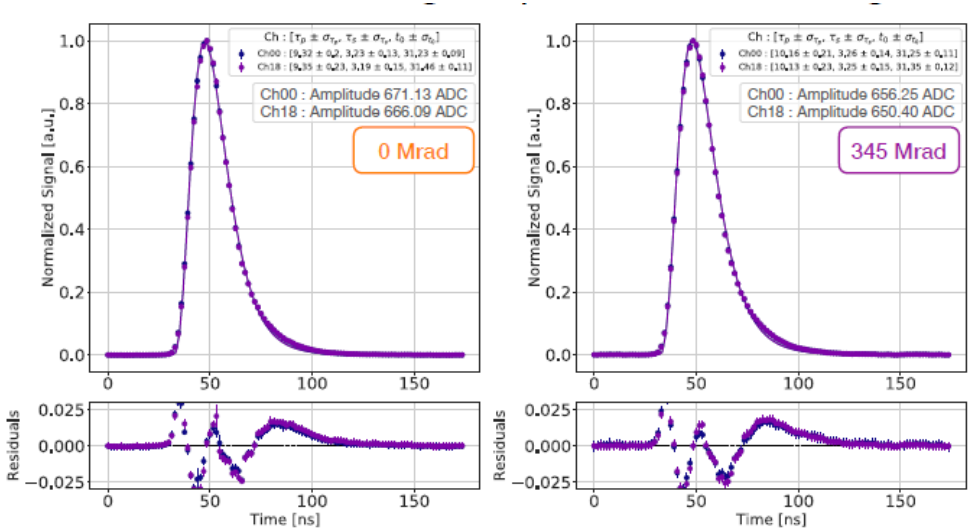


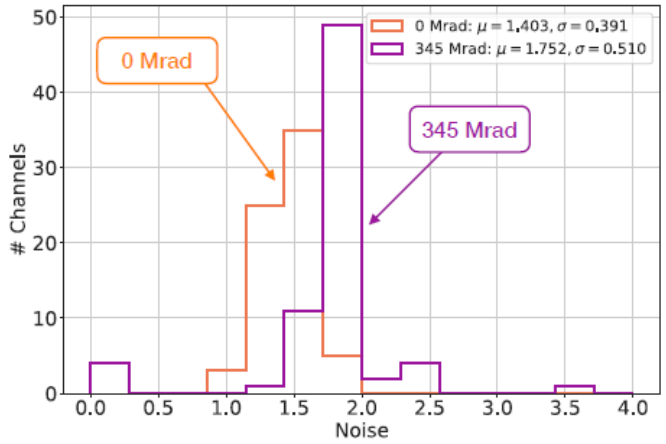
Single Event Effect (SEE): test the non-cumulative damage induced by single particles

TID tests

- The chip was placed on a **mezzanine** and **thinned** to **~ 70 µm**
  - *Beam*: 10 keV X-rays (Obelix facility at CERN)
  - *Temperature*: -10° C
  - *Dose rate*: 0.245 and 2.45 Mrad/h
  - *Total integrated dose*: **345 Mrad**
- **No big impact** observed on any part of the chip:
  - *No change in the **charge** and **time** measurement (linearity and jitter)*
  - *No misbehaviour in **DRAM***
  - *Preamplifier **noise** slightly increase with dose: ~20 % (1800 e- to 2200 e-)*
  - ***PLL**, **e-links** and **digital** part maintain the good performance as expected*
  - *Power consumption increase (next slide)*

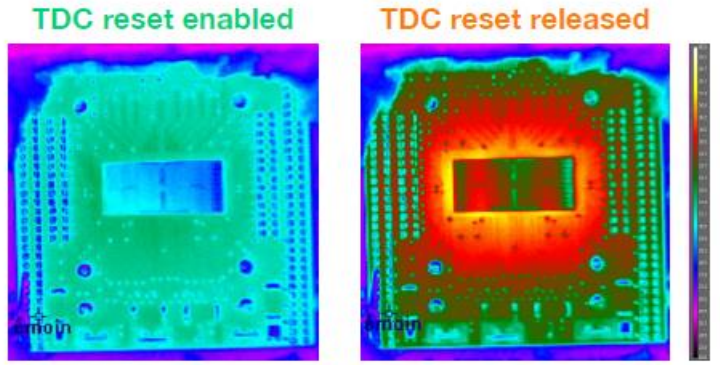


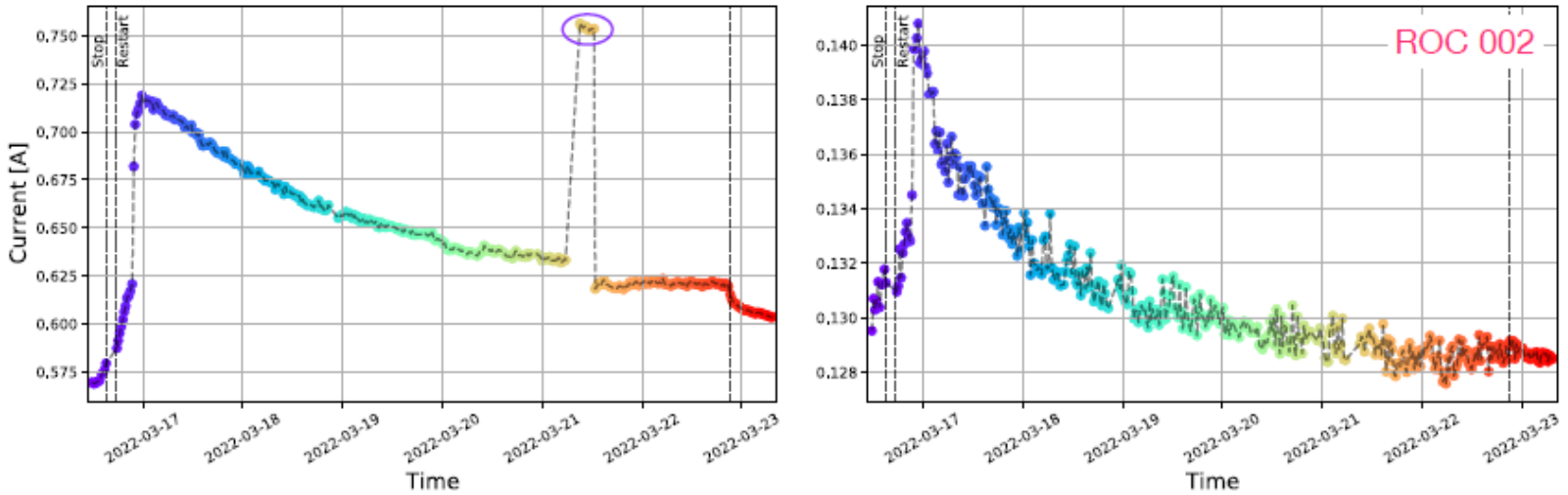




TID: current increases

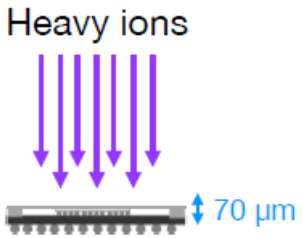
- Analog and digital **currents increase** in the initial phase of the irradiation:
  - *analog: +25% ➔ unexpected*
  - *digital: +8% ➔ expected due to current leakage in the transistors*
- *Current increase traced to TDC with thermal camera*
  - *Extra current is removed when resetting the TDC, comes back when releasing the reset*
  - *Identified floating node in the TDC digital block when in idle mode (not disturb time measurement)*



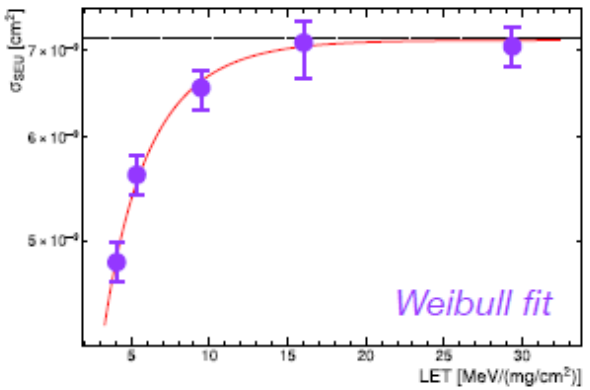


SEE testing: Heavy Ions

- Test the stochastic **non-cumulative** radiation **damage** induced by single particles: 3 possible consequences
  - *Single Event Upset (**SEU**) : digital error, bit flip (0→1 or 1→0)*
  - *Single Event Transient (**SET**) : analog error, bit shift*
  - *Single Event Latch up (**SEL**) : permanent damage*



- Irradiation of HGCROC3 chip with **heavy ions** at UCL cyclotron in Louvain
  - *Beam: low energy heavy ions with different **Linear Energy Transfer** (LET)*
  - *Flux: 10^4 particles/(s·cm^2)*
  - *Temperature: 7.2° C*
- Two main measurements:
  - *Configuration: I2C registers*
  - *Digital & memory: DAQ tests*



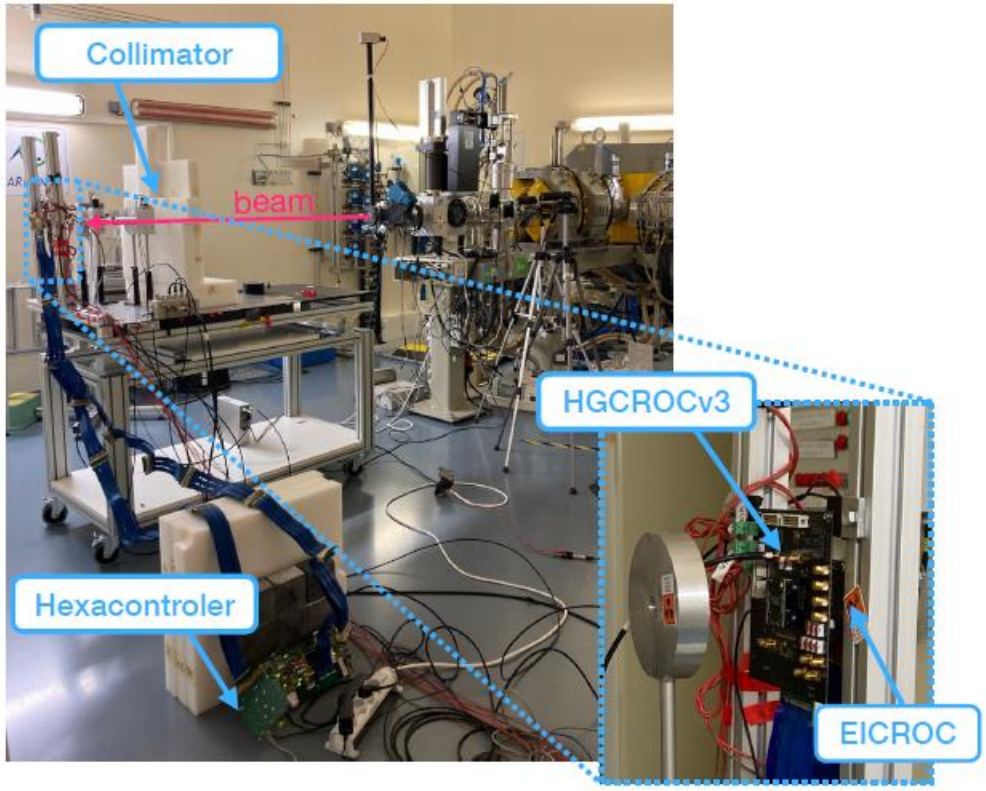
Ion	M/Q	Range [µm Si]	LET [MeV/mg/cm^2]
Ne	3.14	202.0	3.3
Al	3.37	131.2	5.7
Ar	3.33	120.5	9.9
Cr	3.31	107.6	16.0
Ni	3.22	100.5	20.4
Kr	3.35	94.2	32.4
Xe	3.54	73.1	62.5

SEE testing: protons

- **Proton** irradiation campaigns at *Arronax* in Nantes (22nd December 2022, 3rd February 2023)
  - *Beam*: 64 MeV protons
  - *Flux*: 10^{10} particles/s/cm^2 (expected at HL-LHC: 10^6 p/s/cm^2) (continuous mode: packets every 33ns)
  - *Duration*: 12*2 hours
  - *Temperature*: room temperature
  - *Total integrated dose*: 140 Mrad
- **Complex** experimental **setup**:
  - Long cables to protect the hexacontroler
  - No access to the cavern for days (activation)
- **HGCAL** radiation environment dominated by light hadrons

→ more **realistic** description of the HGCROC3 behaviour

→ higher flux and more error **statistics**



SEE testing results

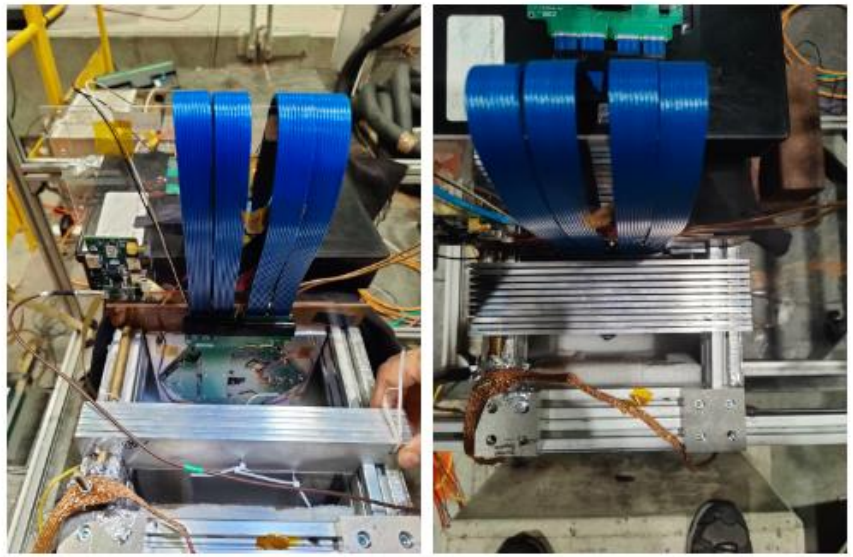
- Heavy ions results
  - No SEL
  - No I2C bitflips (when AutoReload enable)
- Protons results
  - Flux = **2.20 10^{10}** $s^{-1} \cdot cm^{-2}$, total time = **13 h** → ~ 10 years of HL-LHC

	SEU counters	SEU trigger	SEU CRC	SEU memory	Short SET	Long SET
# errors	< 1	38	30	127	85	190
DAQ time	13.011 h	34 s	340 s	4352 s	340 s	13.011 h
Rate $_{Arronax}$ [err/s]	< 2.1 10^{-5}	1.12 ± 0.18	0.09 ± 0.01	0.029 ± 0.002	0.25 ± 0.03	0.0041 ± 0.0003
Rate $_{HGCAL\ av}$ [err/s]	**< 1.9 10^{-9}**	**(1.0 ± 0.2) 10^{-4}**	**(8.1 ± 1.6) 10^{-6}**	**(2.6 ± 0.2) 10^{-6}**	**(2.2 ± 0.3) 10^{-5}**	**(3.6 ± 0.3) 10^{-7}**
Rate $_{HGCAL\ max}$ [err/s]	< 1.9 10^{-8}	(1.0 ± 0.2) 10^{-3}	(8.1 ± 1.6) 10^{-5}	(2.6 ± 0.2) 10^{-5}	(2.2 ± 0.3) 10^{-4}	(3.6 ± 0.3) 10^{-6}
Rate $_{All\ chips}$ [err/s]	< 0.00019	10 ± 2	0.81 ± 0.16	0.26 ± 0.02	2.2 ± 0.3	0.036 ± 0.003
Cross section [cm^2]	< 9.7 10^{-16}	(5.7 ± 0.9) 10^{-11}	(4.5 ± 0.8) 10^{-12}	(1.5 ± 0.1) 10^{-12}	(1.3 ± 0.1) 10^{-11}	(2.1 ± 0.1) 10^{-13}

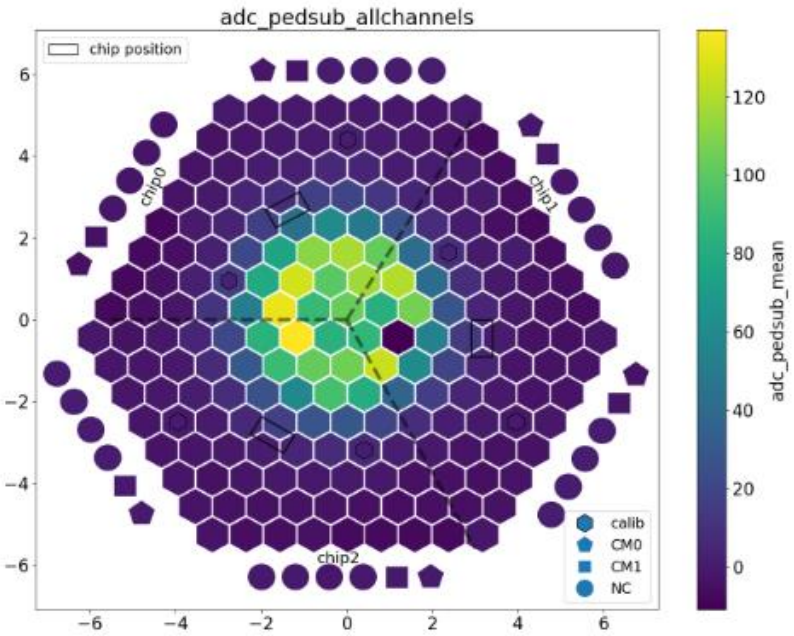
  - For each chip (on average): 1 link loss / 2.5 years
  - For HGCAL (on average): 1 link loss / 2 min

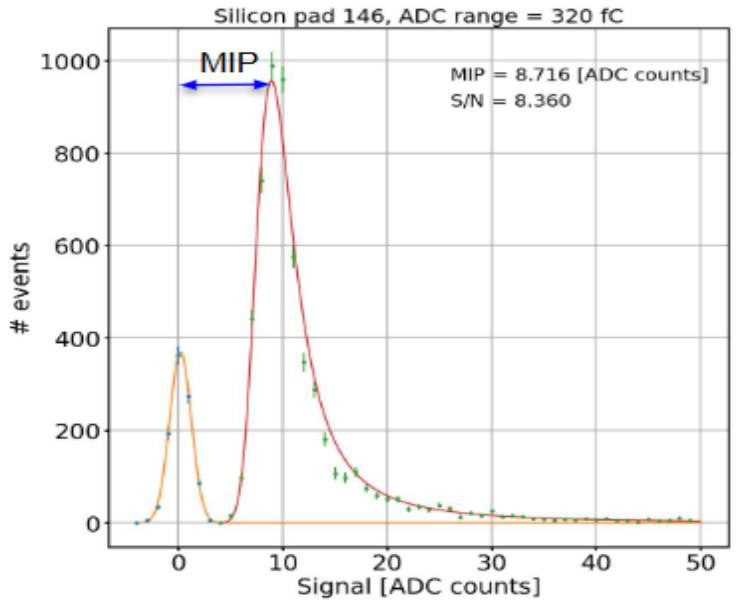
Test beam at CERN (October 2022)

V3-LD hexaboard with 300 µm thick sensor



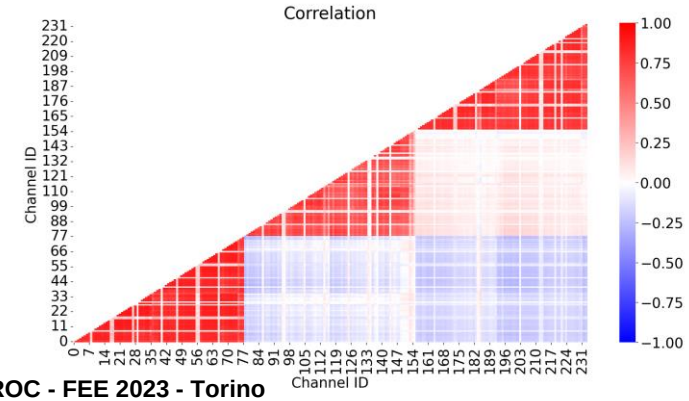
250 GeV electron, default gain, with absorber

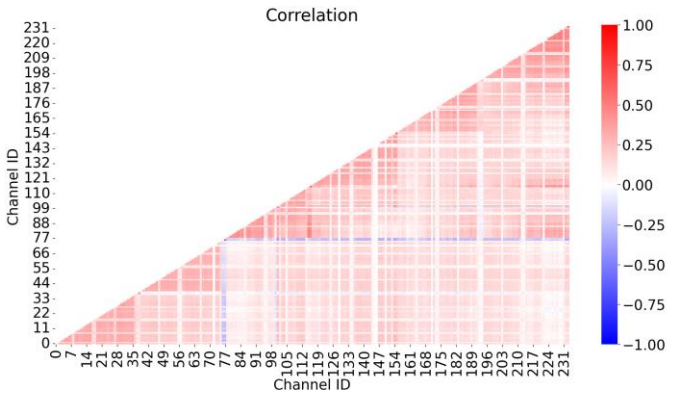




NSH HB module (Oct. 21) vs. V3-LD module (Oct. 22)

Digital noise: > 120 ADCu ~10 ADCu





Summary

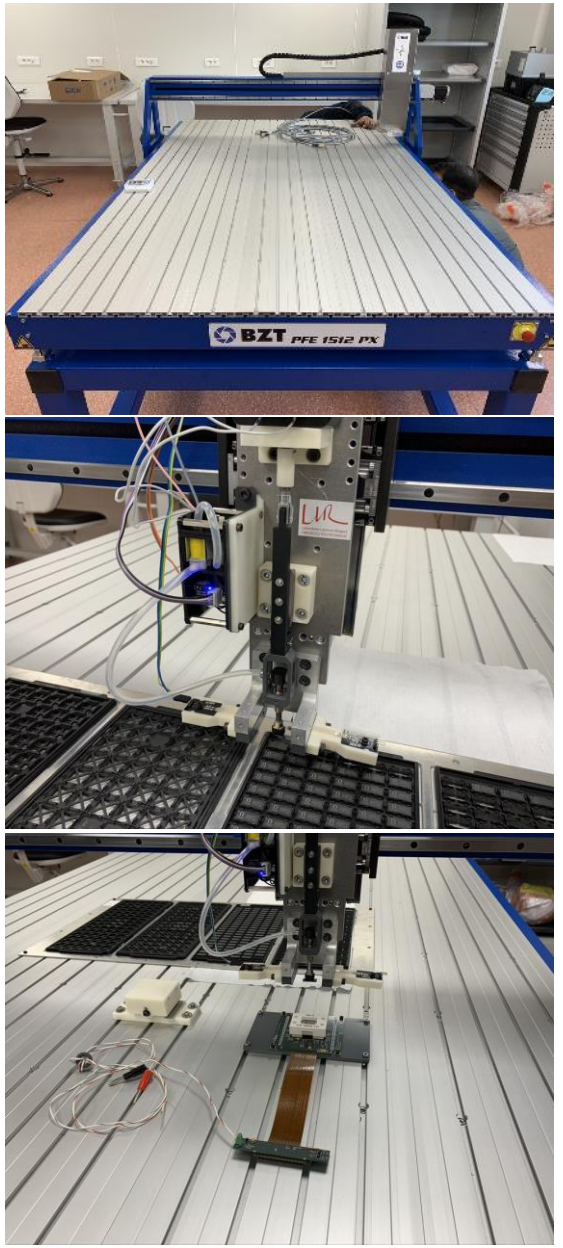
- HGCROC3 for HGCAL has been extensively measured and reaches good performance
  - < 1% linearity for charge measurement over the full dynamic
  - Noise level as expected
  - Timing (Time walk and jitter) as expected: TW < 1.4 ns, jitter ~ 1.8 ns/Q(fC) and 13 ps floor
- But still need to fight against digital activity
  - Digital « noise » on pedestals
  - Lower Toa threshold 15 fC (24 fC for the module)
- HGCROC3 is radiation tolerant
  - Still working properly up to ~ 400 Mrad
    - 20% noise increase not understood yet
- Main concern now is the packaging
  - HD and LD
  - Common or separated grounds

Backup

Robot for production testing

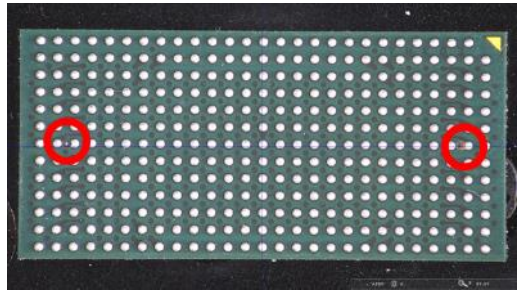
- 2 robots: LLR and OMEGA
- Pick and placing features work
- DAQ and analysis software work
- ~ 450 HD-ROCv3 have been tested
- ~ 300 LDROCv3 have been tested

Preliminary tests list:
- Power consumption
- Write/read fuse number
- Write/read the 8 bits of the 800 SC registers
- Measure the 2*64 probe_dc values
- Measure the 10bits DACs and 12 bits calibration
- Measure the 6 bits channel wise tuning dacs : 78 x 6 bits x 3 dacs
    - Adjust the pedestals, TOA/TOT thresholds channel wise
- Check the fast commands and links
- Check rms to detect bad or unconnected channels
- Make a phase scan to check shifter OK
- Run the DRAM tests
- Check ADC linearity with test pulse injection : 10 points* 72 channels * 100 meas.
- Set threshold to ~10 fC measure TOA and TOT vs Qinj (DAQ and TRIG paths)
- **Specific tests for the SiPM version**
    - 2V5 power consumption
    - Input DC level adjustment (Input DAC)
    - Conveyor gain (DACb adjustment)



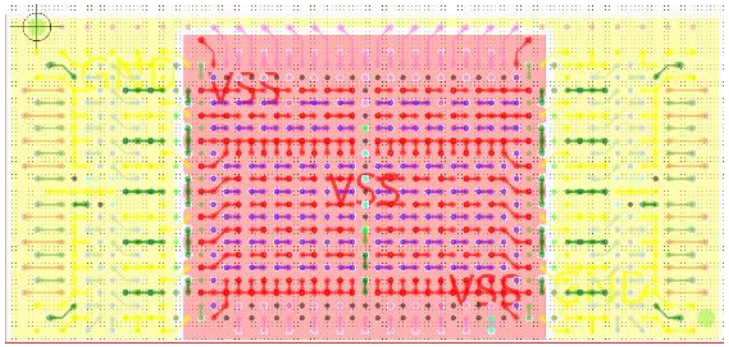
Chips & Package: High Density

- High density Si-version HGCROC3
  - Short circuit in the BGA substrate (vdd_pad tied to ground)
  - ~ 2000 drilled packages
  - ~ 150 pieces tested: > 90 % short circuit removed
  - Tests with packages on Mezzanine, production testboard works, robot in progress at LLR
- Module performance
  - NSH HD HB: good with HDROCv2, terrible with HDROCv3
  - Waiting for results with HDROCv3 mounted on V3 HD HB
  - But most likely, should go back to « HGCROC2 » package with separated gnda/vss

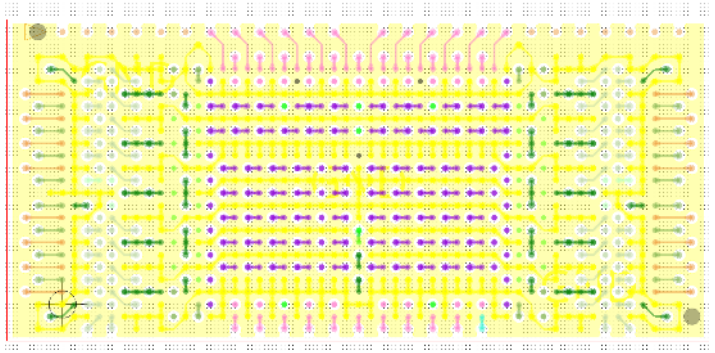


		noise	delta pedestal
ROCv2	bare NSH HB	1,3	3
	module	2,5 - 3	16
ROCv3	bare NSh HB	1	16
	module	> 2,5	> 170

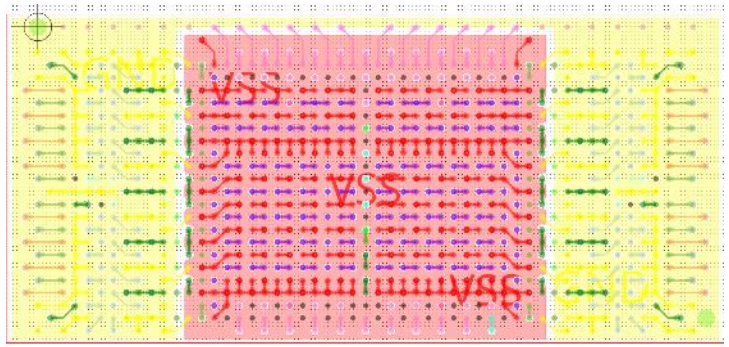
HGCROC2



HGCROC3



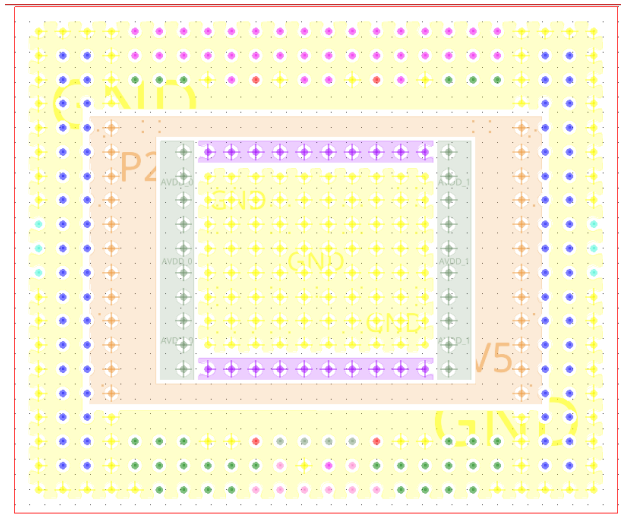
HGCROC3b (not yet in fabrication)



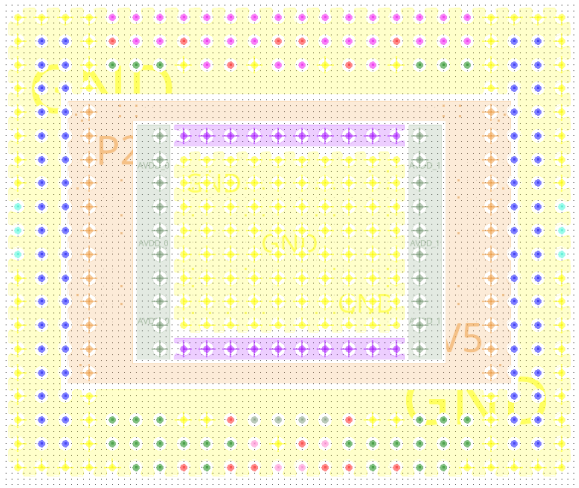
Chips & Package: Low Density

- Low density Si-version HGCROC3
  - ~ 10 pieces mounted in the first version of LD substrate (SERMA)
    - request laser drilling
    - Incompatible for H2GCROC3
  - ~ 50 pieces mounted in the corrected LD substrate (SERMA)
    - Compatible for both HGCROC3 and H2GCROC3
    - New batch of 1000 substrate arrived these days at OMEGA
      - All H2GCROC3
    - Waiting for results with LDROCv3 mounted on V3 LD HB
  - New LD packaged with gnda/vss separated sent to fabrication to NCAP (China)
    - Expected back in 2-3 months

HGCROC2



HGCROC3



New HGCROC3
(fabrication on-going)