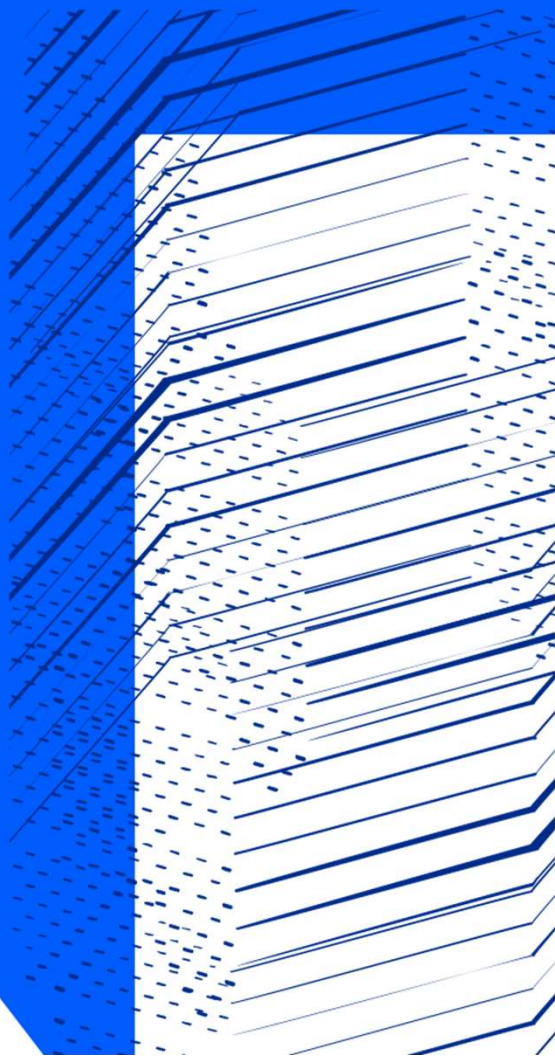
Science and Technology Facilities Council

65nm IP development for CMOS sensors at the Electron-Ion Collider

Soniya Mathew(STFC), Iain Sedgwick(STFC), Nicola Guerrini(STFC), Laura Gonella(UoB), Marcello Borri (STFC)

STFC RAL
14 June 2023

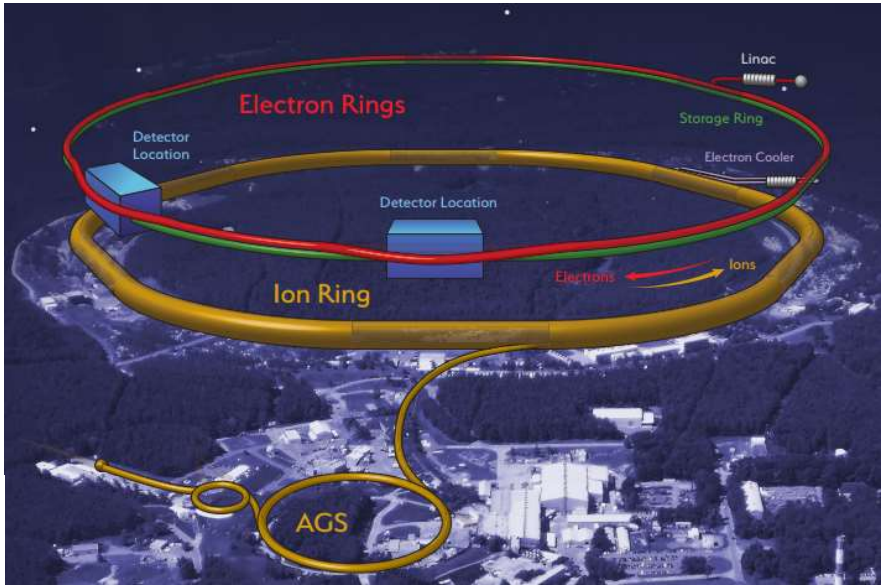


Overview

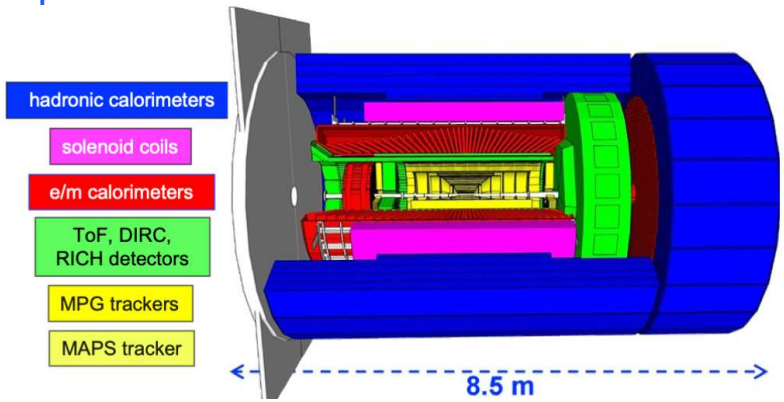
- What is EIC and why is it interesting?
- Why TPSCo 65nm (Tower Partners Semiconductor Company) is the chosen technology?
- IP's developed by STFC RAL for EIC
    1. Dual Mode Phase Locked Loop
    2. High Speed IO's
    3. I²C Module
    4. PRBS Generator
- Serial Powering of outer barrel layers in EIC
    1. Concept of Serial Powering
    2. Shunt LDO
- Conclusion

What is Electron Ion Collider

- Electron Ion Collider (EIC) is a High Energy Experiment facility located at the Brookhaven National Laboratory in the US.
- The EIC will bring high-energy electrons into head-on collisions with high-energy protons or atomic nuclei to produce 3D images of those particles' inner structure.
- Aims to deliver some cutting-edge technologies, development of new computational tools, and other particle accelerator components.
- EIC is planned to be fully operational in the early 2030s with the ePIC(Electron Proton Ion Collider) detector as its first experiment and the development of sensors will be part of the first implementation phase.

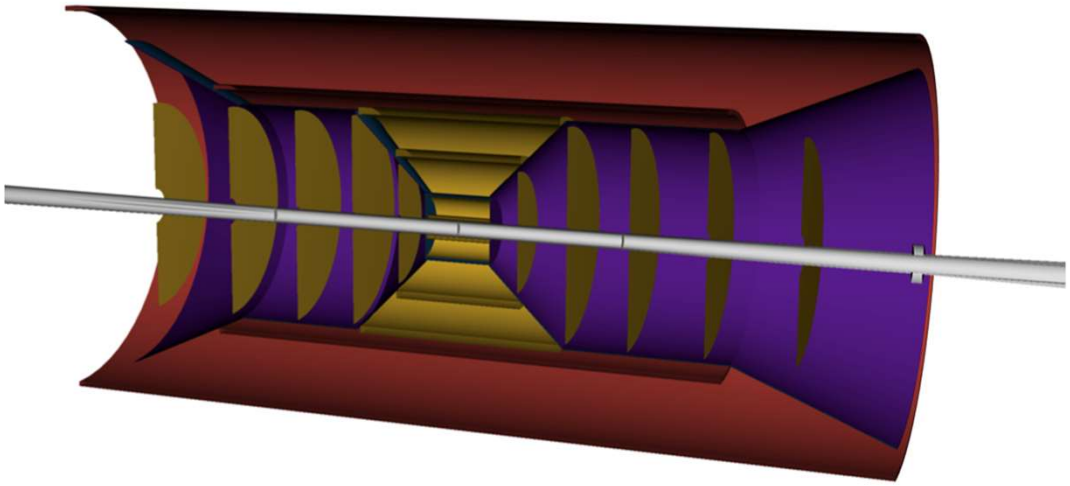


Electron Ion Collider Conceptual Design Report : https://www.bnl.gov



Vertex and Tracking detector system of EIC

- The ePIC vertex and tracking detector comprises silicon Monolithic Active Pixel Sensors (MAPS) closest to the interaction point and Micro-Pattern Gaseous Detectors (MPGD) further out.
- The ePIC vertex layers will use the wafer-scale, curved, 65 nm ALICE-ITS3 MAPS sensor; the outer barrel layers and disks will use a smaller version of the ALICE-ITS3 sensor on carbon fiber support structures with integrated cooling and electrical interfaces.



MAPS based Silicon Vertex Tracker

MPGD

Updated barrel reference geometry:

- 2 curved silicon vertex layers, r = 36, 48 mm, l = 270mm
- 1 curved silicon dual purpose layer r = 120mm, l = 270mm
- 1 stave-based sagita layer r = 270 mm, l = 540 mm
- 1 stave-based outer layer r = 420 mm, l = 840 mm

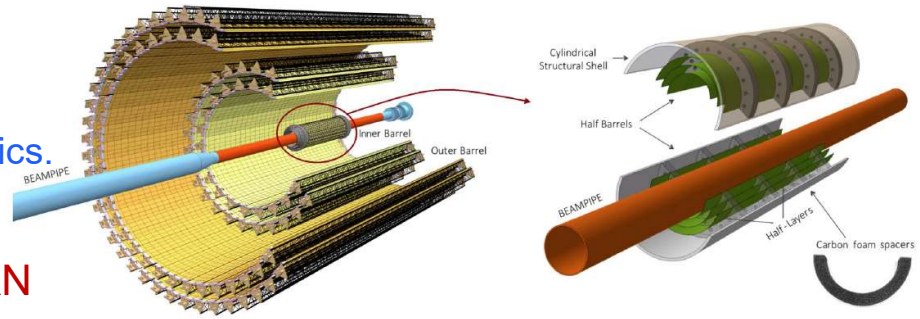
Updated disk reference geometry:

- 5 disks on either side of the nominal IP,
  - z = -250, -450, -650, -900, -1150 mm
  - z = 250, 450, 700, 1000, 1350 mm
  - inner radii >= 36 mm, outer radii <= 430 mm

Why TPSCo 65nm technology?

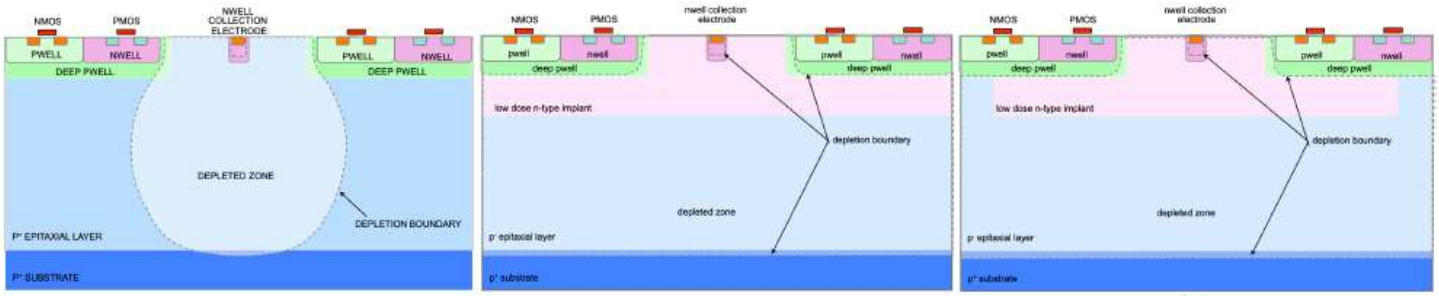
- The ePIC Vertex layers will make use of the curved ALICE ITS3 vertex layers which are designed using TPSCo 65nm technology

- Less material achieves better physics performance.
- Less power consumption allows air cooling.
- Thinned and bent Silicon wafer allow more stable mechanics.
- Mechanics and services will be outside active area.



- Process Validation for Image Sensor done by CERN

- Early designs and structures were taped out as a part of Multi Layer Reticle(MLR) run and was tested in 2021.
- Validated the suitability of TPSCo 65nm for the ITS3 upgrade.
- Collaboration of multiple institutes which performed the study of pixels, high speed I/O's ,different functional blocks and on radiation tolerance.
- Advanced designs were submitted in 2022 as Engineering Run with the scope of learning about the stitching and yield of large area sensor.

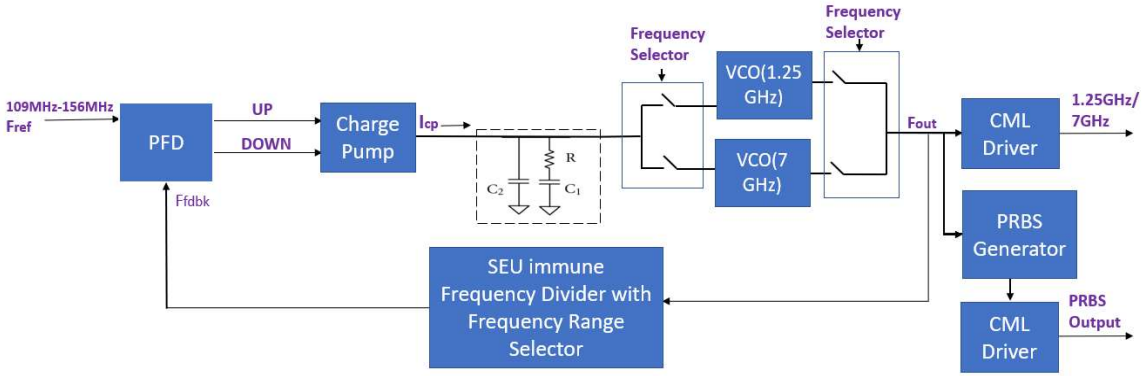


20230525_LHCP_Carnesecchi.pdf (cern.ch)

Science and Technology Facilities Council

TPSCo65nm Designs

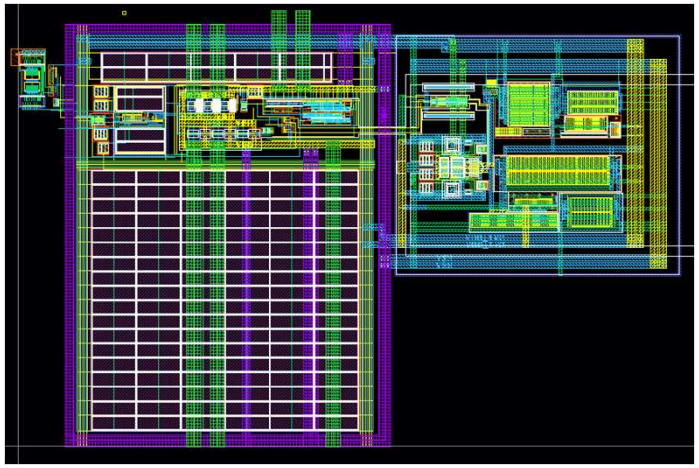
1. Dual Mode Phase Locked Loop



Target Specifications	
Output Frequency	1.25GHz or 7GHz
Input Frequency	156.25 MHz
Period Jitter	<10% of output period
Duty Cycle	45 % - 55 %
Supply Voltage	1.2V +/- 10 %
Power(max)	40mW

❑ Features:

- Dual frequency mode
- 800 MHz-2GHz in the lower frequency mode
- 5.5GHz to 7GHz in the higher frequency mode
- Radiation Tolerance(SEU)
- Shared Loop filter to optimise silicon Area
- Integrated PRBS Generator



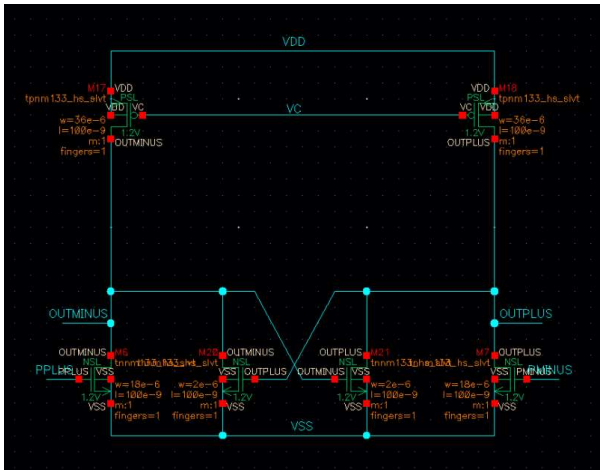
Layout Size : 400umx300um

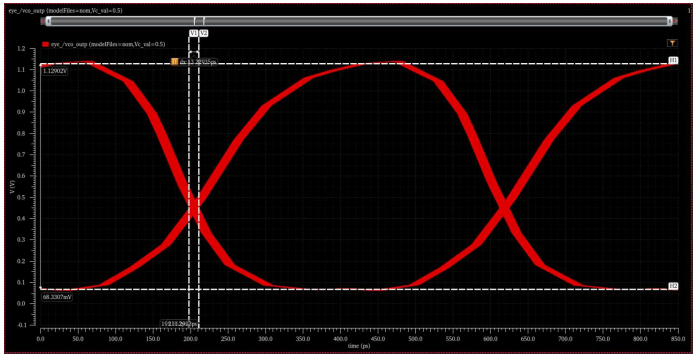
Building blocks of PLL

Voltage controlled Oscillator:

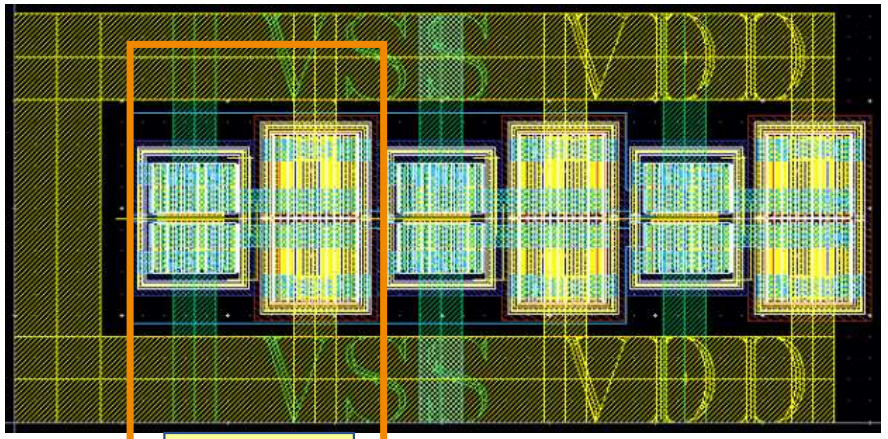
- Operates up to 10GHz.
- Cross coupled delay cell based architecture
- Architecture uses no tail current biasing which reduces the phase noise
- Rail to rail swing mode
- NMOS latch to speed up the transition and make the circuit less sensitive to supply voltage variation and ground bouncing

Delay Cell





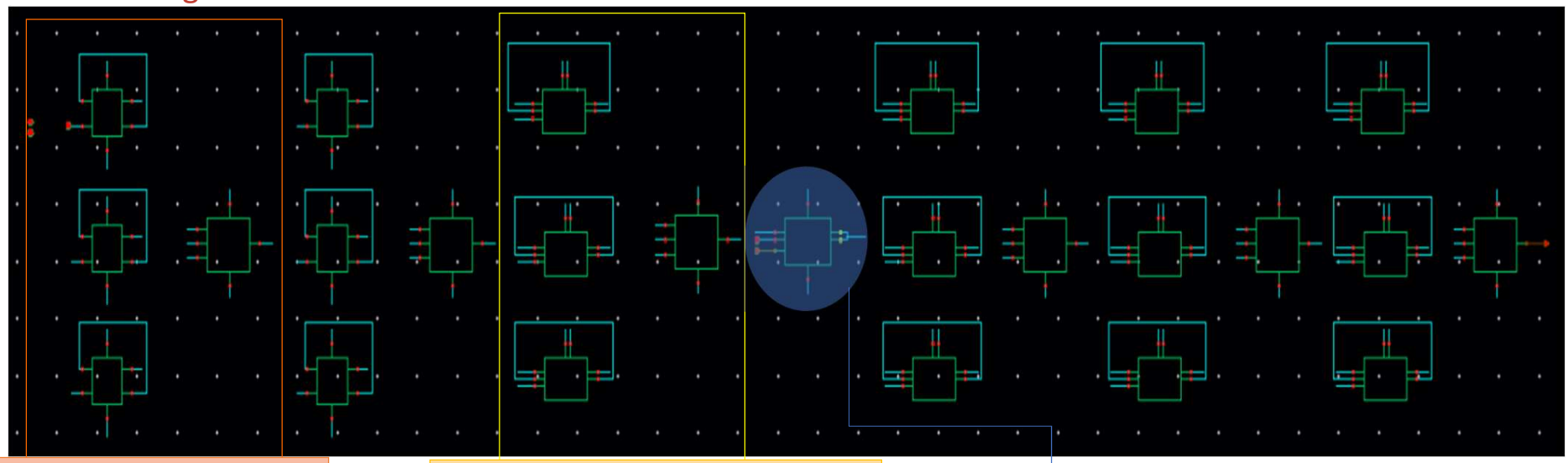
Eye diagram(OUTP) :
Eye opening :1.129V



Layout Of VCO

64 / 8 Frequency divider

First stage



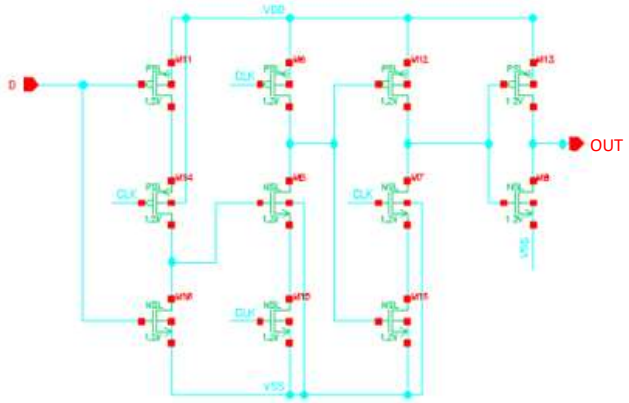
TSPC FF's in combination with TMV

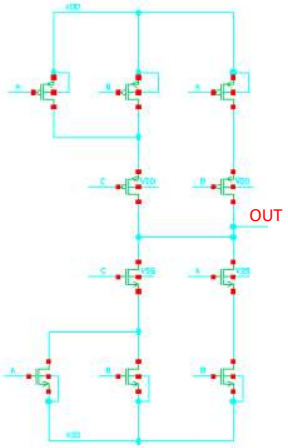
Standard FF's in combination with TMV

Divider selector switch

- Frequency divider with the option to select two divider ratios (64 and 8).
- Different frequency options are possible as the output of each divider stage can be used as PLL output.
- TSPC(True Single Phase Clock) Flip-flops are used for high frequency operation.
- Triple Majority Voter is used for SEU immunity

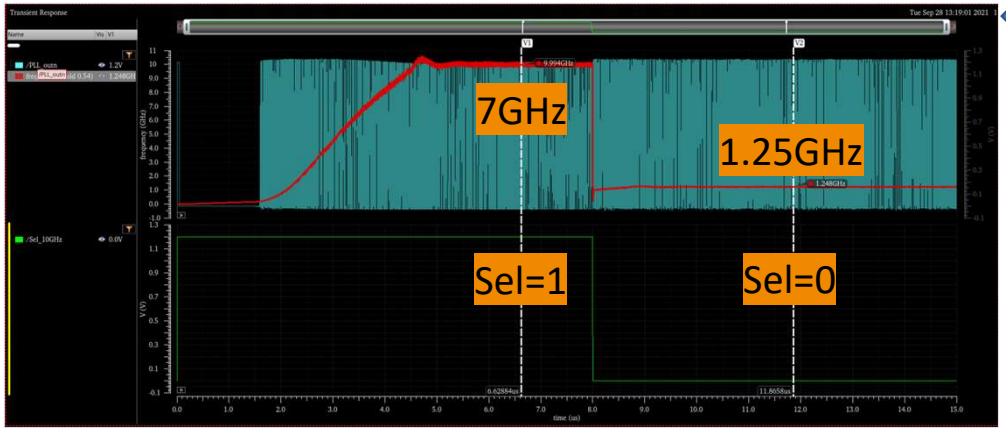
TSPC Flip flop and Triple Majority Voter



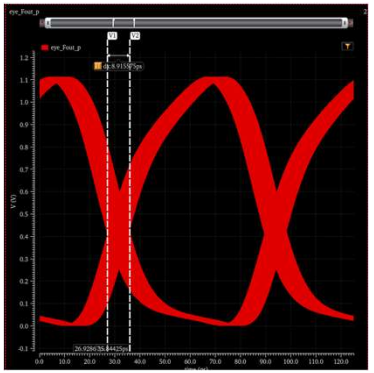


- True Single Phase Clock Flipflop(TSPC) is used for the initial stages for its high frequency operation capability.
- SEU Hard Majority Voter for triple redundancy makes the PLL suitable for EIC environment

PLL operation



Dual Frequency operation



Eye Diagram

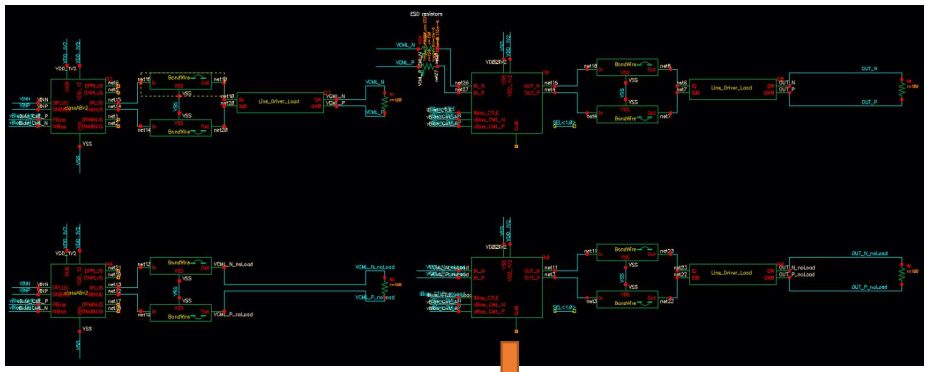
PLL Simulation Results

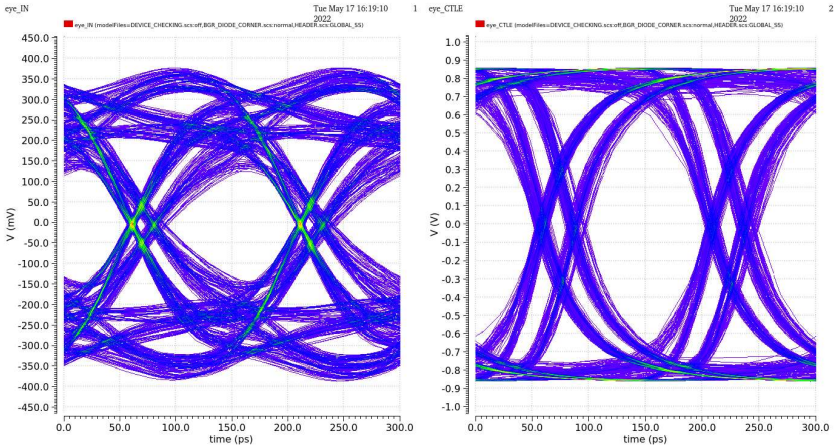
Parameters	
Output frequency	5.5GHz to7GHz OR 800 MHz-2GHz (for input frequency:109MHz-156.25 MHz)
Period Jitter	<7%of output period
Duty Cycle	45% - 55%
Supply Voltage	1.2V +/- 5 %
Power(max)	38mW

2. High Speed I/O's :Current Mode Logic (CML) Receiver

- Continuous time linear equaliser (CTLE) in combination with CMOS to CML circuit operates up to 10GHz

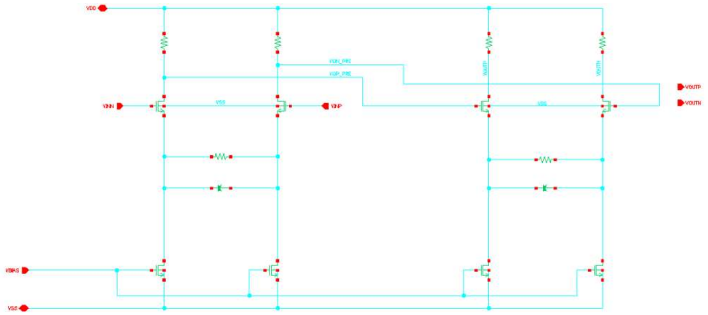
Test set up of CML link simulation to verify the influence of CTLE

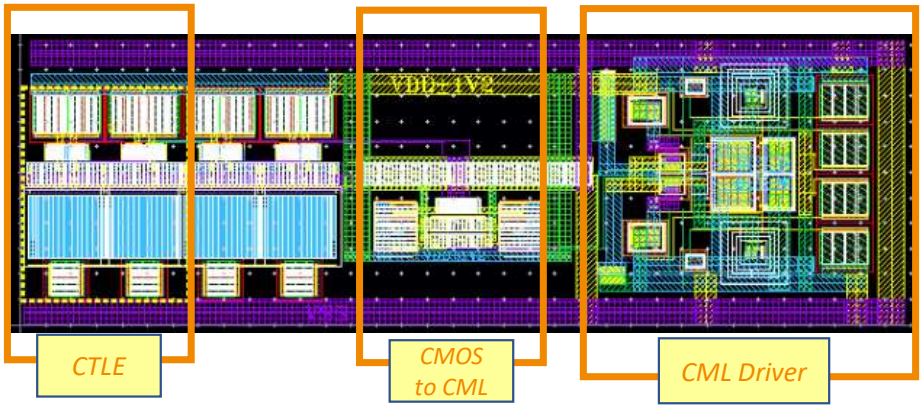




Corrected waveform

Continuous Time Linear Equaliser single stage

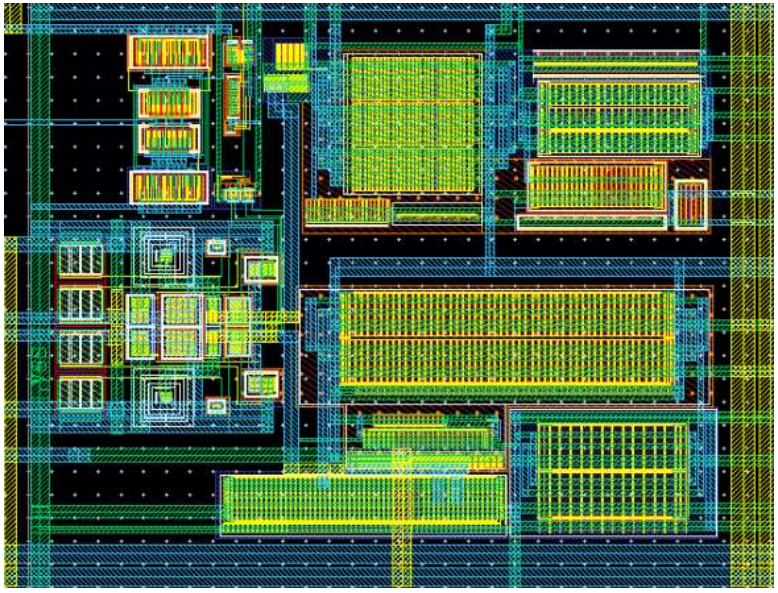


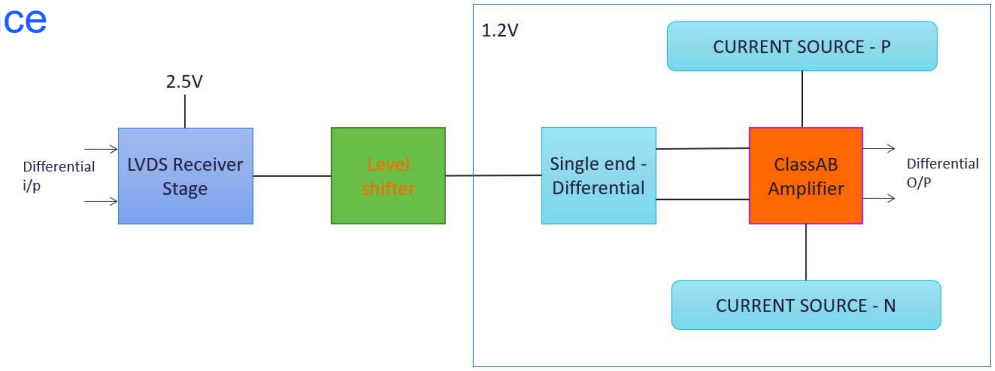


Layout : 170umX 60um

High Speed I/O's : LVDS receiver and CML driver

- Was done to check the suitability of TPSCo 65nm process for the proposed upgrade
- Study power schemes, speed, radiation tolerance
- CML driver operational up to 10GHz



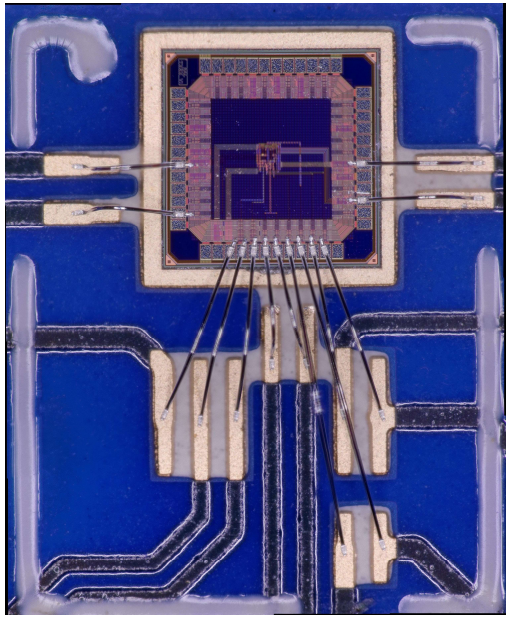


Specifications

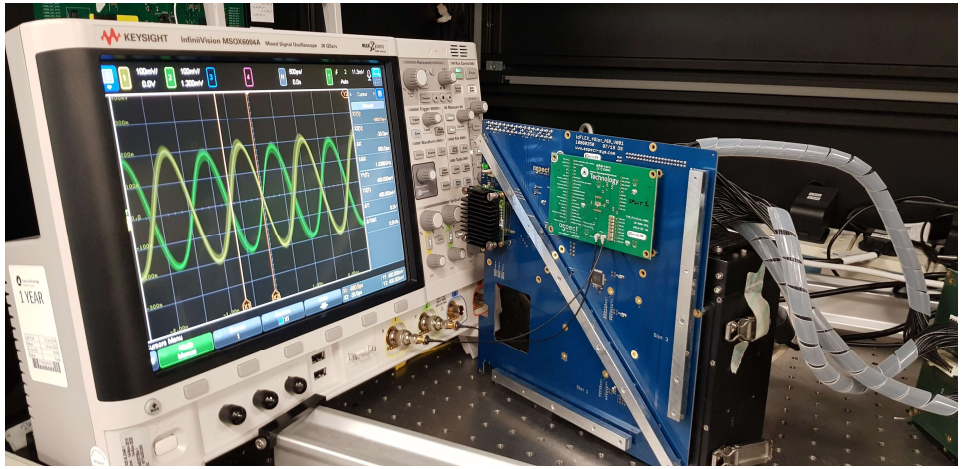
Frequency	1GHz
Input Swing	300mVpp(VCM=1.25 V)
Eye Aperture	>150mV
Duty Cycle	45%-55%
High Voltage Supply	2.5V+/- 10%
Low Voltage Supply	1.2V+/- 10%

Test Results of high speed I/O's

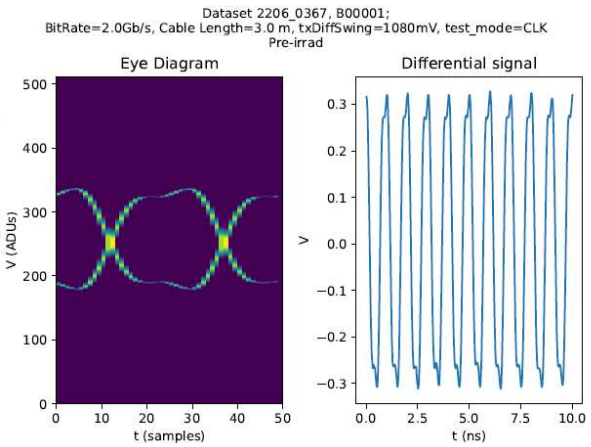
LVDS receiver and CML driver
Bonded (MLR1)



Initial Set up that was used to do the measurement



Test Results done at
Daresbury



VDD 2V5= 2.5V
VDD 1V2= 1.2V
2206_0367
eye_hpos: edge left w.r.t eye centre: -15 ; -3.0000E-10 s
eye_hpos: eye left w.r.t eye centre: -11 ; -2.2000E-10 s
eye_hpos: eye right w.r.t eye centre: 10 ; 2.0000E-10 s
eye_hpos: edge right w.r.t eye centre: 14 ; 2.8000E-10 s
eye_width: noise left: 3 ; 6.0000E-11 s
eye_width: noise right: 3 ; 6.0000E-11 s
eye_width: eye width: 22 ; 4.4000E-10 s
eye_vstat: mean bottom: 187.9807732546471 ; 7.5192E-01 V
eye_vstat: mean top: 328.35964809592224 ; 1.3134E+00 V
eye_vstat: std.dev. bottom: 1.2320215331126614 ; 4.9281E-03
eye_vstat: std.dev. top: 1.3913691244797908 ; 5.5655E-03 V
eye_vpos: bottom w.r.t eye centre: -62 ; -2.4800E-01 V
eye_vpos: top w.r.t eye centre: 66 ; 2.6400E-01 V
eye_vpos: eye height: 129 ; 5.1600E-01 V

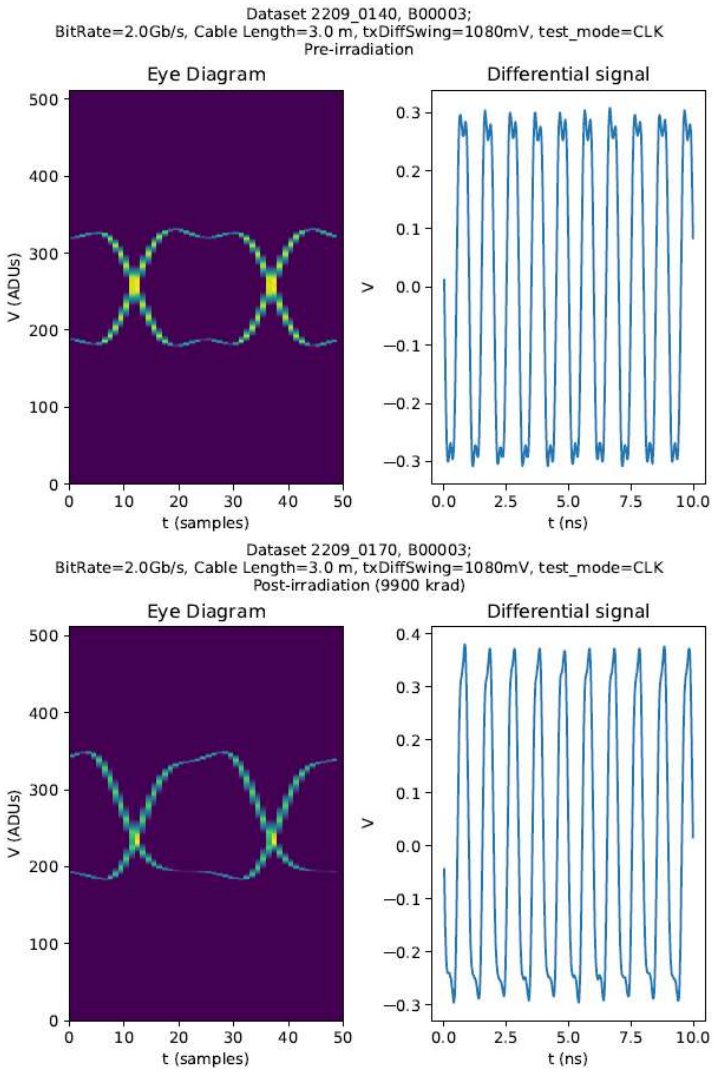
Test Results of high speed I/O's

- 5 DUTs irradiated at CERN.
- DUTs operated in CLK mode: mostly at 2.0Gb/s
- Irradiation steps:

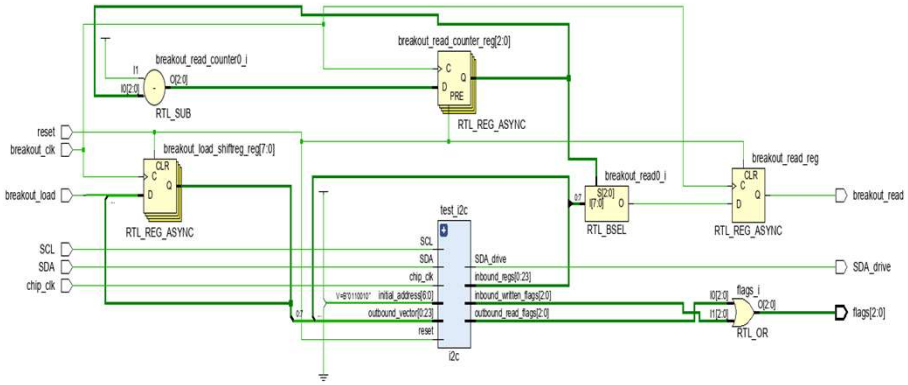
0krad; ~100krad; ~200krad; ~500krad;
~1Mrad to ~10Mrad in steps of ~1Mrad

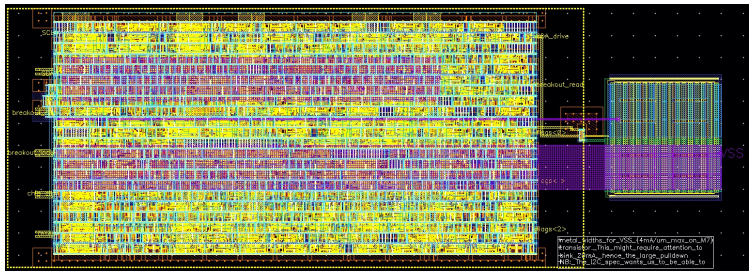
- Functional after the irradiation

Irradiation set up that was used to do the measurement



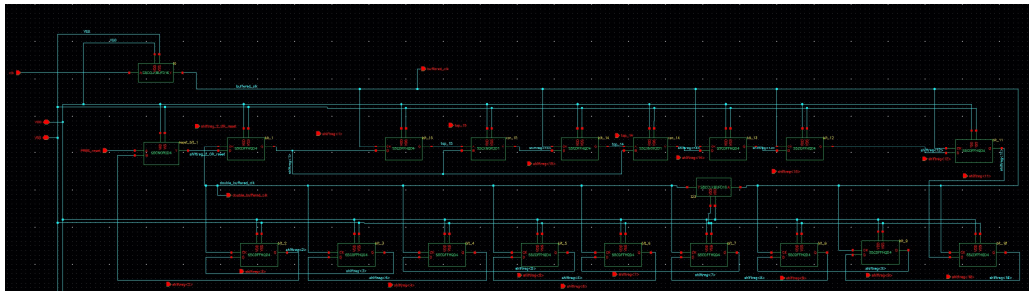
3. I²C Module with TMV

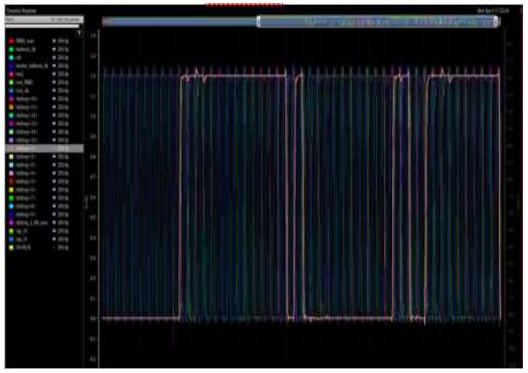


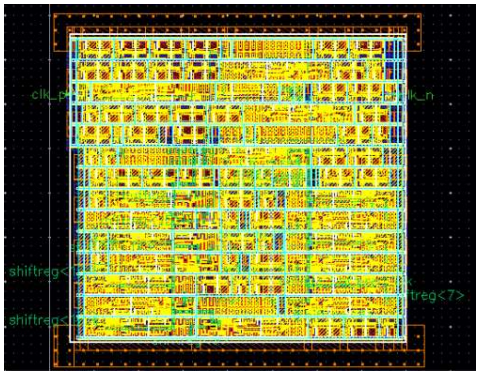


- Radiation hardness using Triple majority voter
- 20mA pull down current

4. PRBS Generator





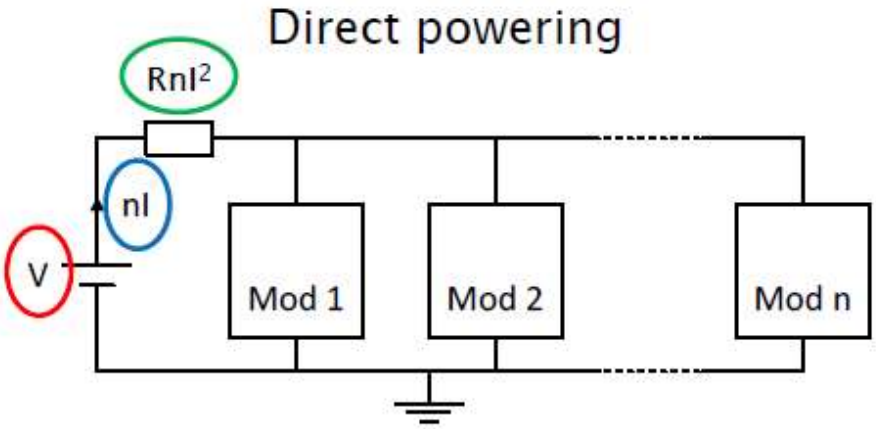


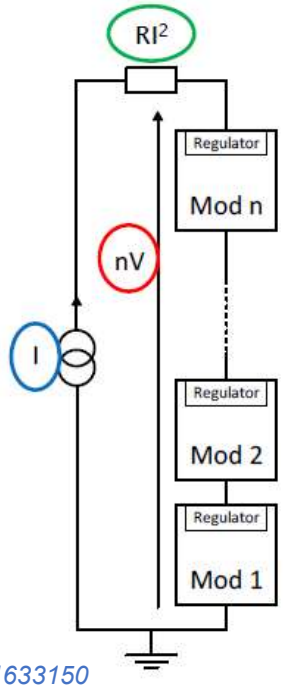
- Based on 16 bit Galois LFSR
- Generates 5Gbps random Bits
- Supports the testing of PLL and CML receiver

Serial Powering of Outer Barrel Layers in the EIC

1.Concept of Serial powering

- Serial powering is a current based powering scheme, where modules are powered in series by a constant current. The current to voltage conversion is done by regulators on module.
- In a serial powering chain made of n modules, the transmitted current is the only current needed by one module.
- The voltage across the chain is nV, where V is the voltage on a module. Each module sits on a different ground potential.
- Higher power efficiency and reduced cable volume.



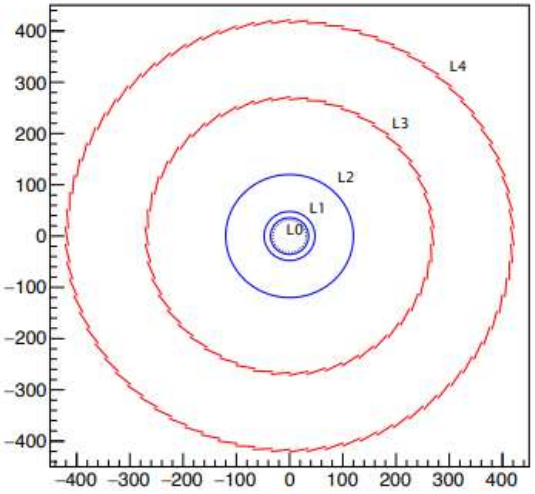


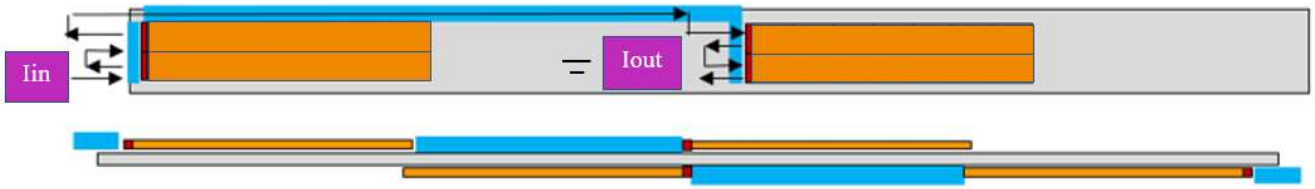
Serial powering

*A serial powering scheme for the ATLAS pixel detector at sLHC JINST **5** C12002*
Low mass hybrid pixel detectors for the high luminosity LHC upgrade https://cds.cern.ch/record/1633150

Proposed Powering scheme for EIC Sagitta Layers

- L3 Barrel layer has 4 sensors per stave and L4 has 8 sensors per stave (4 per side).
- Two master SLDO regulators (analogue and digital domains) per sensor
- In the current conceptual design, serial powering chains of 2 and 4 sensors are envisaged for L3 and L4 respectively
- Current is reduced by a factor of 2 in L3 sagitta layer and by a factor of 4 in L4





L4 serial powering scheme;
top – stave top view, bottom – stave side view

Pixel Array
Periphery
Power Path
Support

2.Shunt LDO

- Combining the Shunt Regulator and LDO design.
- SLDO has an ohmic characteristic which generates Vin when constant Iin is supplied to the module

LDO regulation loop → constant V_{out}

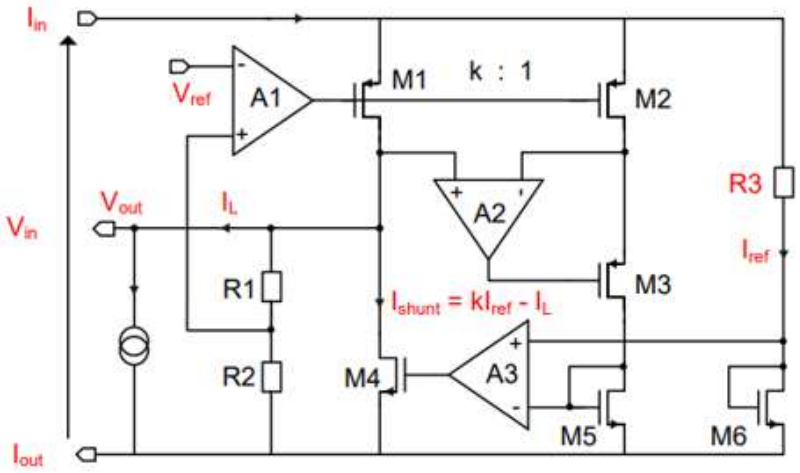
$$V_{out} = 2 \cdot V_{ref}$$

Shunt regulation circuitry → const I_{load}

- I_{ref} set by R3, depends on V_{in} (→ I_{in})
- I_{M1} mirrored and drained in M5
- I_{M1} and I_{ref} compared in A3
- M4 shunts the current not drawn by the load

$$I_{in} \approx kI_{ref} \approx k\frac{V_{in} - V_{thM6}}{R3}$$

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$



Simplified SLDO Diagram

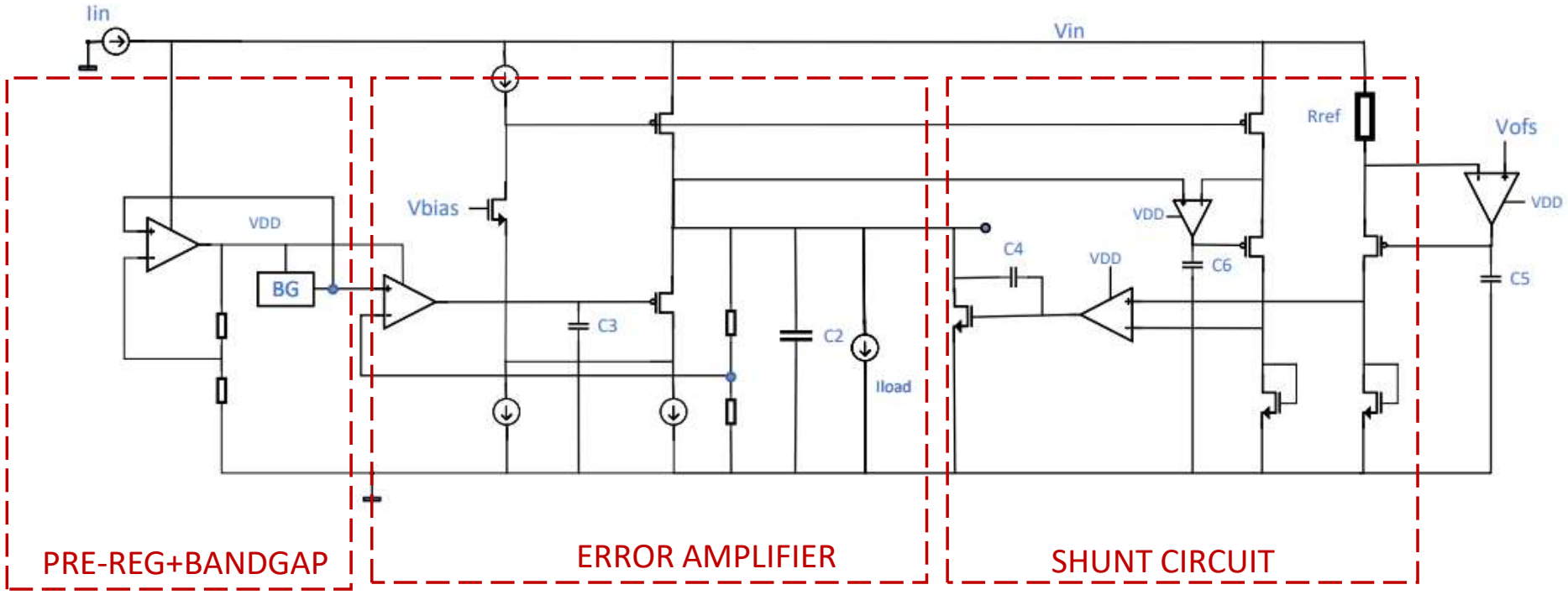
Design Specifications of SLDO

Parameter(Nominal)	
Input Current to the first module	1A
Shunt Current	400mA
Input voltage(for each module)	2V
Output voltage	1.2V
Reference input	0.6V
Load current	200mA

M. Karagounis, D. Arutinov, M. Barbero et al. 'An Integrated Shunt-LDO Regulator for Serial Powered Systems'. In: Proc. of the European Solid-State Device Conference, ESSCIRC 2009 (2009), pp. 276–279. doi: 10.1109/ESSCIRC.2009.5325974.

https://indico.cern.ch/event/879686/contributions/3706455/attachments/1975390/3287622/SLDO_RD53B_Features.pdf

Implementation of Shunt LDO



- Flipped voltage follower architecture for faster transient response without using an off-chip capacitor.
- Pre-regulator to generate 1.2 V supply voltage for the amplifiers

Features of SLDO

❑ Over Voltage Protection:

- Protects the circuitry in case of over voltage, for e.g., Failure of one/multiple module failure.
- Operated in parallel to SLDO
- Takes all excess current in case Vin =>2v

❑ Under shunt Protection:

- Protects the regulator from exceeding load currents
- High load current reduces shunt current
- In under shunt current situation, Vref is reduced and current to the output is reduced.

❑ Configurable Offset Voltage

- To improve the shunt current accuracy

❑ Start Up circuits

- Reference current can't reach the desired value during power up, a further current is added to increase reference values.
- As soon as the preregular bandgap is activated, startup circuit will be switched off.

Conclusion

- TPSCo 65nm IP's development:
  - High Speed I/O's are tested on silicon and are functional up to 2Gbps.
  - Dual mode Phase locked loop design is simulated, and results are presented.
  - High speed Current mode logic receiver ,I2C module, PRBS Generator are simulated and are taped out.
- Serial Powering of Sagitta layers in Electron Ion Collider:
  - Initial concept of serial powering in the outer barrel layers L3 and L4.
  - Initial design of SLDO core.
  - Design goals for SLDO.

Science and Technology Facilities Council

Thank you