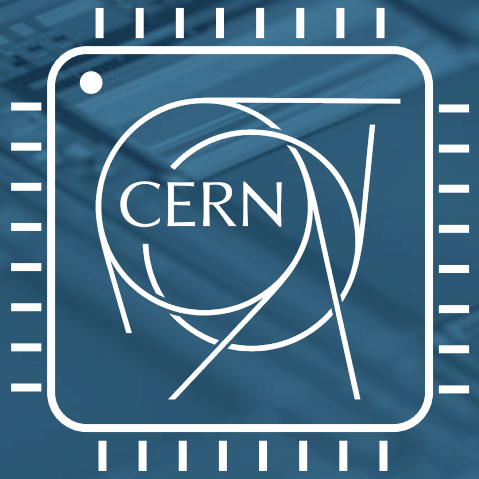
XII Front-End Electronics Workshop

12th – 16th June 2023



ASIC Support & Foundry Services

Kostas Kloukinas – Alessandro Caratelli – Marco Andorno

alessandro.caratelli@cern.ch

CERN ASIC Support & Foundry Services

THE CERN ASIC SUPPORT & FOUNDRY SERVICES FOR HEP

THE COMMON DESIGN PLATFORMS

THE IPs LIBRERY

MORE TOPICS

RESOURCES

SUMMARY

Addressing the challenges

Technology Challenges

- Complex deep-submicron silicon manufacturing processes
- Powerful, Flexible but highly Complex EDA Tools

Design Challenges

- Designs of increasing complexity and size in HEP community
- Novel designs for scientific instrumentation
- Radiation Tolerance
- Power requirements

Productivity Requirements

- Large, fragmented, multinational design teams
- Designers with different levels of expertise
- Work on common design projects
- Costly technologies
- Importance of 'first-time-right' designs!

Enablers for collaborative work

Legal Framework

- Well established commercial contracts with silicon foundries
- 3-way NDAs with Foundries permitting **technology data exchange:**
  - Standard NDAs allow the team to design in a specific technology but do not allow information sharing among universities or institutes
- EULAs of EDA tool providers permitting IP-blocks and libraries sharing
- IP block sharing agreements among design teams
- Export Control regulations

Technical Framework

- Access to common EDA tools
- Common set of technology nodes
- Comprehensive “common design platforms”
  - Foundry PDKs & Foundry IP blocks
  - Rad-Tol IP blocks and IP block repositories
  - Rad-Tol SoC infrastructure
  - Design & Verification methodologies
- Maintenance, Training & Support services

The "ASIC Support" and the "Foundry Access" Services

Bring consistency in the design approaches, technology and and fabrication of ASICs in the HEP community

Special terms where negotiated the first time back in the '97 with the IBM 0.25um process

Later with Fundry-1 and Fundry-2 for a set of selected technologies (the most commonly used in HEP)

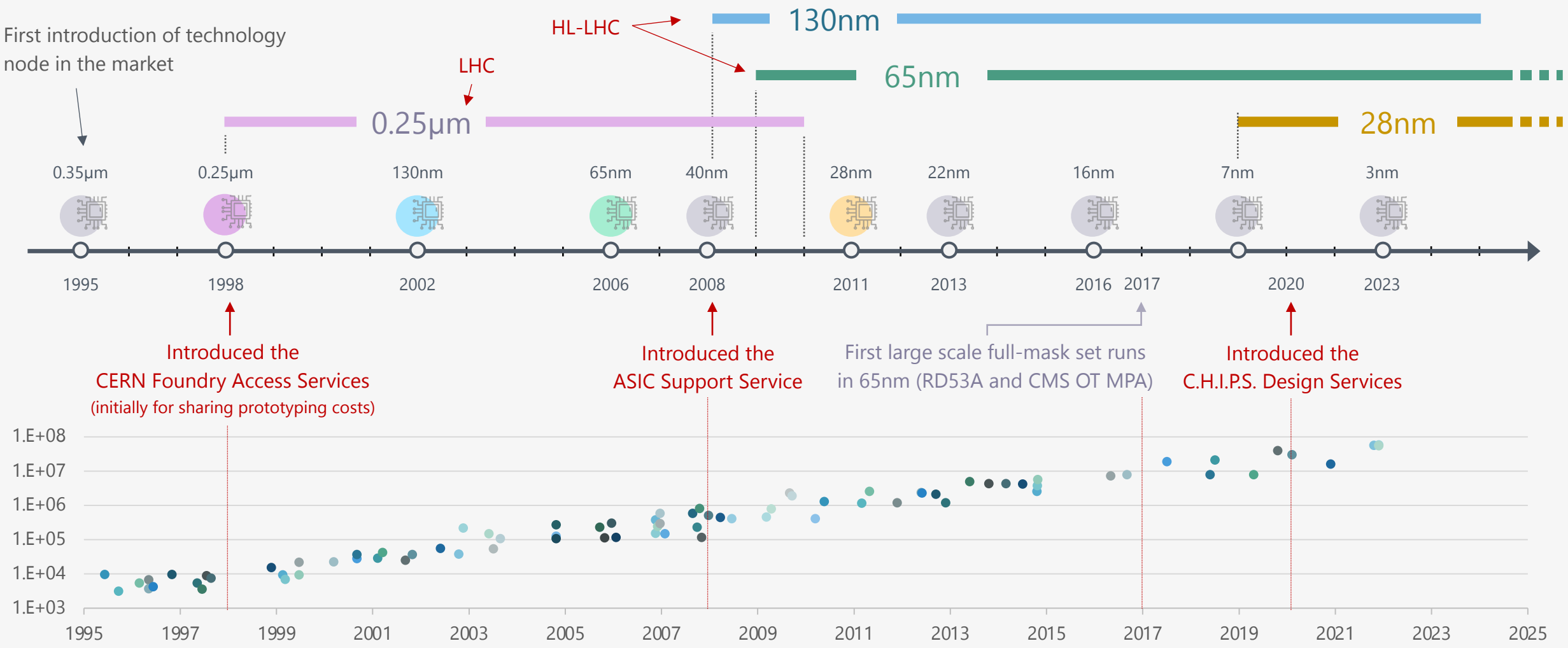
Most common supported technologies:

F1 130nm	F2 130nm	F1 65nm	F1 28nm
CMOS 8RF-DM Stable node, no more updates	*HPC* Last updated September 2022	*LP* Last updated March 2022	*HPC+* Last updated May 2023

It become important to unify the design process providing the community common maintained PDKs and a common library of the basic IP blocks that are needed for most of the designs.

The support was enhanced providing as well technical support, basic design flows and strategies

A bit of history



Average processor number of transistors per chip, [source ourworldindata.org]

ASICs Design Support for High Energy Physics

- Promote the collaborative works and knowledge sharing
- Provide support to HEP community for technology and EDA tool usage
- Enhance, update and maintain the PDKs for commonly used technologies in HEP environment
- Develop and distribute the Common Design Platforms for mixed-signal ASICs design
- Distribution and maintenance of common macro blocks
- Preparation and maintenance of design flows of general use
- Organize training workshops for HEP specific

ASICs Design Support for High Energy Physics

Foundry vendors

IP block vendors

3rd party Design Services

EDA tools

Manufacturing Services

EUROPRACTICE IC SERVICE

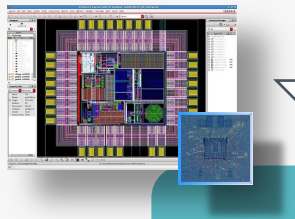
Science & Technology Facilities Council Rutherford Appleton Laboratory

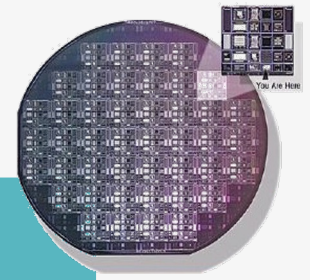
CERN ASIC Support

- **Common design platforms**
- Distribution
- Support

EUROPRACTICE imec

Lead Partner, MPW Service and Communications





HEP Design Teams

The CERN Foundry Access Services

Establish Commercial Contracts with silicon vendors

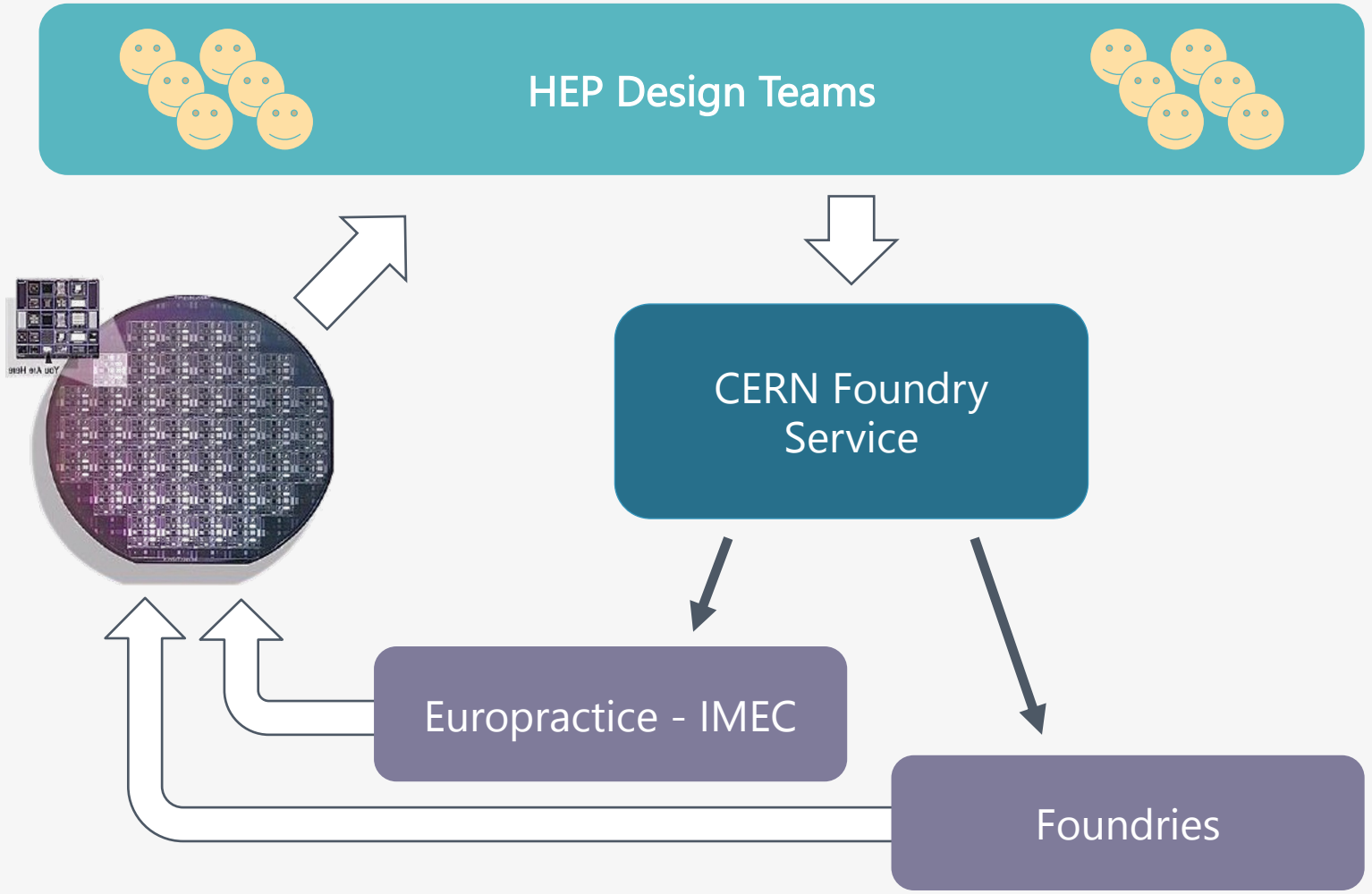
Establish NDAs that allow for collaborative work

Organize prototyping Multi Project Wafer runs, for sharing fabrication costs

Coordinate silicon fabrication: Engineering & Production runs

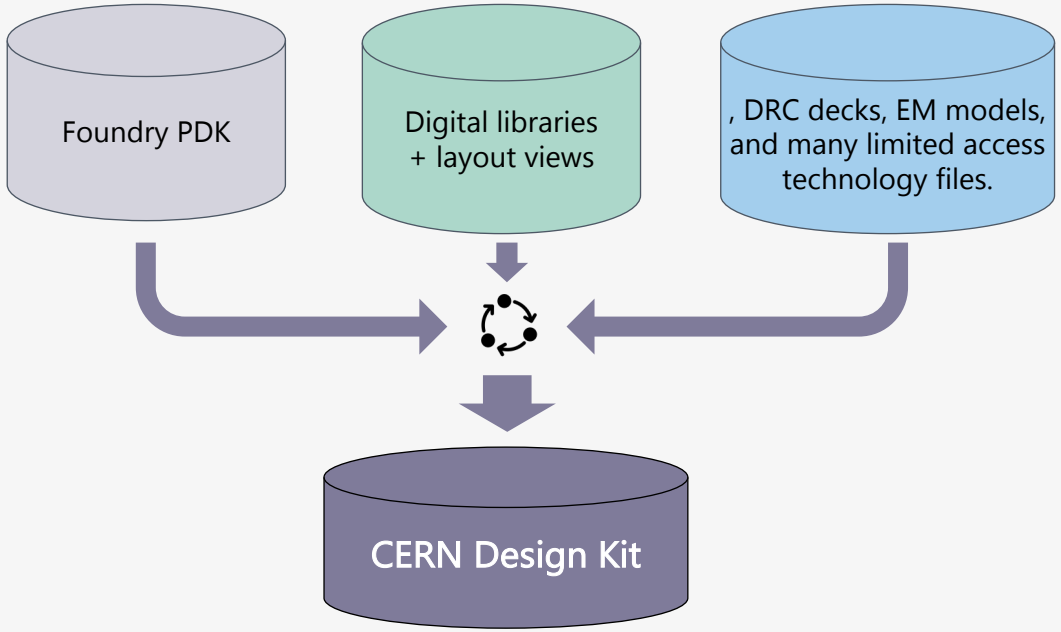
For silicon fabrication services (MPWs, engineering & production runs)
please contact foundry.services@cern.ch

The CERN Foundry Access Services



The CERN Design Kits

CERN enhance the PDK expanding it and tailoring it to our specific design styles and requirements.



Allow for an interoperable mixed analog+digital design flows

- CERN ASIC Support refurbish, maintain and update the PDK
- The CERN Design Kit is optimised to provide a **tested and reliable solution** that provide **Interoperability within the HEP community** avoiding incompatibilities across design teams
- Optimize efforts to integrate a design environment
- The design kits is **updated** following all the major **foundry releases** and, **radiation tolerance requirements** and the **needs and findings of the designers**
- Every year the design kits are tested and eventually adapted to **support the latest EDA tools** Europractice release

Digital libraries

The special 3-way NDA negotiated by the CERN Foundry Service allowed to place the digital libraries (including back-end views) under the same NDA signature therefore allowing the sharing among institutes.

For **28nm** design kit, **57** digital libraries:

- 7, 9, 12 tracks
- 30, 35, 40 nm transistor length
- Ultra-low, low, standard, ultra-high Vt
- Coarse grain libraries (for power gating)
- Power-optimized cells

Front-end

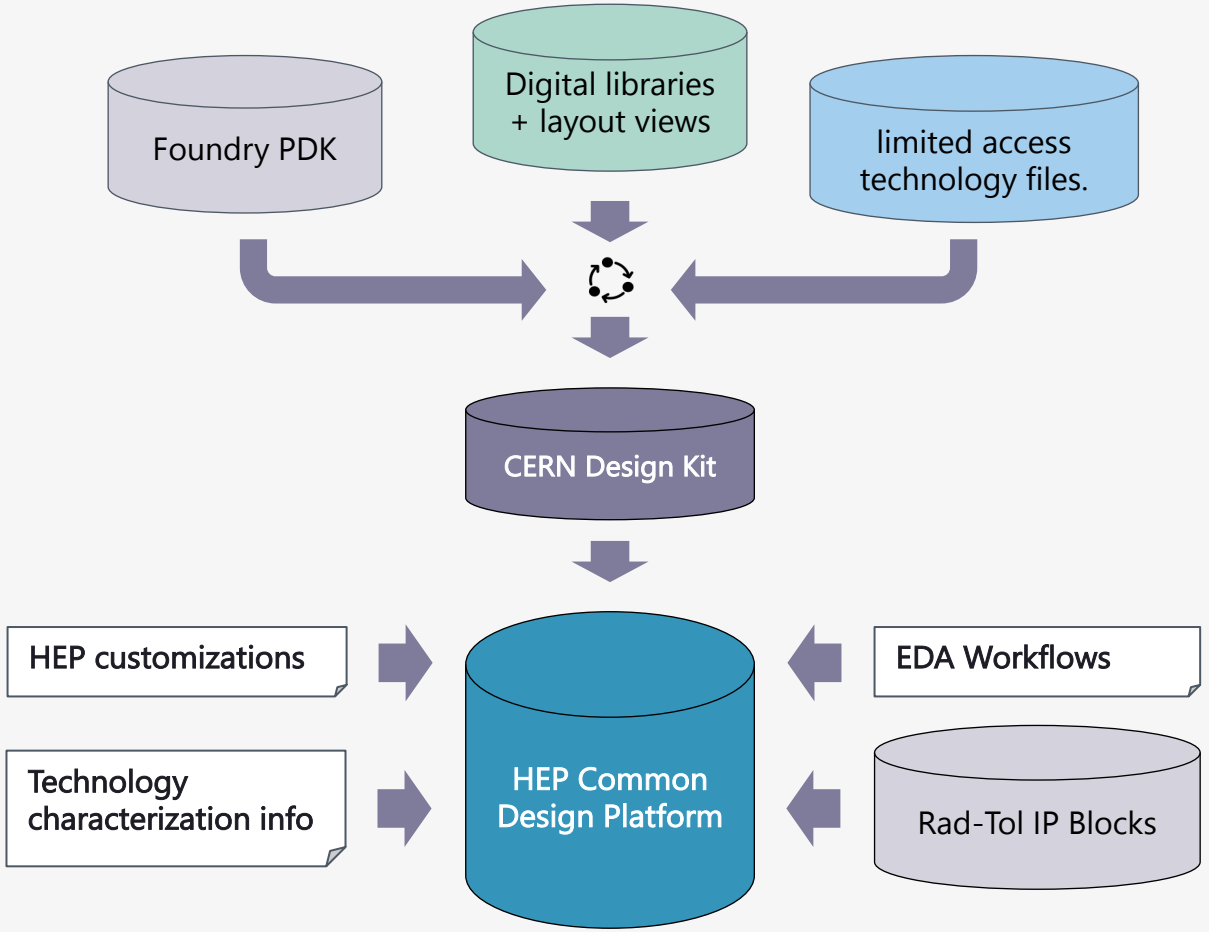
- Timing models (NLDM, CCS, ECSM)
- Stage-based OCV
- Verilog models
- VHDL (VITAL) models
- Mentor DFT models
- LEF
- Cadence OA Abstracts *
- SEE injection models *

Back-end

- SPICE models
- Extracted SPICE models
- GDS
- Synopsys Milkyway db
- Cadence OA Schematics *
- Cadence OA Layout *
- DEF
- CeltIc models

* CERN generated

The HEP Common Design Platforms

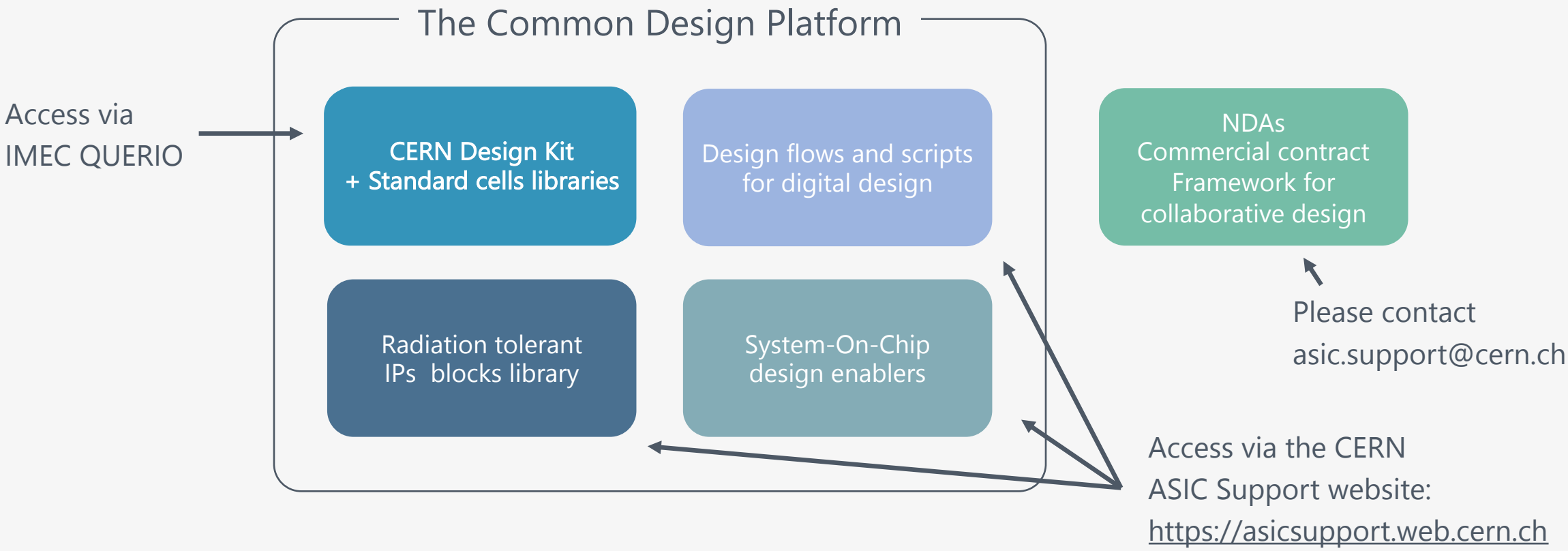


Common ASIC design platforms for HEP community

- **Design kits** that support analog and digital designs
- **Design Workflows** that are standardized and validated using selected EDA tools
- **Compatible Design Workflows** across multiple silicon foundries
- **Rad-Tol IP blocks**
- Maintenance
- Technical Support
- Training

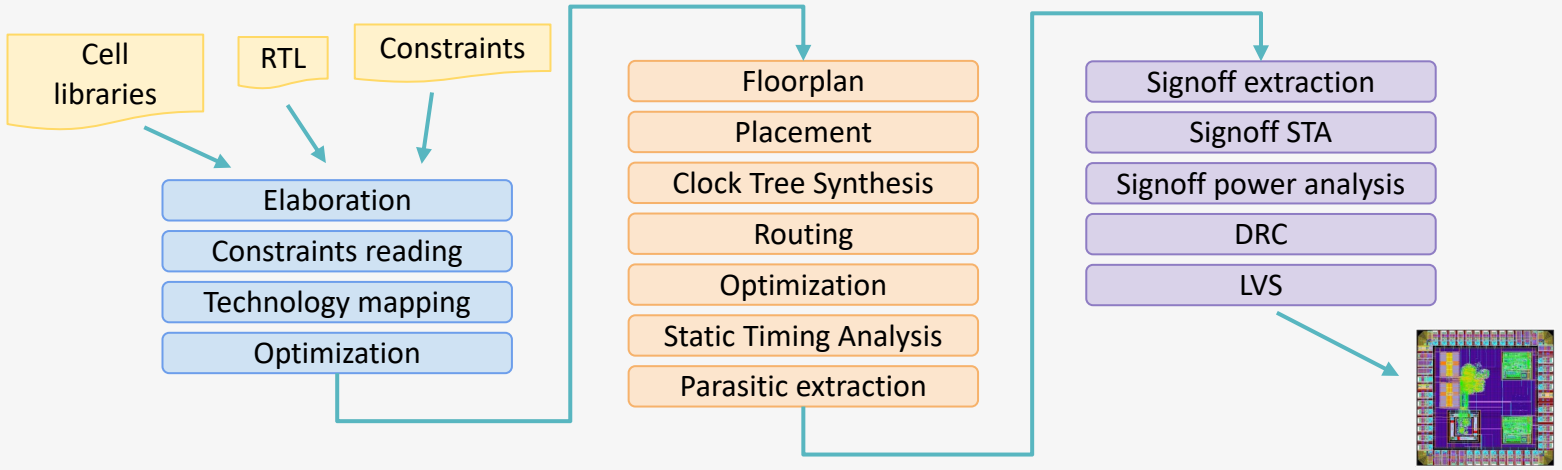
Access to the Common Design Platforms

An integrated solution that provides all the essential instruments, blocks and experience to facilitate the future ASICs collaborative design work



Digital design flows and other useful scripts

- Full digital implementation flow, from RTL to GDS



- Developed to support radiation-tolerant design
- Based on Cadence tools (Genus, Innovus, Tempus, Voltus) and Siemens Calibre for DRC and LVS
- Available for all the technology nodes supported by the service at this link
- It represents an easily customizable flow to start the implementation of complex designs

Digital design flow scrips

For 28 nm, we moved to Cadence Flowkit

- Easier configuration with YAML files
- Self-contained flow steps
- Support for TMR design
- Support for all libraries, OCVs and other Foundry recommendations
- Support for mixed-signal OA database export and sharing

Latest version (v1.2.2) available at:

https://gitlab.cern.ch/asic-design-support/hep28/cern-digital-flow-28nm

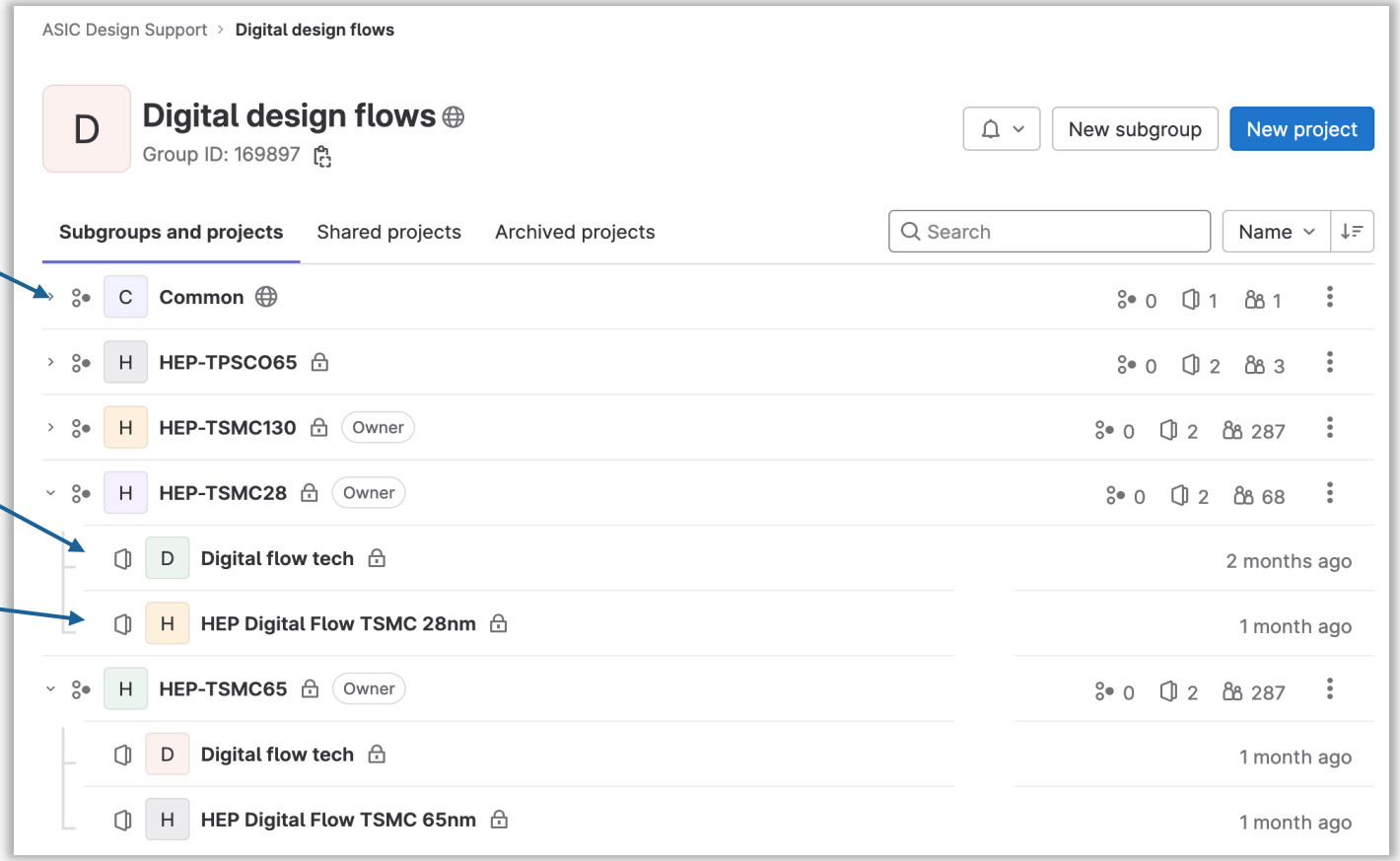
```
- place:
    features:
    args: -owner cadence
    steps:
      - block_start:
      - init_innovus:
      - c_set_ocv:
      - add_clock_spec:
      - c_cts_manage_skew_groups:
      - c_add_clock_route_types:
      - add_clock_htree_spec:
          enabled: "clock_flexible_htree"
      - commit_route_types:
      - c_tmr_set_place_distance:
          enabled: "tmr_design"
      - run_place_opt:
      - block_finish:
      - SCHEDULE: -flow report_place -include_in_metrics

- cts:
    features: #(opt) -setup_views <val> -hold_views <val> -dynamic_v
    args: -owner cadence
    steps:
      - block_start:
      - init_innovus:
      - add_clock_htree:
          enabled: "clock_flexible_htree"
      - add_clock_tree:
      - add_tieoffs:
      - c_tmr_set_tieoffs_distance:
          enabled: "tmr_design"
      - block_finish:
      - SCHEDULE: -flow report_postcts -include_in_metrics

- postcts:
    features: #(opt) -setup_views <val> list of setup analysis_views
      -leakage_view <val> single leakage analysis_view to activate
    args: -owner cadence
    steps:
      - block_start:
      - init_innovus:
      - run_opt_postcts_hold:
      - block_finish:
      - SCHEDULE: -flow report_postcts -include_in_metrics

- route:
```

Digital design flow scrips

Common set of scripts (submodule) **for:**
● synthesis ● implementation,
● signoff STA ● power analysis
● physical verification

Technology specific flow customization
(submodule) NDA protected

Top repository for digital design flow
(with the design specific customization files)



We would be very happy to see more participation from universities in maintaining and improving design flows and add support for other technologies!

RadTol Analog IP blocks library for Fundry-1 130nm (slide for reference)

RAD-TOLERANT AND SEU TOLERANT SRAMs

CERN - IMEC

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

E-FUSEs

Foundry IP block access via CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Rad-Tolerant CERN IO pads

Jan Kaplon (CERN EP-ESE)

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAD-TOLERANT ESD STRUCTURES

Outsourced to SOFICS by the CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAD-TOL BANDGAP REFERENCE VOLTAGE

Stefano Michelis (CERN EP-ESE)

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol Analog IP blocks library for Fundry-2 130nm (slide for reference)

ESD structures for IO pads

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

12-bit, 32-input monitoring ADC

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

LVDS drivers/receivers

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SLVS drivers/receivers

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SRAM generator (40MHz, dual-port synchronous)

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

E-FUSES

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol Bandgap (diode based)

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol DAC: 8-bit, current output, 40 nA LSB

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol Analog IP blocks library for Fundry-1 65nm 1/2 (slide for reference)

RAD-TOLERANT AND SEU TOLERANT SRAMs

CERN - IMEC

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

E-FUSEs

Foundry IP block access via CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SINGLE PORT FUNDRY SRAMs

Foundry IP block access via CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DUAL PORT FUNDRY SRAMs

Foundry IP block access via CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAD-TOL BANDGAP REFERENCE VOLTAGE DIODE BASED

Stefano Michelis (CERN EP-ESE)

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAD-TOL REFERENCE VOLTAGE GENERATOR DTNMOS BASED

Stefano Michelis (CERN EP-ESE)

Used in many HEP designs

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol Analog IP blocks library for Fundry-1 65nm 2/2 (slide for reference)

RAD-TOLERANT ESD STRUCTURES

Outsourced to SOFICS by the CERN ASIC Support

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Rad-Tolerant SLVS Drivers/Receivers

INFN Bergamo / Pavia

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Rad-Tolerant CERN IO pads

Iraklis Klemastiotis (CERN EP-ESE)

Used in many HEP designs

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RadTol Analog IP blocks library for Fundry-1 28nm 1/3 (slide for reference)

RADIATION TOLERANT ESD PROTECTIONS

- Outsourced to SOFICS by the CERN ASIC Support
- Submitted in 2022. Radiation characterization completed.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RADIATION TOLERANT CMOS IO PAD

- outsourced to SOFICS by the CERN ASIC Support
- Design completed. To be submitted in Sept 2023.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SRAM MEMORIES

- Compilers purchased from the Foundry by the CERN ASIC Support
- We can distribute precompiled memory upon request
- Submitted in 2022. Radiation characterization completed.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

EFUSES

- IP block purchased from the Foundry by the CERN ASIC Support
- To be submitted in Sept 2023.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Details in the dedicated presentation by Franco Bandi: https://agenda.infn.it/event/36206/contributions/202618/

RadTol Analog IP blocks library for Fundry-1 28nm 2/3 (slide for reference)

BANDGAP VOLTAGE REFERENCE & TEMP MONITOR

G. Traversi (Bergamo/Pavia) / INFN Falaphel project

Design completed. Submitted in Jan 2022

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SLVS DIFFERENTIAL LINE DRIVERS AND RECEIVERS

Franco Bandi (CERN EP-R&D WP5)

Design completed. Submitted in Jan 2022

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAIL TO RAIL OPERATIONAL AMPLIFIER

Jan Kaplon (CERN EP-ESE)

Design completed. To be submitted in Sept 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

LOW-POWER RAIL TO RAIL OPERATIONAL AMPLIFIER

Markus Piller (DOCT, CERN EP-R&D WP5)

Design in progress. To be submitted in Sept 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIGITAL TO ANALOG CONVERTER (8-BIT)

Markus Piller (DOCT, CERN EP-R&D WP5)

Design completed. Submitted in Jan 2022

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAIL-TO-RAIL DIGITAL TO ANALOG CONVERTER (8-BIT)

V. Sriskaran (CERN EP-ESE)

Design in progress. To be submitted in Sept 2023.

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Details in the dedicated presentation by Franco Bandi: https://agenda.infn.it/event/36206/contributions/202618/

RadTol Analog IP blocks library for Fundry-1 28nm 3/3 (slide for reference)

ΣΔ ADC for monitoring (12b incremental/16b free running)

Tobias Hoffman (CERN EP-ESE)

Design in progress. To be submitted in Sept 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

ΣΔ ADC for monitoring (12b)

O. C. Akgun

Design in progress. To be submitted in Sept 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

TID MONITORING CIRCUIT

Giulio Borghello (CERN EP-ESE)

Design completed. To be submitted in Sept 2023.

datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Multichannel TDC

C. Rudorf (University of Ulm)

Design in progress. To be submitted in Sept 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIGITAL PLL

?

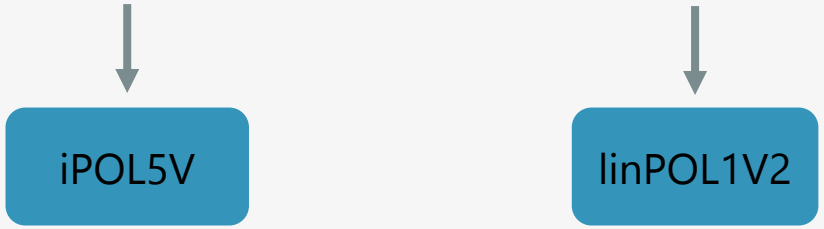
Design will start Q3 2023.

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Details in the dedicated presentation by Franco Bandi: https://agenda.infn.it/event/36206/contributions/202618/

RadTol Analog IP blocks library for 28nm (slide for reference)

Integrated powering solutions on 28 nm (**Stefano Michelis – Giacomo Ripamonti**)



To generate 0.8 – 1V voltage domain

Design in progress at CERN

Design in progress at **TU Graz**

- No external passive components
- Goal TID tolerance in excess of 1 Grad
- Output voltage configurable on the fly
- Custom inductors on 1p9m metal stack

For more info refer to this presentation by Giacomo Ripamonti from the last 28nm Forum

RadTol Analog IP blocks library for 28nm

The CERN ASIC Support is currently taking care of:

- Packaging in an uniform way the IP blocks
- Maintenance of the shared repositories (Cliosoft) and sharing with institutes
- Design and implementation of a test chip that will integrate several of the IP blocks designed up to now (Marco Andorno)
  - Tapeout expected in September 2023 MPW
  - Testing and radiation tolerance characterization will follow

Those IP blocks will be available to the the institutes that have signed the 3-way NDA.

All institutes that wish to contribute are strongly invited to participate to common repositories with analog and digital IP blocks, shared within the community!

Please contact asic.support@cern.ch for more info

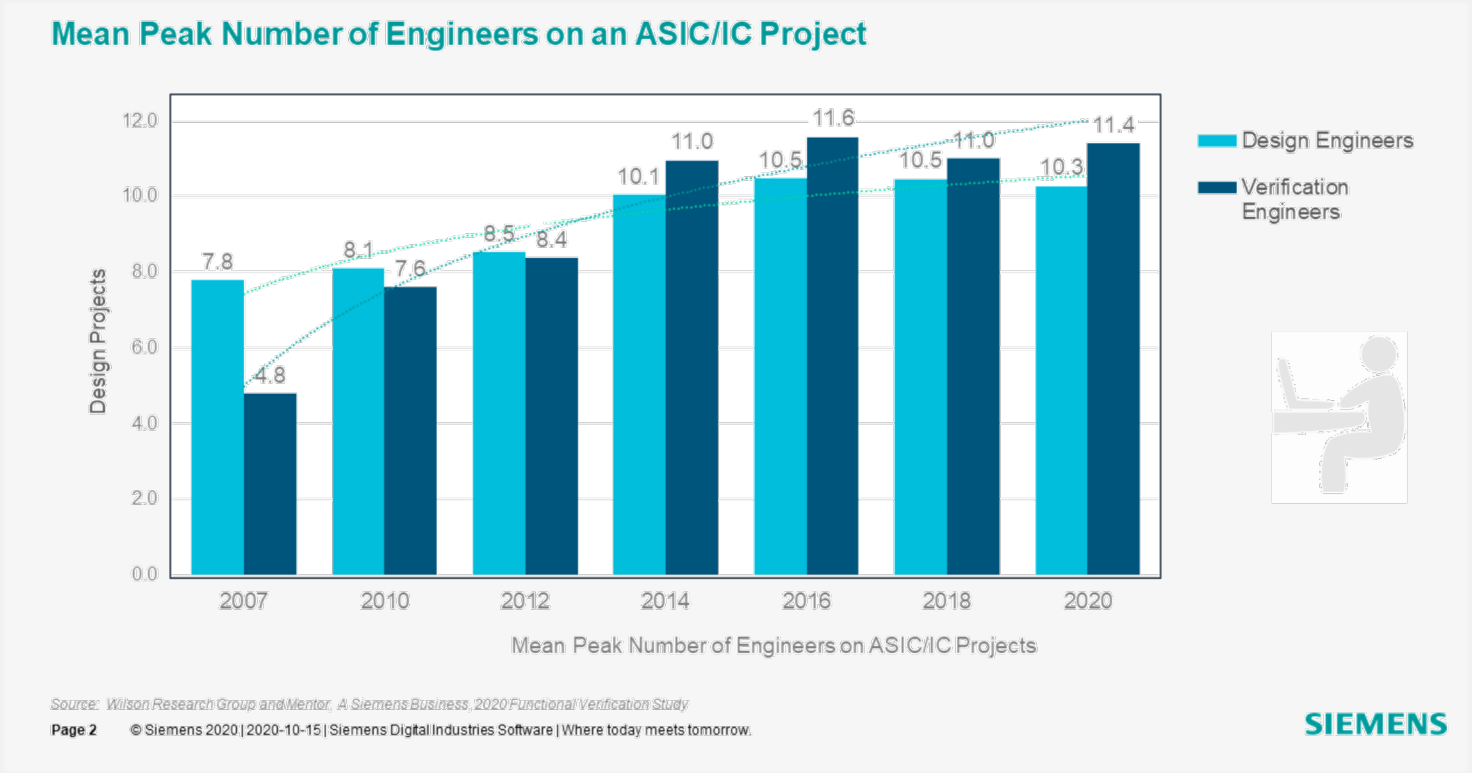
Verification IPs ?

In industry, on average, close to 60% of project time is spent on verification.

Verification cannot be neglected.

Under discussion the possibility to integrate verification IPs in the common design platform for distribution.

The CHIPS activities lead by Xavi Llopart started already building several reusable VIPs



RadTol SoC infrastructure

The increase in **design complexity** calls for the need of a more **abstract design methodology**

Introduce Programmability in the detectors

- Allows retargeting an ASIC for different applications
- Change the algorithms during runtime

Simplify system integration and reduce design time

- Introduce modularity
- Accelerate digital design and speedup verification
- Accelerate physical implementation

Provide a RadTol Digital IP blocks library

- Provide pre-verified building blocks
- All IPs are coherent with a standardize interconnect
- Helps design reusability within the community

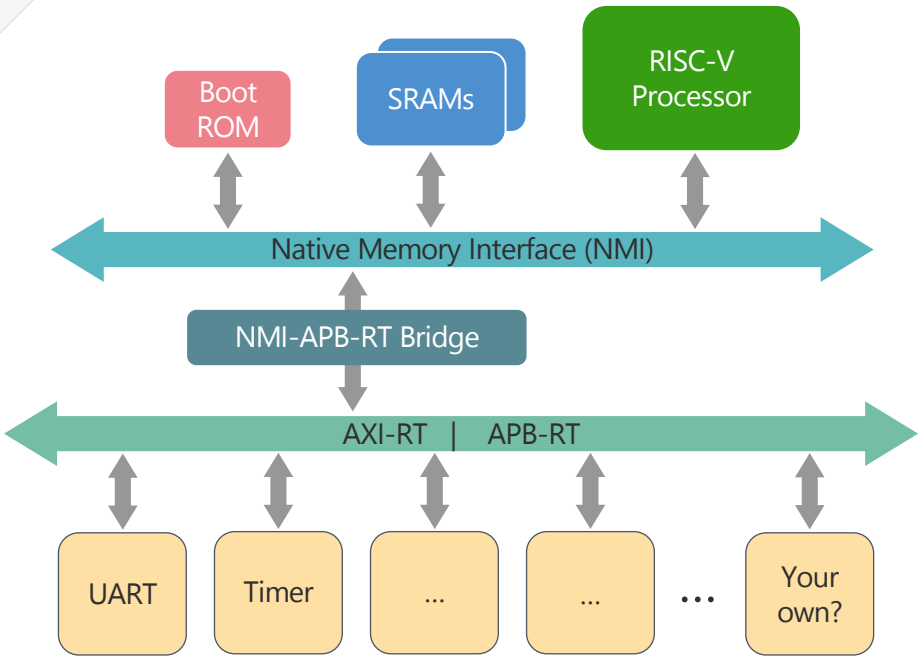
RadTol SoC infrastructure

Radiation-tolerant System-on-Chip platform generation → Faster design and verification turnaround time

> Goal: Generate a flexible and open platform, that can be extended and tailored with custom hardware blocks, peripherals and ASIPs, and embedded in future complex ASICS

- It aims to provide a complete workflow for simulating, designing and implementing fully customizable System on Chip designs
- Abstract design approach to tackle complexity increase
- Software programmability
- Currently several tools are under development for automatizing:
  - RadTol interconnects generation (AXI-RT, APB-RT)
  - Drivers generation
  - Verification components generation (System-C UVM)
  - Documentation generation
  - SEE hardening
  - ---

An example of generation output:



Containers ?

We are currently investigating the possibility of running the EDA tools in containers:

- Aptainer (Singularity fork)
- Investigations started for internal use
- Possibility to provide pre-configured containers to interested institutes for specific set of EDA tools
  - EDA tool installation outside of the container
- Simplify system maintenance
- Uniform environment among interested institutes and universities

Thanks Kennedy Caisley (Bonn university) for the fruitful discussions and support

28nm Technology access & design sharing framework

28nm access and legal framework:

- The foundry “standard” NDA does not allow the disclosure of technology information to third parties and thus prohibits collaborative work
- CERN, IMEC and the Foundry negotiated a HEP specific 3-way NDA that **permits the collaborative work among HEP institutes and universities**
- The **HEP specific 3-way NDA** has similar terms & conditions as the 3-way NDA covering the 130nm and 65nm technologies from the same Foundry
- Since Q1 2022 **the 3-way NDA (CERN-IMEC-Foundry) was signed**
- Consequently, many institutes received and signed their 3-way NDA
- Institutes can contact **CERN ASIC Support Service** asic.support@cern.ch

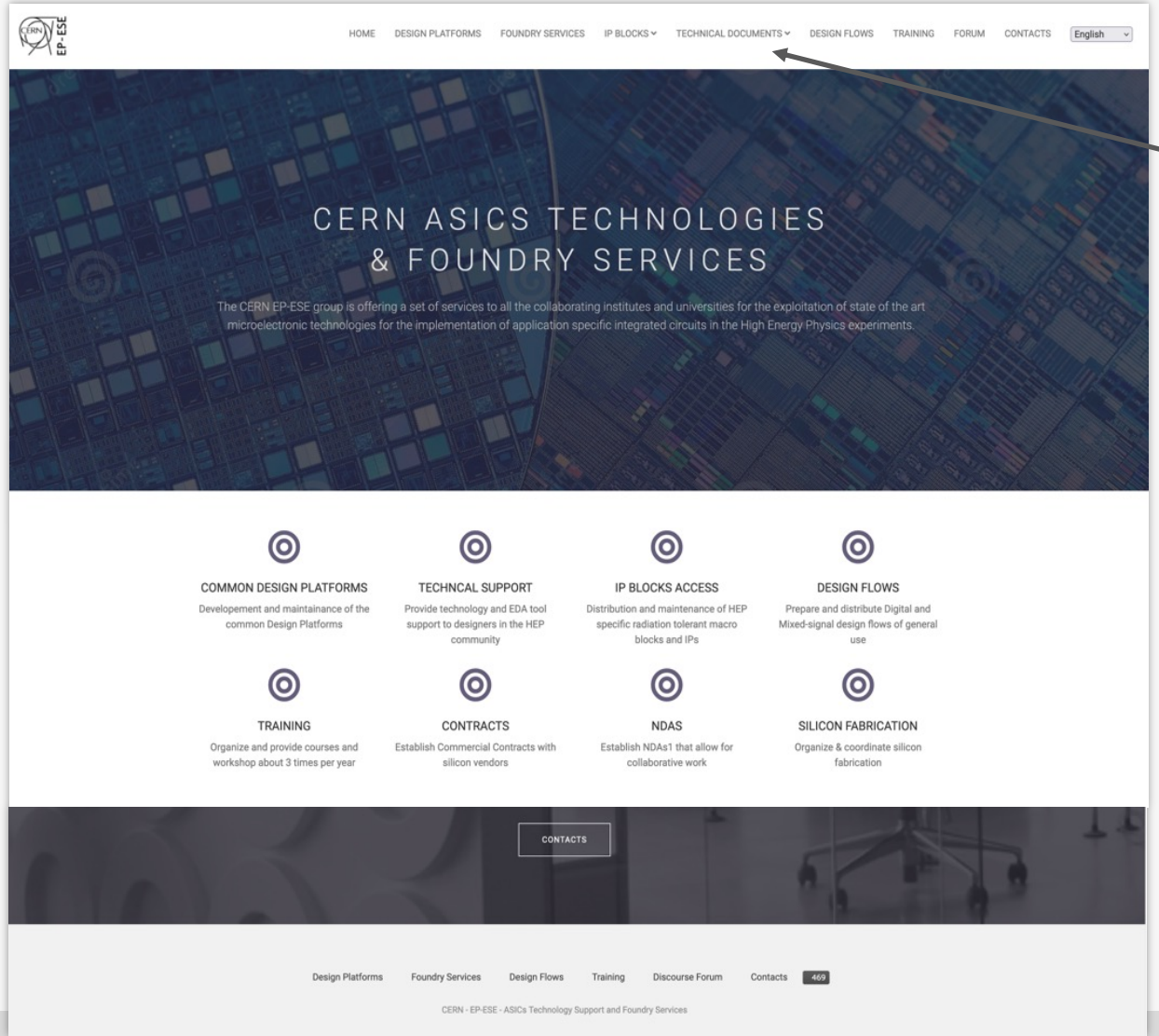
28nm Technology access & design sharing framework

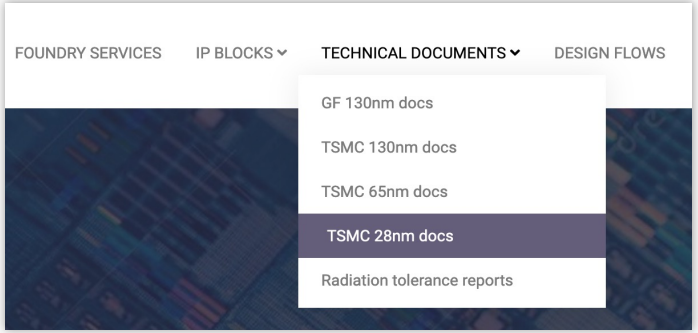
- The 28nm NDA document incorporates a static list of participating institutes (based on 65/130nm NDA list)
  A **dynamic list of institutes** incorporates the static list with additional institutes (newcomers)
  - IMEC maintains the dynamic list of institutes
  - Institutes will be able to consult the dynamic list on the CERN ASIC Support website https://asicsupport.web.cern.ch, to know with whom they can exchange technical information
- The 28nm Common Design Platform is distributed as follows:

I. MSOA PDK (Mixed Signal Design Kit) **via the IMEC QUERIO** platform

II. IP blocks, SRAMs, Radiation Tolerant Macros, Design Flows and Scripts **via CERN ASIC Support Service**:
  - Shared Cliosoft repositories for analog macros
  - Shared Git repositories for digital blocks and scripts
  - Technical website for accessing technology information and tutorials

ASIC Support documentation website





The ASIC Support documentation website is the place for searching documents, IP blocks datasheets, flows and scripts information:

https://asicsupport.web.cern.ch

ASIC Support documentation website

DESIGN MANUALS AND GUIDELINES

March 2, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

In this section you can access the design manuals and PDK documentation

CONTINUE READING

LIMITED-ACCESS DOCUMENTS AND DESIGN GUIDELINES

March 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

In this section you can access the Limited Access documents and design guidelines

CONTINUE READING

CALIBRE DRC RULES

February 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

All Calibre DRC files are in the directory: $PDK_PATH/$PDK_RELEASE/pdk/1P9M_5X1Y1Z1U_UT_AlRDL/cdsPDK /Calibre/drc For ease of updating, rule definitions and switches are kept in separate files, so that when a new rule update comes, there is no need to change the switches as well.

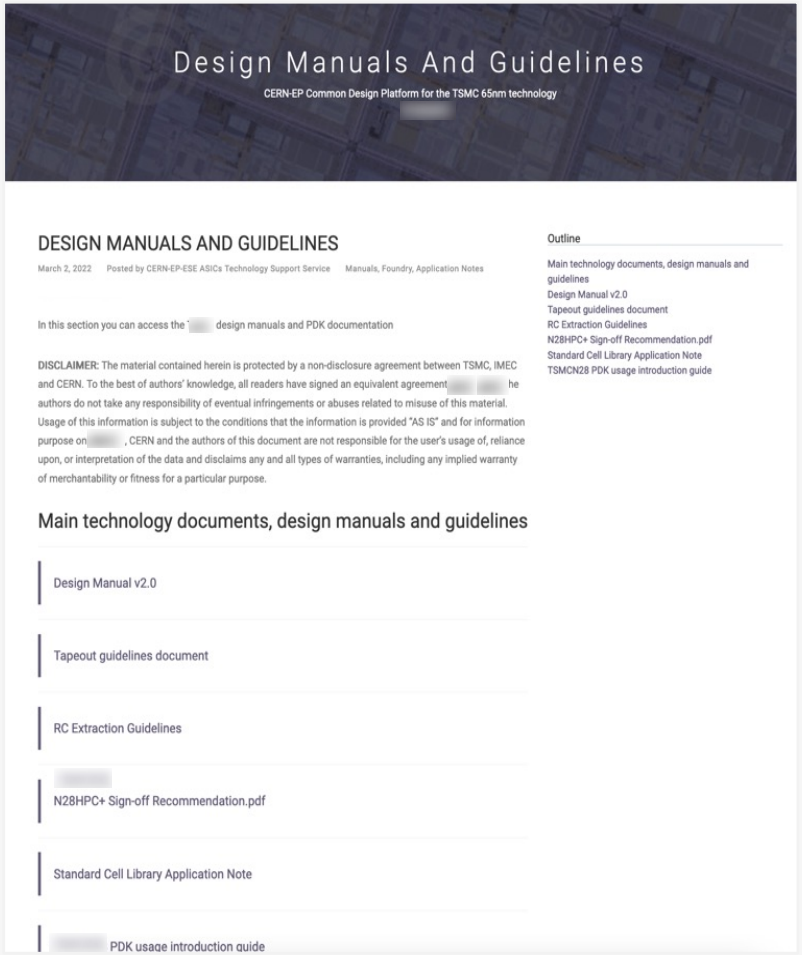
CONTINUE READING

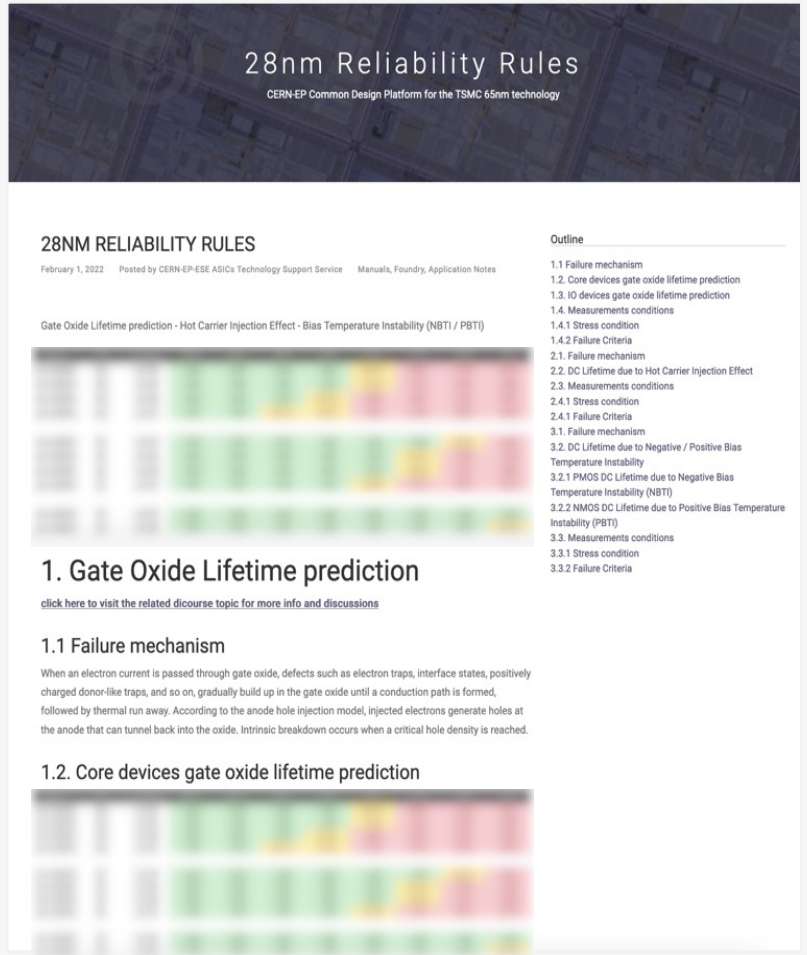
CERN MSOA DESIGN KIT ACCESS AND INSTALLATION

January 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service MSOA Design Kit

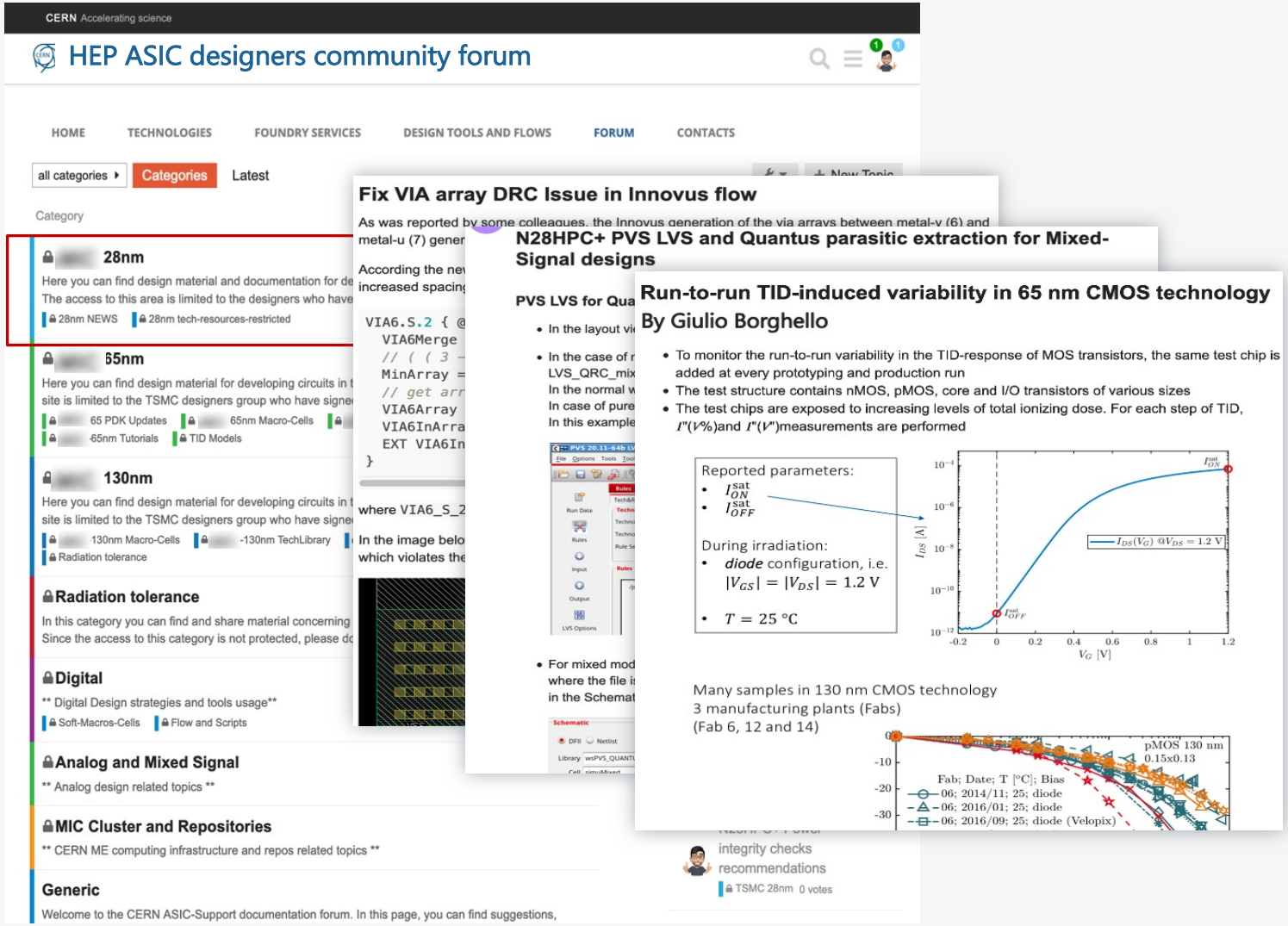
The HEP Common Design Platform is built by CERN EP-ESE in collaboration with Cadence around the 65nm foundry PDK to facilitate the collaborative work among the institutes, supporting the interoperability within the HEP community, avoiding incompatibilities across design teams.

CONTINUE READING





HEP community forum



The forum is a hub for knowledge sharing and open discussion for all things HEP ASICs related: https://asicsupport-community.web.cern.ch/

We encourage everyone to interact with posts, feedback and suggestions to really make these a place for discussion and not a one-way channel.

Training courses

Digital-on-top hierarchical Implementation in workshop

DoT Workshop

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2020 TO 2022: 6 TRAINING SESSIONS

System Verilog Advanced Verification Environment using UVM workshop

Verification / UVM

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

SINCE 2020: **3 TRAINING SESSIONS**
NEXT SESSION TO BE SCHEDULED

Workshop on Mixed-Signal design in 28nm process

MS Designing in 28nm

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the analog and Mixed-Signal design in 28nm, and analog IP characterization
- Learn main concepts about TIDs and SEUs tolerance design
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)

SINCE JAN 2023: **3 TRAINING SESSIONS**
NEXT SESSION AROUND OCTOBER ‘23

A total of 145 Designers from HEP institutes have participated to those training workshops in the last 3 years

We are looking forward in developing new ideas, building methodologies and improve the support and available resources for the HEP community

Get in touch if you wish to collaborate to the future steps!