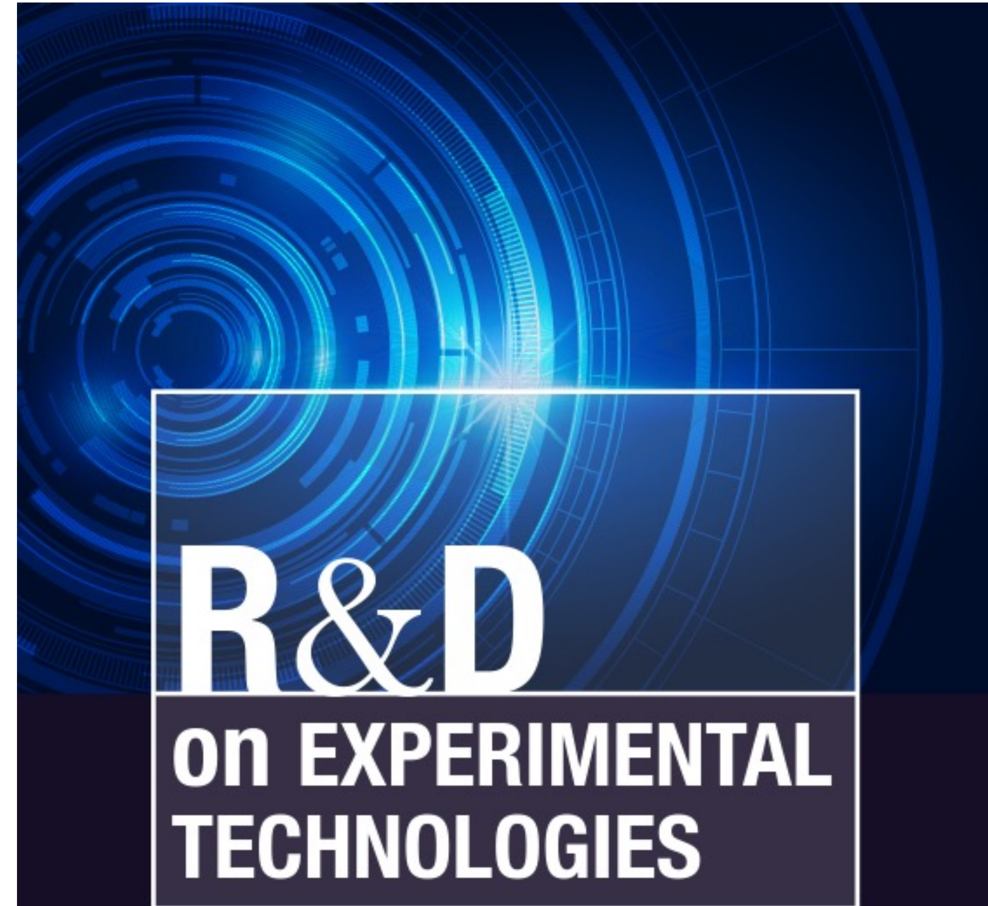
Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

CERN EP R&D

WP1.2 Monolithic Pixel Detectors

Many contributors, see next page

Strong synergy with ALICE ITS3 upgrade



Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

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EP RD WP1.2 on monolithic CMOS sensors

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Long term goal: develop CMOS sensors in sub 100nm technologies

- Synergy with development of the stitched sensor in the ALICE ITS3 upgrade

First technology selected: TPSCo 65 nm CMOS imaging technology

- TPSCo (joint venture TJ & Panasonic): several 65 nm flavors: high density logic, RF, and imaging (ISC)
- ISC preferred: 2D stitching experience, special sensor features, different starting materials, lower defect densities, etc
- Initially 5 metal layers, now 7 metals

First submission: MLR1 December 2020

Second submission: ER1 November 2022

65 nm development profited significantly from 10 years of experience in TowerJazz 180 nm.

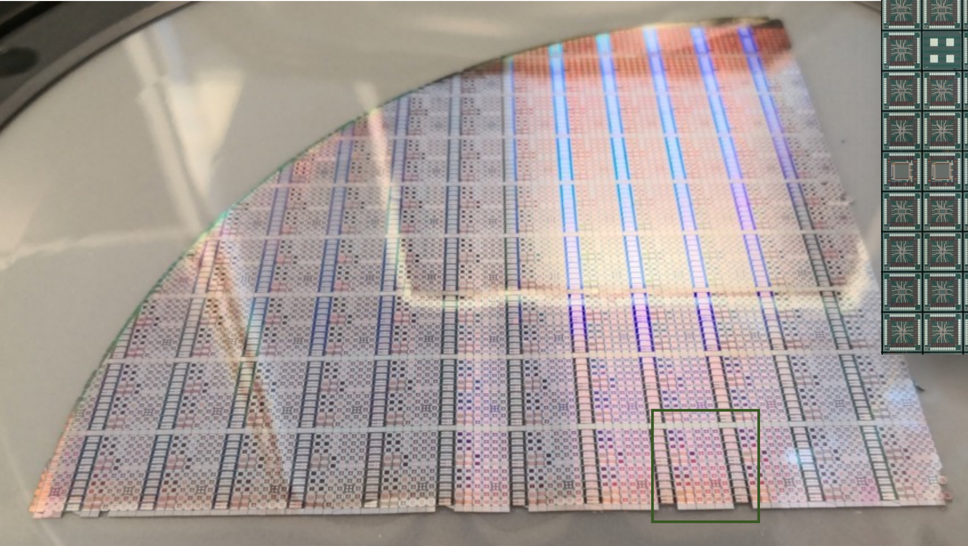
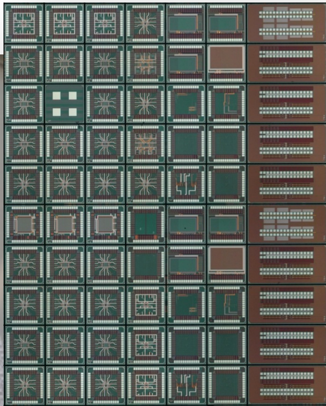
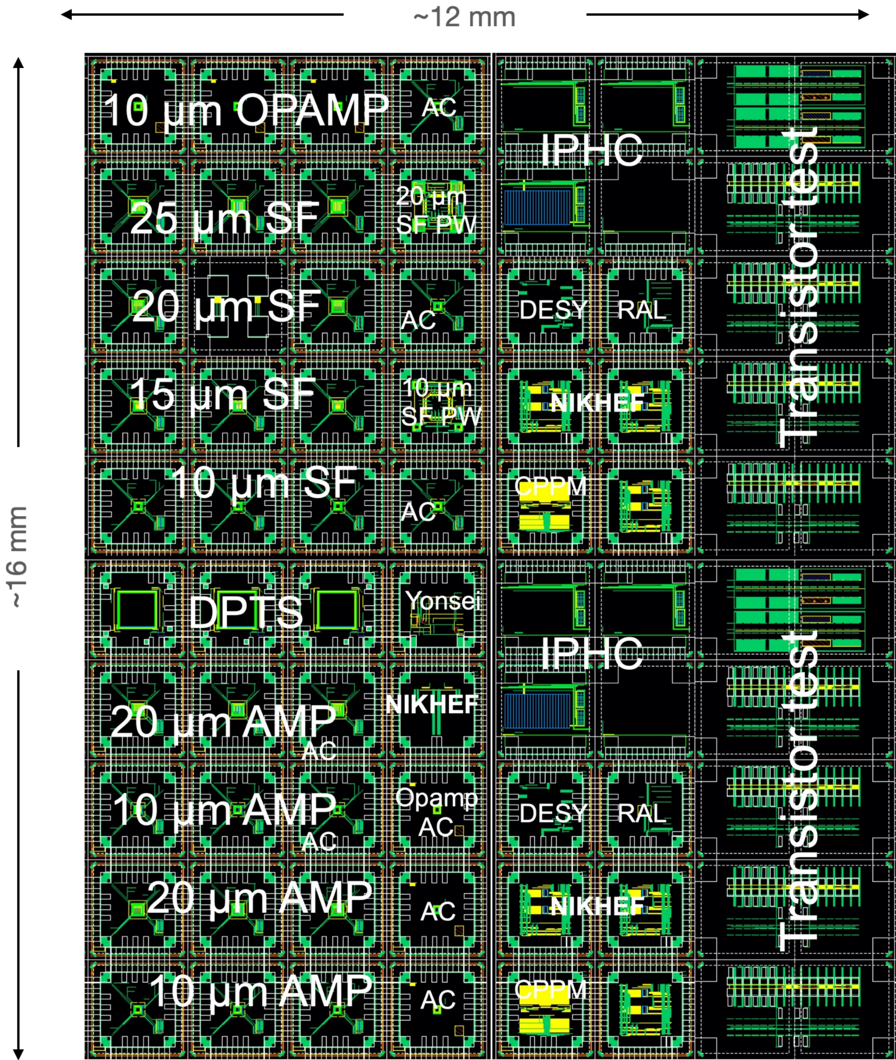
ALICE Inner Tracker System 2 (ITS2) taking data

ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

MLR1 Submission – December 2020

- First submission in TPSCo 65 nm CMOS Imaging
  - Learn technology features
  - Characterize devices
- Prototype circuits, blocks and pixel structures
  - 1.5 × 1.5 mm^2 test chips

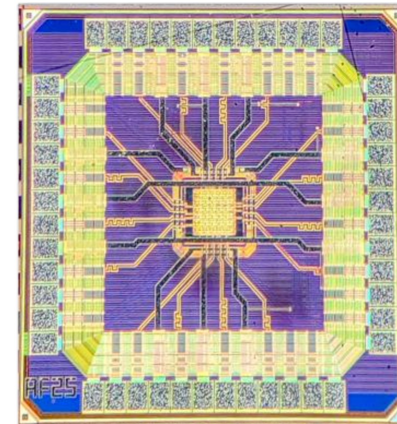




MLR1 Chips and Features

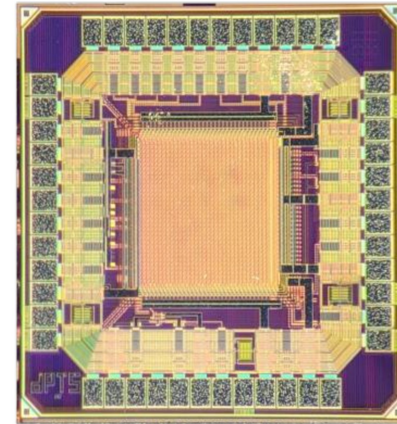
- Transistor Test Structures
- Building blocks
  Bandgap, DACs, Temperature sensor, VCO, drivers …
  NIKHEF, IPHC, STFC, DESY, CPPM
- Pixel Prototypes APTS, DPTS, CE65

  Other pixel prototypes from DESY, Yonsei
- Process Optimisation
  - Increase margins on sensing performance

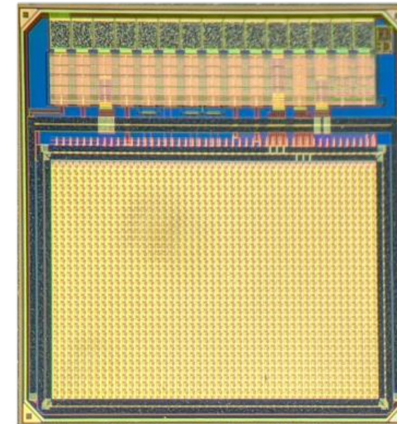
1.5 mm



APTS
4x4 pixel matrix
10, 15, 20, 25 µm pitches
Pixel variants
Direct analogue readout



DPTS
32 × 32 pixels
15 µm pitch
Asynchronous digital readout
ToT information



CE65
64 × 32 pixels
15 µm pitch
Rolling shutter analog readout
3 pixel architectures

Pixel optimization in 180 nm (started in 2012)

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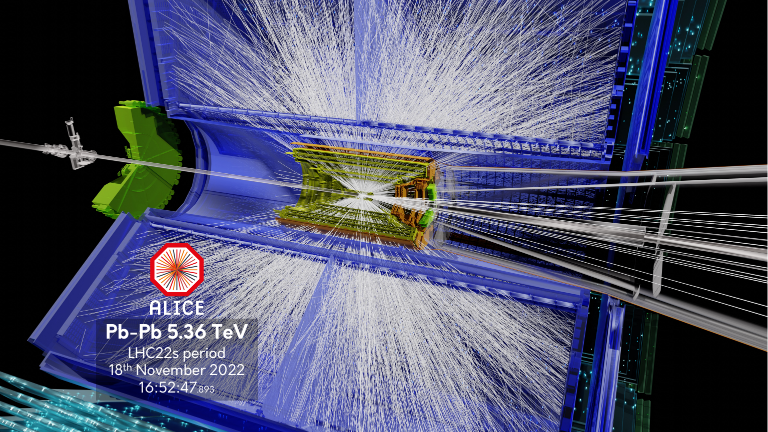
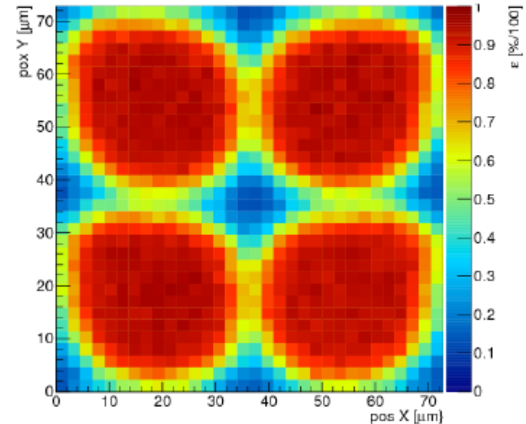
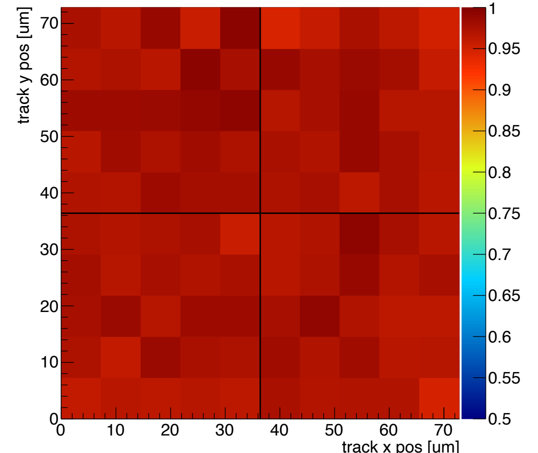
efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2



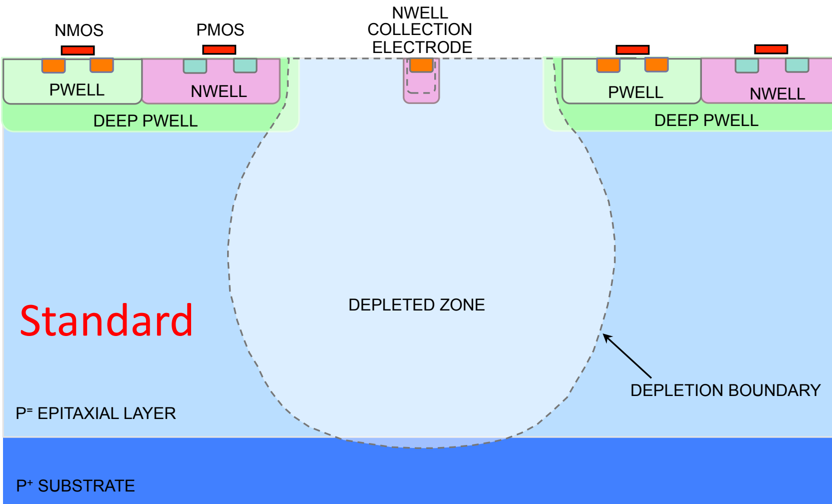
ALPIDE and ITS2 in ALICE (10 m^2)

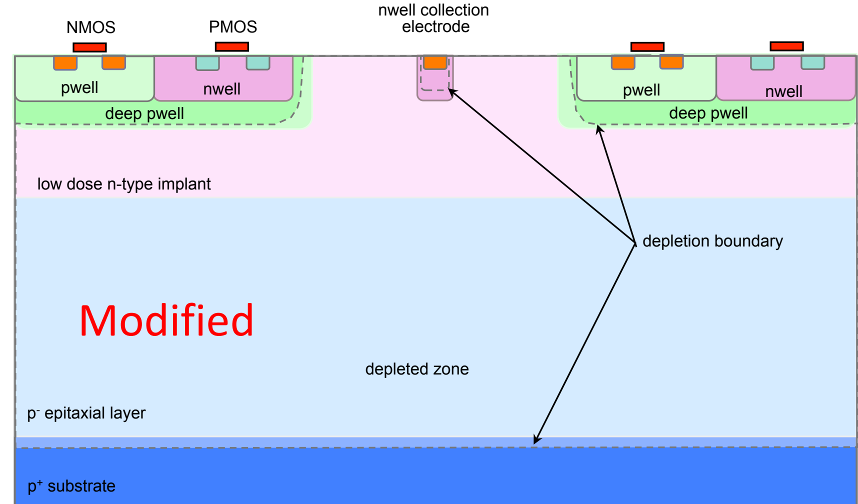


E. Schioppa et al, VCI 2019

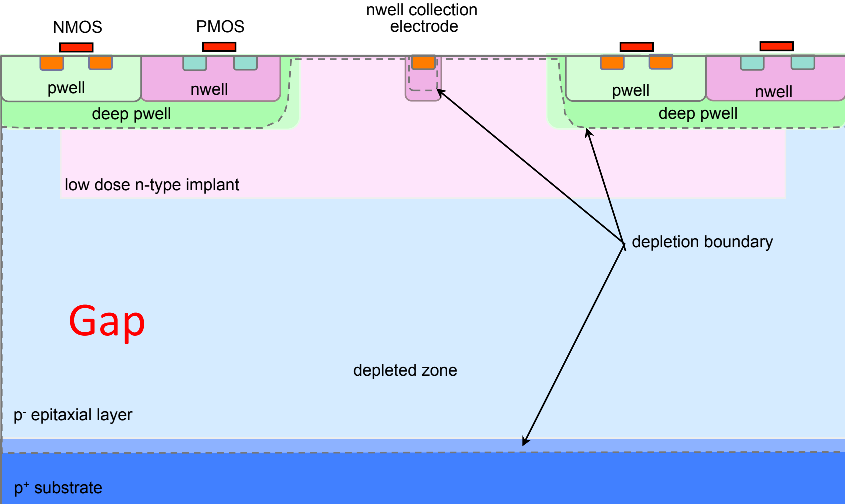


H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200





https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

Charge sharing

Process optimization: 65 nm very similar

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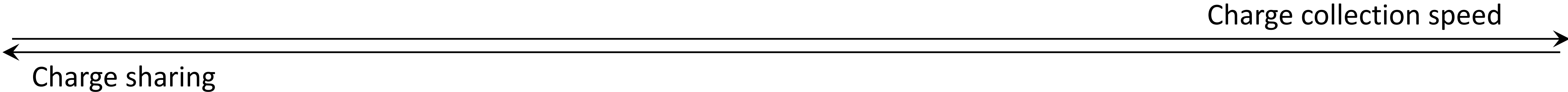
NMOS
PMOS
NWELL COLLECTION ELECTRODE
PWELL
NWELL
DEEP PWELL
DEPLETED ZONE
DEPLETION BOUNDARY
Standard
P⁼ EPITAXIAL LAYER
P⁺ SUBSTRATE

NMOS
PMOS
nwell collection electrode
pwell
nwell
deep pwell
low dose n-type implant
depletion boundary
Modified
depleted zone
p⁻ epitaxial layer
p⁺ substrate

https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

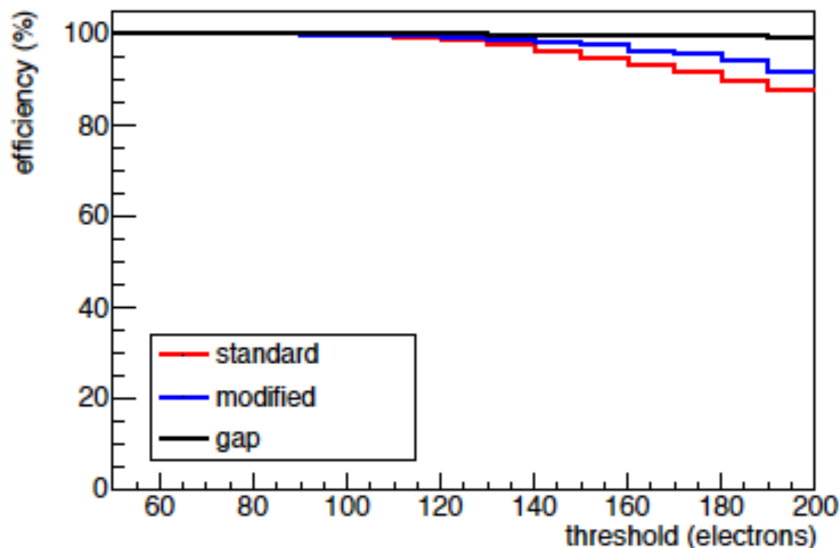
NMOS
PMOS
nwell collection electrode
pwell
nwell
deep pwell
low dose n-type implant
depletion boundary
Gap
depleted zone
p⁻ epitaxial layer
p⁺ substrate

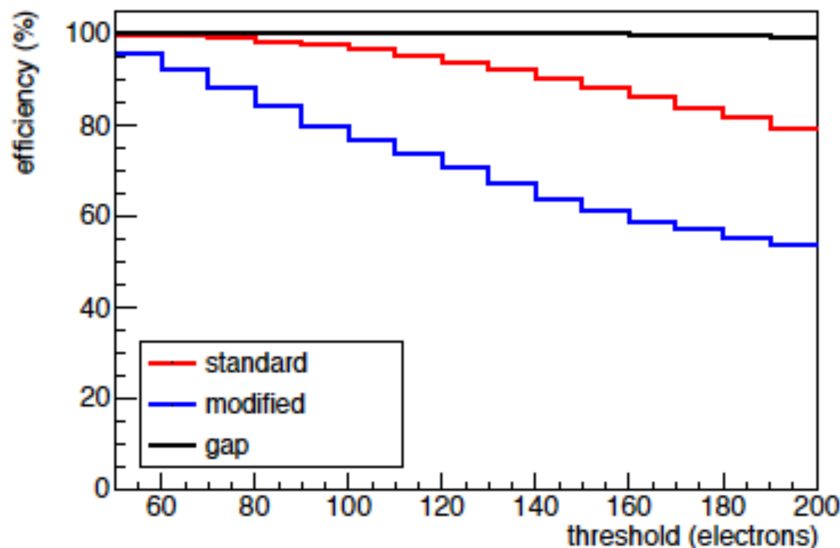
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

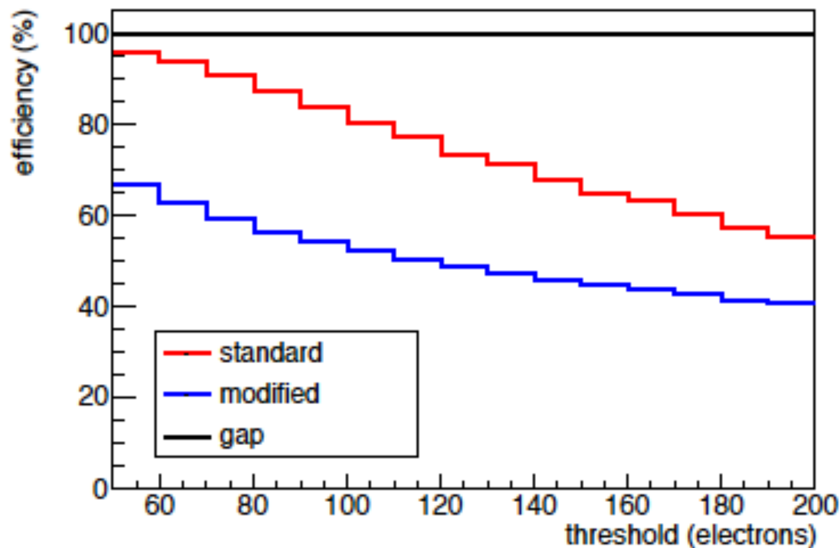


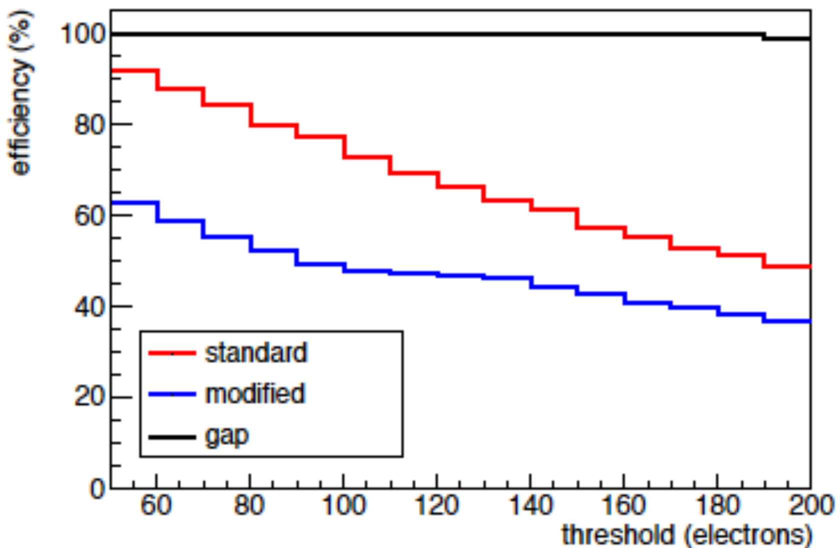
"10th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging" PoS(Pixel2022)001, DOI: https://doi.org/10.22323/1.420.0001

Different pixel flavors at larger pixel pitches









Simulations by J. Hasenbichler for MIPS

Charge sharing reduces the signal in a single pixel and reduces efficiency especially for larger thresholds.

Only the gap concentrates charge sufficiently to remain efficient for large pixel pitches

Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

Standard pixel design

ALICE ITS3 *preliminary*
Fe-55 source measurements
Plotted on 28 Sep 2022

NMOS
PMOS
NWELL COLLECTION ELECTRODE
PWELL
NWELL
DEEP PWELL
DEPLETED ZONE
DEPLETION BOUNDARY
P⁻ EPITAXIAL LAYER
P⁺ SUBSTRATE

Relative frequency (per 20 e^-)

0.0000, 0.0005, 0.0010, 0.0015, 0.0020, 0.0025

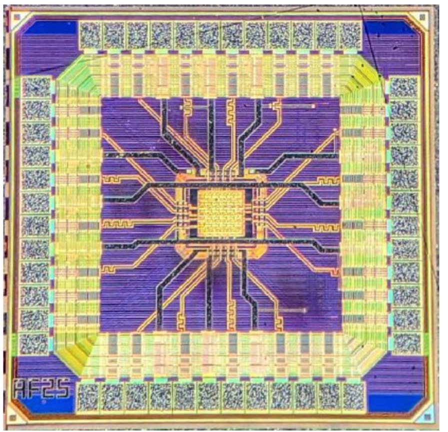
Seed pixel signal (e^-)

0, 250, 500, 750, 1000, 1250, 1500, 1750, 2000

APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1{,}2\,\mathrm{V}$
$I_{reset} = 100\,\mathrm{pA}$
$I_{biasn} = 5\,\mu\mathrm{A}$
$I_{biasp} = 0{,}5\,\mu\mathrm{A}$
$I_{bias4} = 150\,\mu\mathrm{A}$
$I_{bias3} = 200\,\mu\mathrm{A}$
$V_{reset} = 500\,\mathrm{mV}$

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

APTS SF



Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

Remarkable result !

ALICE ITS3 *preliminary*
Fe-55 source measurements
Plotted on 28 Sep 2022

Modified with gap

NMOS
PMOS
nwell collection electrode
pwell
nwell
deep pwell
pwell
nwell
deep pwell
low dose n-type implant
depletion boundary
depleted zone
p^- epitaxial layer
p^+ substrate

Relative frequency (per 20 e^-)

0.0035, 0.0030, 0.0025, 0.0020, 0.0015, 0.0010, 0.0005, 0.0000

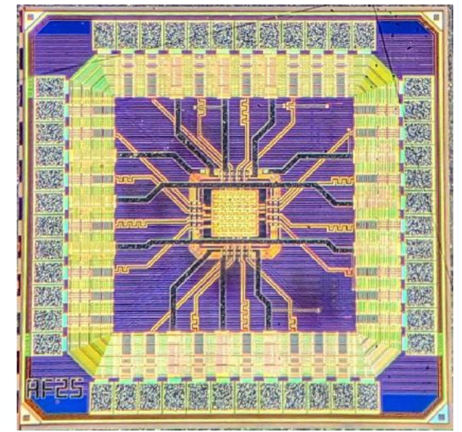
0, 250, 500, 750, 1000, 1250, 1500, 1750, 2000

Seed pixel signal (e^-)

APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1{,}2\,\mathrm{V}$
$I_{reset} = 100\,\mathrm{pA}$
$I_{biasn} = 5\,\mu\mathrm{A}$
$I_{biasp} = 0{,}5\,\mu\mathrm{A}$
$I_{bias4} = 150\,\mu\mathrm{A}$
$I_{bias3} = 200\,\mu\mathrm{A}$
$V_{reset} = 500\,\mathrm{mV}$

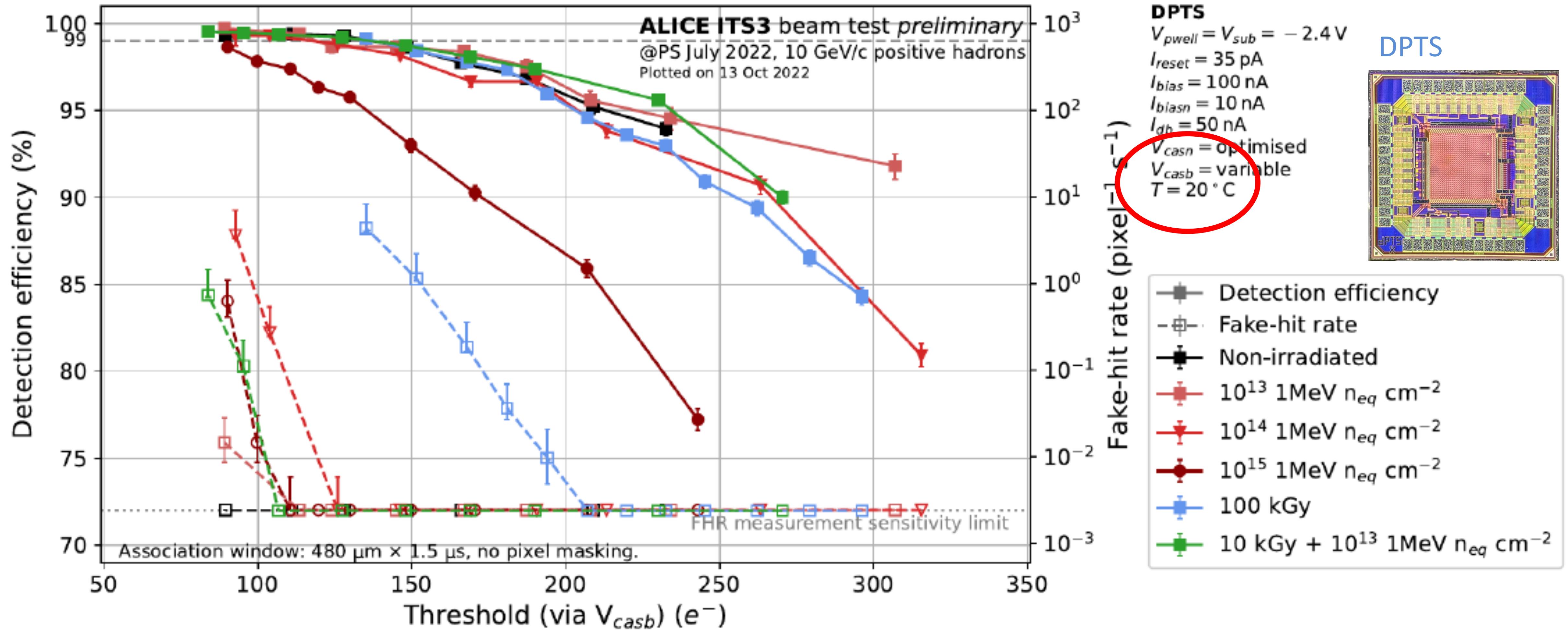
- pitch = 10 µm
- pitch = 15 µm
- pitch = 20 µm
- pitch = 25 µm

APTS SF



~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature

ADD REFERENCE



- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 μm^2 pixel (DPTS) including sensor optimization

Irradiation results: exploring paths to higher fluences

CERN EP R&D

ALICE ITS3 *preliminary*
Fe55 source measurements
Plotted on 24 Okt 2022

Modified with gap

NMOS
PMOS
nwell collection electrode
pwell
nwell
deep pwell
low dose n-type implant
depletion boundary
depleted zone
p⁻ epitaxial layer
p⁺ substrate

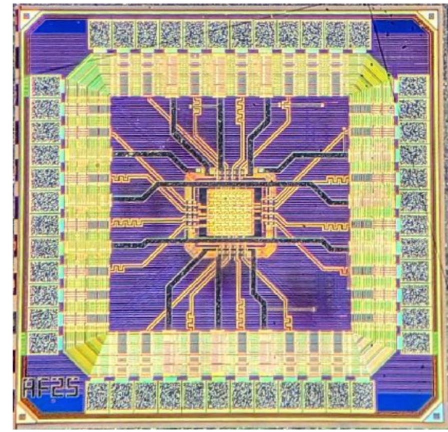
Relative frequency (per 20 e^-)
0.0000
0.0005
0.0010
0.0015
0.0020
0.0025

Seed pixel signal (e^-)
0 250 500 750 1000 1250 1500 1750 2000

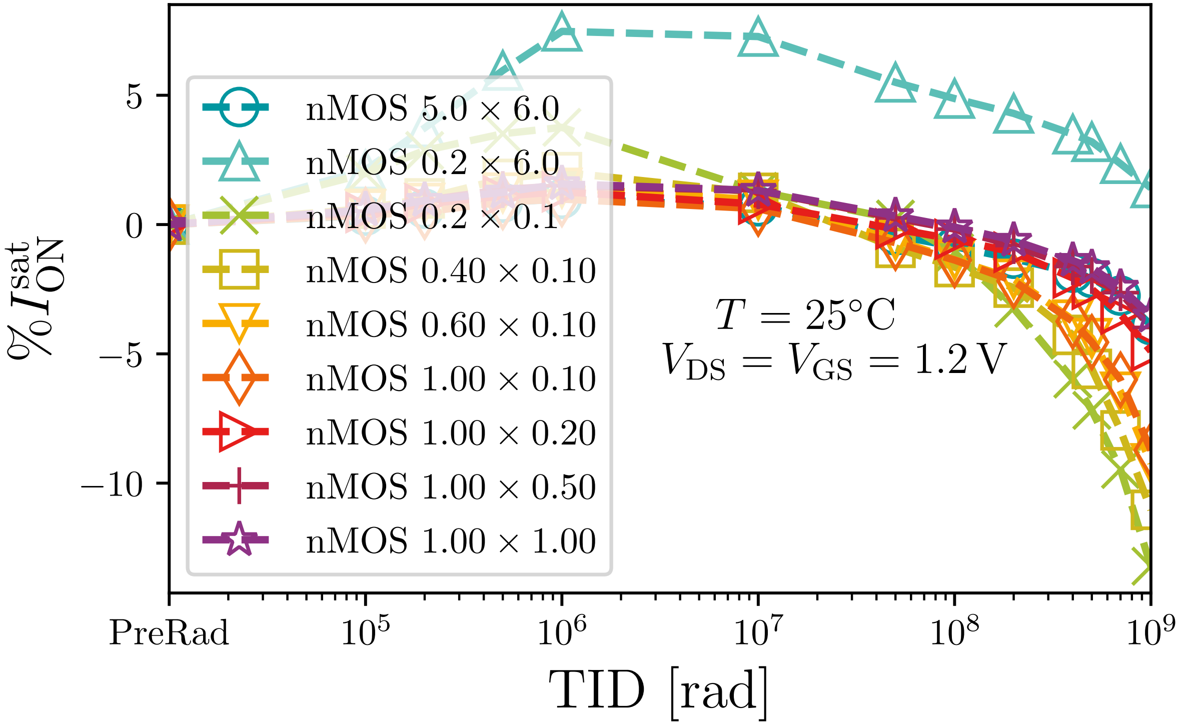
APTS SF
pitch: 15 µm
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 250\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$
temperature = 14 °C

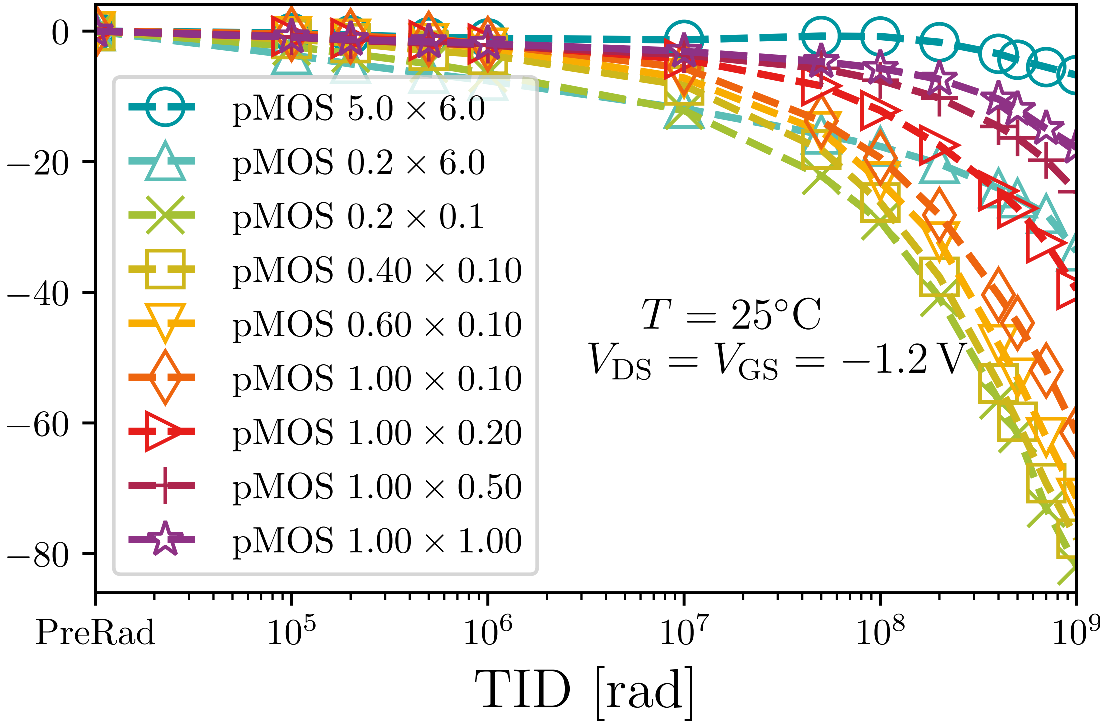
- Not irradiated
- 1e13
- 1e14
- 1e15
- 2e15
- 1e16

DPTS still efficient at RT



Transistor radiation tolerance

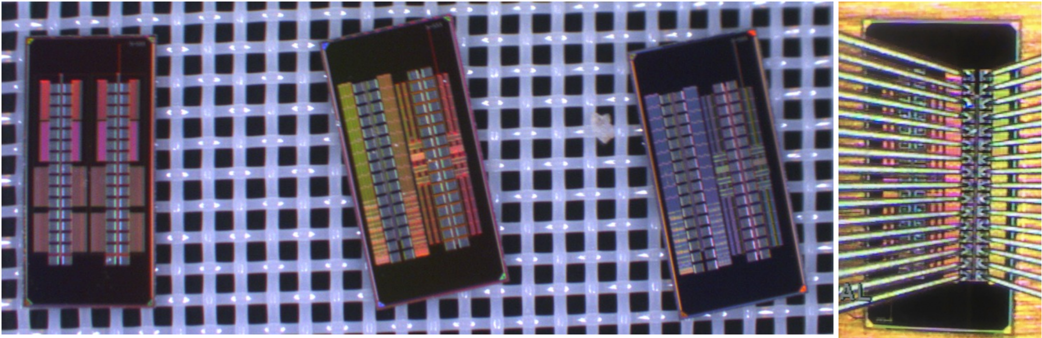




In line with other 65 nm technologies, no showstoppers.

Small size PMOS transistors degrade significantly after several hundred Mrad.

Caveat: modeling of transistors with significant reverse bias



A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

Ringoscillator test chip

CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud (TWEPP 2022)

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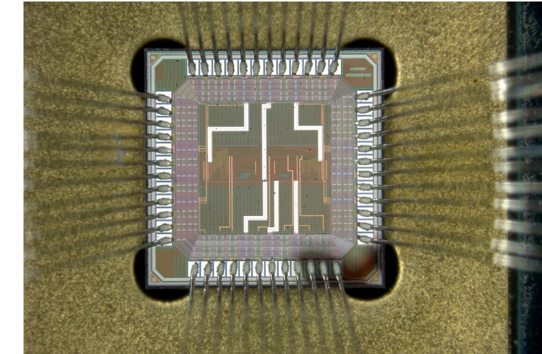
Inv0_LVT | Inv4_SLVT | Inv4_LVT | Inv8_SLVT

NOR1_A_LVT | NOR4_A_SLVT | NOR1_B_LVT | NOR_4_B_SLVT

NOR4_A_LVT | NOR8_A_SLVT | NOR4_B_LVT | NOR8_B_SLVT

NAND0_A_LVT | NAND4_A_SLVT | NAND0_B_LVT | NAND4_B_SLVT

Bank F - chip2, Bank S - chip2, Bank F - chip1, Bank S - chip1



- CPPM contributed to MLR1 with a Ring Oscillator test chip to characterize the standard cells of the TJ 65 nm technology.
- The chip contains 48 ring oscillator based on different standard cells.
- 2 banks of 24 Rows each with the purpose of testing two approaches while irradiating:
  - Functional: the oscillation is enabled
  - Static: the oscillation is disabled
- Oscillation frequency drops by 12-25 % after 830 Mrad. Degradation more pronounced for smaller cells.
- Also several analog designs radiation tolerant up to several 100 Mrad, eg DACs (IPHC) , VCO, bandgap (NIKHEF)…

Key achievement after MLR1: TPSCo 65 nm qualified for HEP

- Chain of sensor with process modifications, analog front end, and digital readout fully efficient in test beam validating process modifications and pixel designs.
- Pixel pitch

  DPTS 15 μm pixel pitch, stitched devices in ER1 18 μm and 22.5 μm (180 nm: ALPIDE ~ 28 μm)

  Sensor variant with gap conserves efficiency at larger pixel pitches.

- Radiation tolerance

  NIEL: DPTS 10^{15} n_{eq}/cm^2 at room temperature, 10^{16} n_{eq}/cm^2 will need cooling (needed for 10^{15} for 180 nm)

  TID: transistors in line with other 65 nm CMOS technologies, leads to tested tolerance beyond 100 Mrad for several circuits (ringoscillators, VCO, DAC, bandgap, etc)

  SEU: cross-sections in line with other 65 nm CMOS technologies

- Timing (only established really for the sensor now);

  APTS_OA ~ 80 ps requires further study, no timewalk correction yet etc (180 nm: FASTPIX ~ 100 ps) see backup

- Many features in the technology still unexplored: special imaging devices, wafer stacking, ….

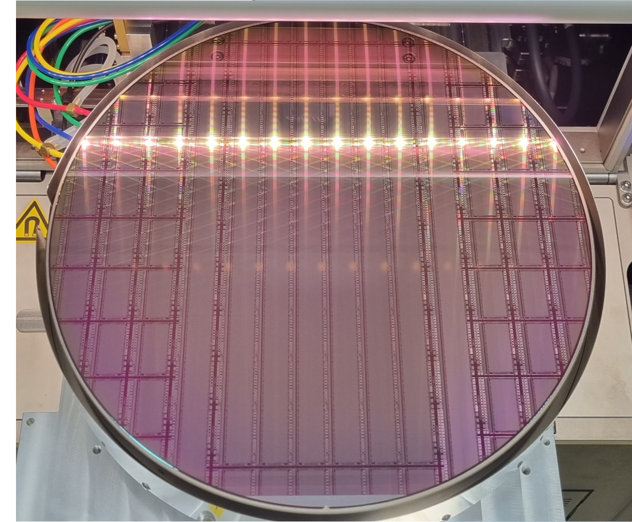
EP R&D Open day 2023, WP1.2 Summary:
https://indico.cern.ch/event/1233482/contributions/5264293/attachments/2596131/4482445/EP_RandD_Days_WP1.2_2023_02_20.pdf
Proceedings on process optimization: https://pos.sissa.it/420/083
Article on DPTS chip (under review at NIMA): https://doi.org/10.48550/arXiv.2212.08621

ER1 submission (Nov 2022)

Objective: prove that we can design wafer scale pixel detectors

- Learn stitching techniques
- Stitching interconnects
- Learn about yield, design for manufacturing (DFM) and defects masking
- Study power schemes, leakage, spread, noise and speed
- Develop wafer assembly and stitching methodology
  – Practical application: Alice ITS3 upgrade[1]

12” wafer (30cm)



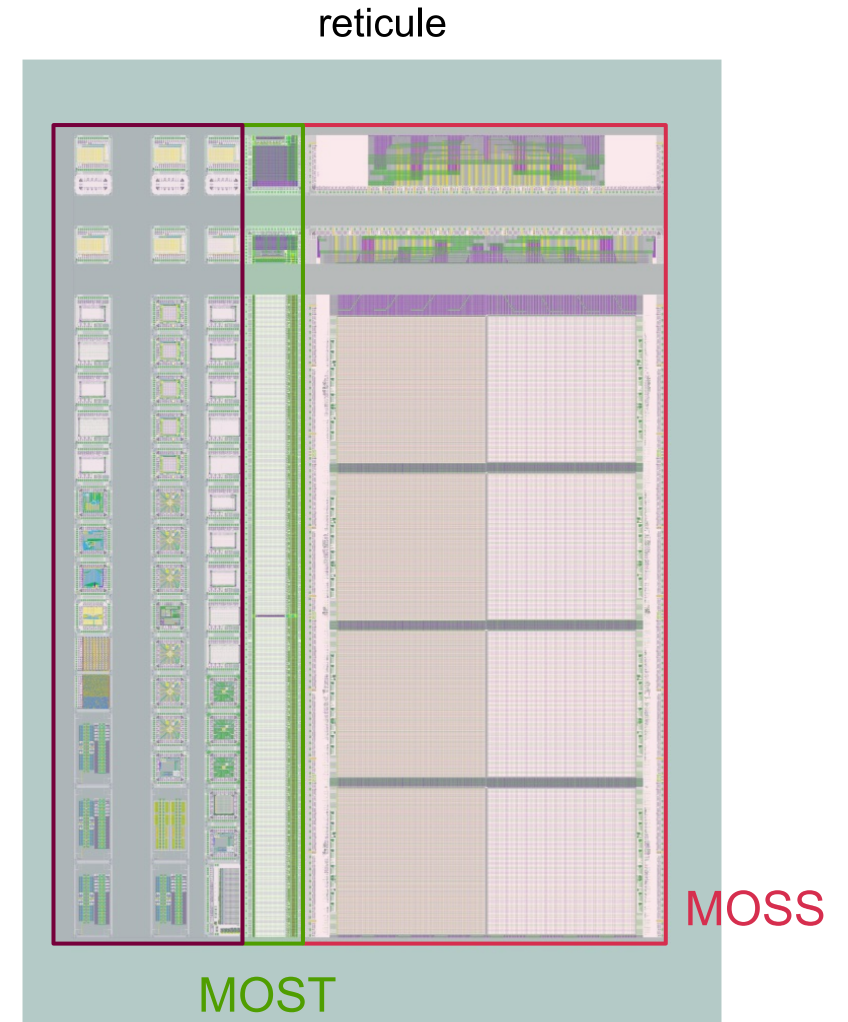
6 MOSS and 6 MOST per Wafer

26cm length single silicon object

(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

ER1 submission

- Features two stitched sensor chips, 6 of each per wafer
  - MOSS chip (1.4 x 26 cm)
    - Conservative layout (DFM rules), Alpide-like readout scheme and 1/20 power segmentation
  - MOST chip (0.25 x 26 cm)
    - High local density with high power gating granularity to mitigate faults, async hit driven readout
- Features 51 chiplets for prototyping blocks and pixel chips
  - PLL, pixel prototypes, fast serial links, SEU test chips, …
  - IPHC, NIKHEF, STFC, DESY, SLAC, INFN, CERN…
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC rules
  - Custom DRC and LVS rule deck implemented
  - Custom DFM standard cell library implemented
  - Setup legal and contractual framework
  - Develop know-how on stitching, wafer assembly & signoff



MOSS Monolithic Stitched Sensor Prototype

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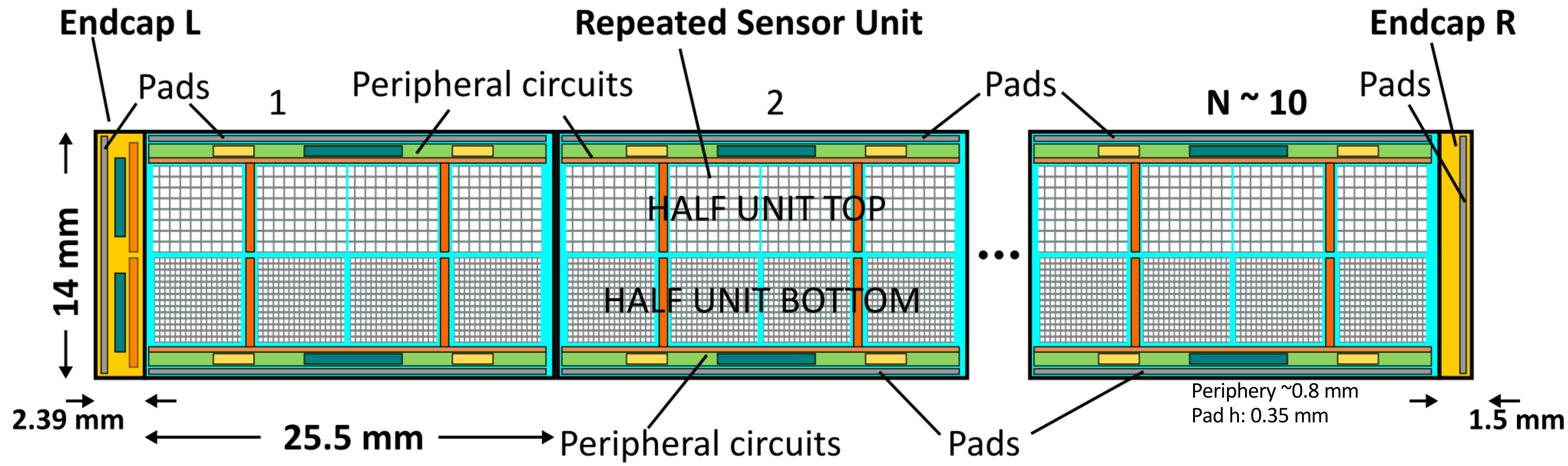


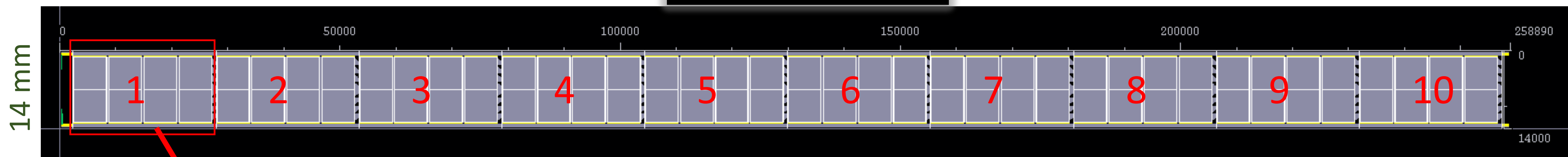
Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

Repeated units abutting on short edges

- Repeated Sensor Unit, Endcap Left, Endcap Right
- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

MOSS Layout

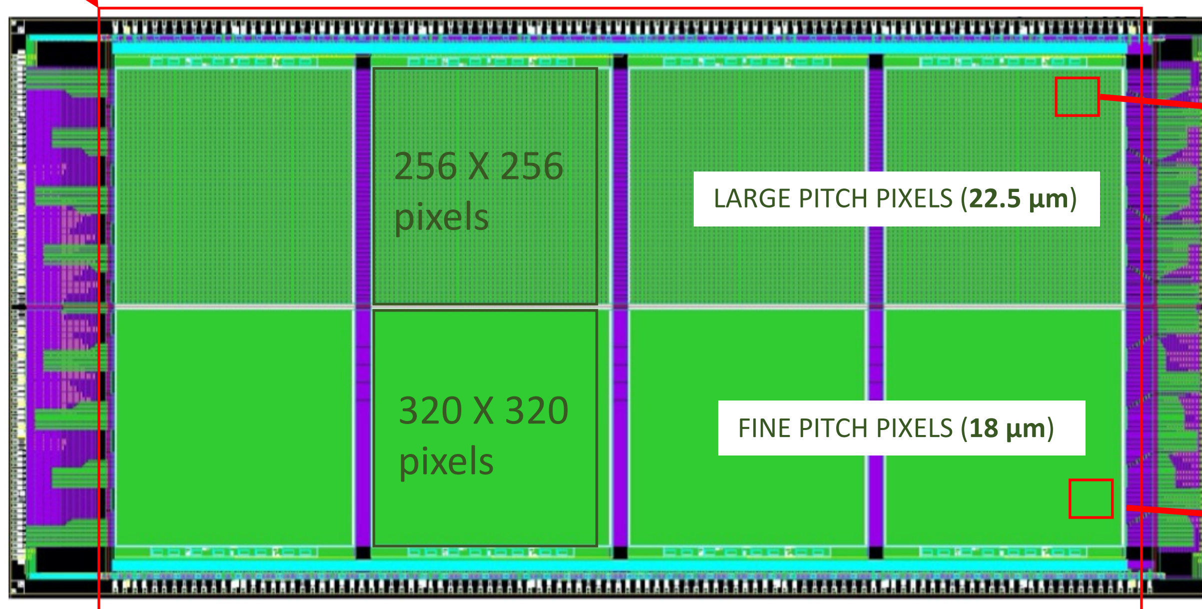
6.72 Mpixels

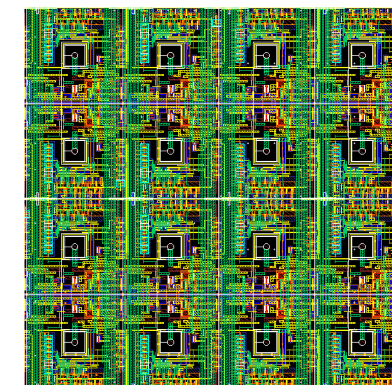


14 mm

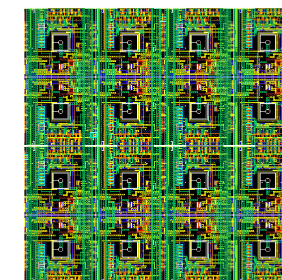
25.9 mm

1 of 10



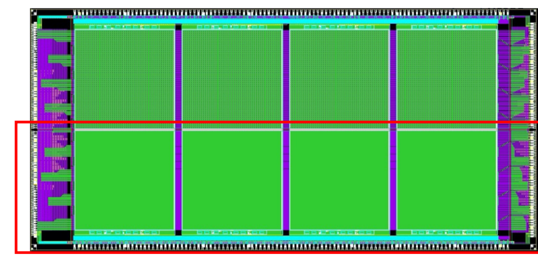


Pitch
22.5 µm



Pitch
18 µm

MOSS - Half Unit



CERN EP R&D

left_endcap

moss_core

right_endcap

Region 0 | Region 1 | Region 2 | Region 3

Matrix
20x20 x 16x16 pixels

row steering

g_C0R0 g_C1R0 g_C19R0 g_C0R1 g_C0R19 g_C19R19

analog-distributed-DAC

Column steering

Pixel Config: Bus Responder, Registers

Region Readout

Control Interface: Bus Responder, Registers

Unit Control: Bus Responder, Registers

Bus Responder, Registers — top readout

Stitched communication backbone

Control

Readout

Supply

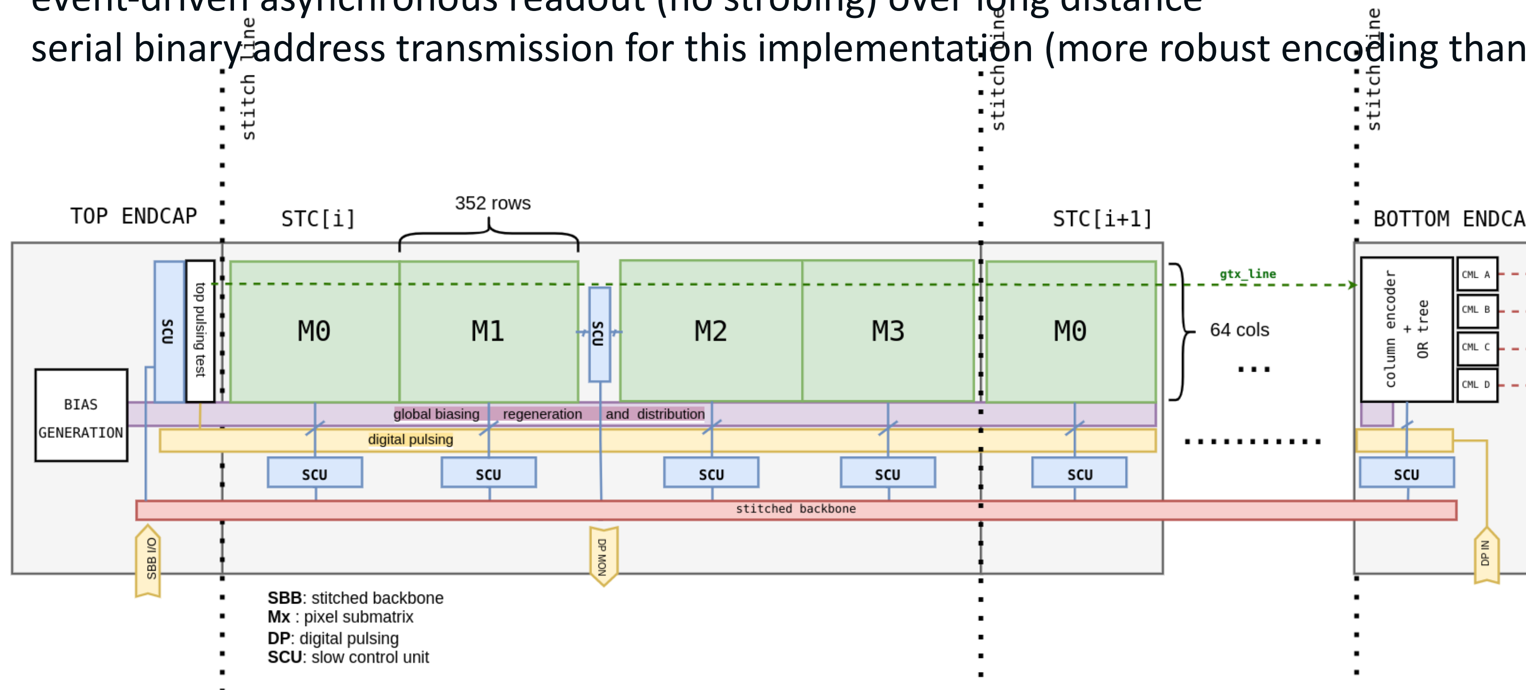
Control

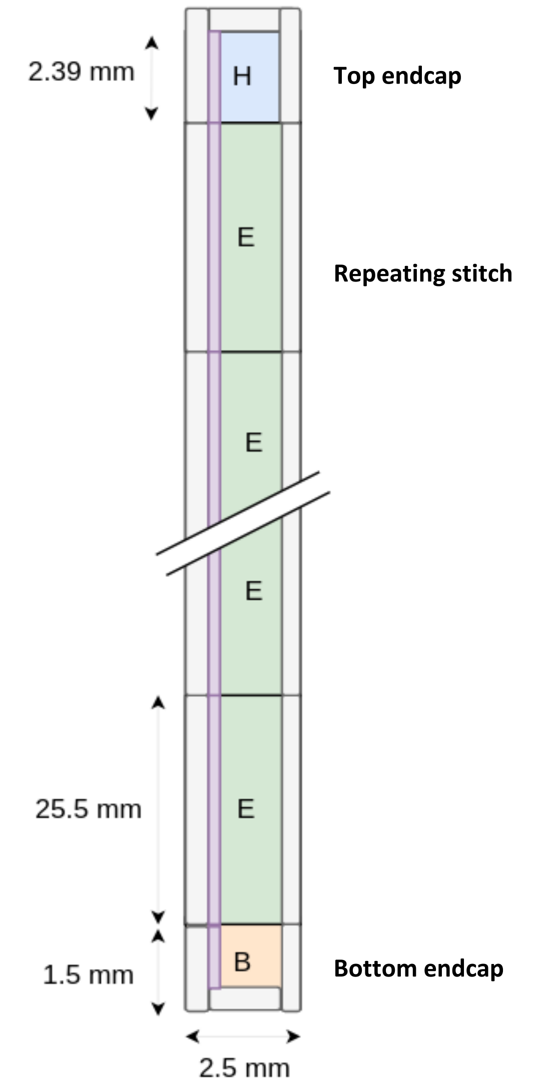
Readout

Supply

MOST Chip

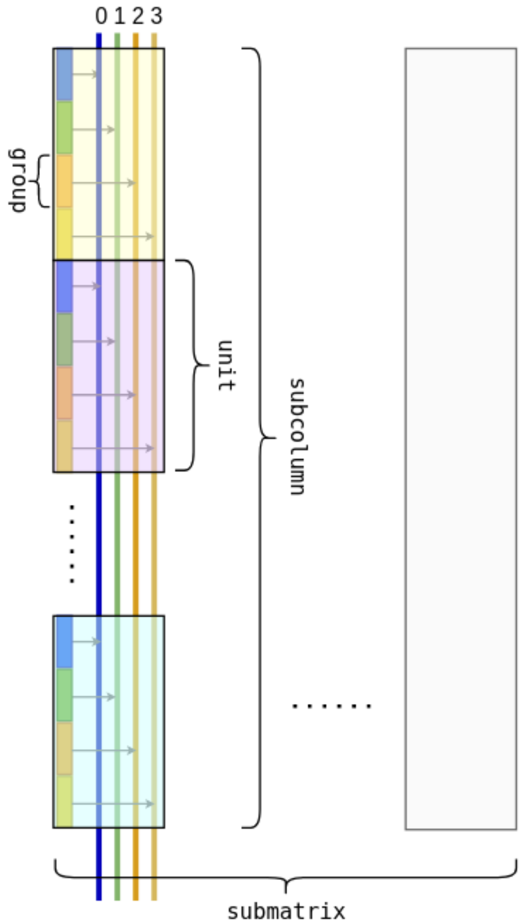
- Investigate **yield** when local density is preserved
  - Global power domains over full chip (Digital/Analog)
  - Higher granularity in power gating in case of a defect of
    - analog (rows of 4 pixels)
    - digital (half columns)
  - PWELL tied to ground
    - reverse sensor biasing achieved by higher power supply
- Immediate transfer of hit data to the periphery (bottom endcap, 4 CML outputs)
  - event-driven asynchronous readout (no strobing) over long distance
  - serial binary address transmission for this implementation (more robust encoding than DPTS)

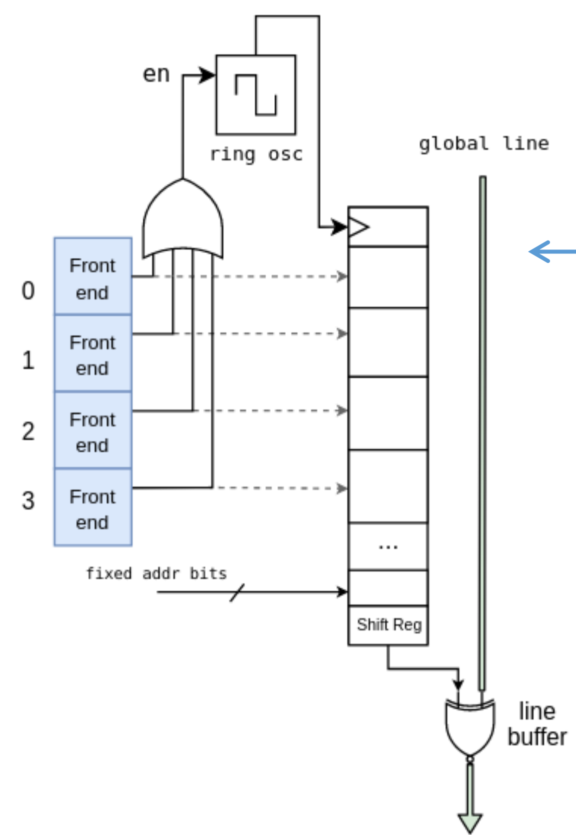




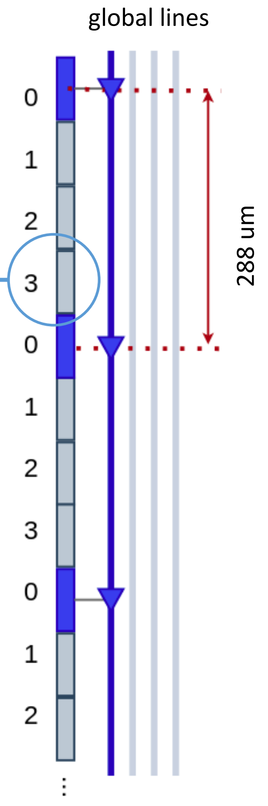
MOST Chip: more detail

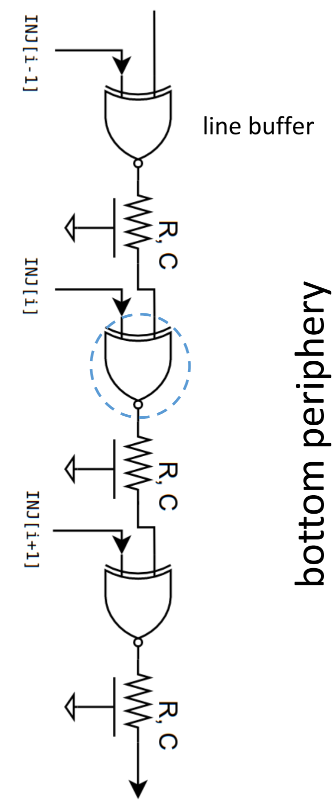
~ 90k pixels per stitch



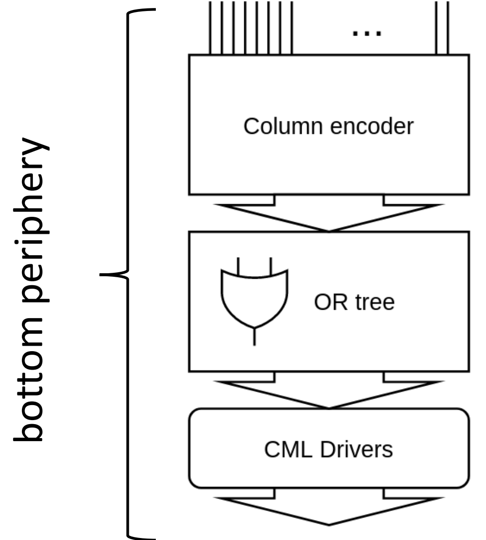


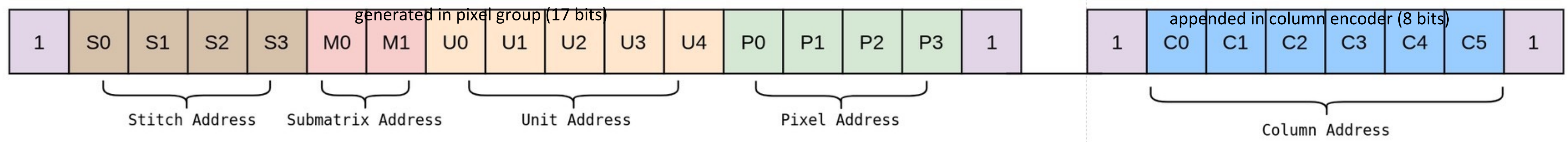
pixel group





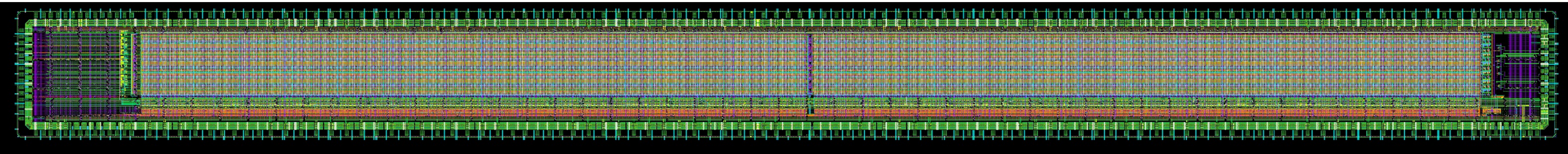
bottom periphery



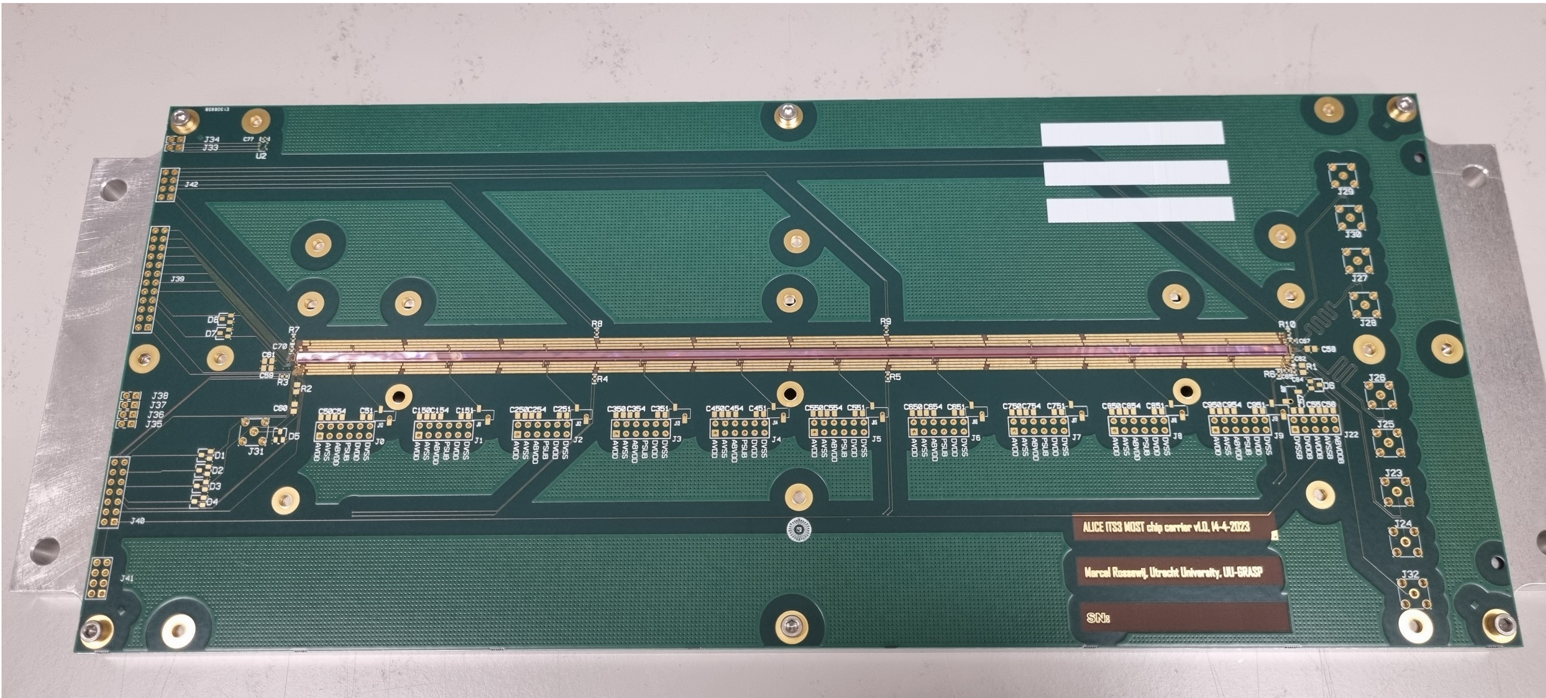


MOST

CERN EP R&D



Single stitch assembly: (1 middle stitch + endcaps)



First mounting of (dummy from pad wafer) MOST on test card

DPTS Analog front-end

see also: F. Piro IEEE NSS 2022

Amplification and reset

Discrimination

AVDD
AVDD
AVDD
IBIAS
M0
IRESET
M5
IDB
M10
M1
VRCAS
M6
IN
VCASB
M7
OUTD
D0
M4
OUTA
M11
SUB
M2
VCASN
M8
M3
IBIASN
M9

Benefits from low sensor capacitance (< 5fF).

- Source follower (M1) to compensate C_{GS} capacitance.
- M2, DC coupled to the source of M1, contributes to the gain using the same current.
- Cascode transistors M4 and M8 provide high gain on OUTA.
- DC coupling requires feedback to input through M7. Current provided by M5-M6.
- M10-M11 form a simple discriminator with threshold set by the IDB current source.

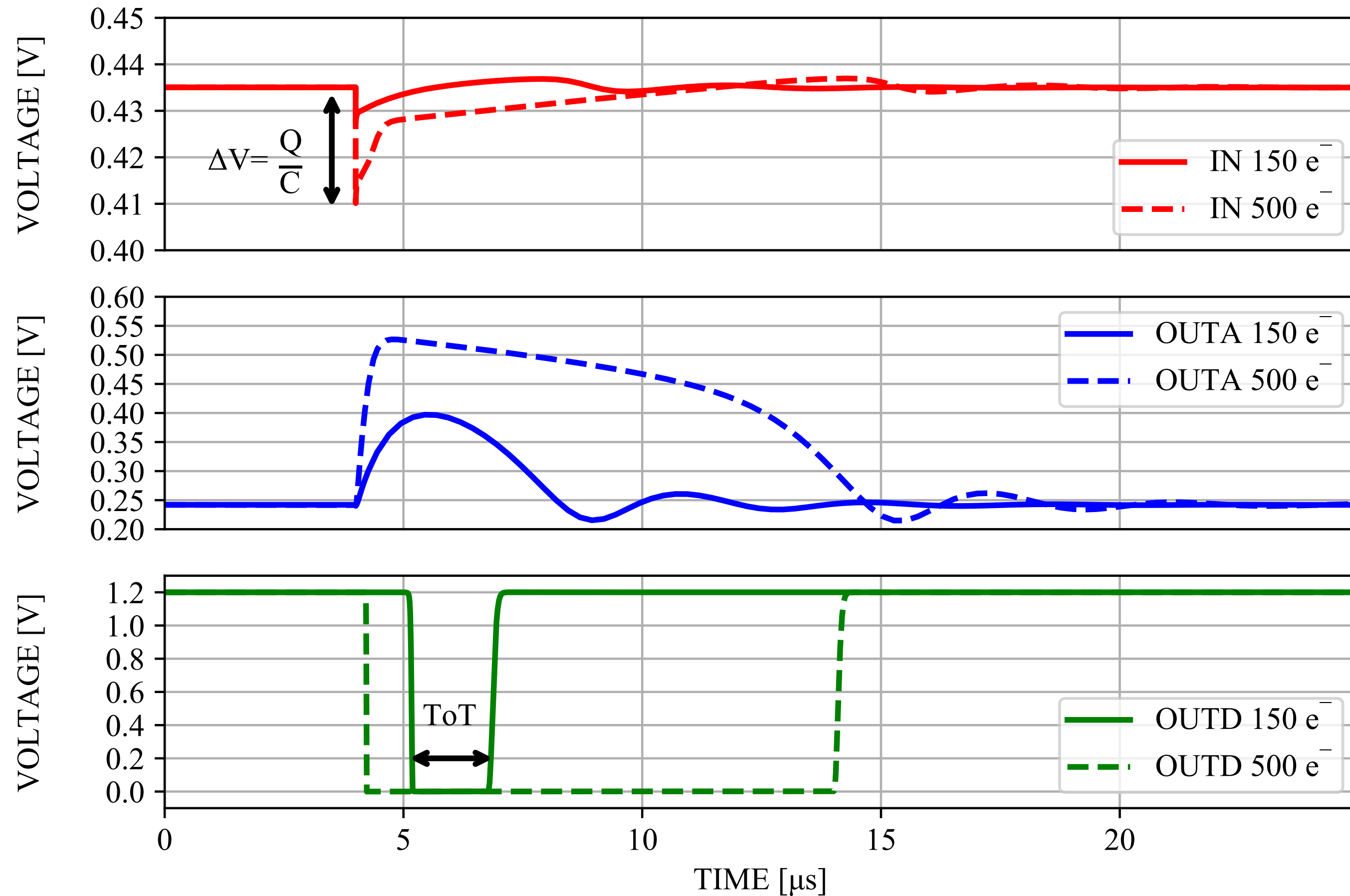
Tunable IBIAS-IBIASN (IBIAS = 10 x IBIASN) currents to set lower power consumption or faster timing response.

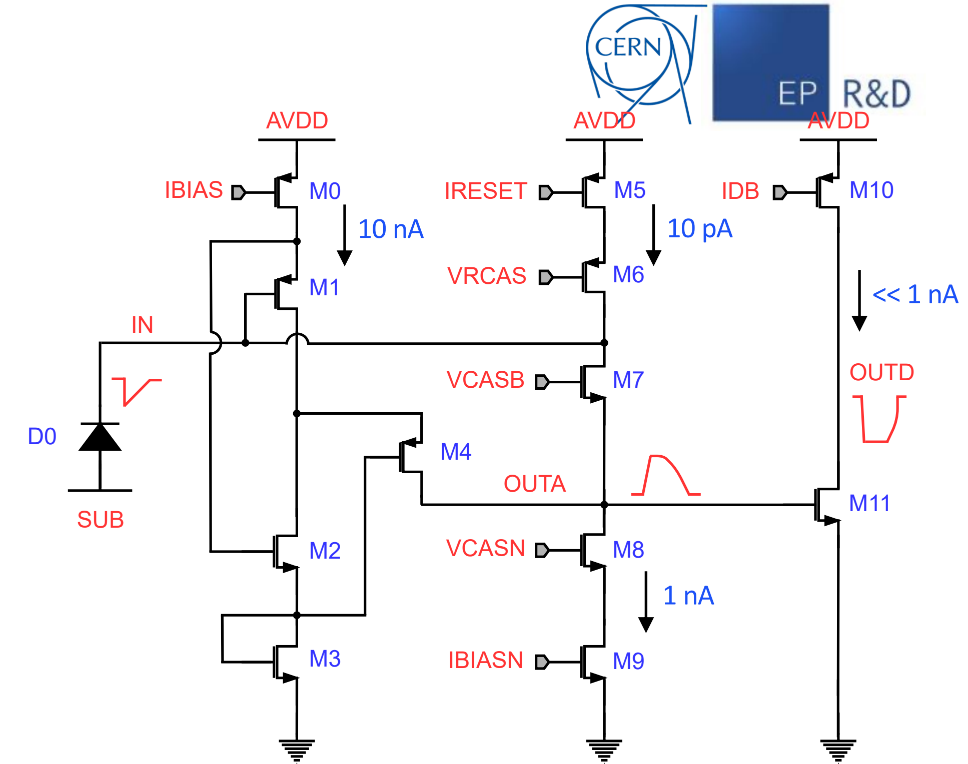
L. Cecconi, et al., “Design and readout architecture of a monolithic binary active pixel sensor in TPSCo 65 nm CMOS imaging technology ”, TWEPP 2022.

DPTS Front-end simulations

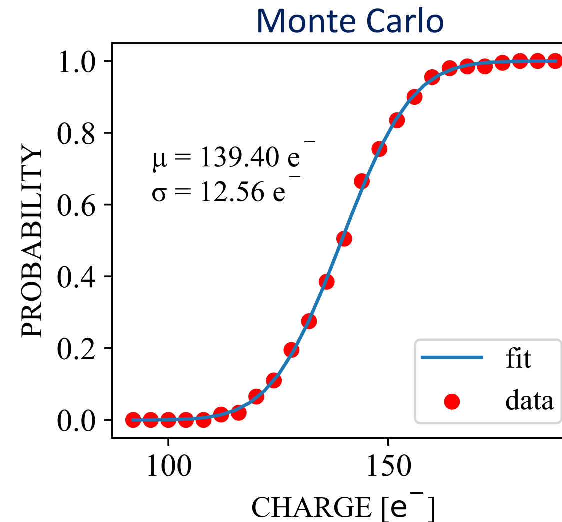
Simulation results with ≈ 12 nW power consumption – lowest power mode.

Gain @ threshold ≈ $1\ \mathrm{mV/e^-}$, $1\ \mu\mathrm{s}$ peaking time.

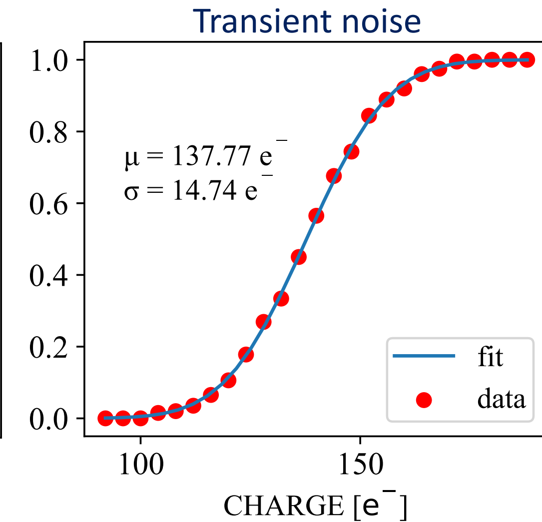




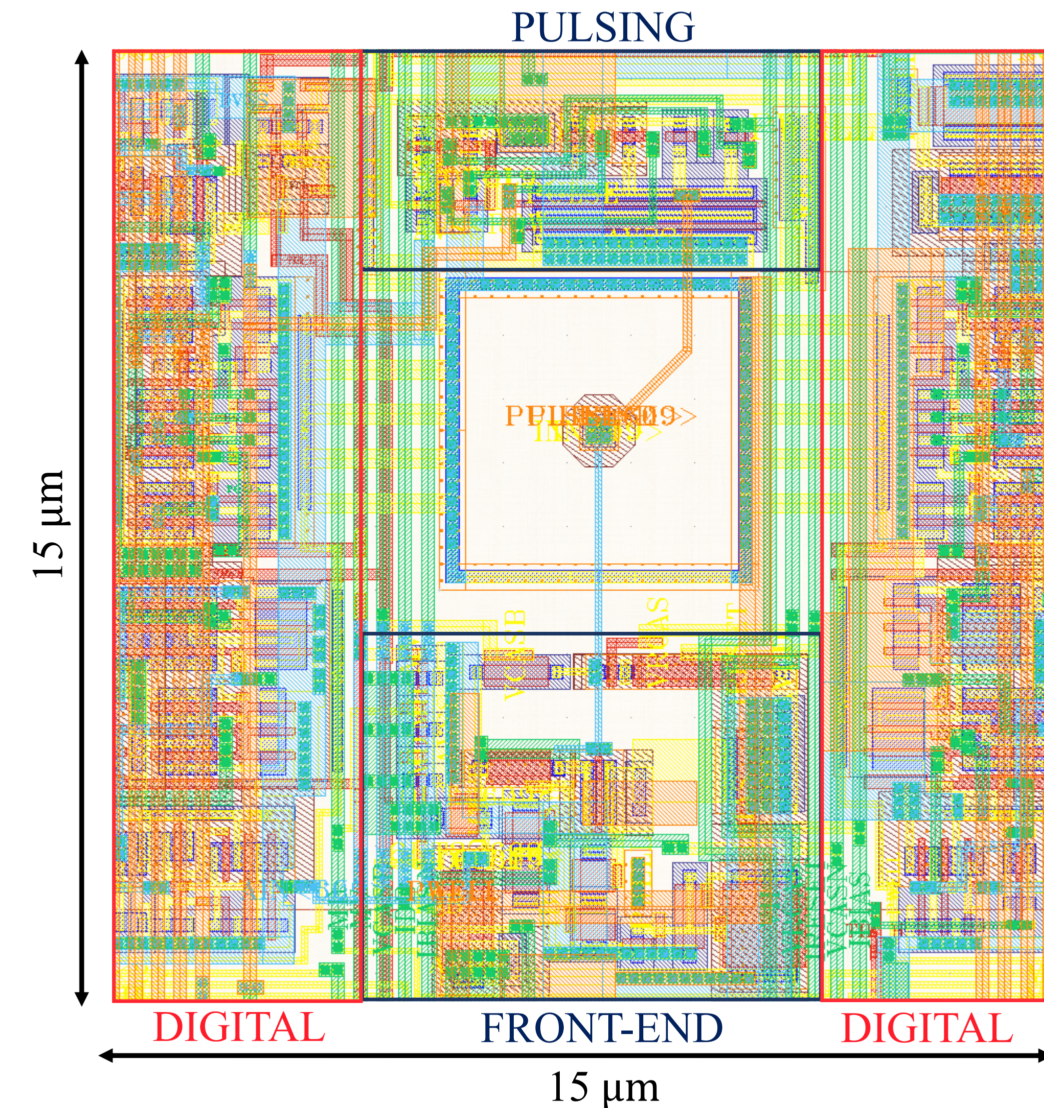
Monte Carlo



Transient noise



DPTS Pixel layout and measurements



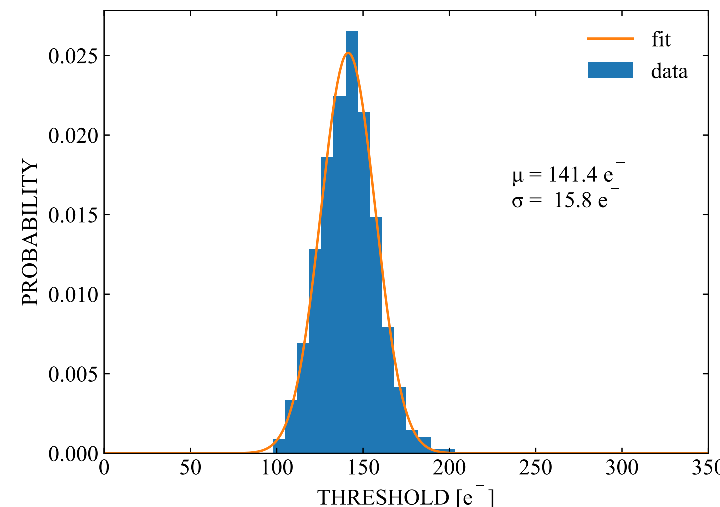
In-pixel circuitry:

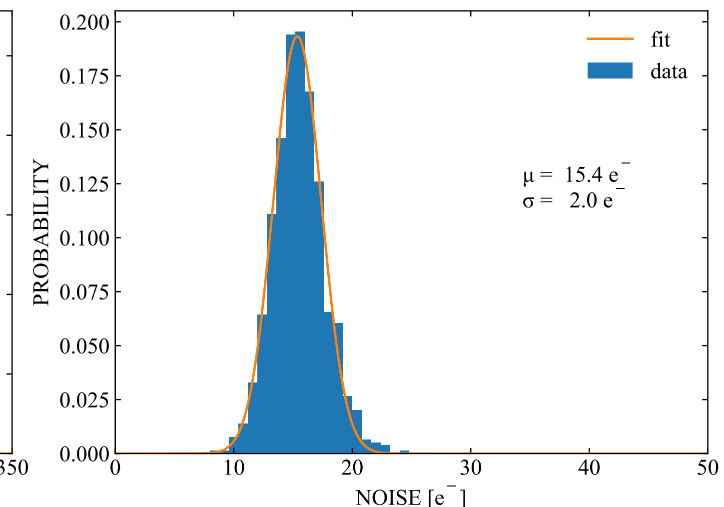
- front-end amplifier and discriminator ($42\ \mu m^2$).
- test pulse injection circuitry ($17\ \mu m^2$).
- digital gates for asynchronous transmission of the time-encoded pixel address ($140\ \mu m^2$).

Analog power density over the matrix as low as $\sim \mathbf{5\ mWcm^{-2}}$.

Good agreement with simulations

threshold dispersion $\approx 15.8\ e^-$ noise $\approx 15.4\ e^-$





Measurements - front-end time walk

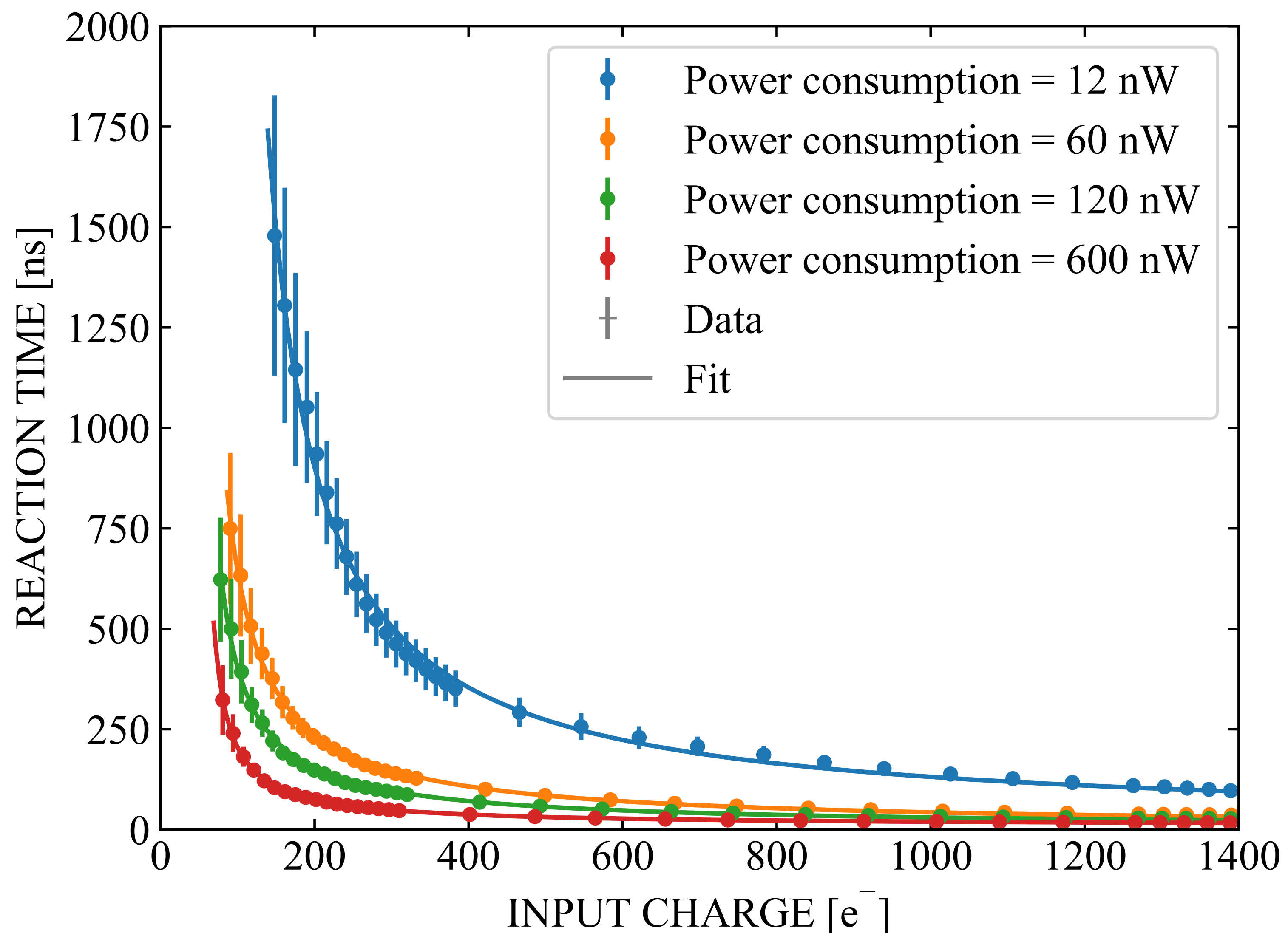
For a power consumption of 12 nW, with charges > 200 e^- (35% of a MIP charge):

- time response < 1 μs
- jitter < 150 ns

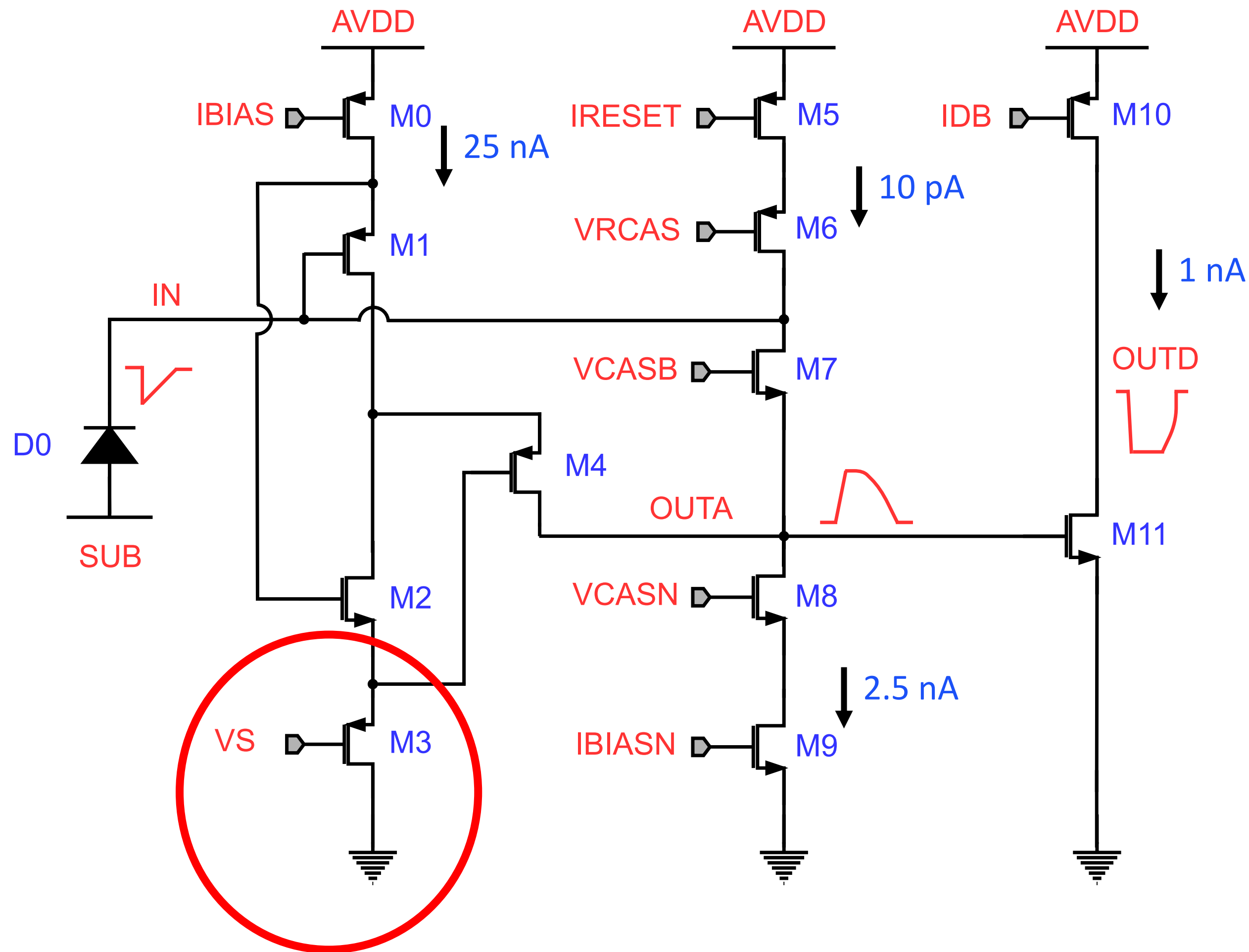
For a power consumption of 600 nW, with charges > 350 e^-:

- time response < 25 ns
- jitter < 1.2 ns

Can go up to a few μW. Power increased by increasing IBIAS = 10 IBIASN.



MOSS front-end



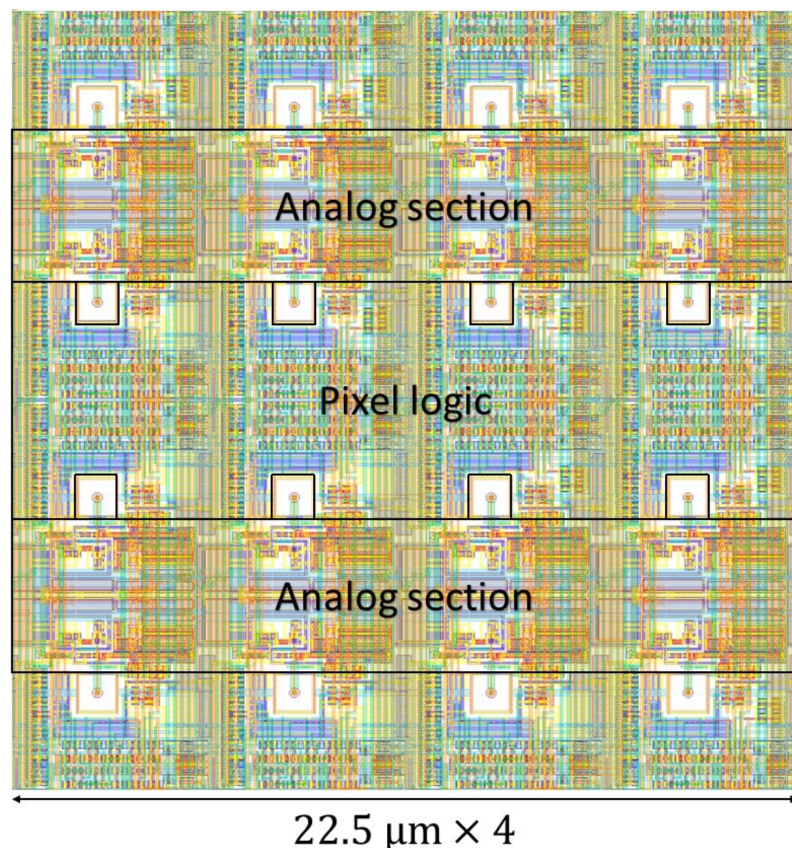
Conservative layout to respect DFM rules.

PWELL/PSUB to be kept at ground for high yield:

- Transistor M3 converted to a PMOS to be able to shift up the collection electrode voltage through front-end settings and increase sensor reverse bias.

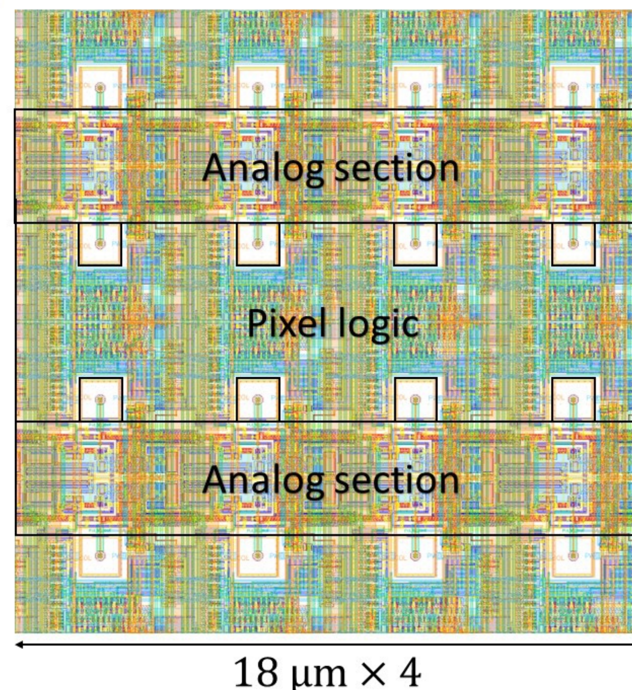
Higher current for more margin

MOSS pixel layout



$22.5\ \mu m \times 4$

Power density $\approx 7.11\ mWcm^{-2}$



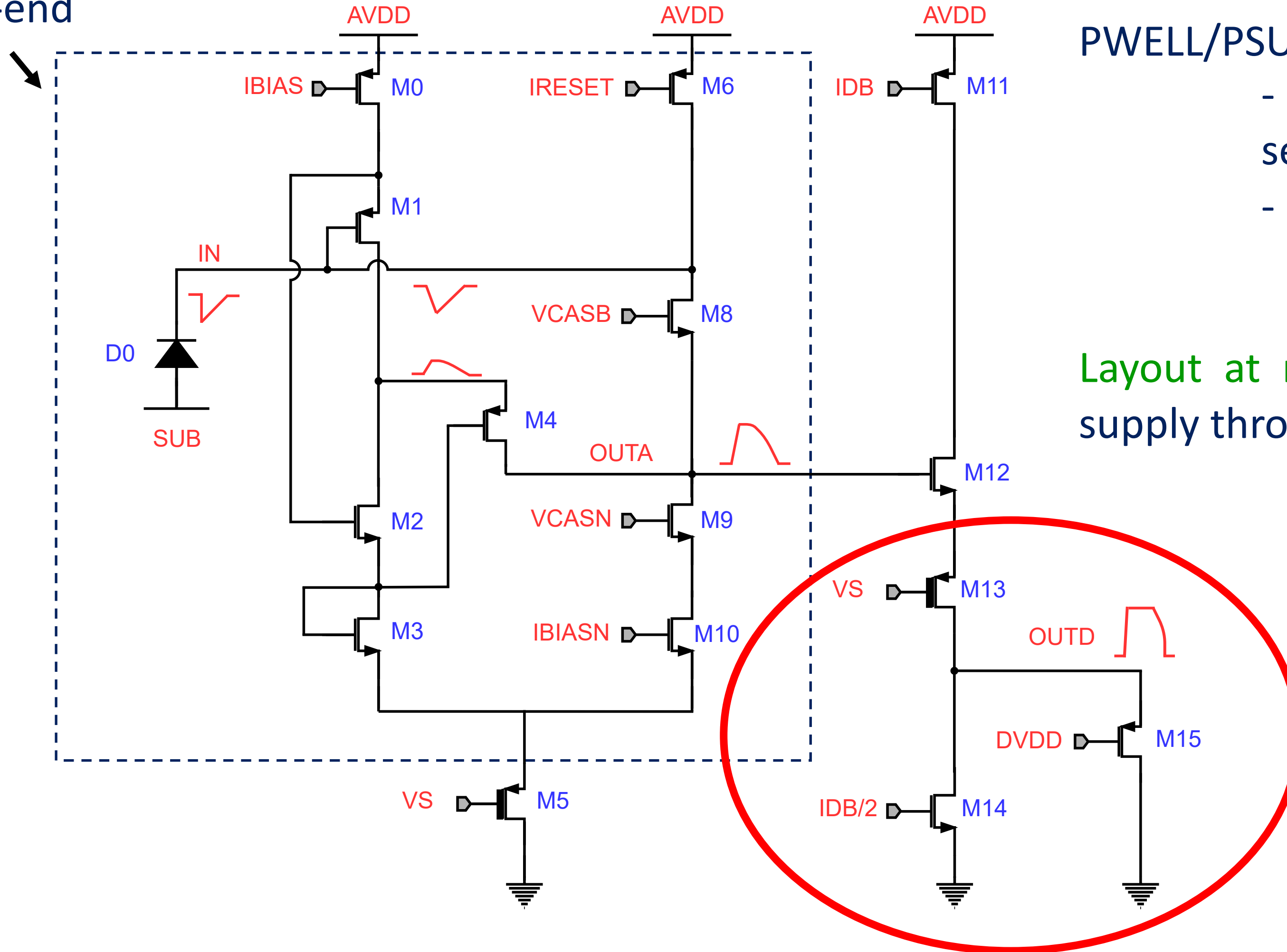
$18\ \mu m \times 4$

Power density $\approx 11.11\ mWcm^{-2}$

Performance obtained with PEX simulations

Parameter	Value
Area	$60\ \mu m^2$
Power	$36\ nW$
Gain	$0.5\ mV/e^-$
Threshold	$150\ e^-$
Peaking Time	$1\ \mu s$
Phase Margin	$60°$
Thr. Dispertion	$11.5\ e^-$
ENC	$12\ e^-$

MOST front-end



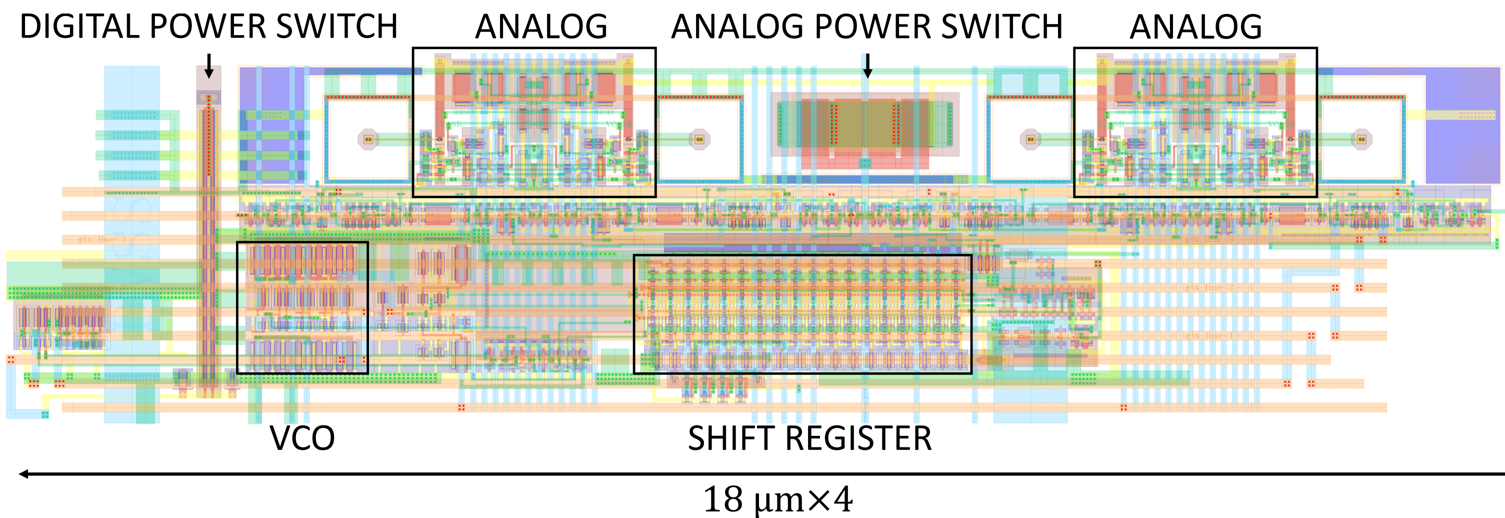
PWELL/PSUB connected to analog ground:

- AVDD to create headroom and accommodate large sensor reverse biases through the front-end settings.
- thick oxide transistors (M5-M13) to allow AVDD > 1.2 V

Layout at normal density -> groups of pixels connected to supply through switches to power gate defect pixels

Adaptation of the interface to the digital domain.

MOST pixel layout



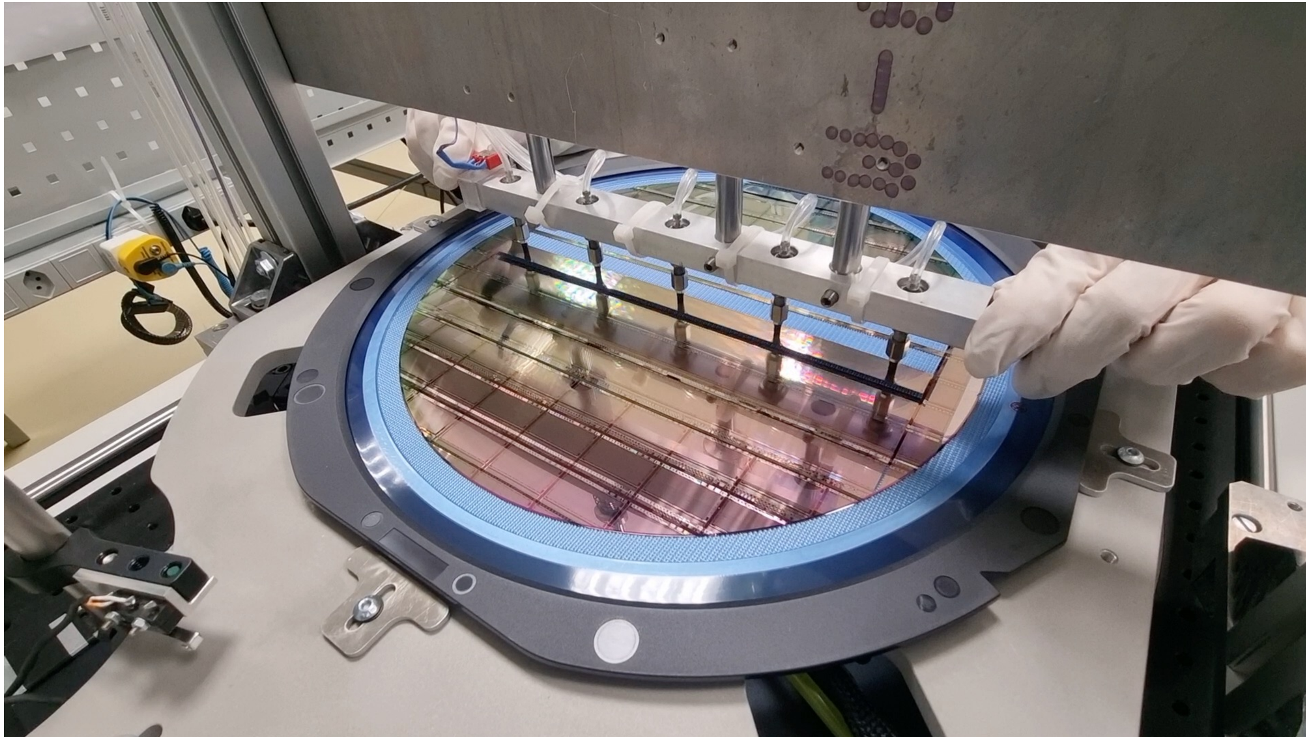
Power density $\approx 11.11\ \mathrm{mWcm^{-2}}$

Performance obtained with PEX simulations

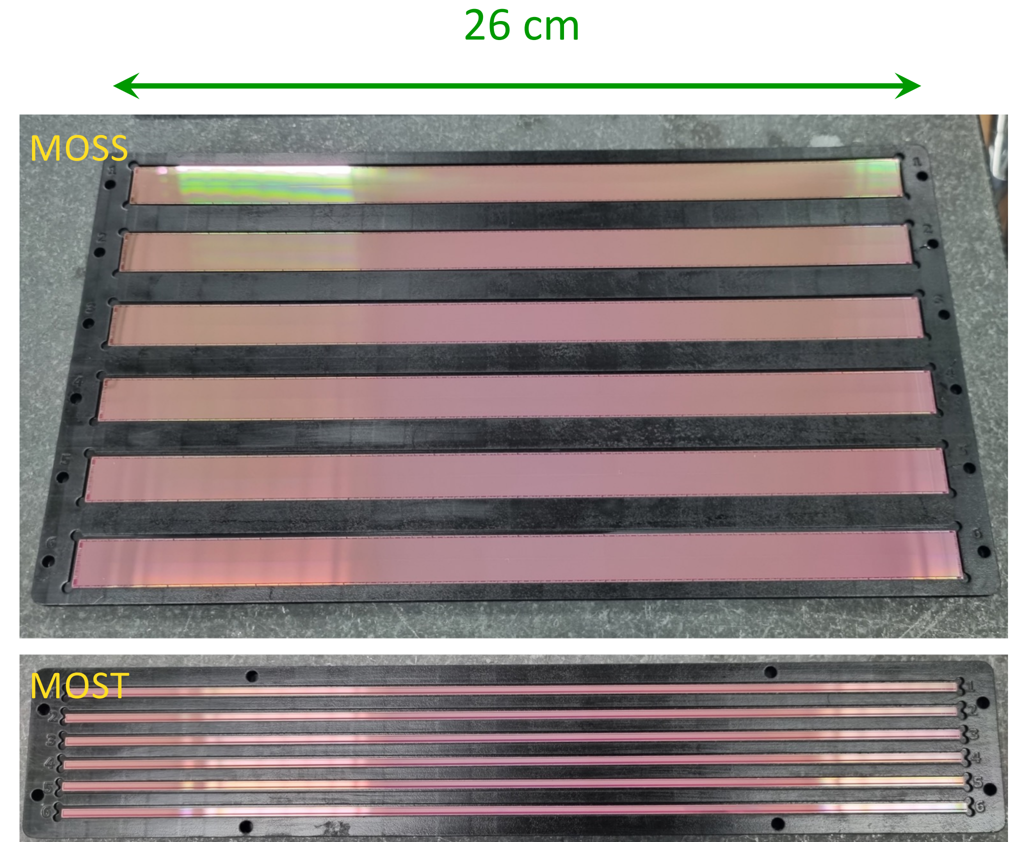
Parameter	Value
Area	$45\ \mu m^2$
Power	36 nW
Gain	$1\ mV/e^-$
Threshold	$150\ e^-$
Peaking time	$1\ \mu s$
Phase Margin	$55°$
Thr. Dispertion	$15\ e^-$
ENC	$10.5\ e^-$

Thinning/Dicing/Picking tests

- Wafers thinned and diced (50 µm)
- Chips picked using dedicated tooling at CERN, similar setup prepared at NIKHEF
- Works!

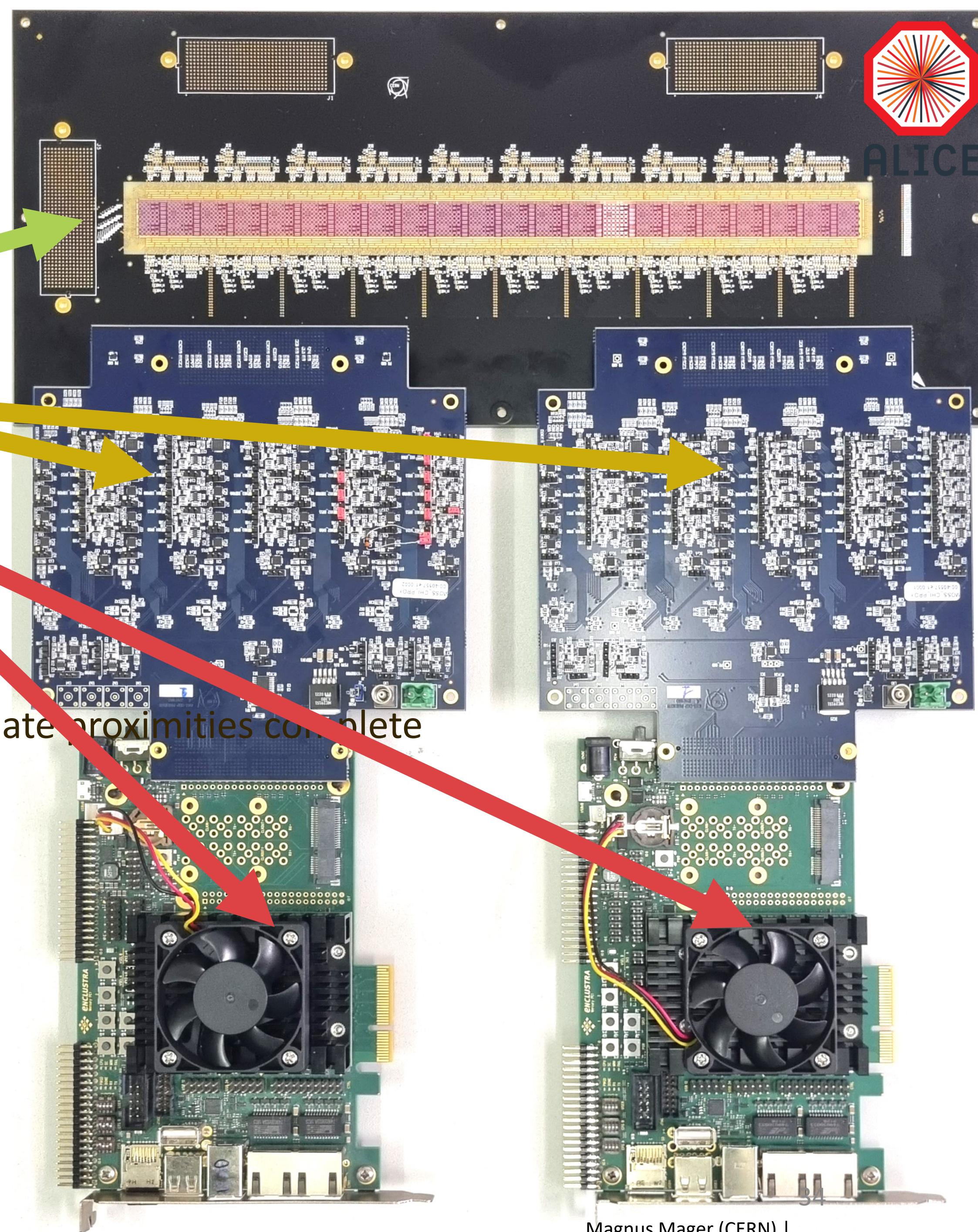


26 cm



ER1 (MOSS) test system

- Based on:
  - carrier card (passive; custom made)
  - 5x proximity card (active; custom made)
  - 5x FPGA board (commercial: enclustra Mercury+ AA1+PE1)
- Status:
  - carrier: V2 (cosmetic changes) in production
  - proximity: V2 (minor bug fixes) in production
  - FPGA boards: delivered (12 units)
  - Soft- and firmware: under development, functionality to validate proximities complete
- Complex system:
  - NB: picture on the right shows only 2/5 parts
  - important to start early, no criticalities
  - Very first tests indicate life in the chip



SUMMARY and OUTLOOK

After MLR1: 65 nm ISC qualified for HEP:

- Building knowledge about this technology for general interest
- Results fully in line with ECFA roadmap
- Very significant effort with **synergy with the ALICE ITS3 upgrade project without which this progress could not have been made.**

ER1: exploration of stitched sensors

- Back from foundry, significant testing effort ahead

ER2: focused on large stitched sensor MOSS2 for ITS3 upgrade

- MOSS2 will need to satisfy ITS3 requirements
- Less chiplets
- Tapeout spring 2024

MLR2…4: Organizing access for wider HEP community and continuing R&D for experiments (ALICE 3, ….)

- See next page

SUMMARY and OUTLOOK

Organize access for HEP community, and continue R&D, coordinate and streamline efforts in the R&D,

also in testing (!), in synergy with the experiments (ALICE3, …) and other R&D projects

As part of CERN EP R&D WP1.2 on monolithic sensors and DRD7. 6 on complex imaging ASICs and technologies, aligned with ECFA roadmap

- Set up joint access for TPSCo 65 nm technology (and possibly others like TJ 180 nm, Lfoundry supported by other institutes, …)
    - Engineering runs MLR2-4 with small chiplets, reticle scale and wafer scale stitched sensors on single wafer
    - Common framework with frame contract, PDK, libraries, …
    - IP blocks (standard pixels, pad rings, ADCs …)
- Shared access to 3 D technologies
- Common QA/ASIC development framework
    - Designer's fora
    - Standardized test setups and readout, MASSIVE testing effort

	2024	2025	2026	2027	2028
Deliverables:		Des.Kit & Libraries; Report ER2		Report MLR2	Report MLR3
Tape-out dates:	ER2	MLR2		MLR3	MLR4

- See call for proposals for DRD 7 (please express your interest before June 30th 2023)
- See also last general WP1.2 general reporting meeting: https://indico.cern.ch/event/1280150/

CERN EP R&D

THANK YOU TO ALL CONTRIBUTING PEOPLE, GROUPS AND INSITUTES

SPARE

ECFA Detector R&D in Electronics: DRD7. Call for projects

Dear Colleagues

You receive this message because you registered to the ECFA DRD7 interest group.

In view of drafting its Letter of Intent, DRD7 is now calling for projects in electronics, following the priorities established in the ECFA Detector R&D roadmap document.

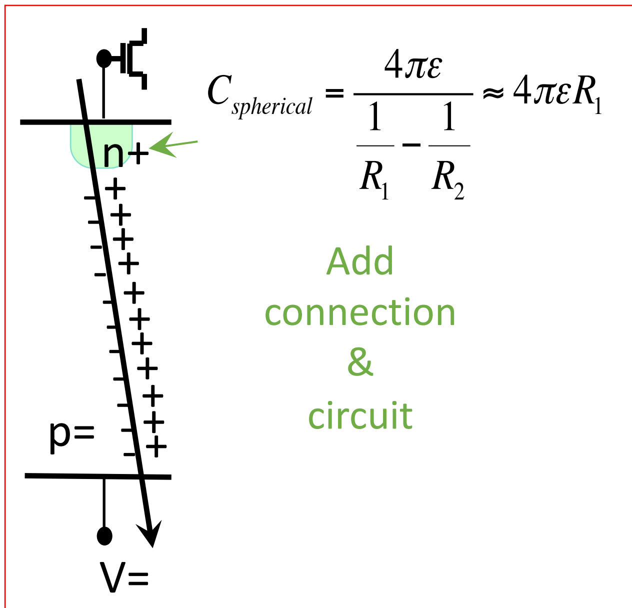
Interested scientists, groups or collaborations are invited to express their interest by contacting the relevant DRD7 WG conveners with their project intentions.
Conveners will collect the community feedback and aggregate it into a portfolio of projects in each WG.
These preliminary project intentions will form the basis of the Letter of Intent, due to be submitted in July 2023.

The two attached documents give all necessary information on the call for projects itself, and on the DRD7 future organization.

Please express your interest before 30 June 2023.

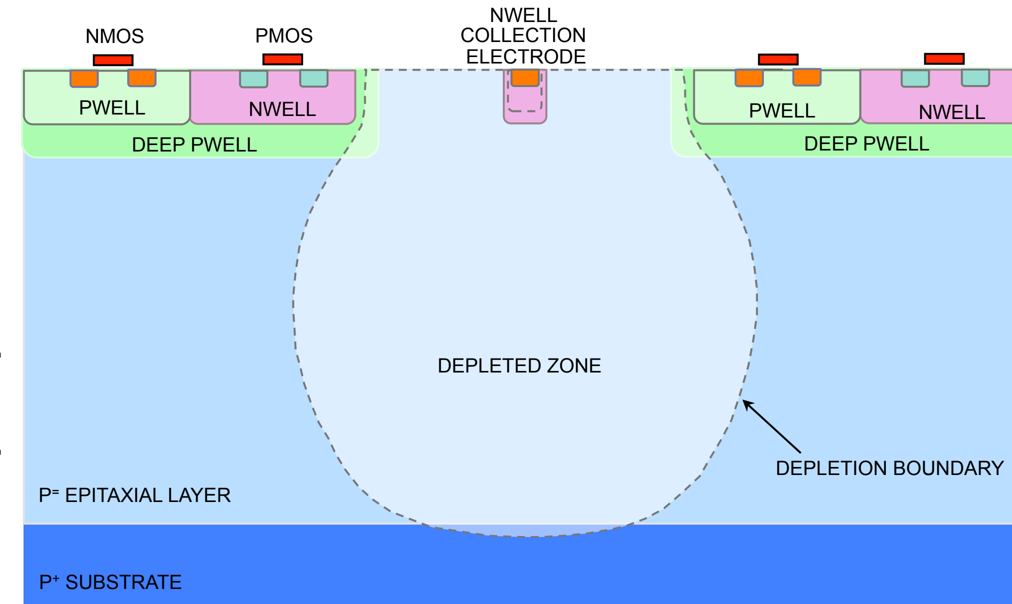
Francois Vasey, on behalf of the steering and technical committees.

The need for sensor optimization to obtain full depletion



Planar junction
Depletion width $= \sqrt{\frac{2\mathcal{E}|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\frac{2\mathcal{E}|V|}{qN_A}\frac{3R_1}{2}}$



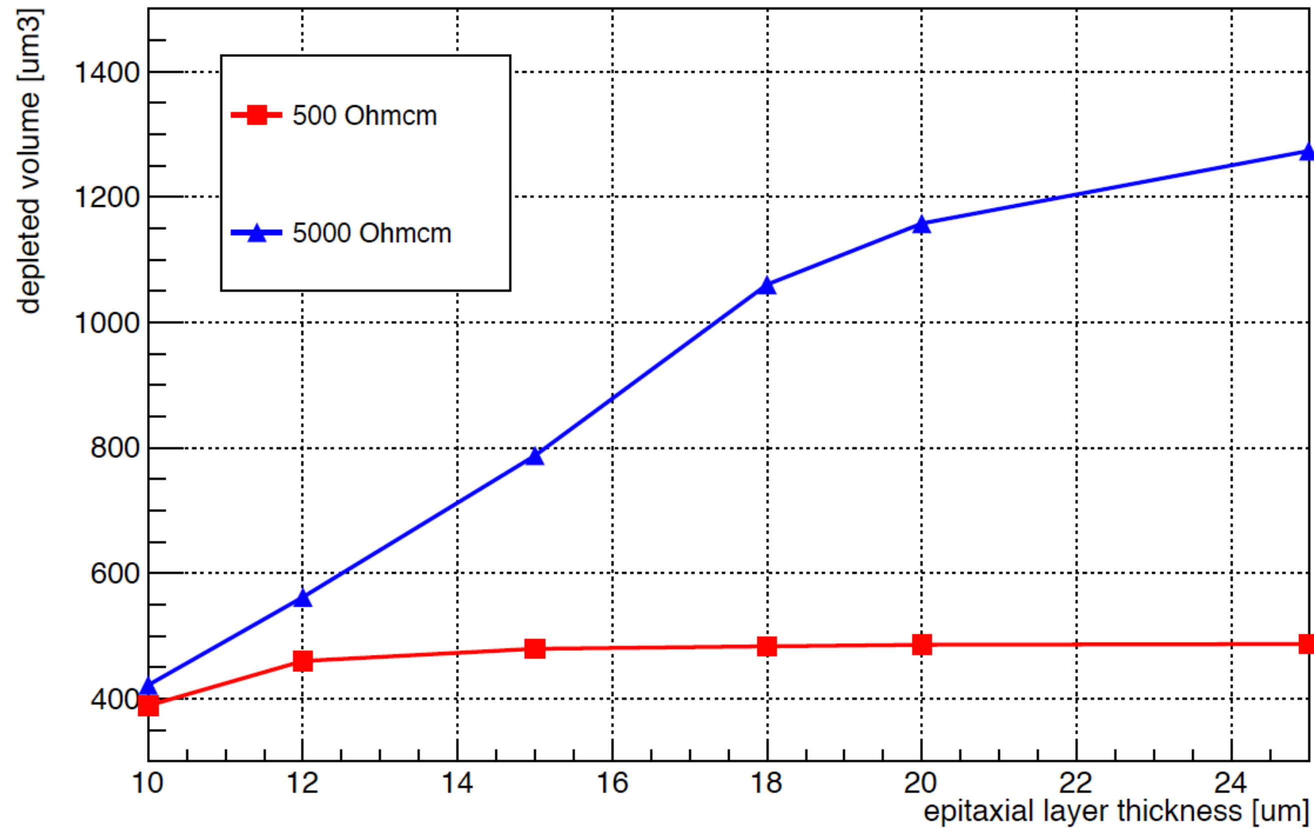
Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation

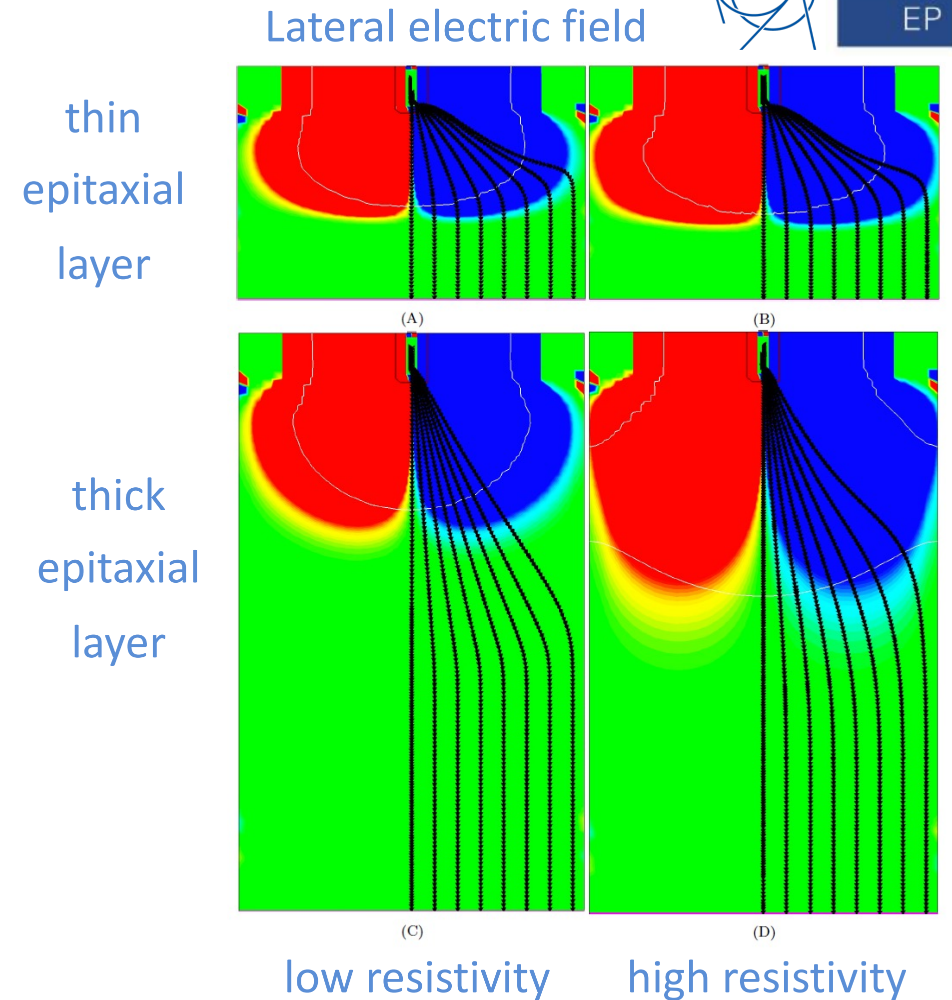
Planar vs spherical junction

- Planar junction: depletion thickness proportional to *square root* of reverse bias.
- Spherical junction : depletion thickness proportional only to *cubic root* of reverse bias, inner radius R1 to be kept small for low capacitance
- Deep pwell and substrate limit extension of the depletion layer -> see next slide

Sensor optimization: influence of the resistivity of the epitaxial layer

CERN EP R&D





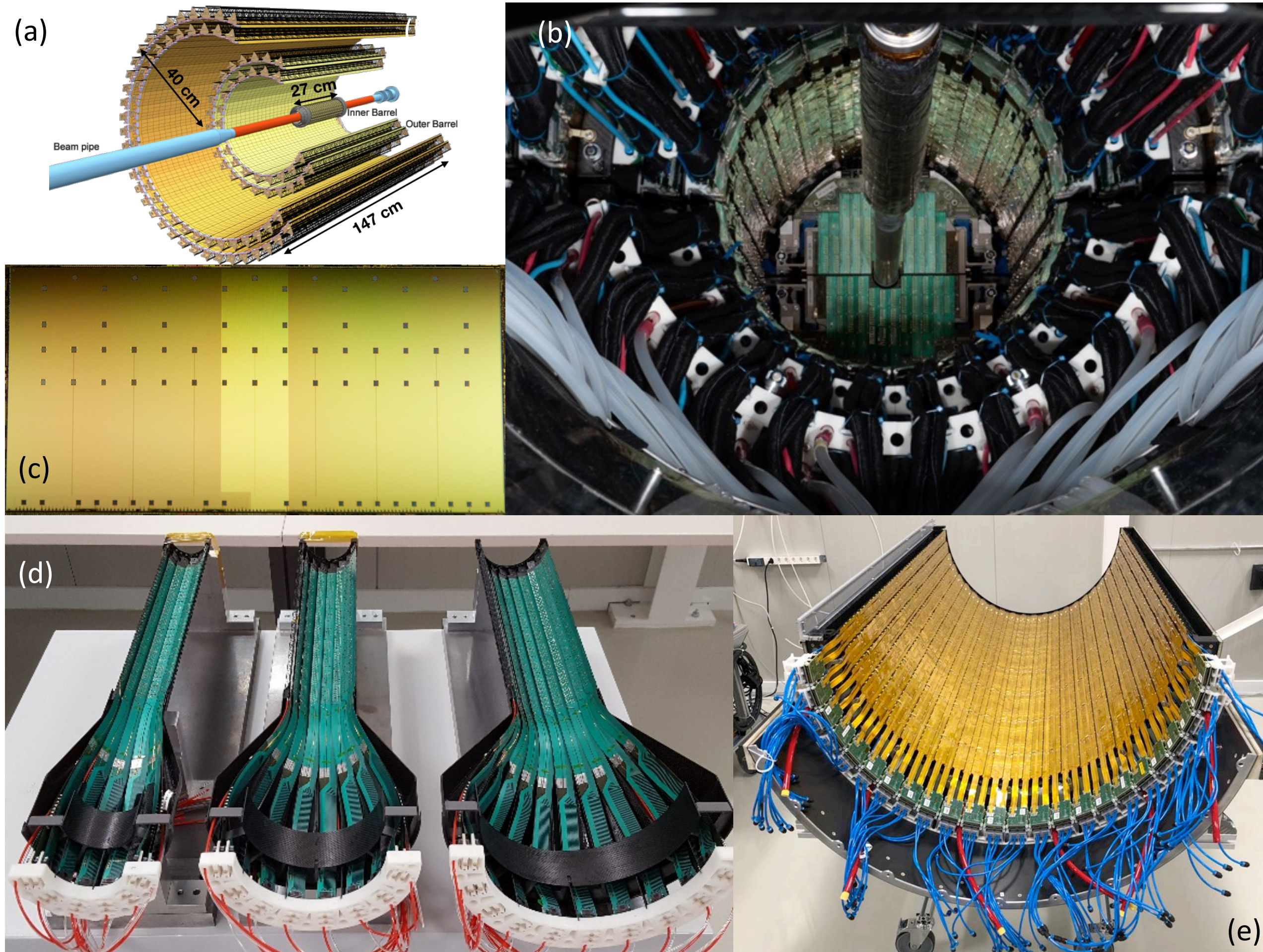
For thinner epitaxial layers, higher resistivity does not help for further depletion due to the proximity of the substrate

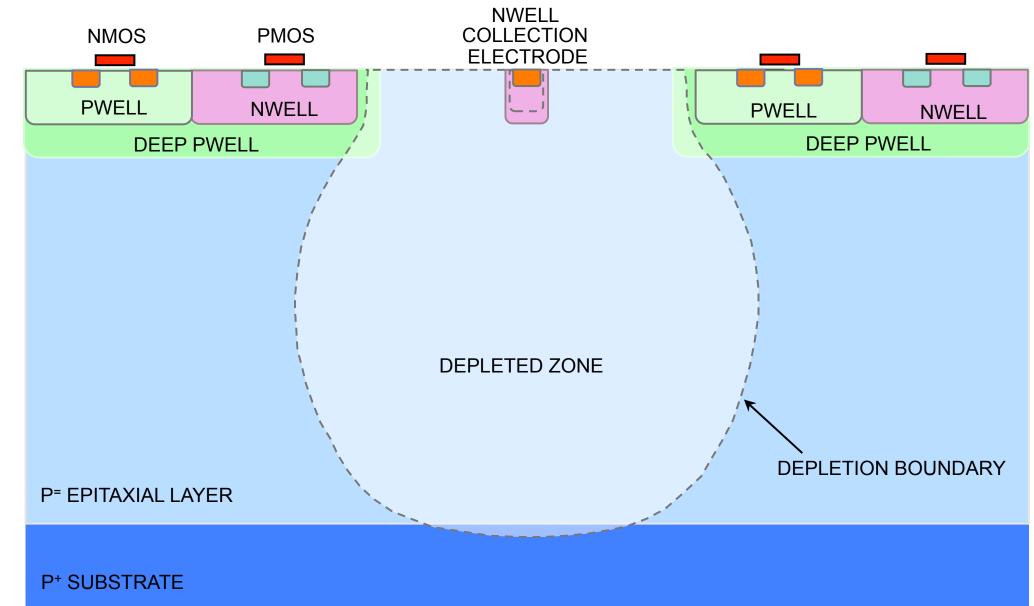
Depletion constrained by the substrate and surrounding pwells

State of the art: ALICE Inner Tracking System 2 : 10 m^2 with 3x1.5 cm^2 ALPIDE chips

TowerJazz 180 nm imaging CMOS technology, development 2012-2016

CERN EP R&D





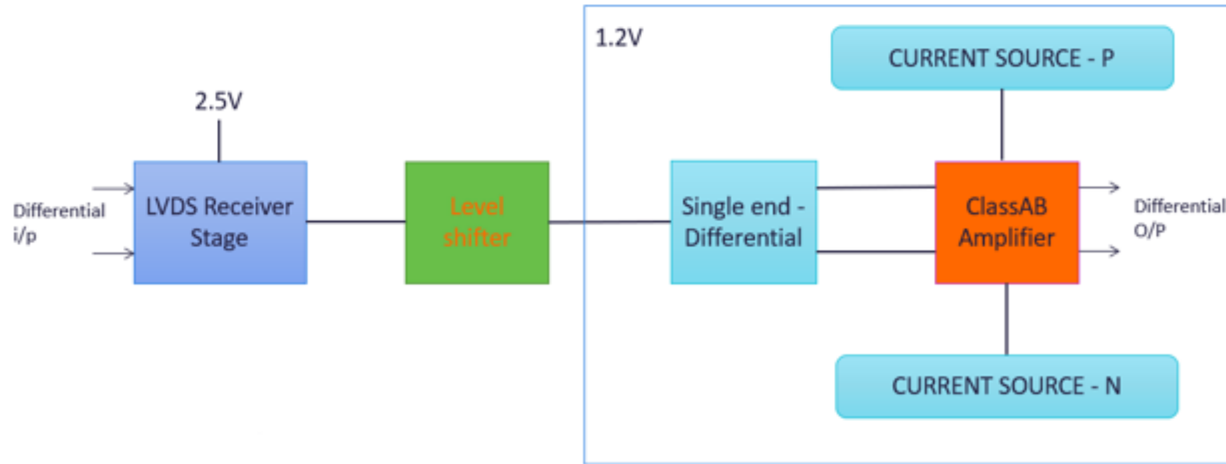
ALPIDE CHIP

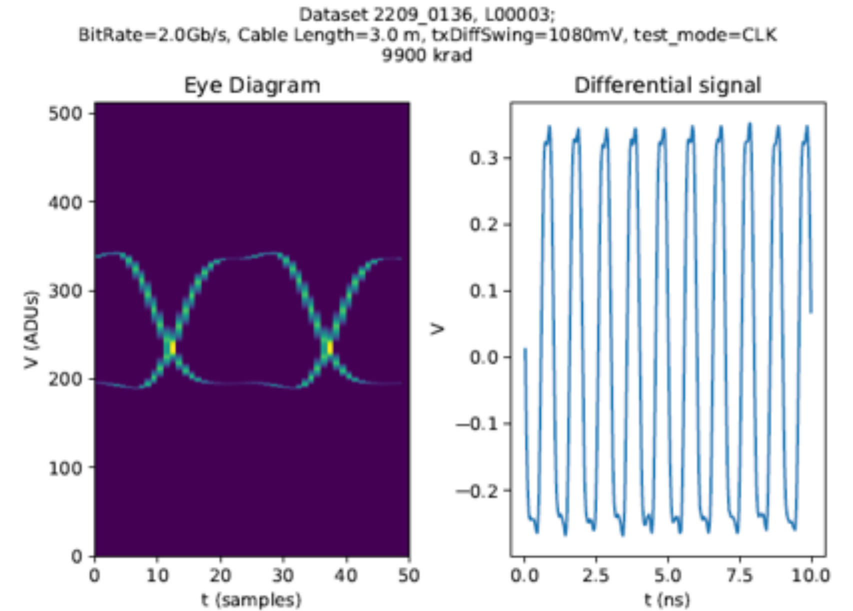
- 512 x 1024 pixels of 28 x 28 μm^2
- Full CMOS in the pixel (deep pwell)
- 40 nW front end, sparse readout
- Matrix 6 mW/cm^2, up to 40 mW/cm^2 including periphery
- Standard process: sensitive epitaxial layer not depleted

STFC

RAL: S. Mathew, Iain Sedgwick

- MLR1 submission with CML driver:





- Several other institutes have submitted test chips: Yonsei and SLAC (pixel test matrix), DESY (test pixels and Krummenacher feedback amplifier)

^{55}Fe measurements confirm influence on charge sharing

See also: I. Sanna IEEE NSS 2022

ALICE ITS3 *preliminary*
Fe-55 source measurements
Plotted on 28 Sep 2022

Charge collection peak

Charge sharing peak

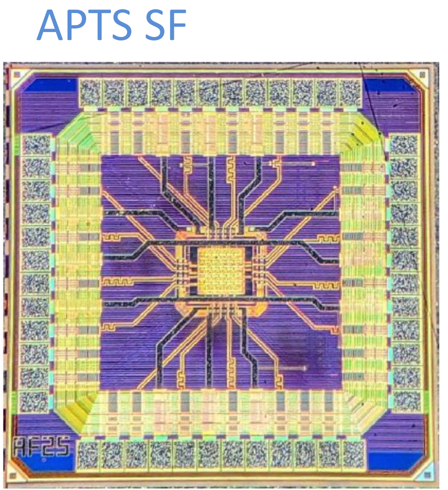
Relative frequency (per 20 e^-)

Seed pixel signal (e^-)

APTS SF
pitch: 15 µm
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

- split 1, standard type
- split 4, standard type
- split 4, modified type
- split 4, modified with gap type

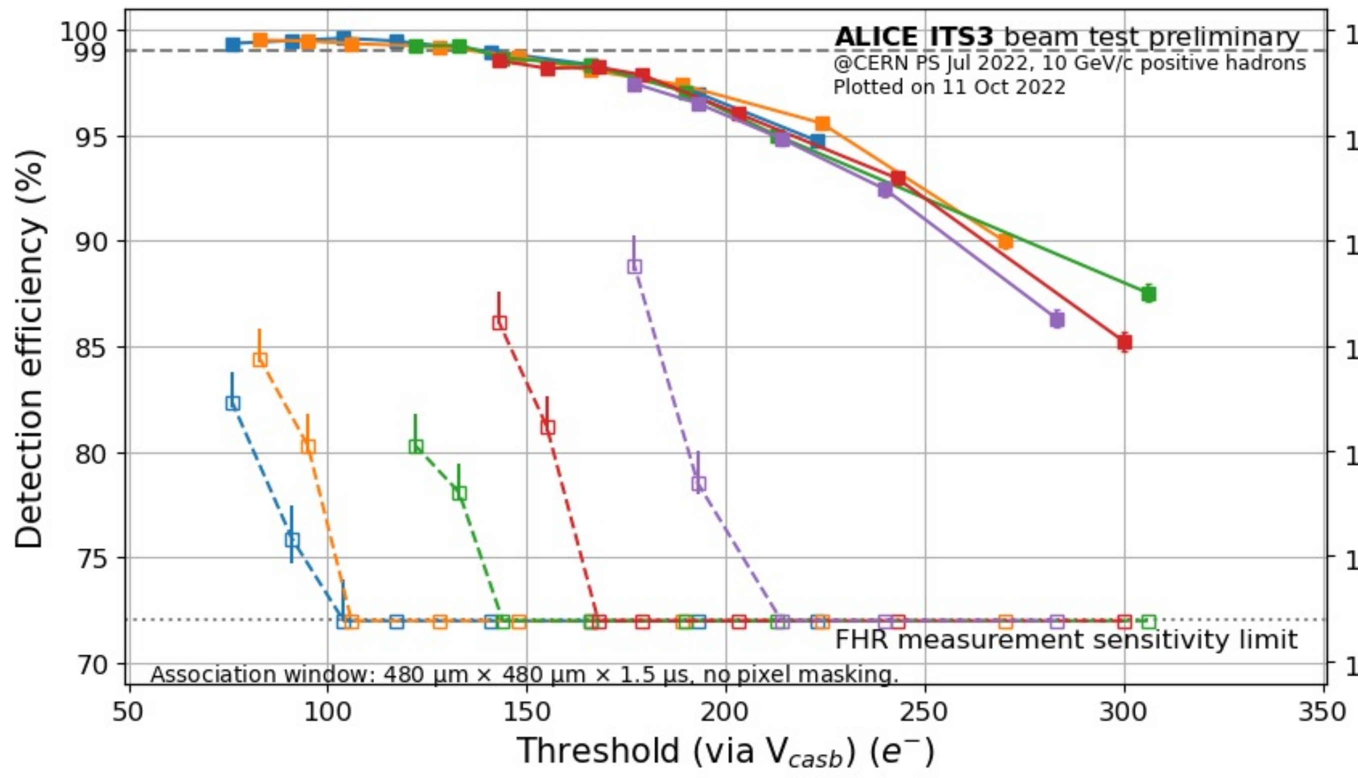
APTS SF



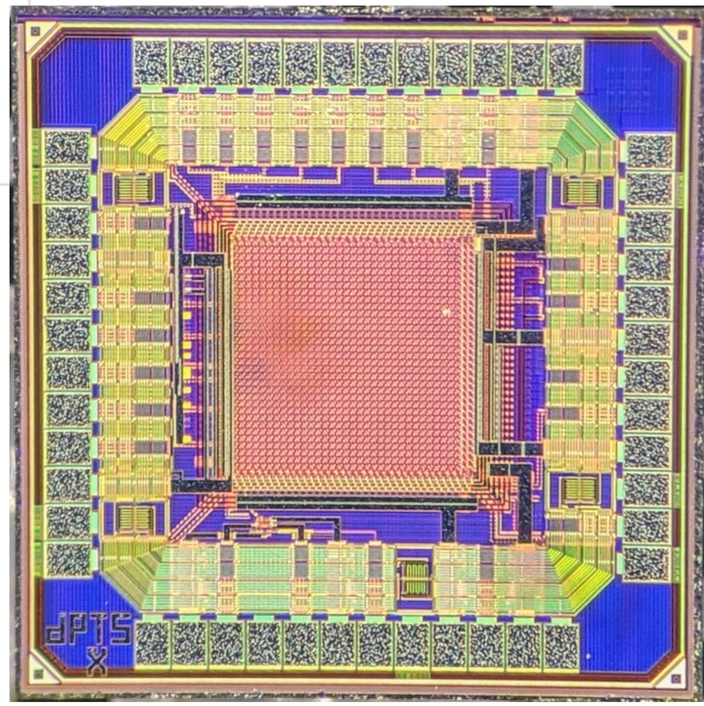
No experimental comparison between split 3 and split 4 available yet.

Detection efficiency/Fake hits/Sensor radiation tolerance

CERN EP R&D



DPTS

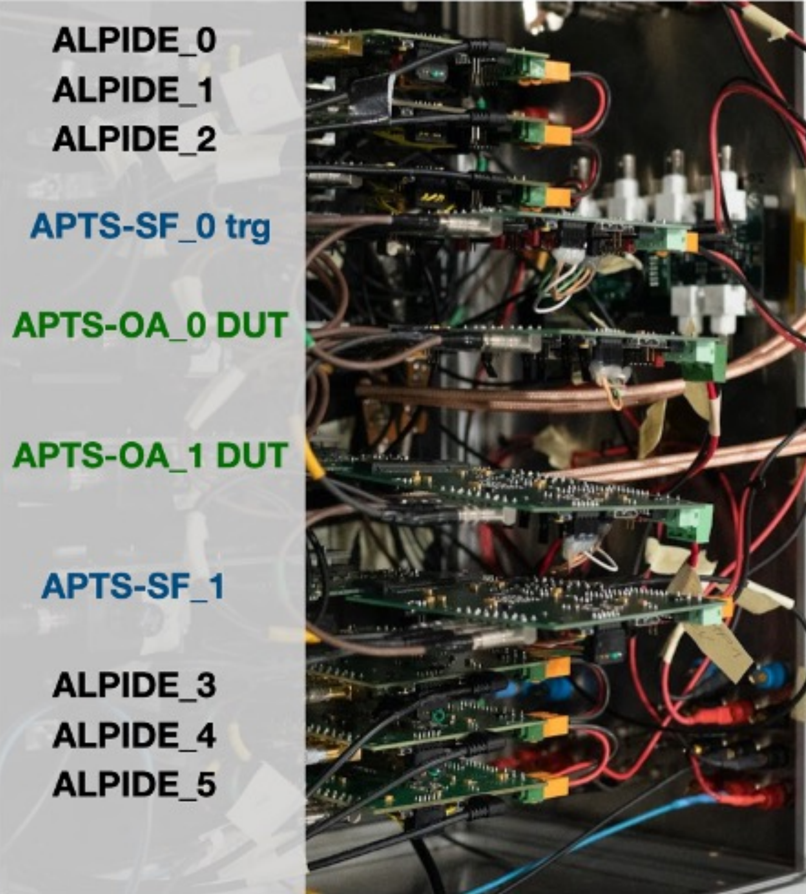


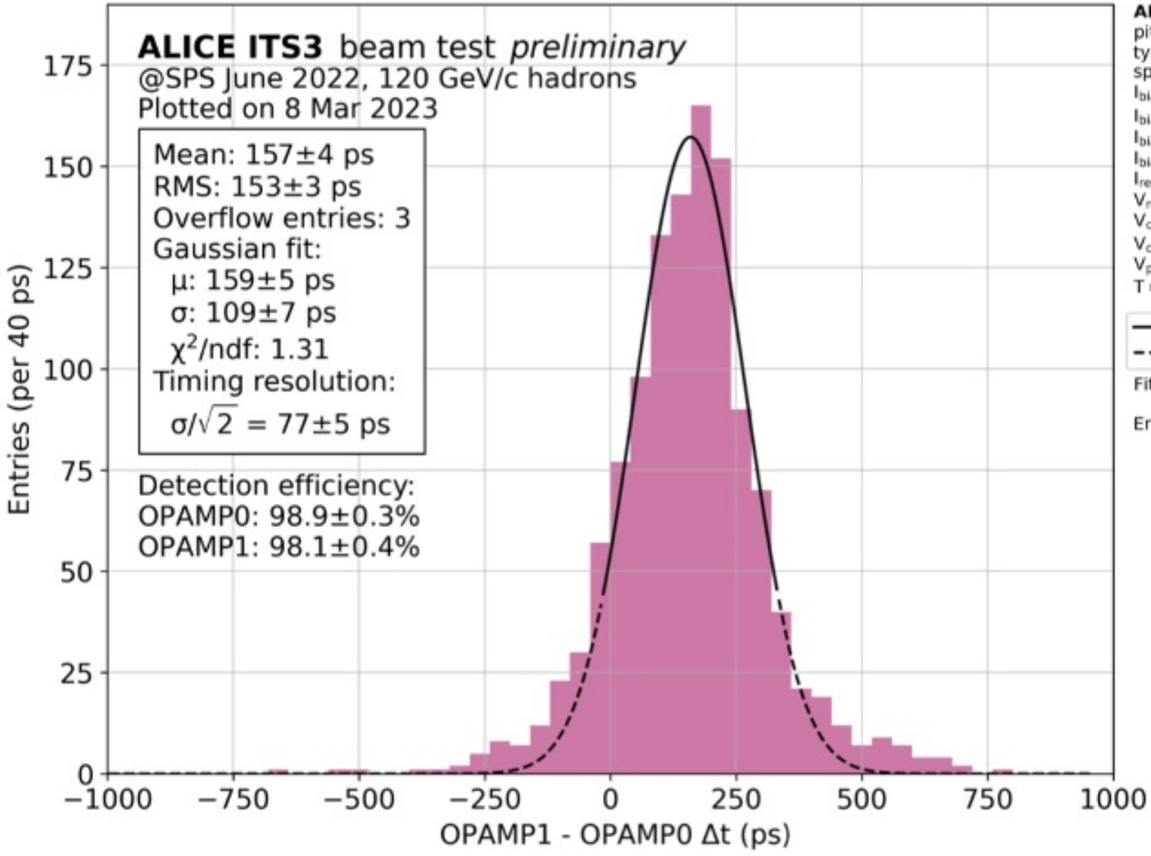
- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm² pixel (DPTS) including sensor optimization
- Large operating margin before irradiation
- After 1E15 n_{eq}/cm^2 efficiency > 99% maintained at room temperature
- Higher fluencies under investigation

https://arxiv.org/abs/2212.08621

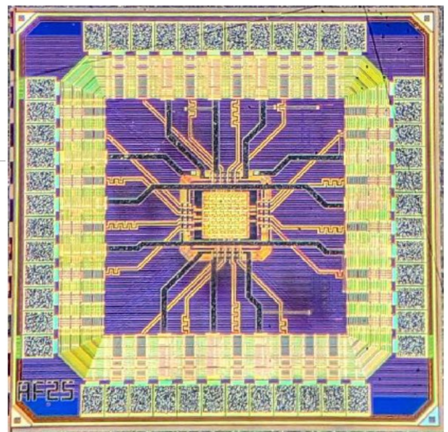
Time resolution of the sensor

(U. Savino et al. ULITIMA 2023)





APTS

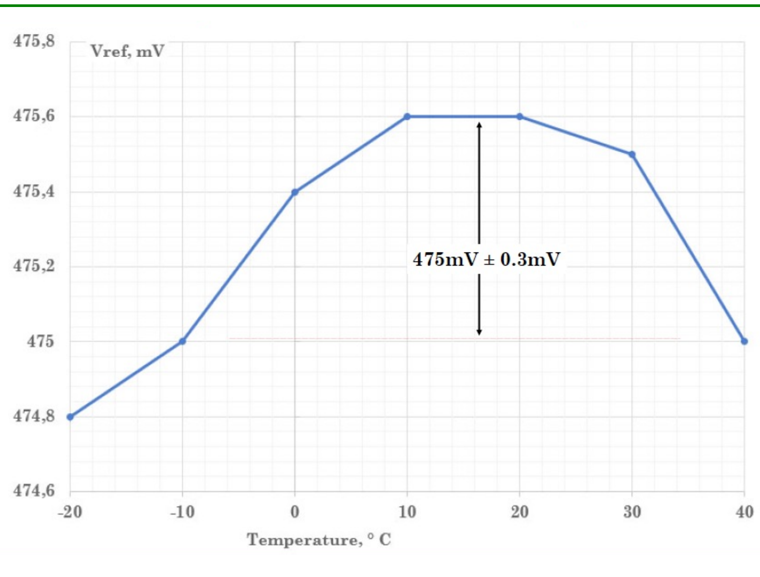


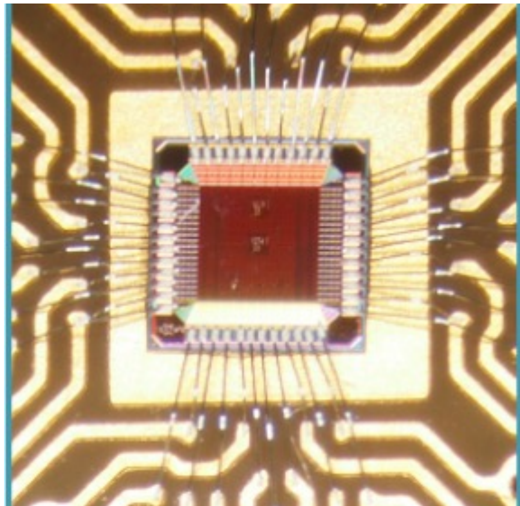
- Two chips with 4 x 4 matrix at 10 µm pitch put into coincidence (!)
- Measured sigma of the time difference = 109 +- 7 ps, per plane 77 ps
- No timewalk correction yet.
- In 180 nm ~100 ps with timewalk and cluster size correction (J. Braach et al. ULITIMA 2023)

IP Block measurements bandgap, T-sensor, VCO: all functional and tolerant to 100 Mrad or beyond

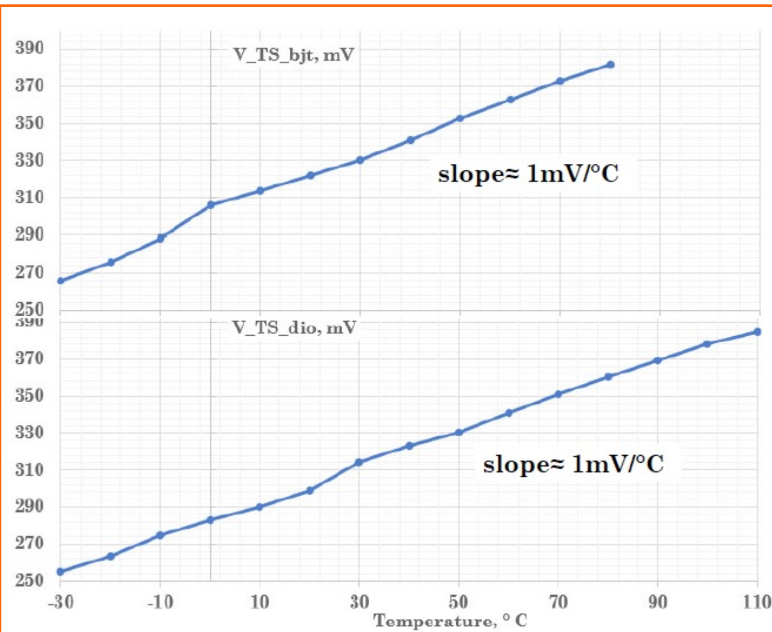
NIKHEF: V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, M. Rossewij (TWEPP 2022)

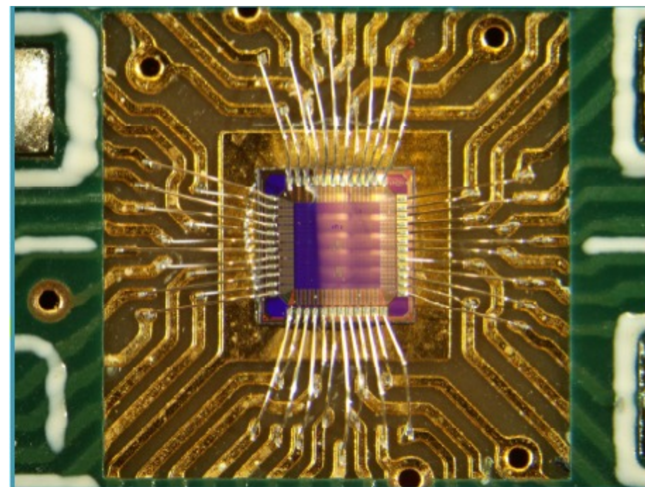
Bandgap



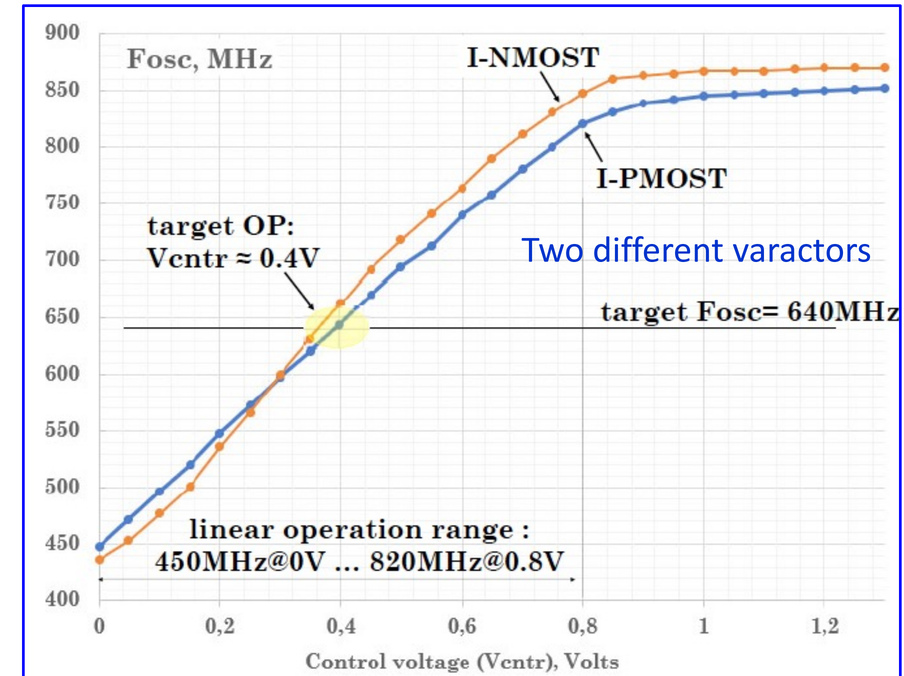


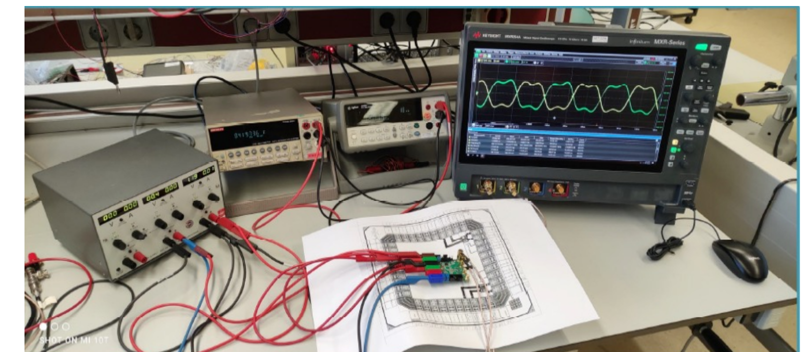
Temperature sensor





Voltage Controlled Oscillator (VCO)





IP Block measurements DAC

IPHC: I. Valin, S. Bugiel, A. Dorokhov, C. Colledani, C. Hu et al.

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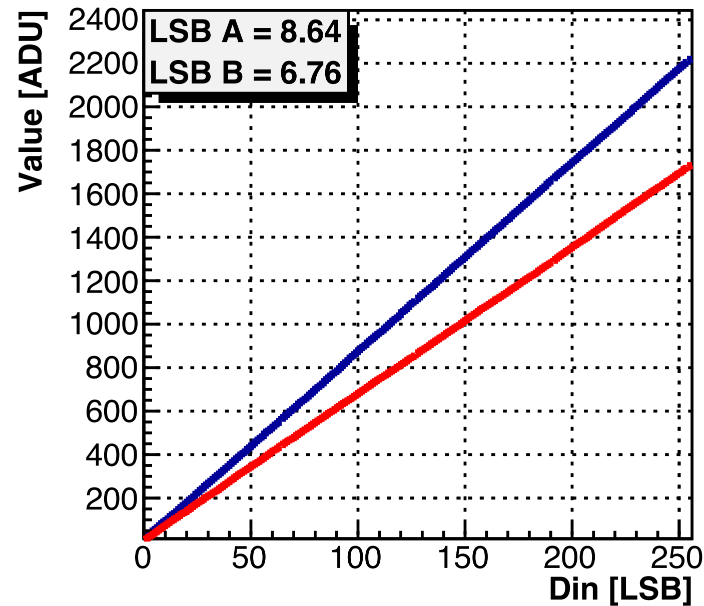
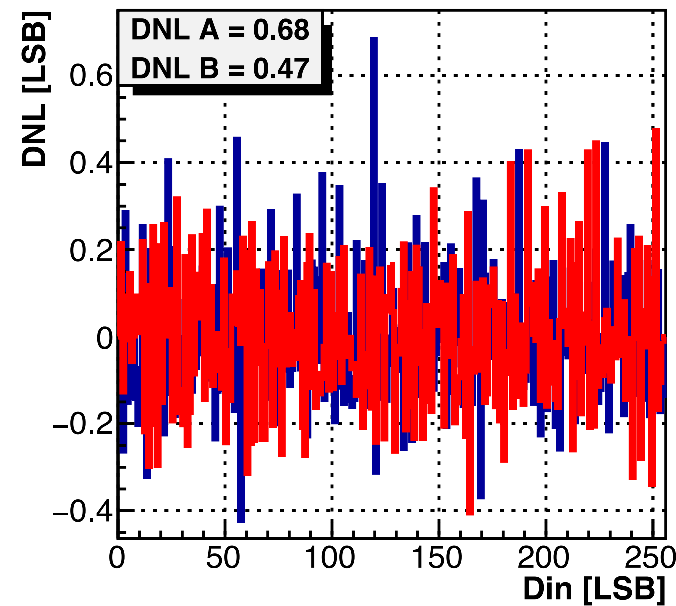
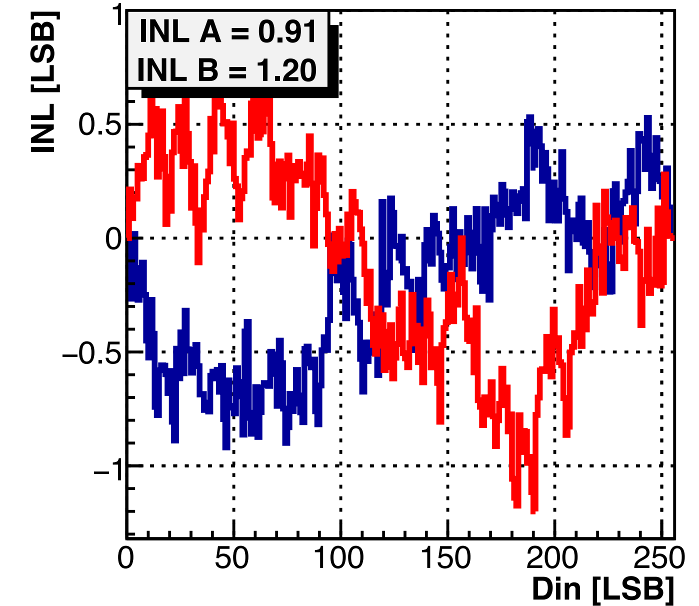
	DAC A	DAC B
Resolution	8 bit	8 bit
LSB [nA]	40	40
Reference current [uA]	-0.8	-10.72
Power [uW] (*)	13	13
Area [um x um]	133x253	143x253

Both DACs remain functional after 500 Mrad irradiation with DNL < 1 LSB, INL < 2 LSB

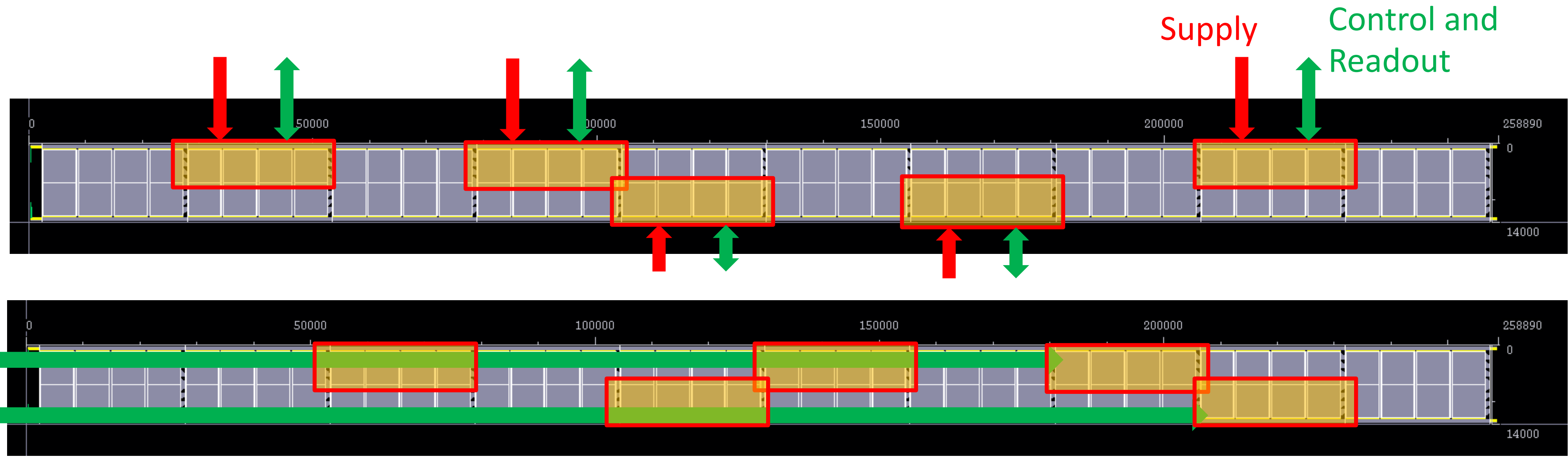
10 keV X-rays 6.5 Mrad/hour







MOSS TESTING SCENARIOS - EXAMPLES



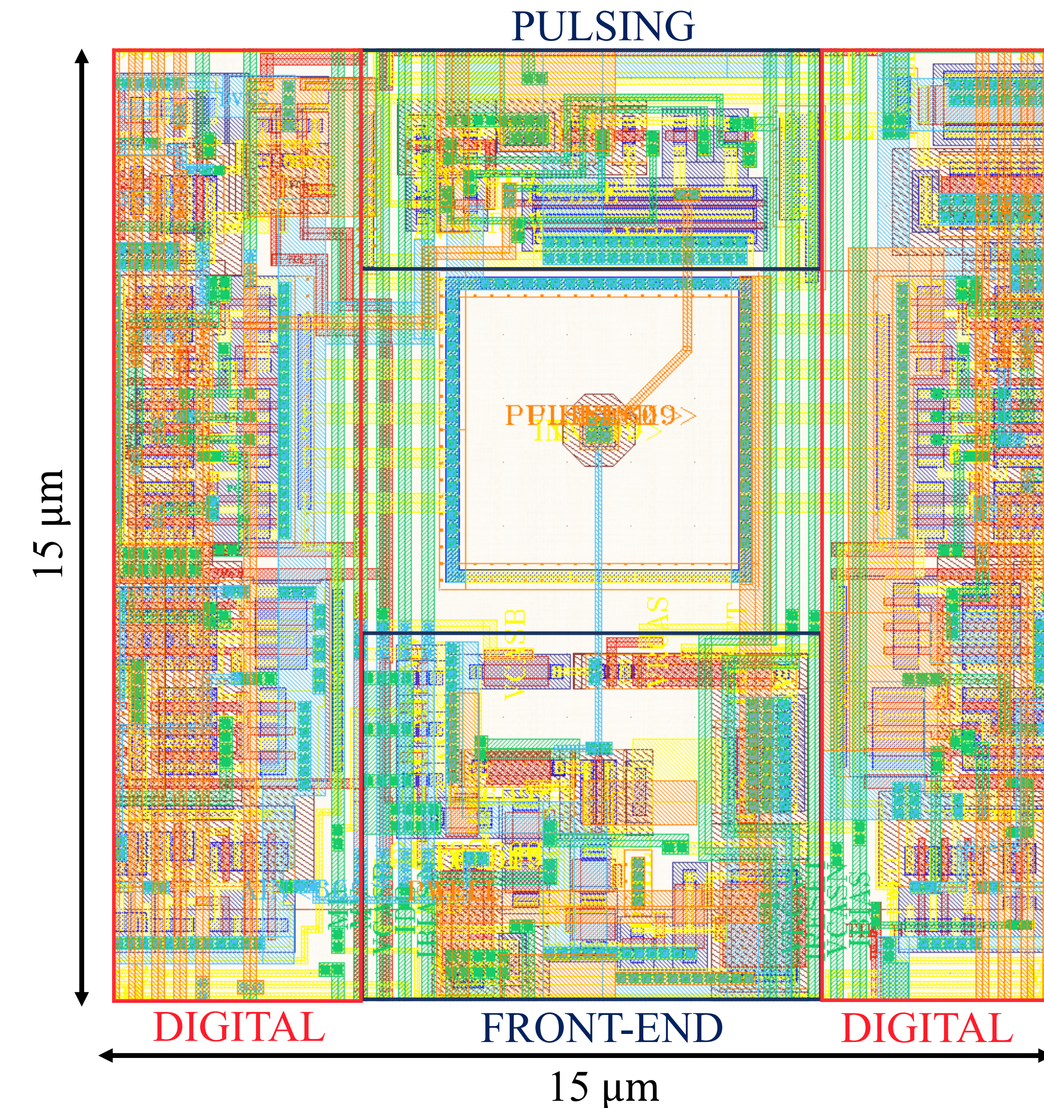
Test the sub-units independently

Study manufacturing yield

- Functional yield at half unit, block, column/row/pixel level granularity
- Possible dependence on pixel pitch and layout density?

Study noise, threshold, position resolution vs pixel variants

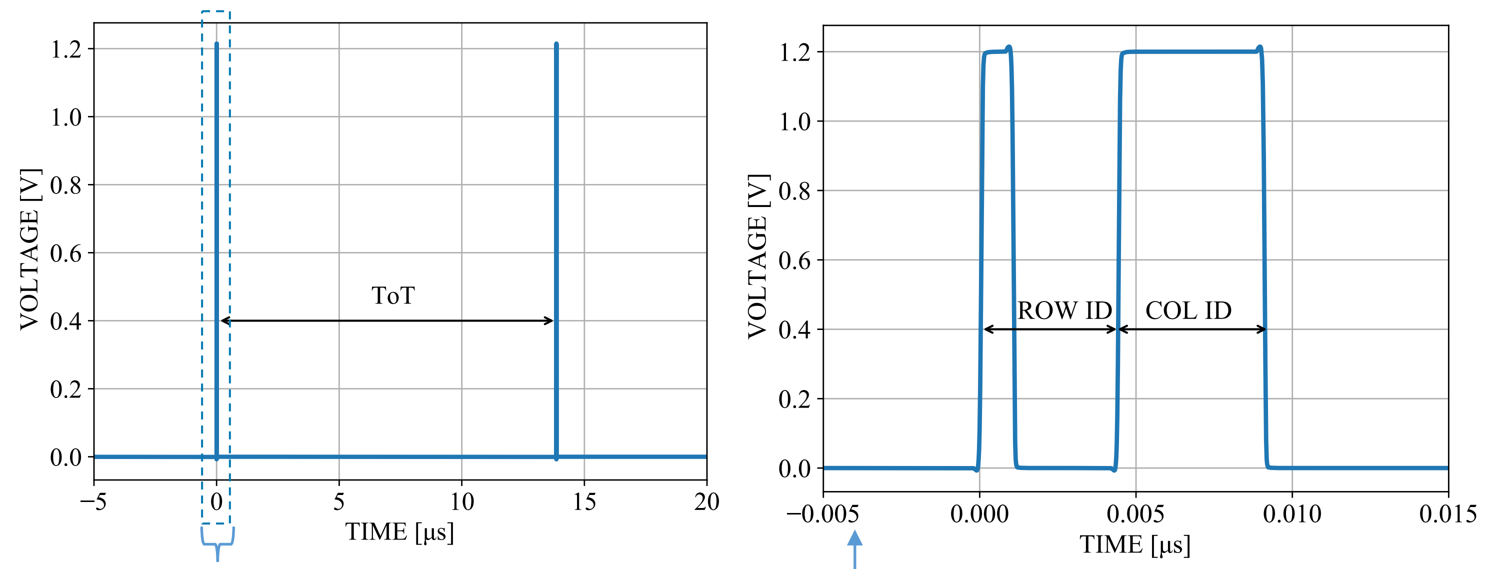
DPTS Pixel layout



In-pixel circuitry:

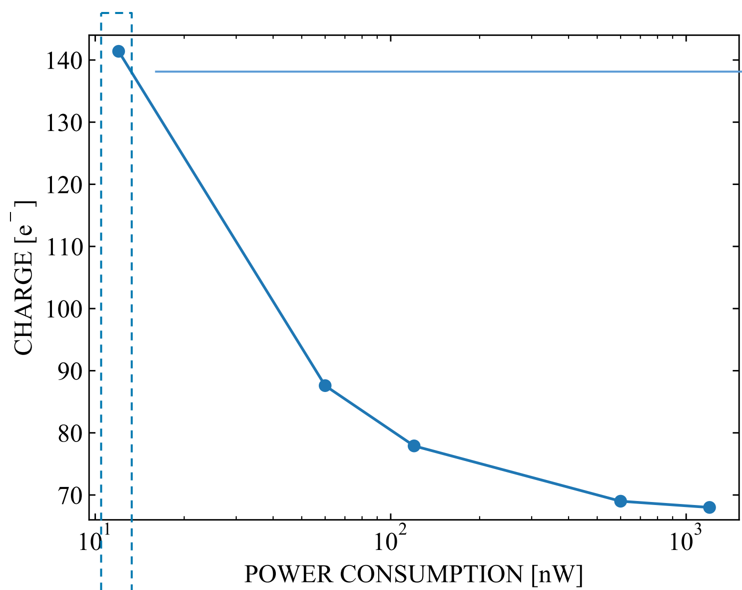
- front-end amplifier and discriminator (42 μm^2).
- test pulse injection circuitry (17 μm^2).
- digital gates for asynchronous transmission of the time-encoded pixel address (140 μm^2).

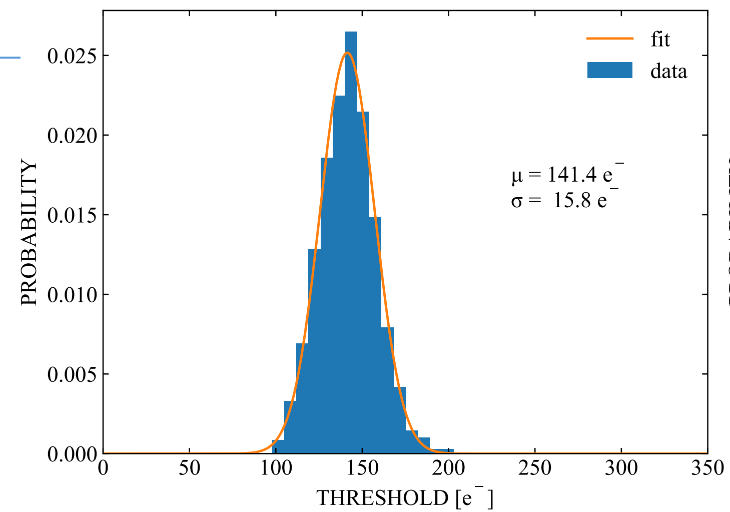
Analog power density over the matrix as low as ~ $\mathbf{5\ mWcm^{-2}}$.

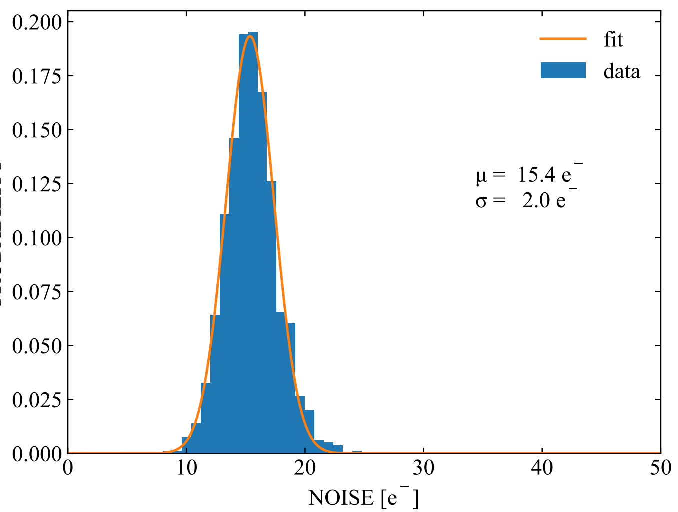


L. Cecconi, et al., "Design and readout architecture of a monolithic binary active pixel sensor in TPSCo 65 nm CMOS imaging technology ", TWEPP 2022.

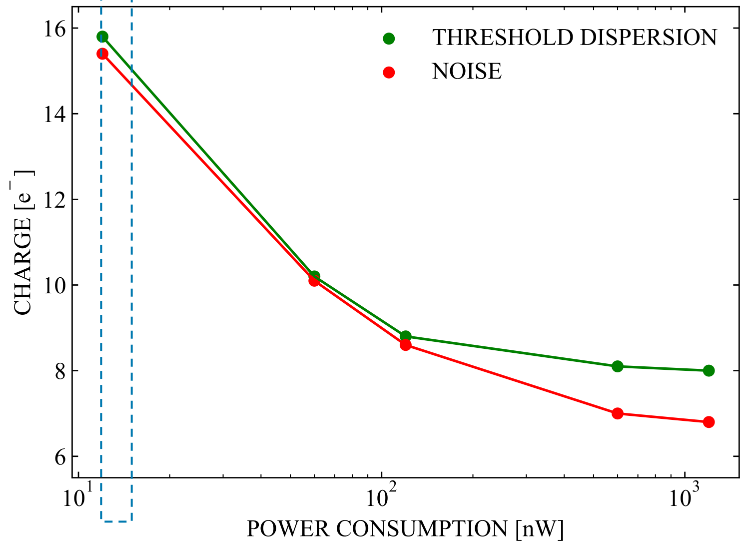
Measurements - threshold dispersion and noise

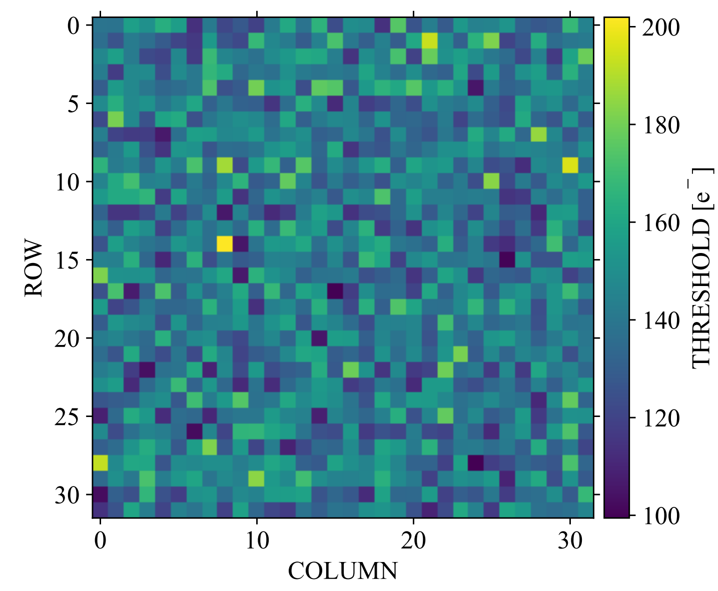


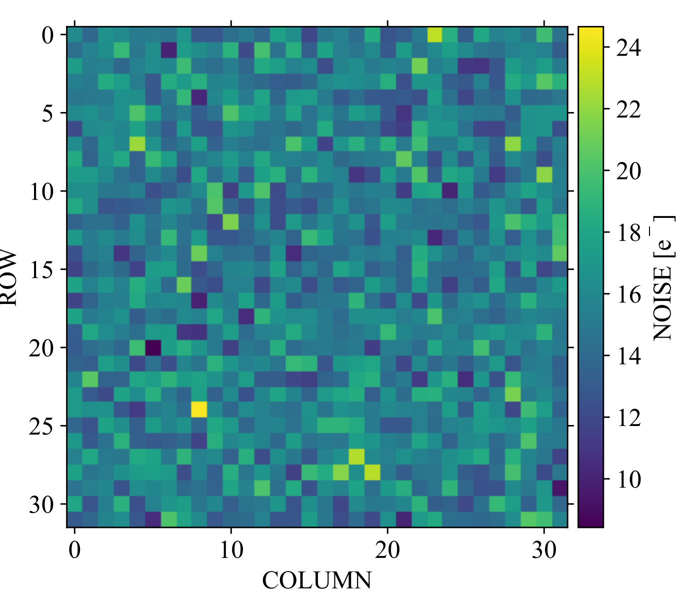




Good agreement with simulations (th.d. $\approx 15.8\ e^-$ noise $\approx 15.4\ e^-$).







No systematic effect over the matrix.

Timing measurements

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