Status of CMOS pixel sensor prototypes for the CEPC vertex detector

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On behalf of the CEPC Vertex detector study team

XII Front-End Electronics Workshop

June 12-16, 2023

Outline

- **Overview of the CEPC Vertex detector R&D**
- **Progress of the JadePix chips**
- **Progress of the TaichuPix chips**
- **Summary and outlook**

CEPC Vertex detector requirements

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

➔ Impact parameter resolution,

$$\sigma_{r\phi} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$

Physics driven requirements	Running constraints	Sensor specifications
$\sigma_{s.p.}$ 2.8 μm		Small pixel ***~16 μm***
Material budget 0.15% X_0/layer		Thinning to ***50 μm***
	Air cooling	low power ***50 mW/cm²***
r of Inner most layer 16 mm	beam-related background	fast readout ***~1 μs***
	radiation damage	radiation tolerance ***≤ 3.4 Mrad/ year*** ***≤ 6.2×10¹²n_eq/ (cm² year)***

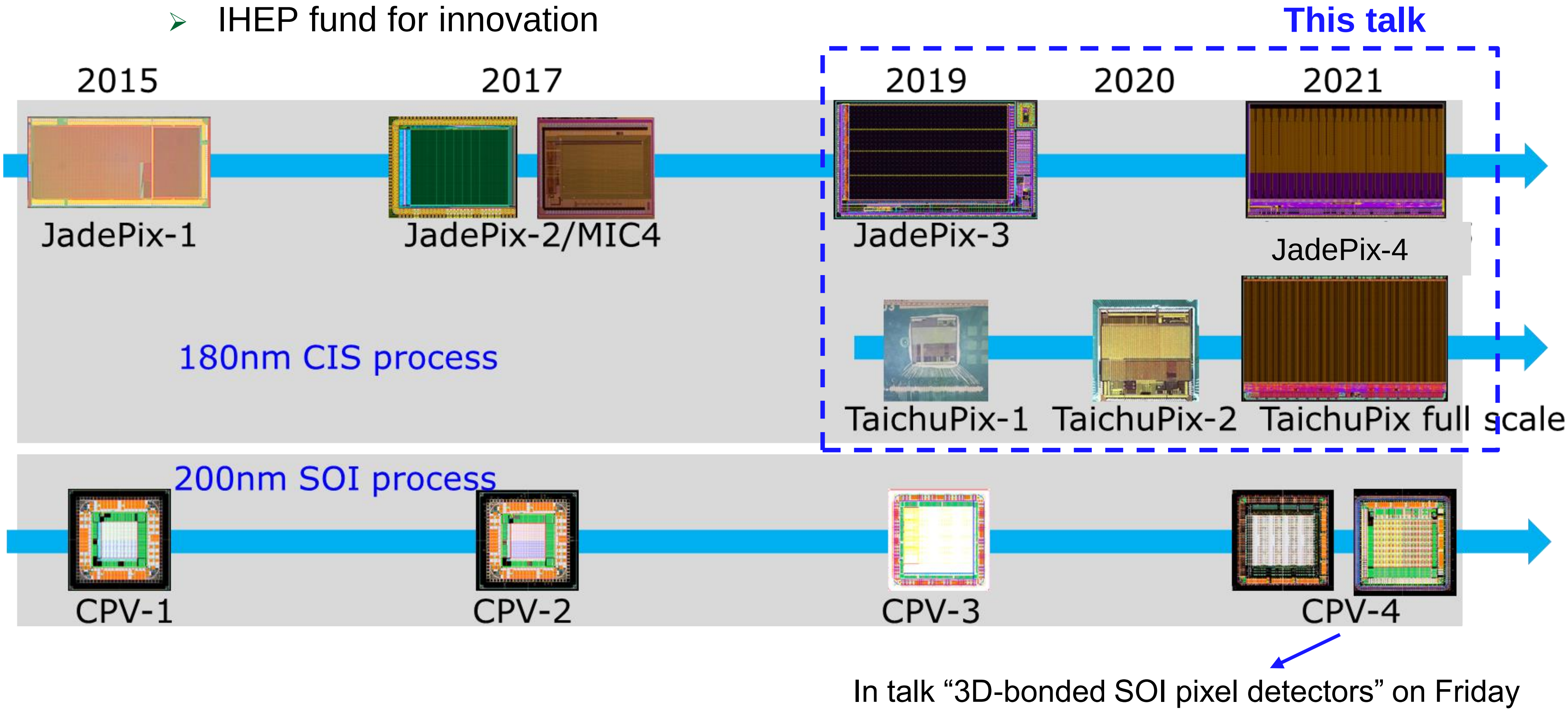
Baseline design parameters for CEPC vertex detector

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	$\sigma(\mu m)$
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Overview of pixel sensors in China for CEPC VTX

- **Development of pixel sensors for CEPC VTX supported by**
  - Ministry of Science and Technology of China (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



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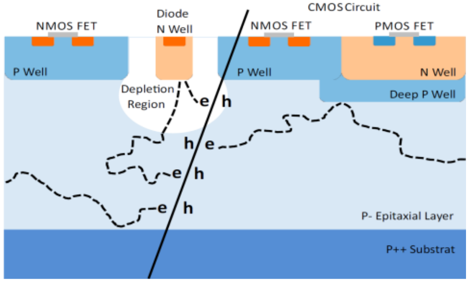
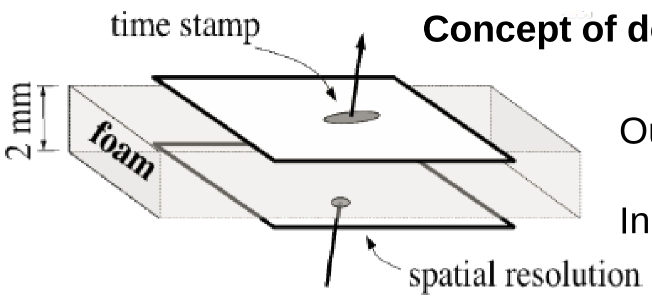


CMOS monolithic pixel sensor

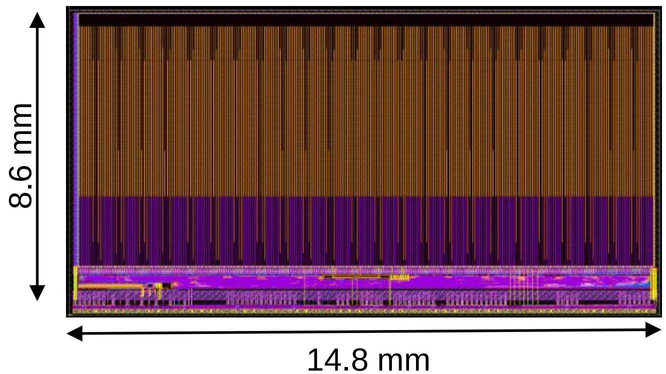
JadePix chips strategy

- **JadePix concerns the concept of double-sided layer**
  - Fine pitch & low power sensor for spatial resolution
    - Laser test on JadePix-3 indicates **s.p. < 3 μm achievable**
  - A faster sensor to provide time-stamp
    - **JadePix-4 s.p. ~5 μm, 1 μs integration time**

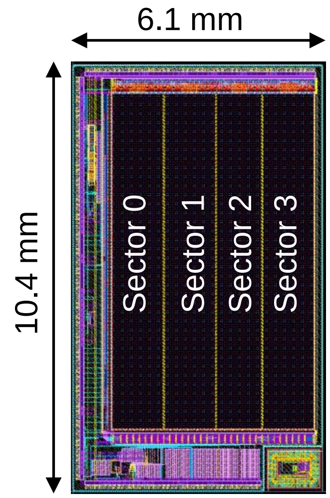
Concept of double-sided layer



JadePix-4 Layout



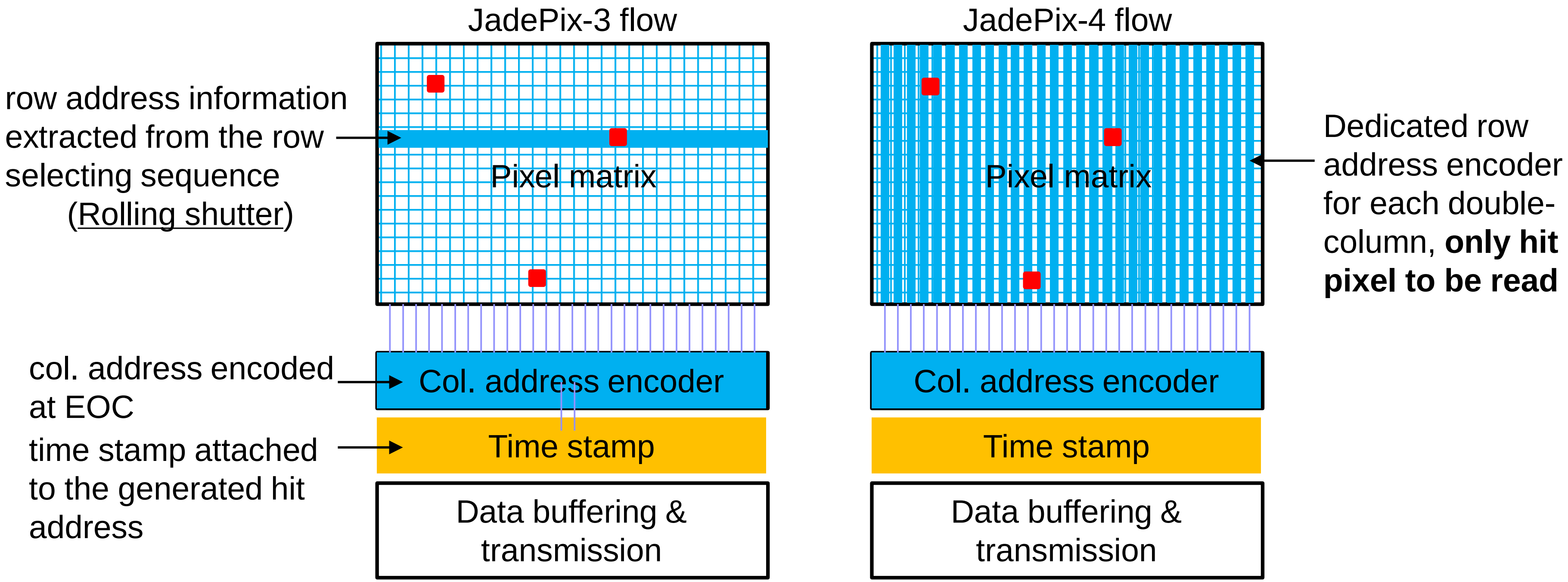
	JadePix-3	JadePix-4
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Integration time	98.3 μs	~ 1 μs
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Die size	10.4 mm × 6.1 mm	8.6 mm × 14.8 mm
Readout mode	Rolling shutter	Data-driven



JadePix-3 Layout

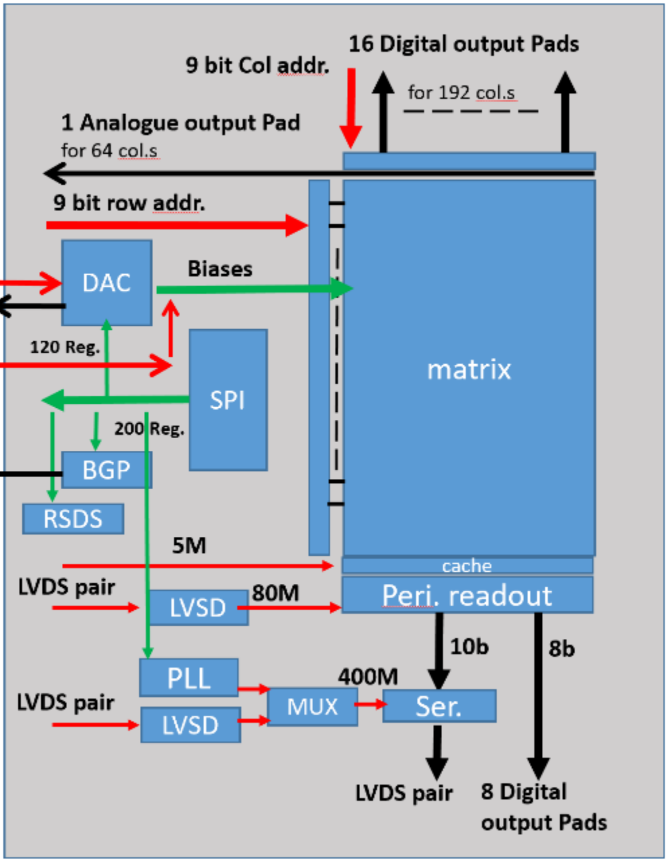
Hit processing flow of JadePix-3/4

- **Hit registered in each pixel needs fast processing**
  - Hit position (col. and row address) to be encoded
  - Time stamp to be attached
  - Register to be reset for the next hit
- **A major modification on the hit processing flow**
  - JadePix-3, rolling shutter → minimized pixel pitches
  - JadePix-4, row address encoder embedded in the matrix → much faster



An overview of the JadePix-3 design

- **Full-sized in the rφ direction of detector layout**
  - Matrix coverage: 16 μm × 512 rows = 8.2 mm
- **4 parallel sectors, scalable in the z direction**
  - 48 × 4 = 192 columns
- **Rolling shutter to avoid heavy logic and routing in pixel matrix**
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: **98.3 μs/frame**
- **Full functional blocks in the chip peripheral**
  - Zero suppression, data buffering, Serializer, PLL, DACs, SPI
  - 8-bit parallel output or serial differential output @ 833 Mbit/s

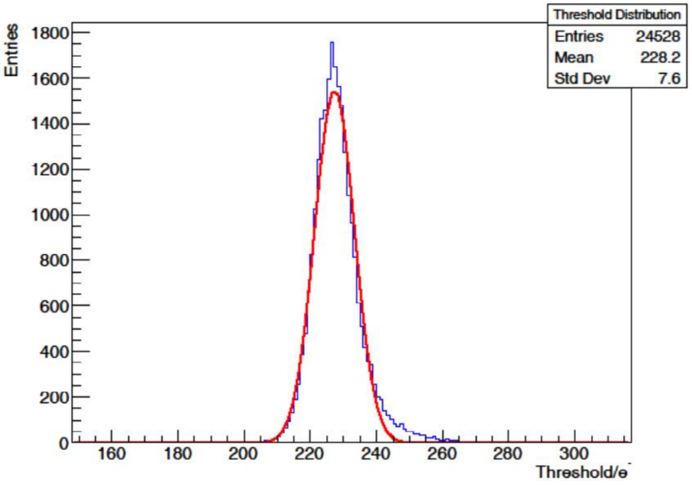


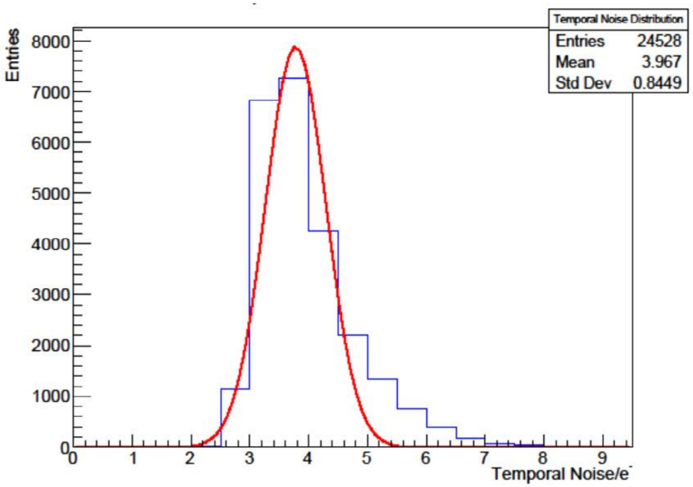
Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm^2
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm^2
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm^2**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm^2

Details in NIMA, 1048 (2023) 167967

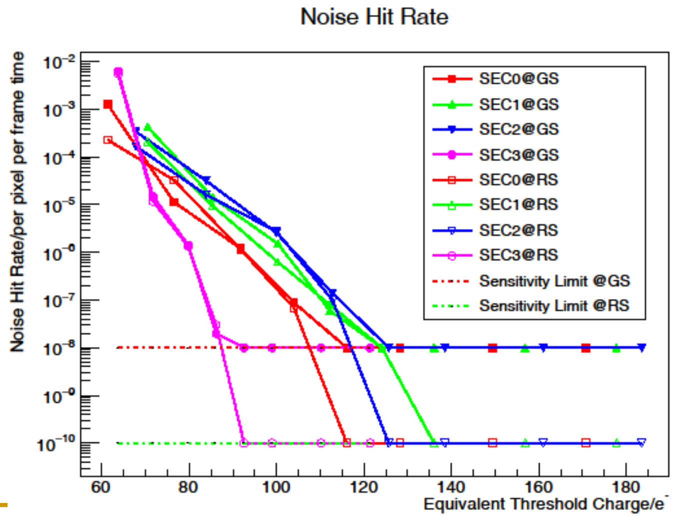
Threshold and noise of JadePix-3

- **Threshold and noise distribution measured with electrical test pulse**
  - Threshold: 228 ± 7.6 e$^-$, temporal noise 4.0 e$^-$ for sector2 of matrix



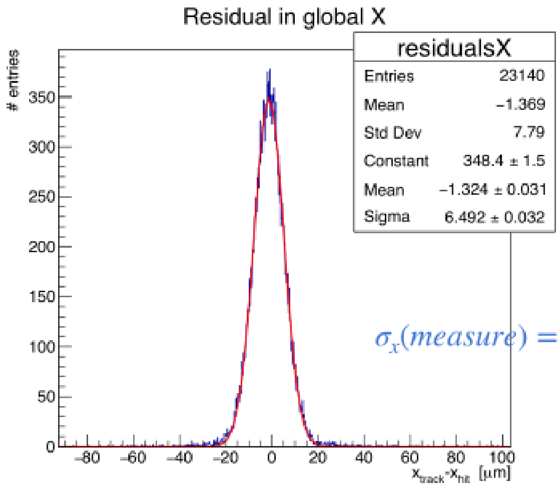


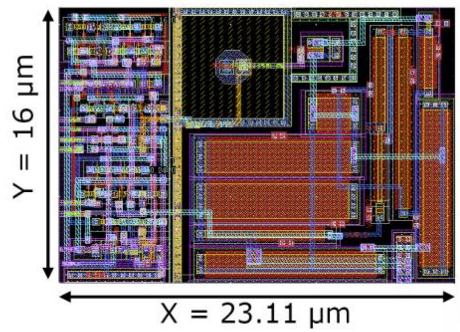
- **Noise hit rate below 10^{-10}/frame/pixel**
  - Sensitivity limit due to the statistics (1k/100k frames sampled for GS/RS)
  - The minimum thresholds are between 90 and 140 e$^-$

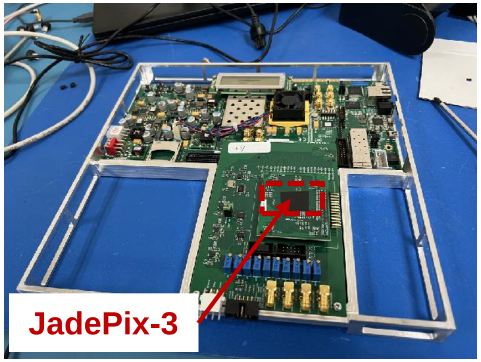


JadePix-3 Telescope

- **Beam test performed in DESY TB21**
  - 4 detector planes assembled, one as DUT
  - Beam energy ~4GeV



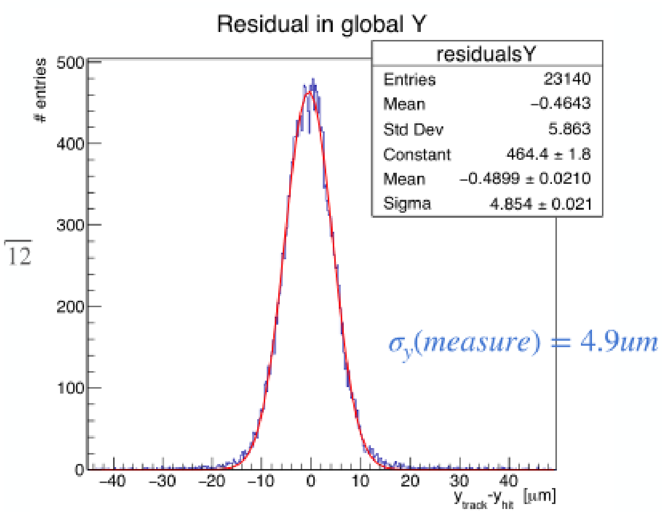


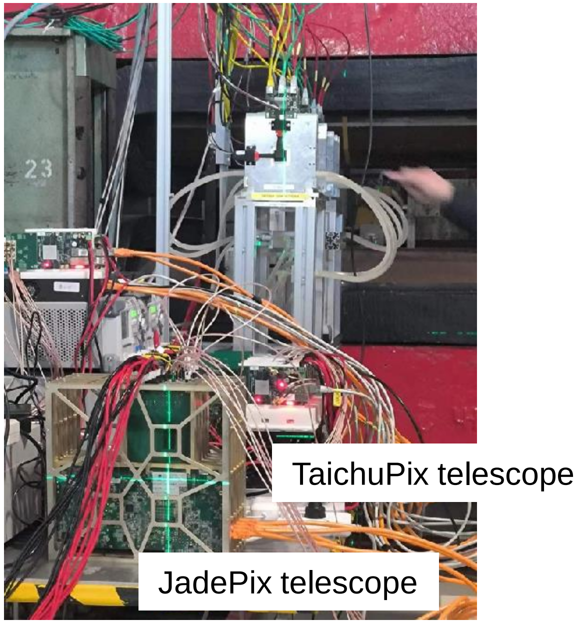


Single plane structure

$$\sigma_{meas}^2 = \sigma_{DUT}^2 + \sigma_{tel}^2$$

$$\boldsymbol{\sigma_x(DUT) = 5.4\ \mu m}$$
$$\boldsymbol{\sigma_y(DUT) = 4.1\ \mu m}$$

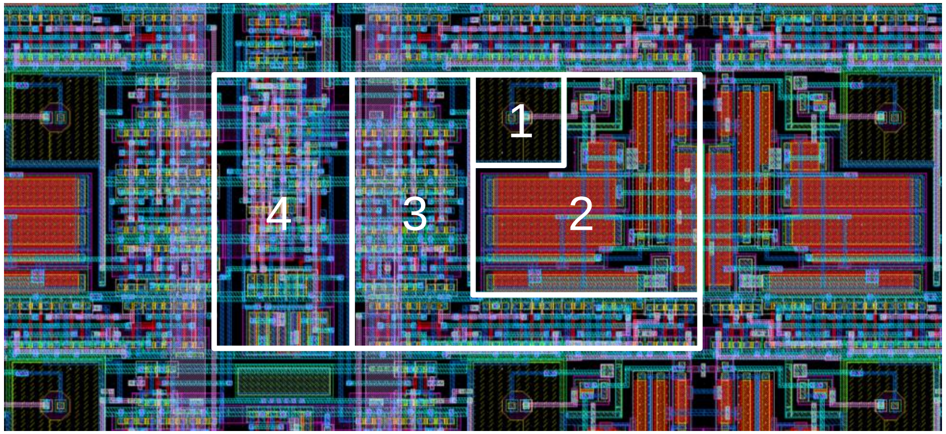




Test setup @DESY Dec 2022

Pixel of JadePix-4 prototype

- **Key component verified and reused from JadePix-3**
  - Diode
  - Analog front-end
  - Hit register
- **Asynchronized Encoder and Reset Decoder (AERD) ***
  - Generating col. and row address from hit pixel
  - Tracing back to reset hit pixel
- **Final layout of pixel matrix**
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm



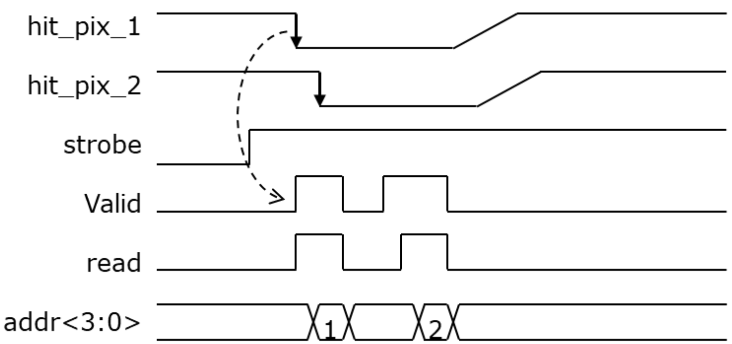
JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode 2. Analog front-end
3. Digital logic; 4. AERD shared by 2 col.

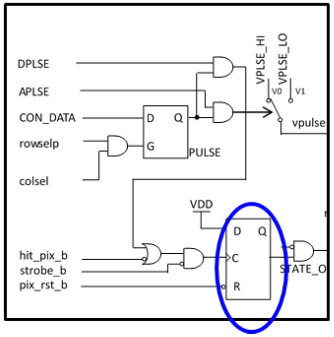
- **Submitted to a shared engineering run in Oct. 2021**
  - Chips received in July 2022, test on-going

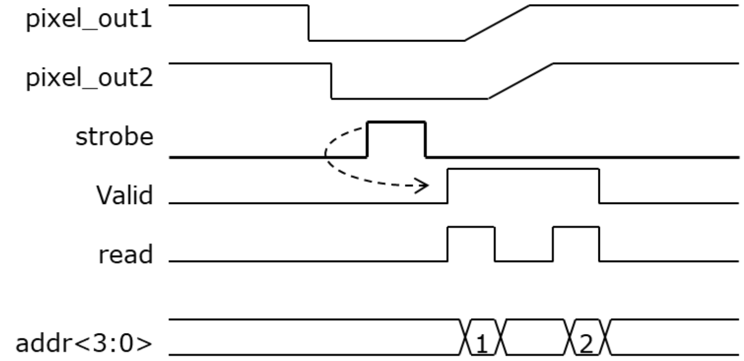
*P.Yang, et al., NIMA 785(2015) 61-69

Readout of JadePix-4

- **Triggerless mode**
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- **Trigger mode**
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger (analog buffer)
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit







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- **Progress of the TaichuPix chips**
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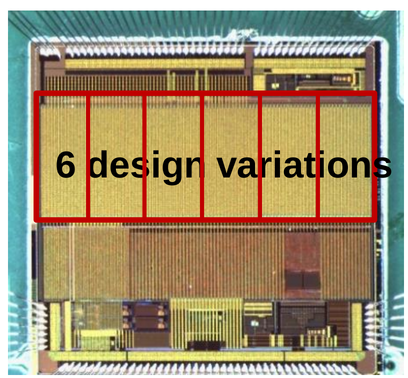
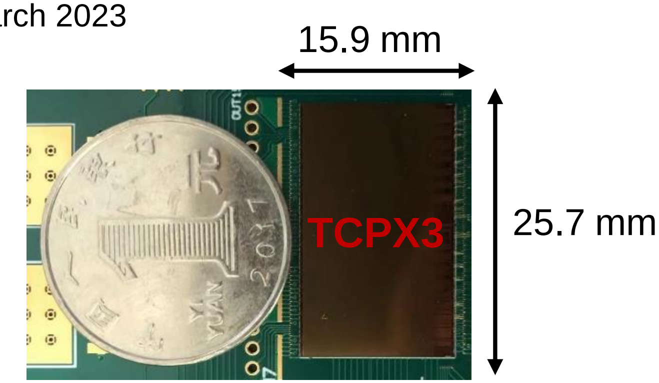
TaichuPix prototypes overview

- **Motivation:** **a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 round of sensor prototyping in 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023

TaichuPix-1

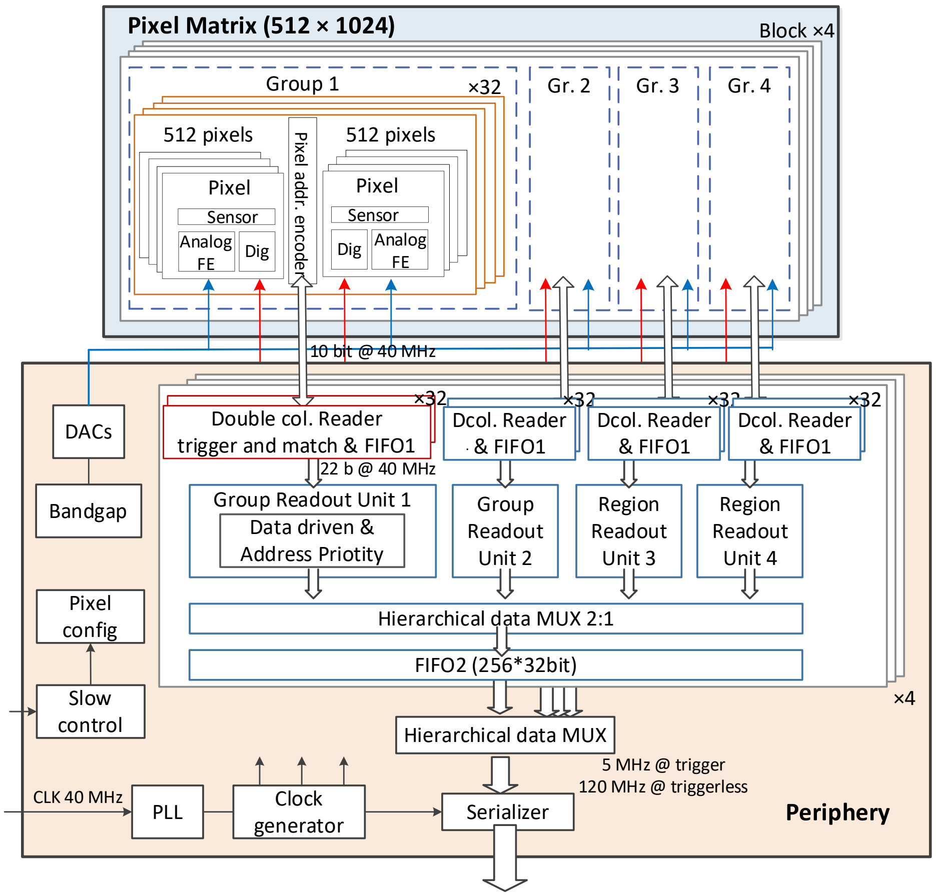


TaichuPix-2



TaichuPix-3
Pixel size：25 μm × 25 μm

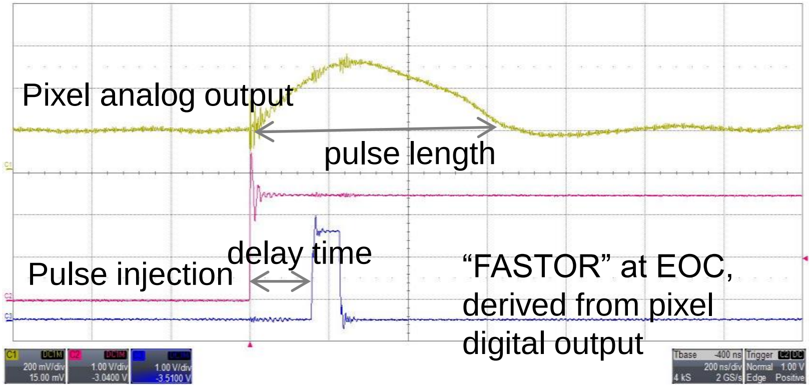
TaichuPix architecture

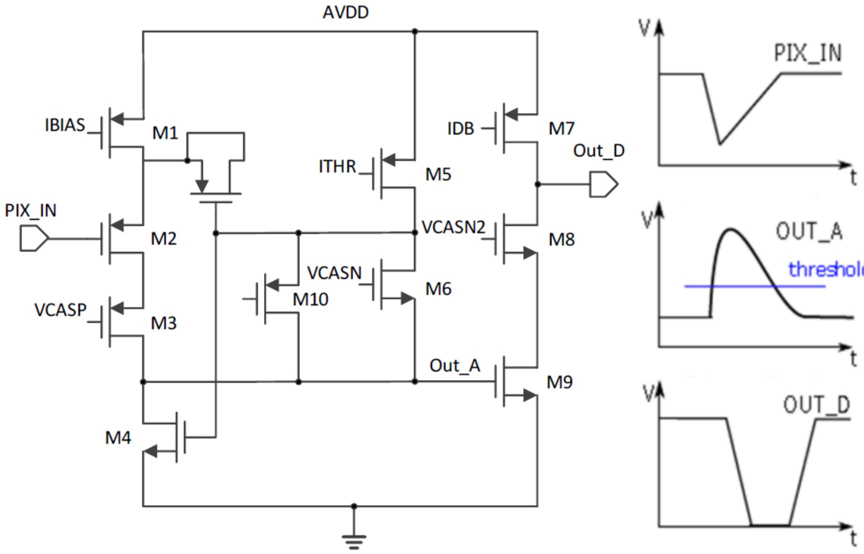


- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at EOC
  - Readout time: 50 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

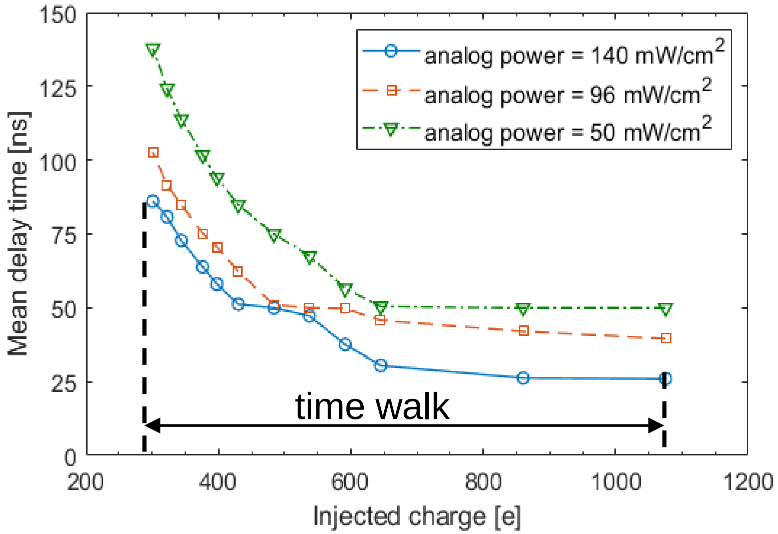
Pixel analog front-end

- **Based on ALPIDE* front-end scheme**
  - modified for faster response
  - ‘FASTOR’ signal delivered to the EOC (end of column) when a pixel fired, timestamps of hit recorded at pos. edge of ‘FASTOR’





Schematic of pixel front-end



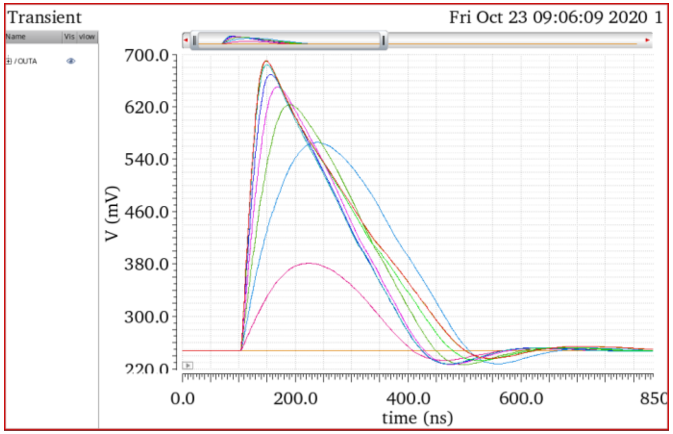
Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

*Ref: D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

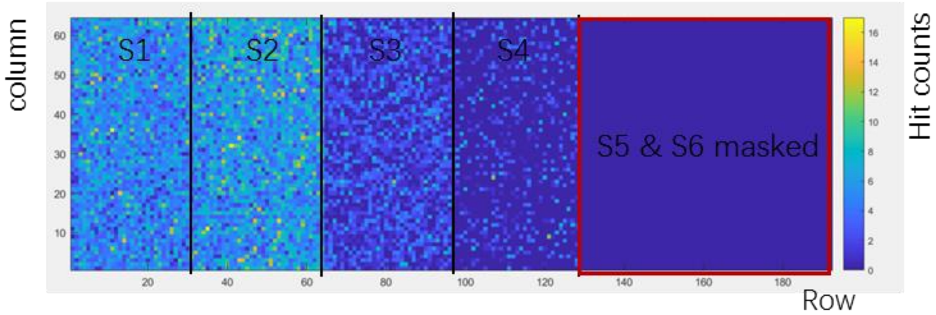
Functionality of complete signal chain of TaichuPix2

- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with an X-ray source and a laser source.**

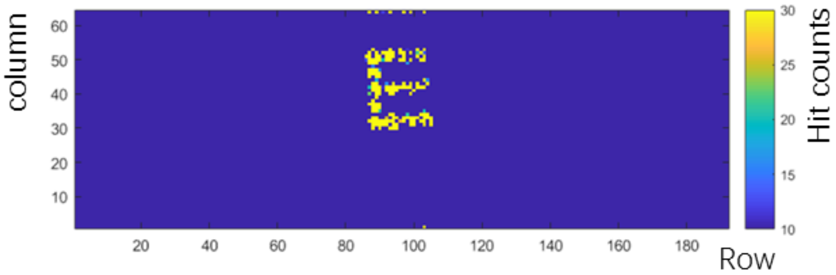
TaichuPix2 response to X-ray tube (cutting energy @ 6keV)



Simulated analog output with different input signal



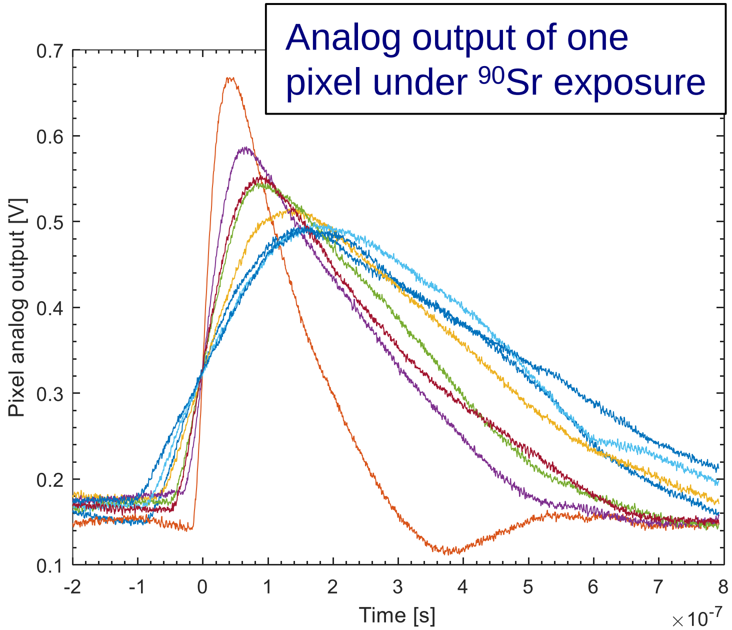
Hit map of the TaichuPix-2 under X-ray from the X-tube voltage of 8 kV for 5 min.

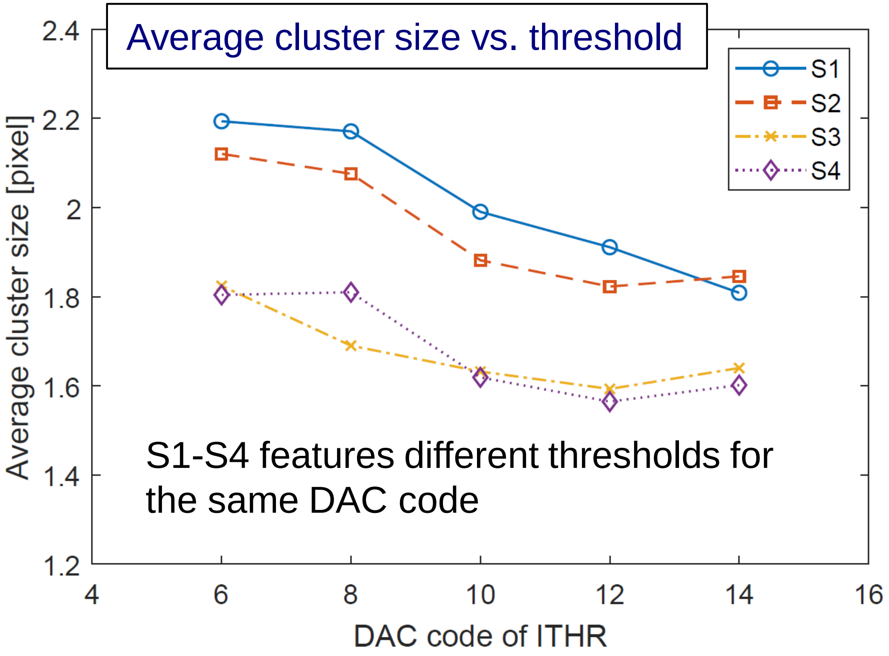


Letter imaging obtained with a 1064 nm laser spot scanning on the TaichuPix-2

TaichuPix2 test with ^{90}Sr

- **TC2 exposure to ^{90}Sr source at different threshold setting (ITHR)**

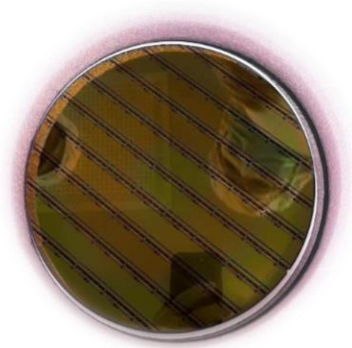




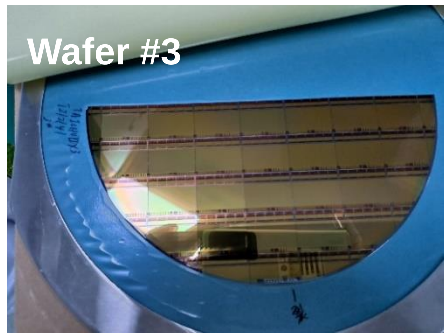
- Shape and amplitude of analog signal as expected, but peaking time and pulse length larger than simulation.
- Average cluster size decreases with threshold as expected
- **Average cluster size for S1-S4 less than 3 as expected**
  - **Indicates the estimated maximum hit rate (36 MHz/cm^2) reasonable**
  - **Cluster size >1, benefits the spatial resolution (better than $pitch/\sqrt{12}$ = 7.2 μm)**

Large-scale sensor TaichuPix-3

- **12 TaichuPix-3 wafers produced from two rounds**
  - **One wafer thinned down to 150 μm and diced**



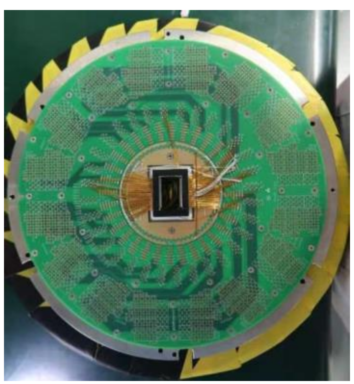
8-inch wafer



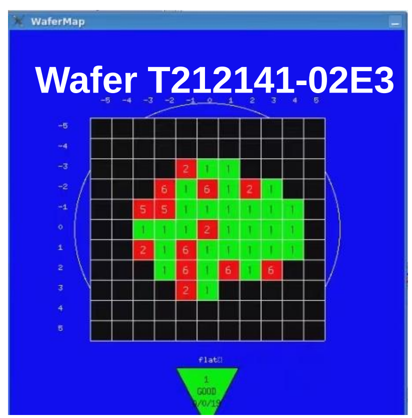
Wafer after thinning and dicing

Thickness after thinning

  - **11 wafers were tested on probe-station before dicing** → chip selecting & yield evaluation



Probe card for wafer test



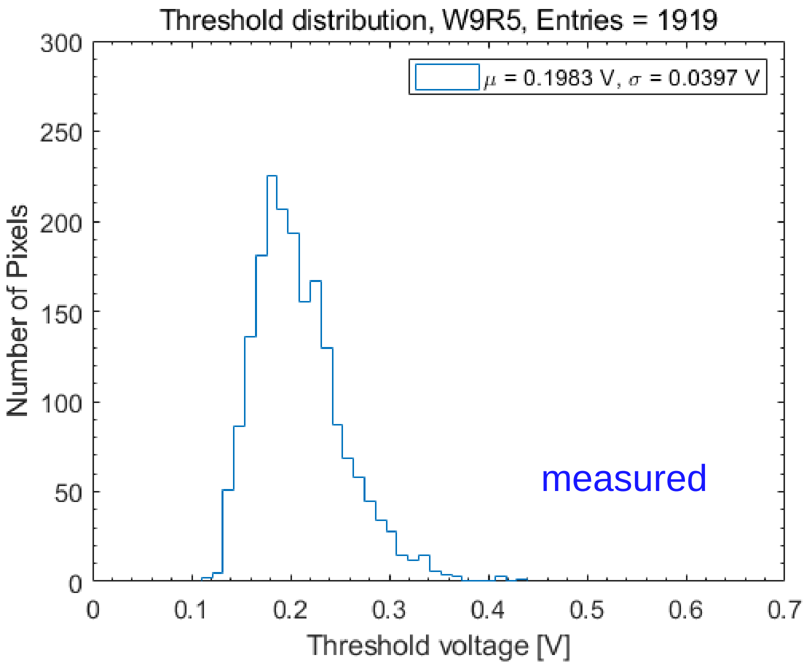
An example of wafer test result

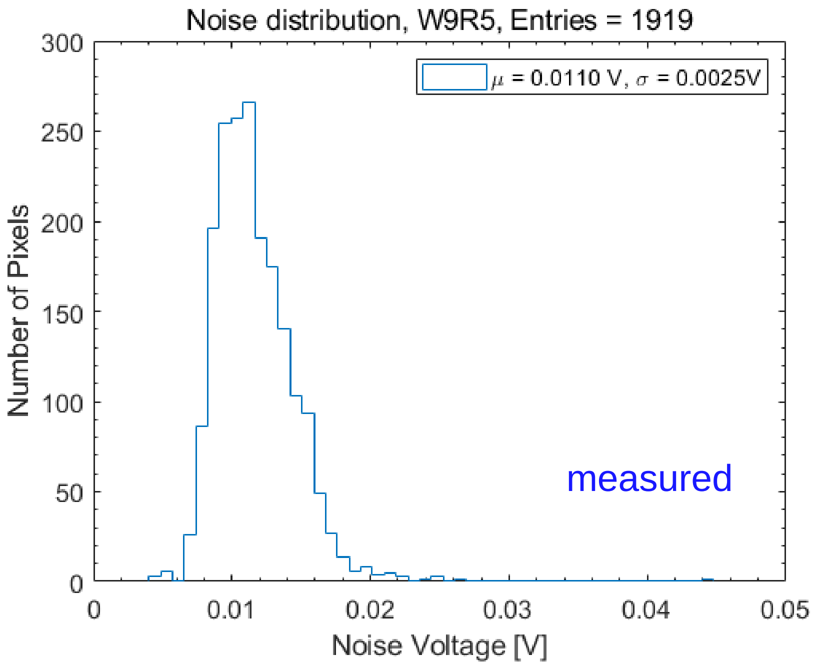
Wafer num.	Yield	Wafer num.	Yield
1	0.65	4	0.475
2	0.725	5	0.625
3	--	6	0.525
7	0.775	10	0.675
8	0.725	11	0.6
9	0.275	12	0.35

1st round 2nd round

Threshold and noise of TaichuPix-3

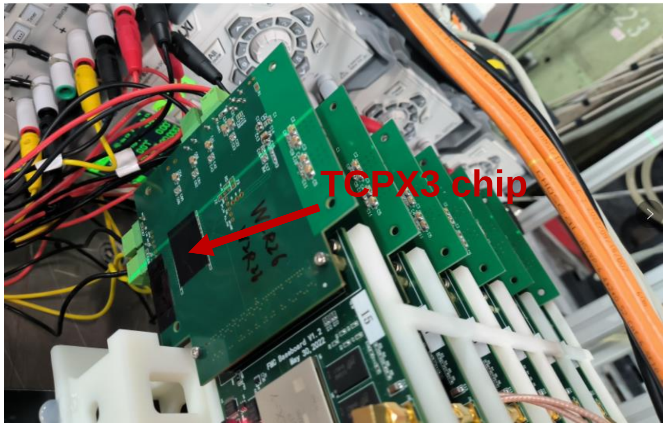
- **Pixel threshold and noise were measured with selected pixels**
  - Average threshold ~215 e^-, threshold dispersion ~43 e^-, temporal noise ~12 e^- @ nominal bias setting





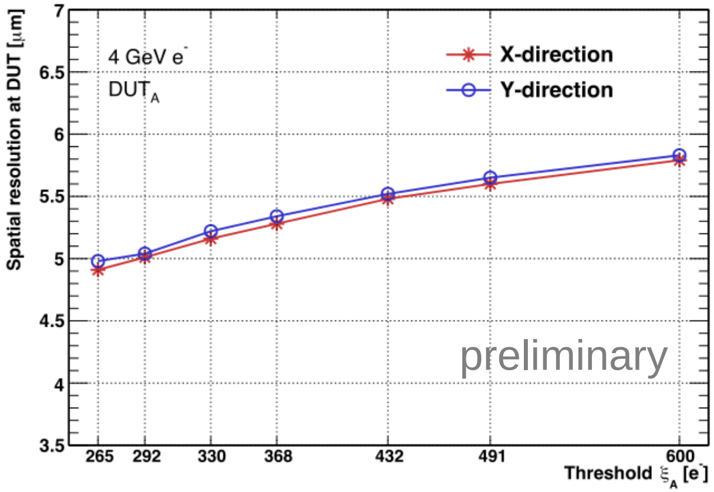
TaichuPix-3 telescope

- **The 6-layer of TaichuPix-3 telescope built**
  - **Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board**

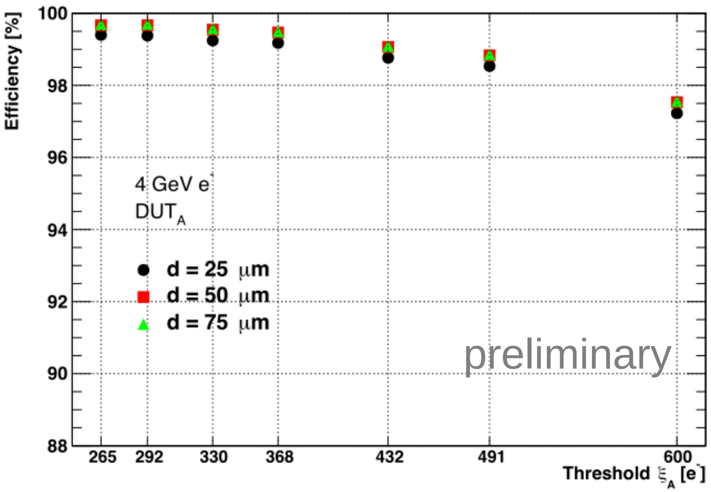


6-layer TaichuPix-3 telescope

- **TaichuPix-3 telescope achieved the expected goal in the DESY testbeam**
  - Basically works well during the beam test time
  - The preliminary offline results indicate the best spat resolution could be < 5 μm



Spatial resolution vs. pixel threshold



Detection efficiency vs. pixel threshold

Summary and outlook

- **Development of JadePix series towards the baseline requirements of CEPC vertex detector**
  - JadePix3: excellent noise performance; spatial resolution close to the requirement in one direction
  - Jadepix4：a complementary design to the JadePix-3, to complete the R&D for the double-sided concept

- **The full-scale and high granularity pixel sensor prototype, TaichuPix-3, has been designed and tested**
  - Spatial resolution ~5 μm measured with 4 GeV electron beam in DESY
  - Full vertex detector prototype assembly in process

- In future, more advanced technology node (65/55nm CMOS) or new process techniques (3D-integrated devices or stitching) may significantly improve the performances of the design

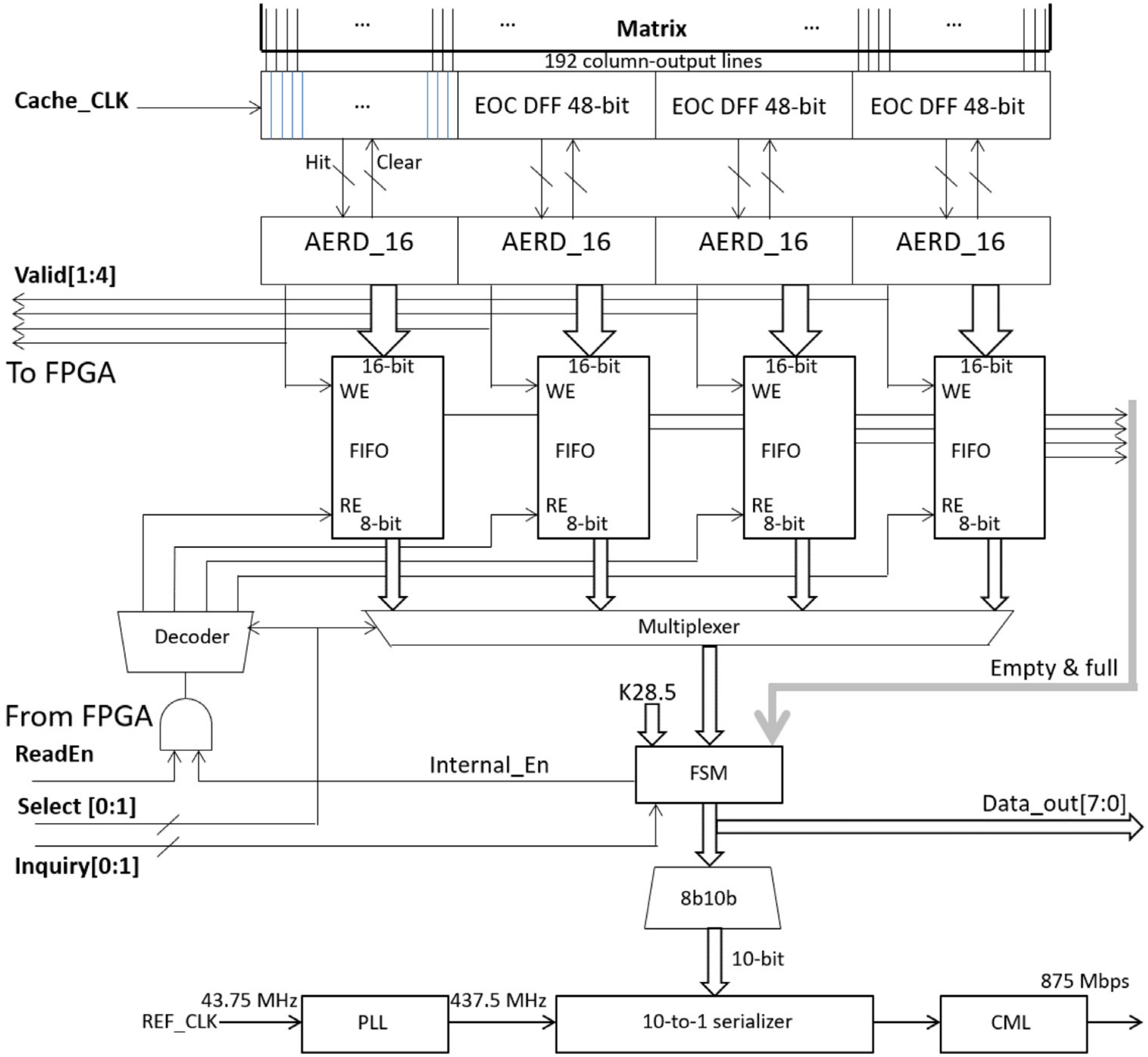
Pixel sensor teams

- **JadePix-3/4**
  - IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing Dong, Wenhao Dong/ USTC, Chunhao Tian/ USTC, Sheng Dong, Yunpeng Lu, Qun Ouyang
  - CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Hulin Wang, Xiangming Sun
  - SDU: Liang Zhang, Meng Wang
  - Dalian Minzu Unv: Zhan Shi
  - USTC: Zhiliang Chen, Lailin Xu
- **TaichuPix**
  - IHEP: Wei Wei, Ying Zhang, Xiaoting Li, Jun Hu, Hongyu Zhang, Zhijun Liang, Joao Guimaraes da Costa
  - CCNU/IFAE: Tianya Wu, Raimon Casanova, Sebastian Grinstein
  - NWPU: Xiaomin Wei, Jia Wang
  - SDU: Liang Zhang, Jianing Dong, Long Li
  - NJU: Xiaoxu Zhang, Yiming HU, Lei Zhang, Ming Qi

Thank you very much for your attention!

Backup

Periphery readout of JadePix-3

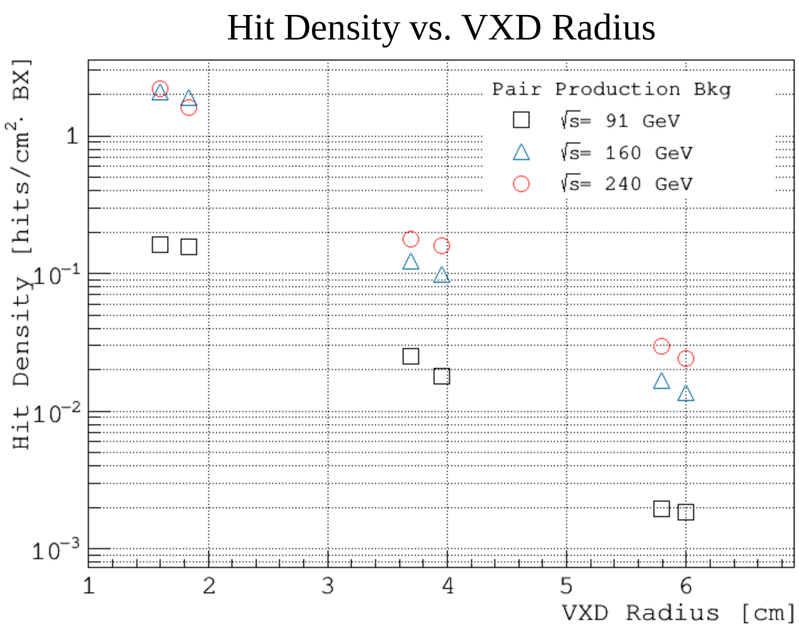


AERD* (Address Encoder and Reset Decoder)

*P.Yang, et al., NIMA 785(2015) 61-69

TaichuPix specification

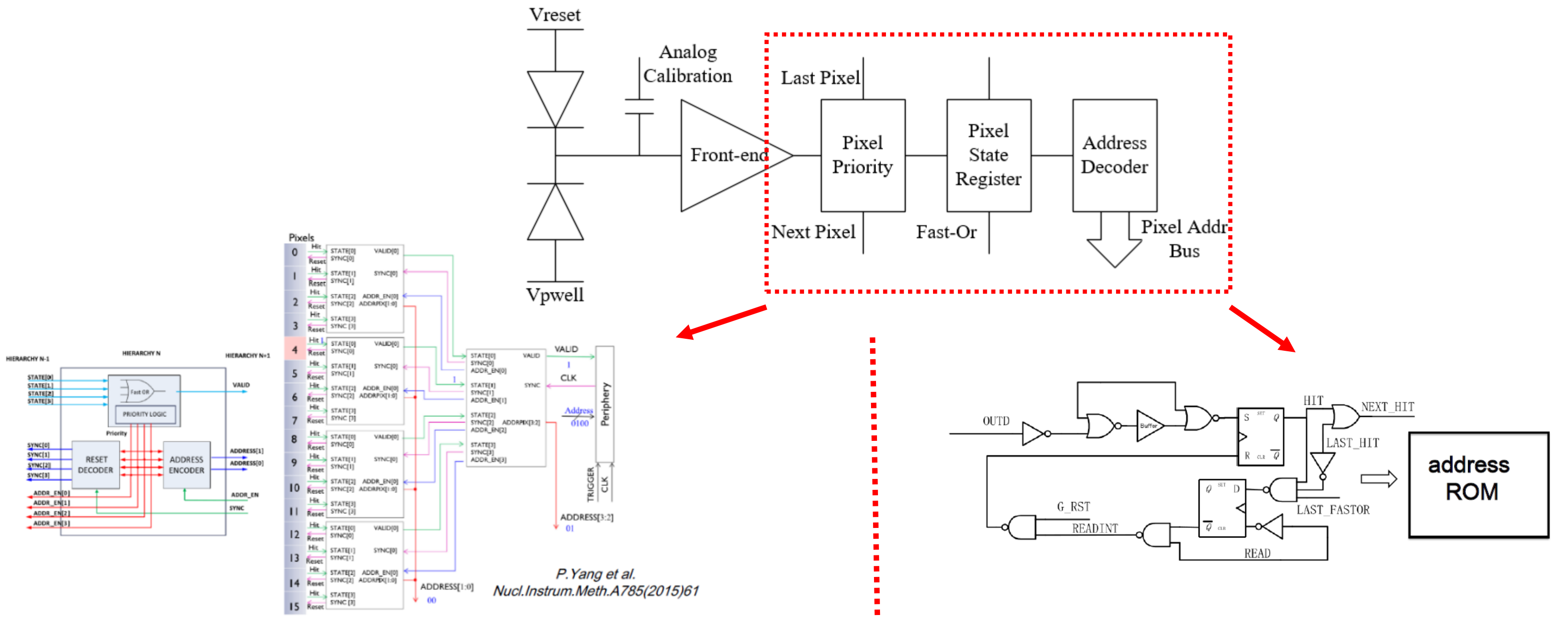
- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness: ~18 μm
  - Pixel size: 25 μm × 25 μm



Ref: CEPC Conceptual Design Report, Volume II

For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Data rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns (for 98% efficiency)	Chip size	~1.4 cm × 2.56 cm

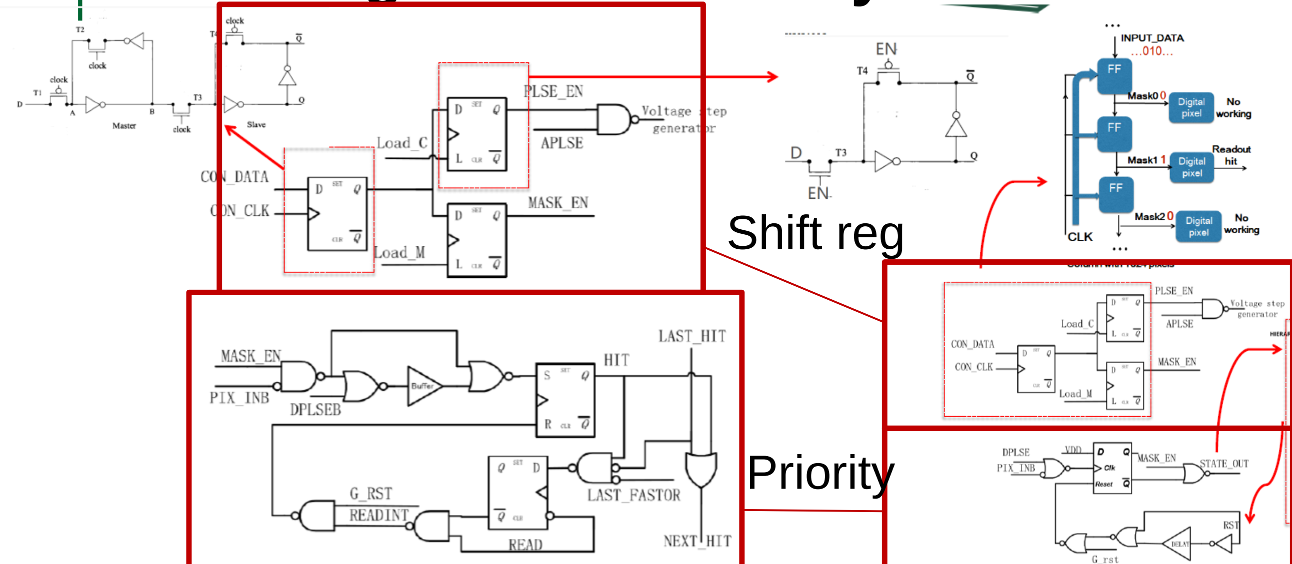
Pixel architecture – parallel digital schemes



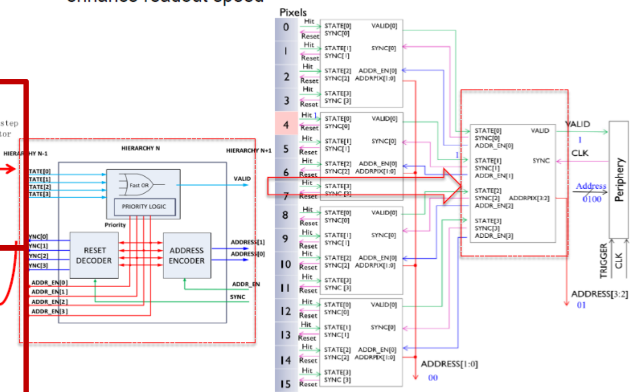
- **Simplified column-drain readout:**
  - Each double column shares a common Fast-Or bus for hit indication
  - Common time stamp register @40MHz will record the hit arrival time
  - Hit pixels in the same cluster will share a common time stamp as the Trigger ID
- **Two parallel digital readout architectures were designed:**
  - Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size
    - Readout speed was enhanced for 40MHz BX
  - Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)
    - Fully customized layout of digital cells and address decoder for smaller area

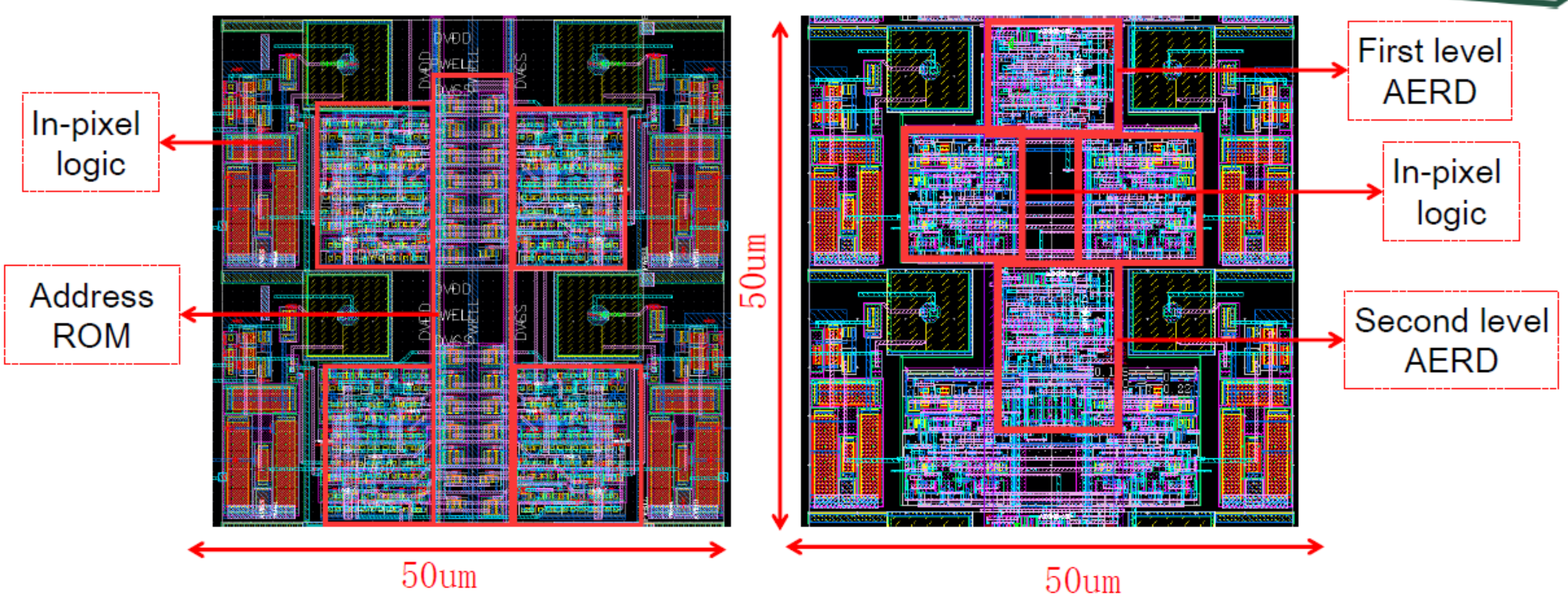
Pixel Digital Circuit- fully customized logic

- 1 bit shifting register chain is used to mask pixel and calibration
- The storage registers and “strobe” is replaced by an edge -triggered flip-flop
- The boosting speed AERD is implemented to enhance readout speed



It will cost around 106 transistors, including
the Analog calibration block

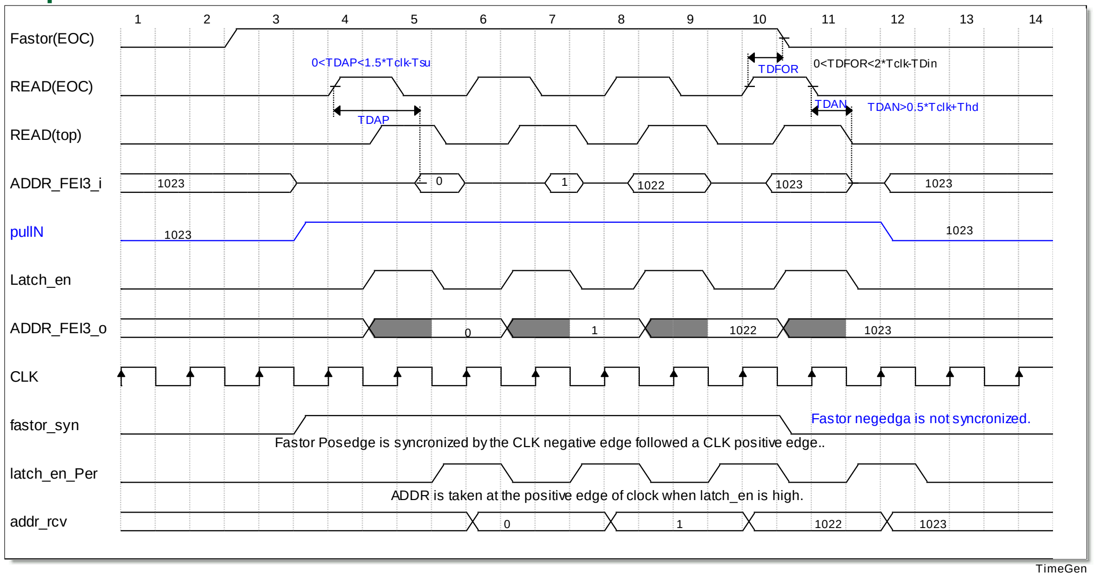




Layout of FE-I3-like scheme

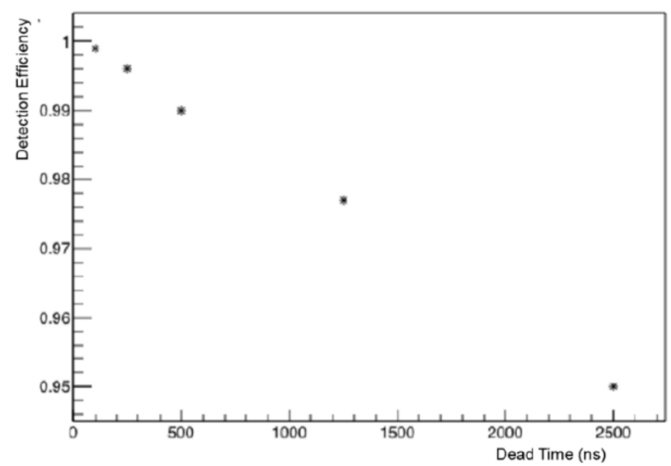
Layout of ALPIDE-like scheme

Readout & Periphery



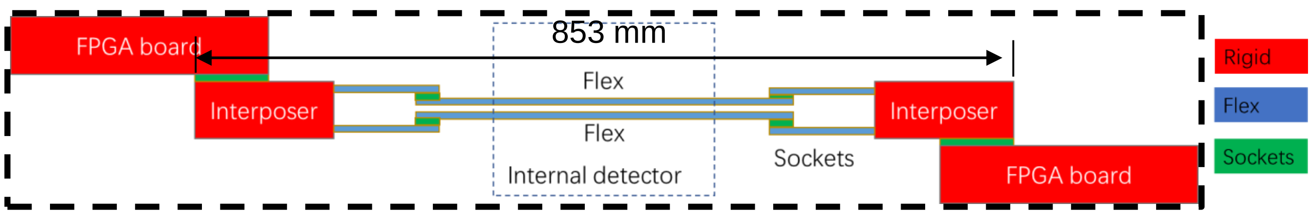
- **Time stamp recorded when Fastor is valid**
- **Each pixel readout by 2 clocks (50ns)**
  - Worst delay ~ 25ns
    - Sim by 512 rows (full size)
    - TDA: read sent –addr come
  - Address latch @ 37.5ns
    - @1.5 clock
    - Enough headroom for all corners

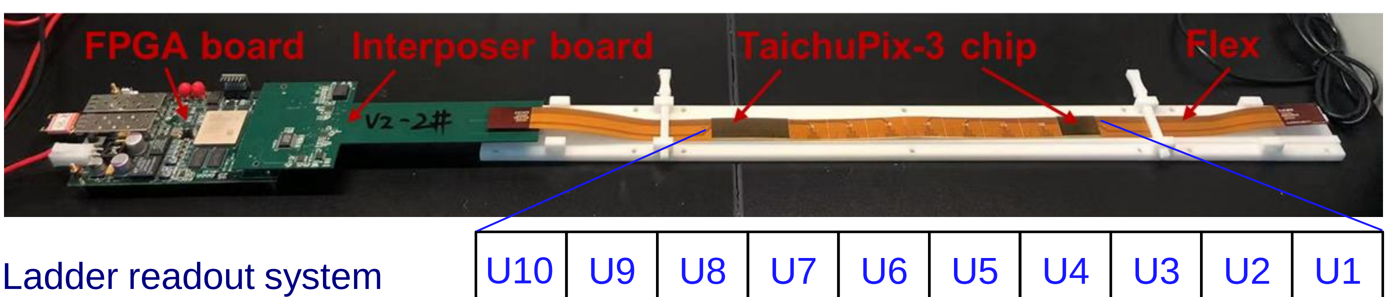
- **Designed for low power**
  - Only the hit (fastor) info & address are fannout from the pixel array
  - Only the read (acquisition) signal is fanned in to the pixel array
    - Clock & time stamp are localized only in the EOC, different from FE-I3
- **Optimized @ CEPC hit rate**
  - Common time stamp recorded for a full double column
    - For low power
    - Column is hit every 8.3us / pixel is readout in 2 clocks (50ns) / cluster size 3 pixels
    - Dead time 500ns – 98% trigger efficiency



Ladder readout

- **Completed detector module (ladder) design**
  - Detector module (ladder) = 10 sensors + readout board + support structure + control board
  - Sensors are glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
  - No debug testing point → hard to debug the flex readout system





Ladder readout system

Detector prototype

- **6 double-sided layers assembled on the detector prototype**
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector