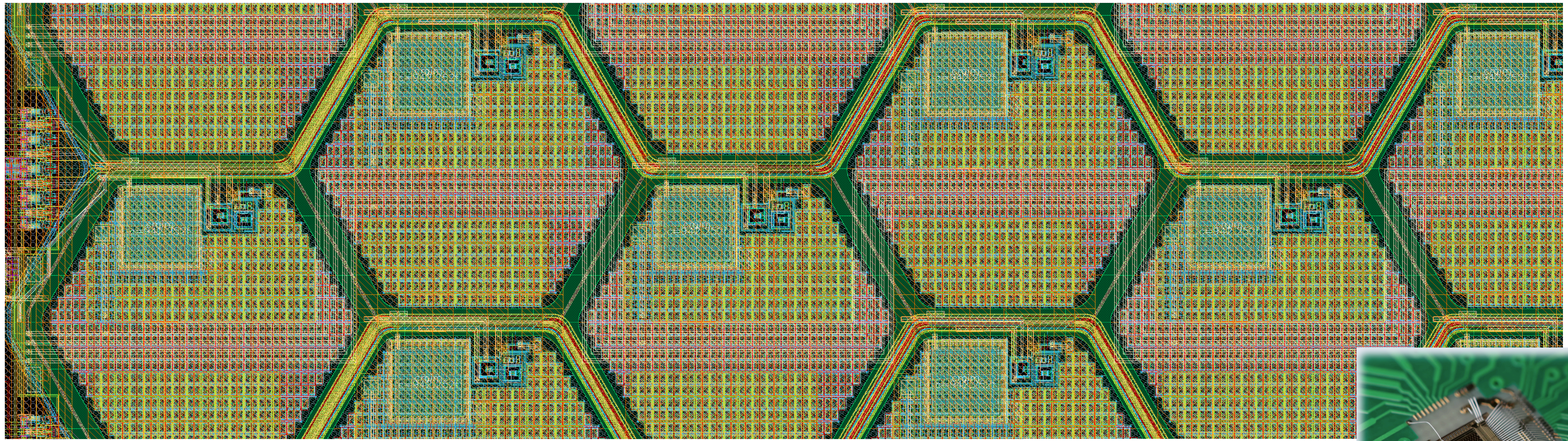
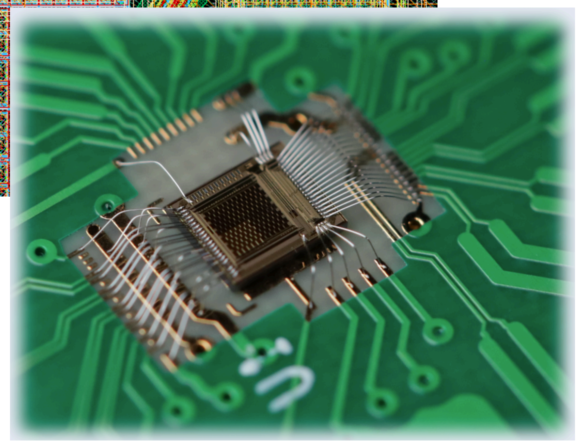
MONOLITH project and results

towards picosecond timing with monolithic silicon

Thanushan Kugathasan — Université de Genève





UNIVERSITÉ DE GENÈVE

Swiss National Science Foundation

European Research Council
Established by the European Commission

The MONOLITH ERC Project

Funded by the H2020 ERC Advanced grant 884447[1]
July 2020 - June 2025

Monolithic silicon sensor for picosecond-level timing

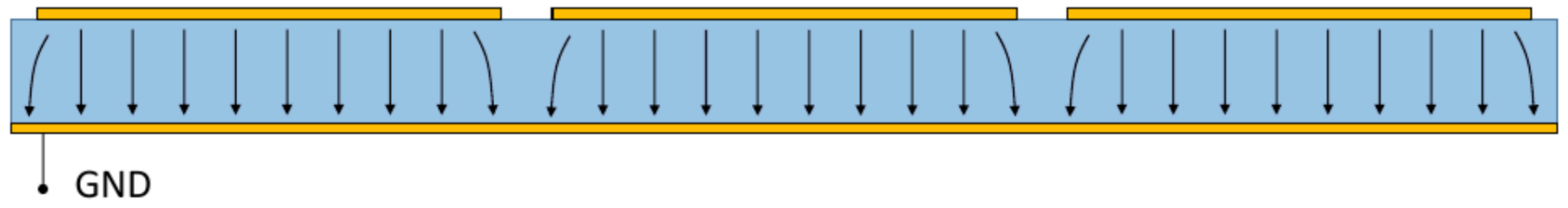
- Good spatial resolution, Low power, Radiation tolerance
- Target: HEP, Nuclear Physics, Space Borne, high tech applications requiring ps level ToF

[1] MONOLITH H2020 ERC Advanced Project Web Page - https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/monolith-erc-advanced-project/

Precise timing with silicon

1. Sensor geometry and fields

Sensor optimization for time measurement means:
Sensor time response **independent** from the particle trajectory



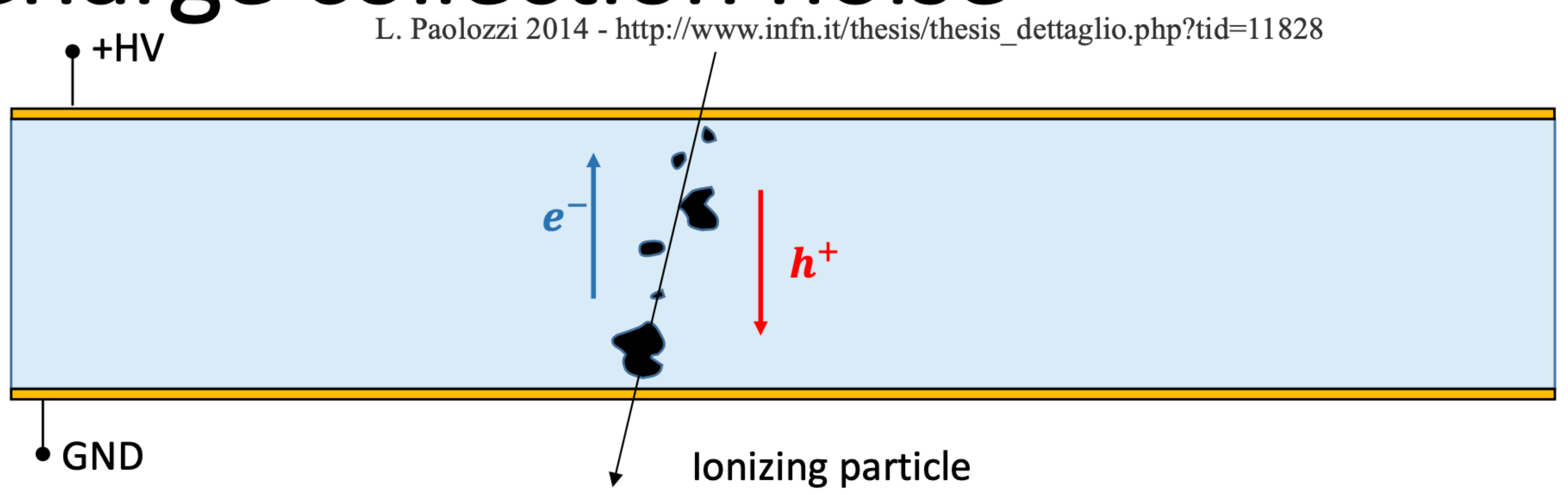
→ "Parallel plate" read out: wide pixels w.r.t. depletion region

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

Scalar, saturated (v_{drift}) — Scalar, uniform ($\frac{1}{D}$)

Desired features:
- Uniform **weighting field** (signal induction)
- Uniform **electric field** (charge transport)
- Saturated charge **drift velocity** (signal speed)

2. Charge collection noise



is produced by the **non uniformity of the charge deposition** in the sensor:

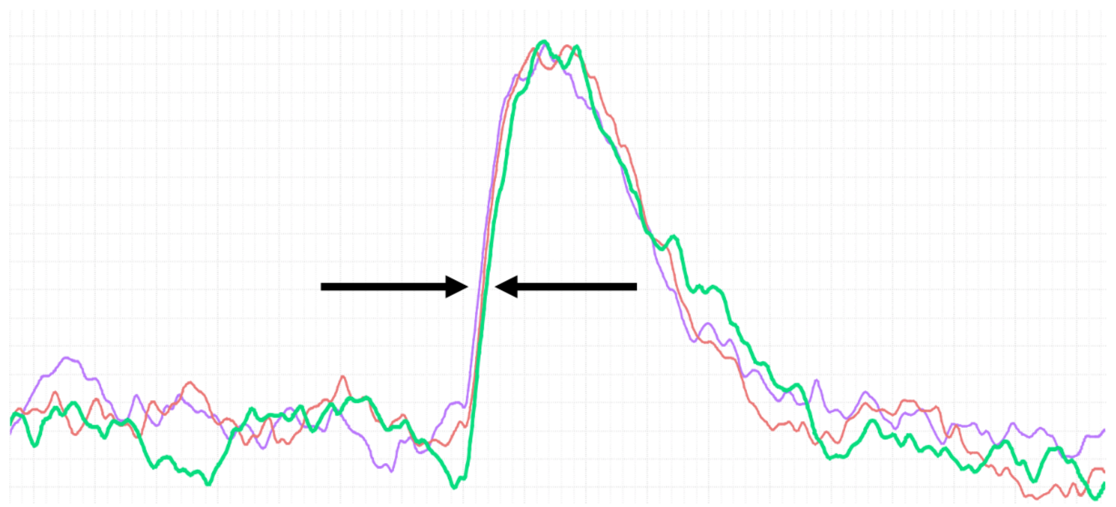
$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the **amplifier performance**.

Time jitter



Fast integration

$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{t_{rise}}{Signal/Noise} \cong \frac{ENC}{I_{Ind}}$$

4. Gain

- A gain layer allows larger signals, and thus, better time resolution

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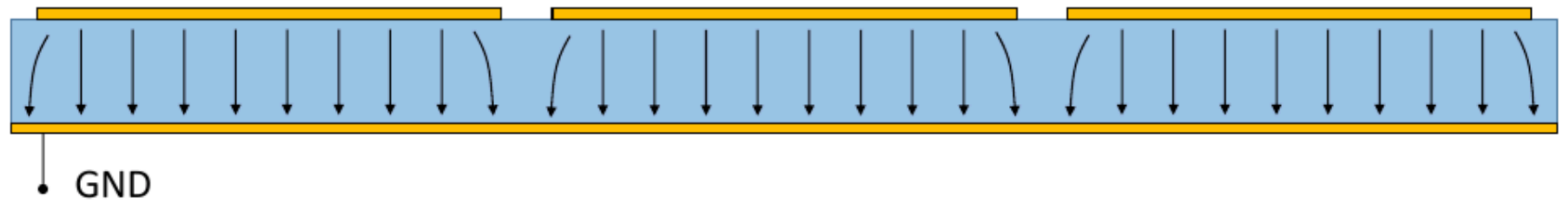

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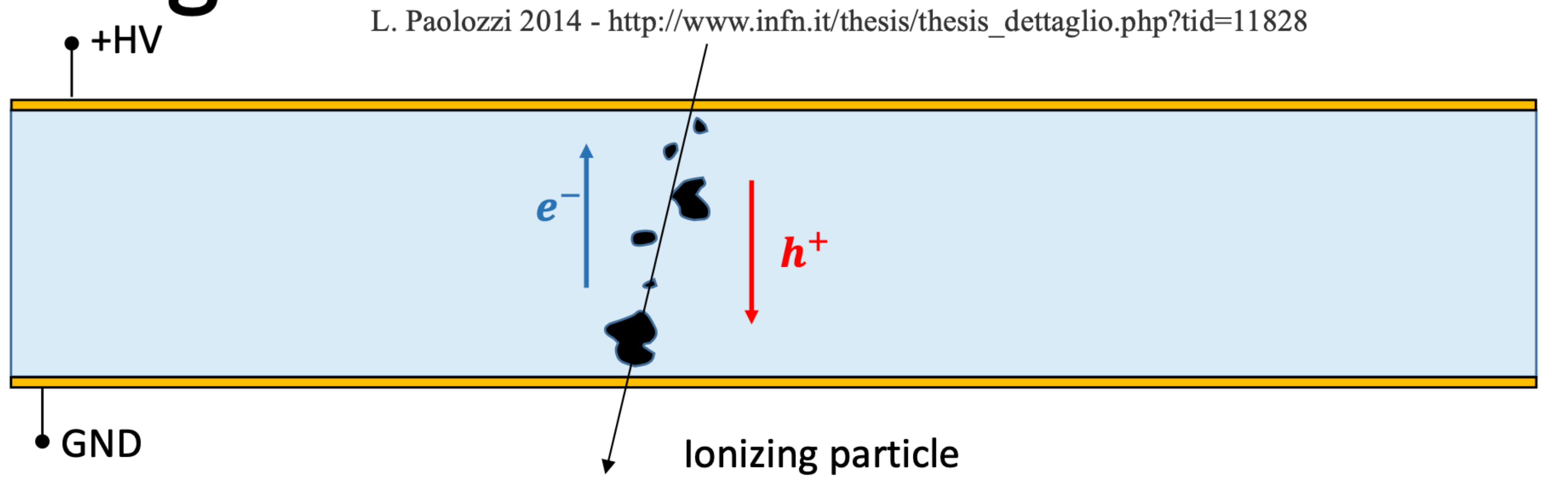

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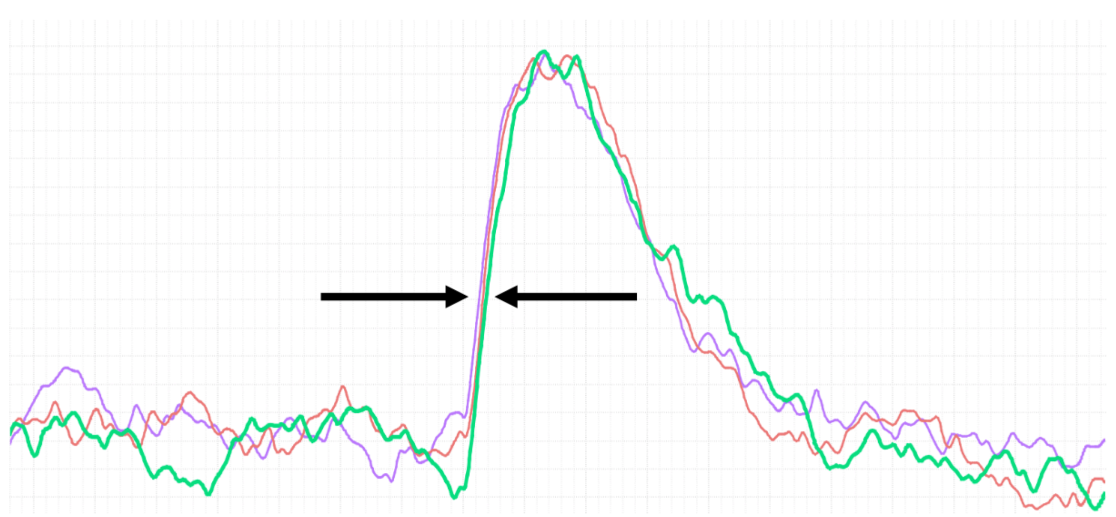

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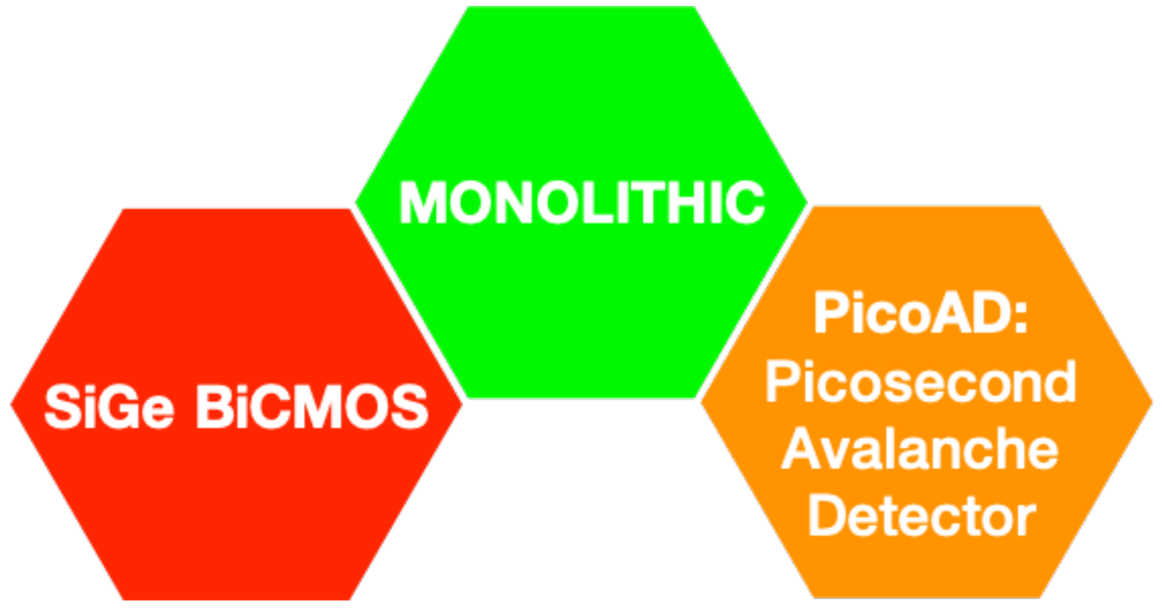


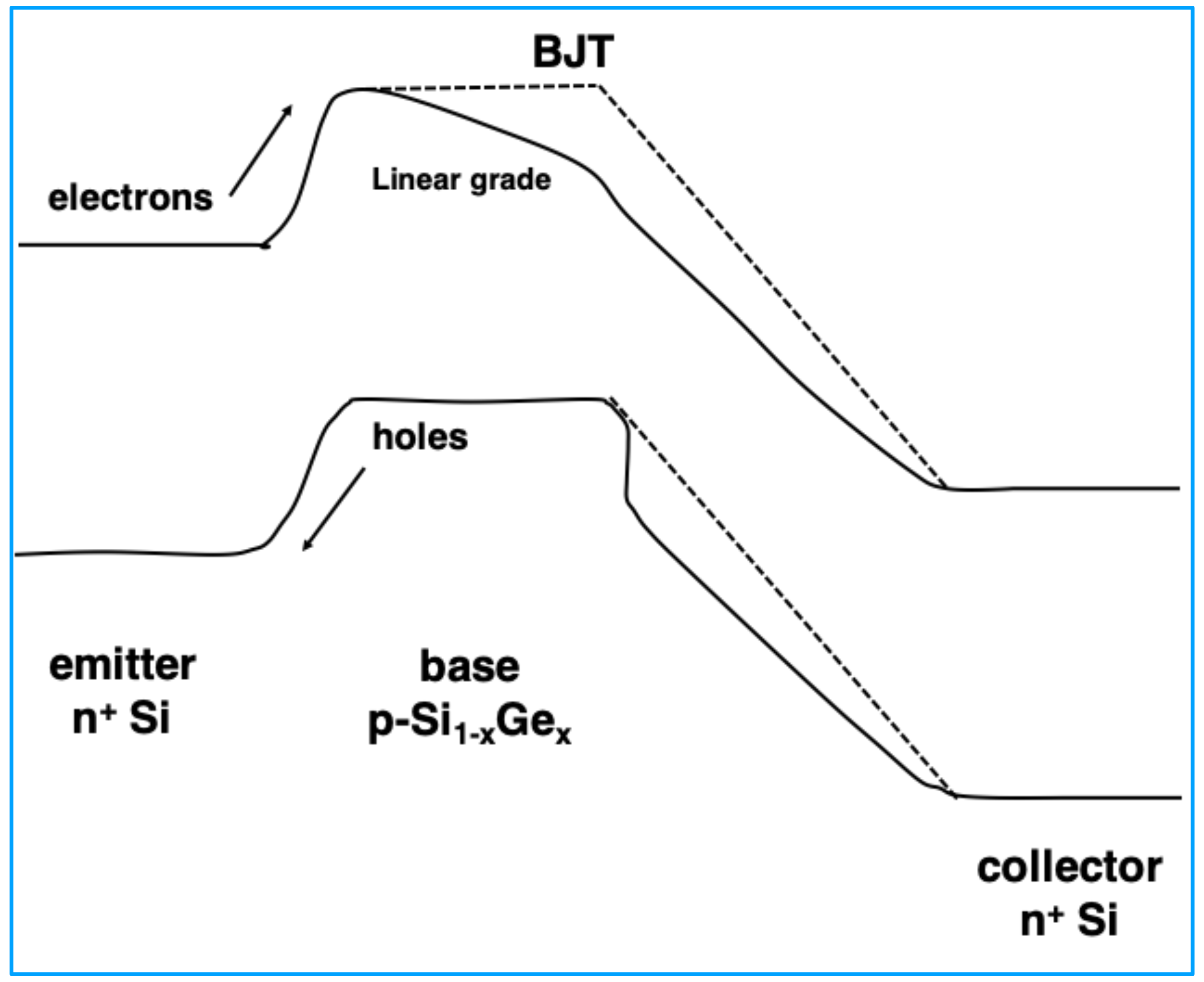
SiGe Heterojunction Bipolar Transistor (HBT)

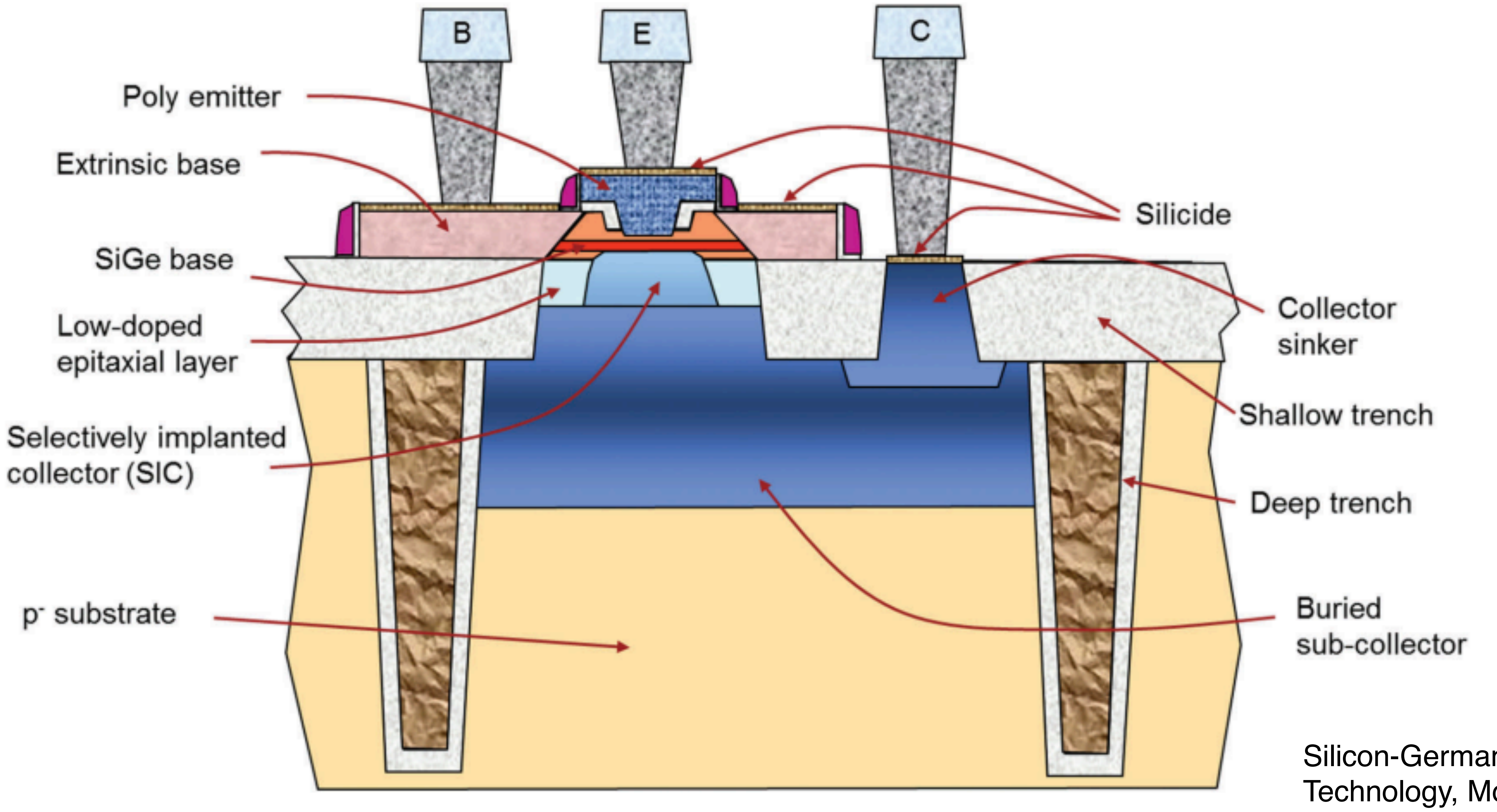
SiGe grading of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:

$\Longrightarrow$ short e⁻ transit time in Base $\Longrightarrow$ very high β

$\Longrightarrow$ smaller size $\Longrightarrow$ reduction of R_b and very high f_t (>100 GHz)

$$ENC_{\text{series noise}} \propto \sqrt{k_1 \cdot \frac{C_{tot}^2}{\beta} + k_2 \cdot R_b C_{tot}^2}$$



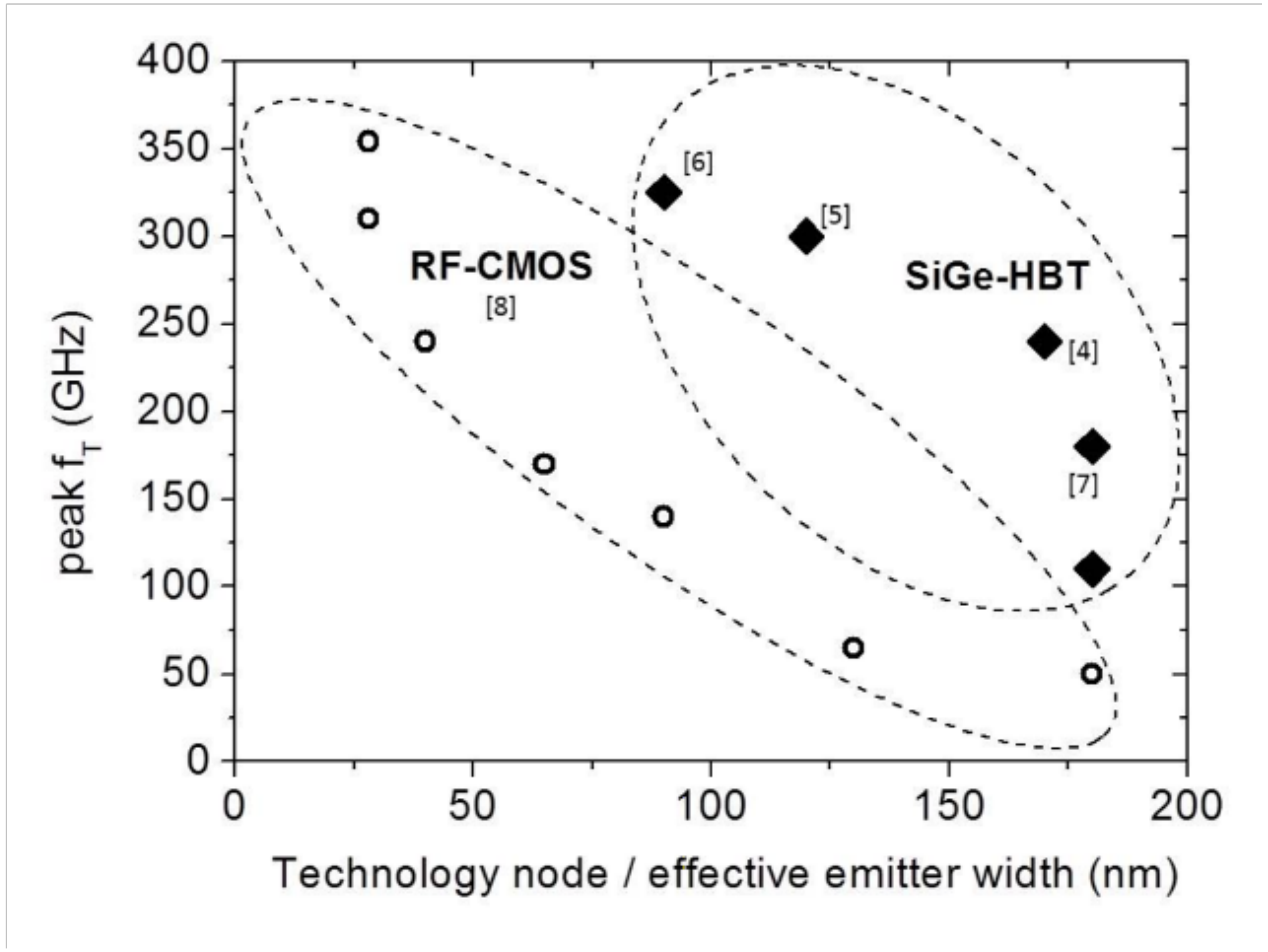


Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications. H. Rucker and B. Heinemann, Chapter 1

Cross section of a High speed SiGe HBT.
Vertical transport device less dependent on lithography than CMOS

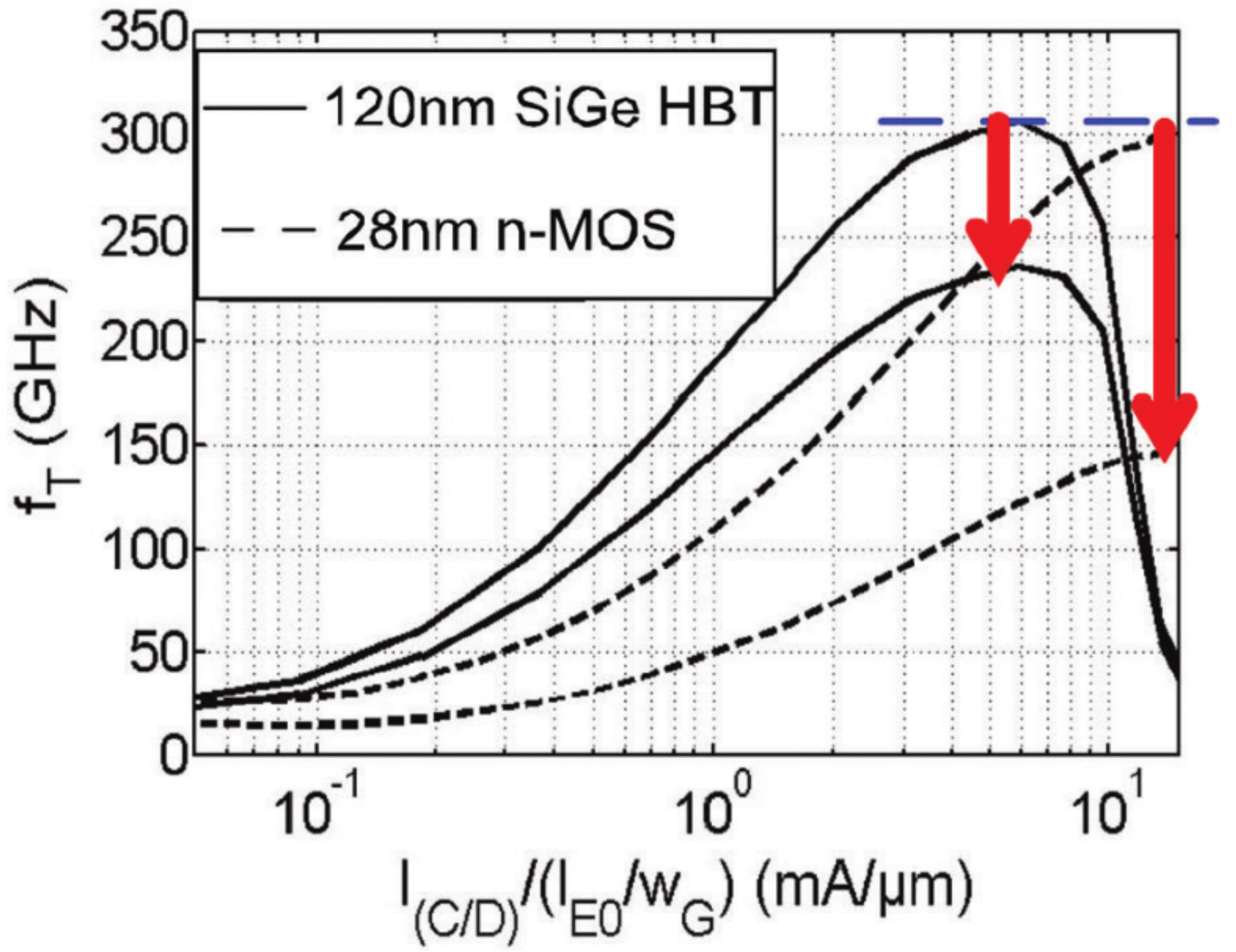
SiGe HBT vs. CMOS

Peak transition frequency vs. technology node



A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

Peak transition frequency vs. current density



Robustness to parasitic

M. Schröter, U. Pfeiffer and R. Jain, Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications.

SiGe Bi-CMOS

SiGe-HBT implemented as add-on in a CMOS technology (increase of cost of ~ 10%)

State of the art HBT by IHP research institute

IHP SG13G2 130 nm process featuring **SiGe HBT** with
- Transistor transition frequency: **f_T/f_{max} = 350/450 GHz**
- Current gain: **β = 900**
- Delay gate: **1.8 ps**

innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

Fast growing technology:

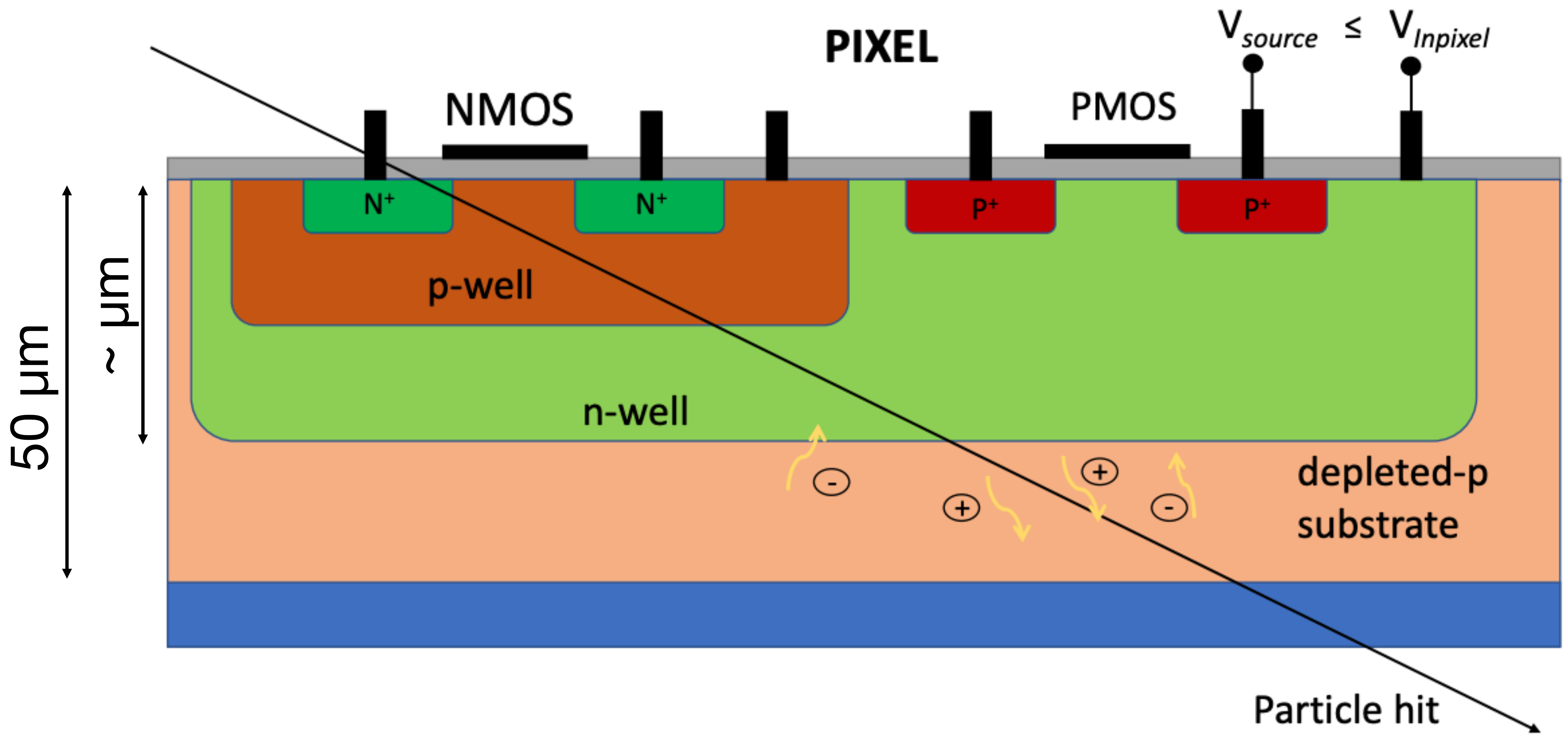
1. new IHP process SG13G3Cu, **now available through EUROPRACTICE,** includes transistor with **f_T/f_{max} = 500/700 GHz**

Several large-volume foundries offer SiGe processes: TJ, TSMC, ST, AMS, GF

SiGe BiCMOS Markets Served

source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

Collection electrode cross-section



Parasitic capacitance dominated by p-well – n-well junction

Large n-well collection electrode (parallel plates) for uniform electric field

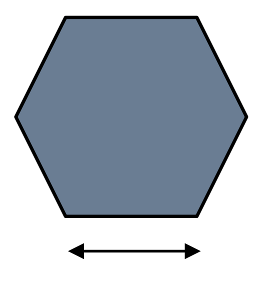
Electronics inside the n-well electrode:

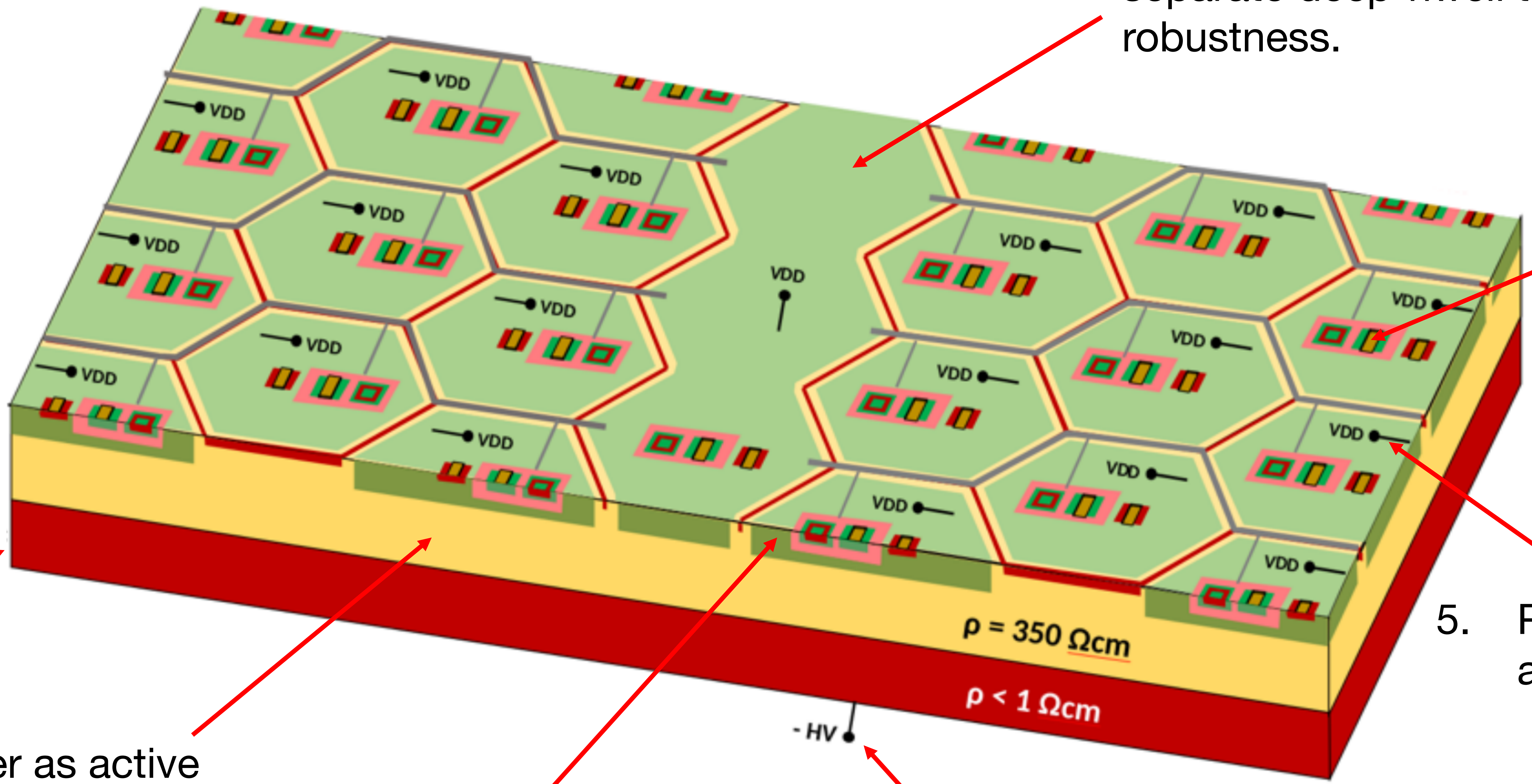
- NMOS in isolated p-well
- PMOS in the collection n-well .
    - Bias condition:
      $V_{pixel} \approx V_{inpixel} \geq V_{ccA}$

- PMOS in isolated n-well: developed by the foundry, soon available.

Pixel matrix cross-section

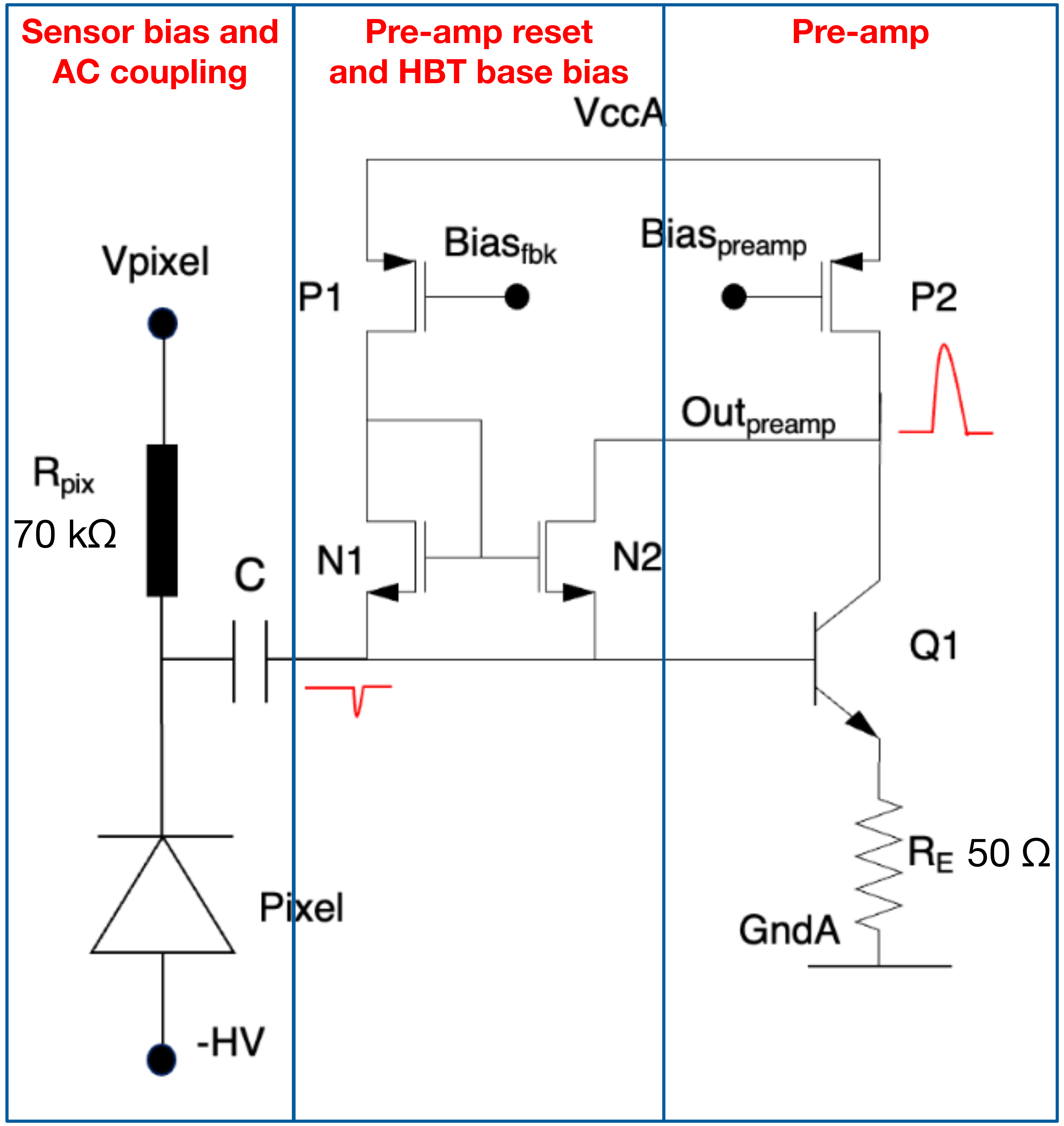
100 µm pitch
Hexagonal grid





1. heavily P-doped substrate.
2. High resistivity epitaxial layer as active volume.
3. Electronics inside the guard-ring, isolated from substrate using deep n-well.
4. Negative High Voltage applied to the substrate.
5. Pixel and electronic deep n-wells are kept at positive low voltage.
6. Analogue electronics in pixel.
7. Digital electronics can be placed in pixel or in a separate deep-nwell to improve noise robustness.

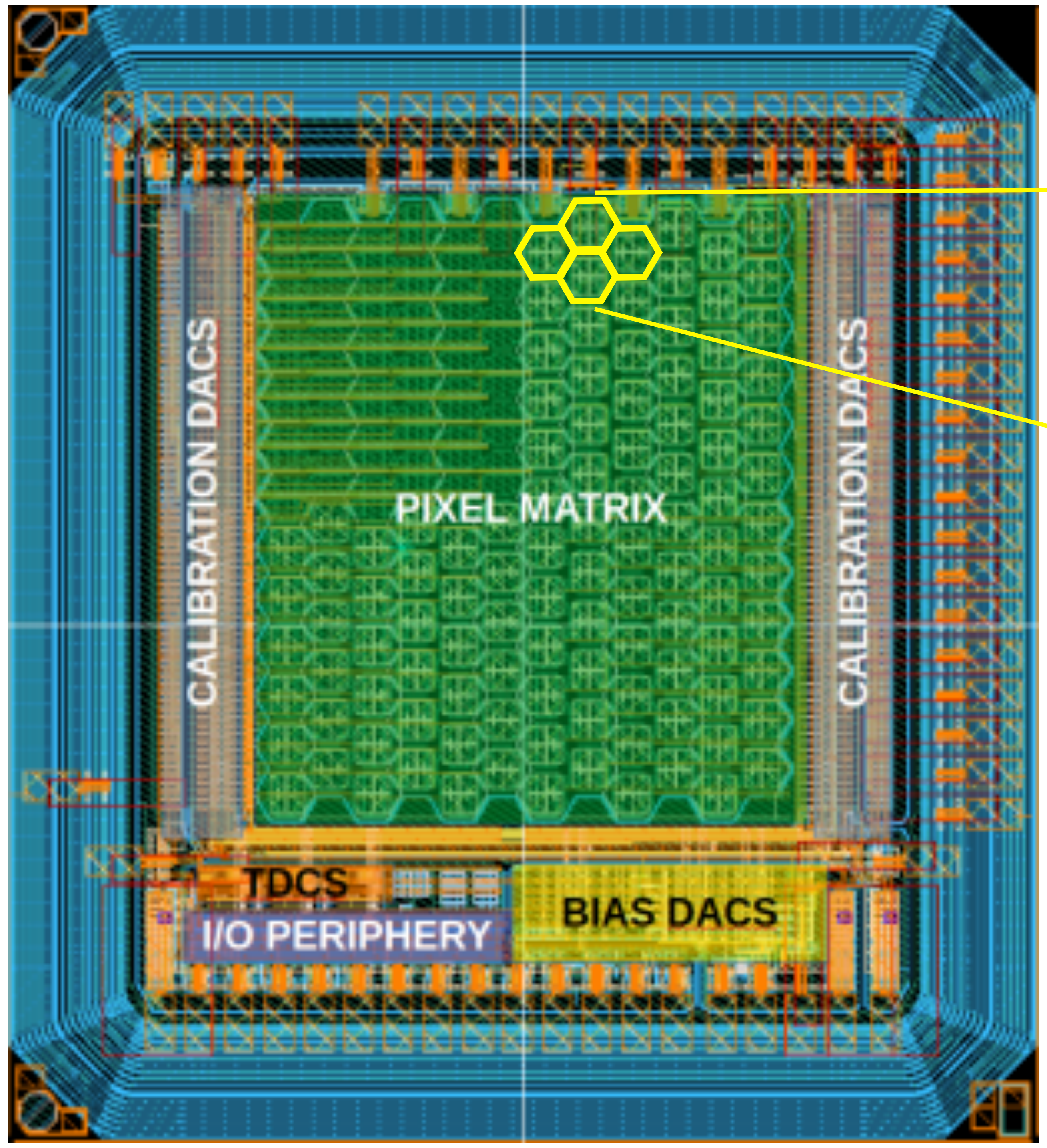
Analog Front-End

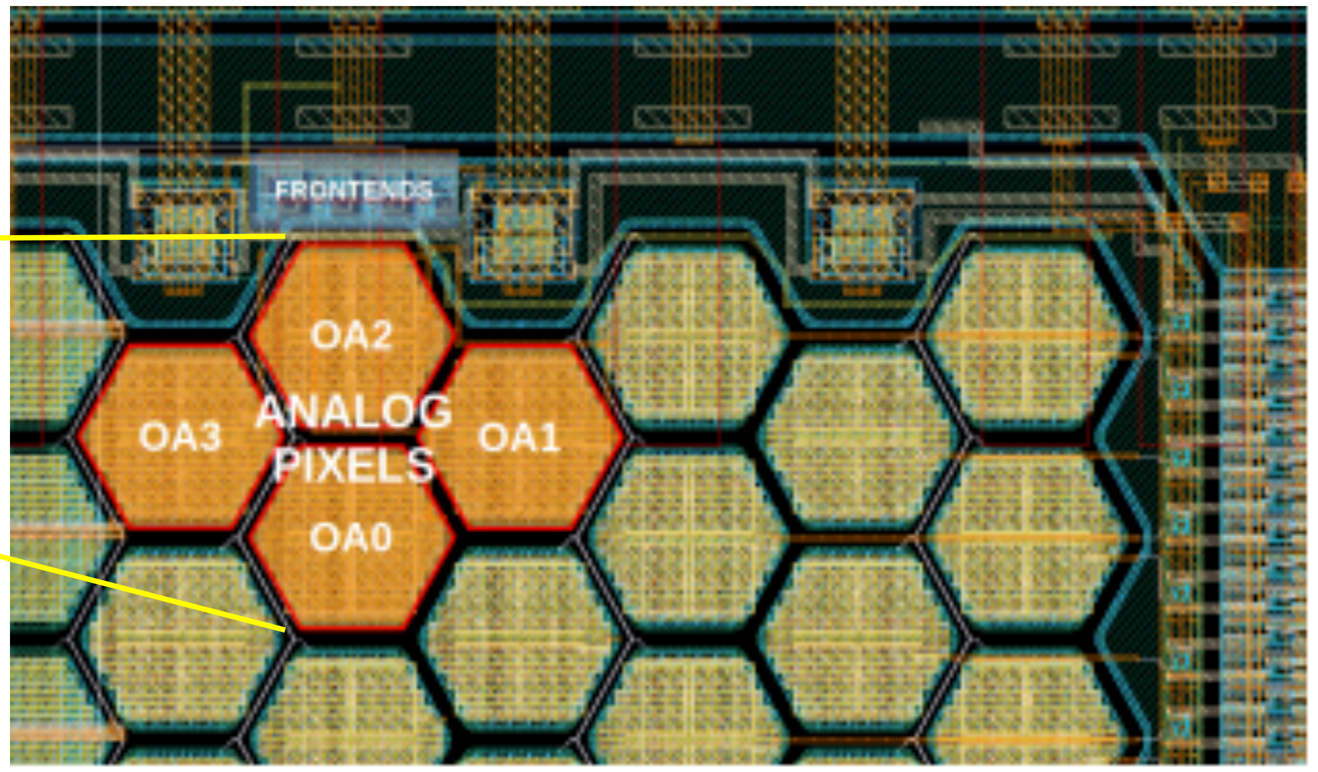


Ibias_preamp : 2 μA to 150 μA
Ibias_fbk: nominal 400 nA

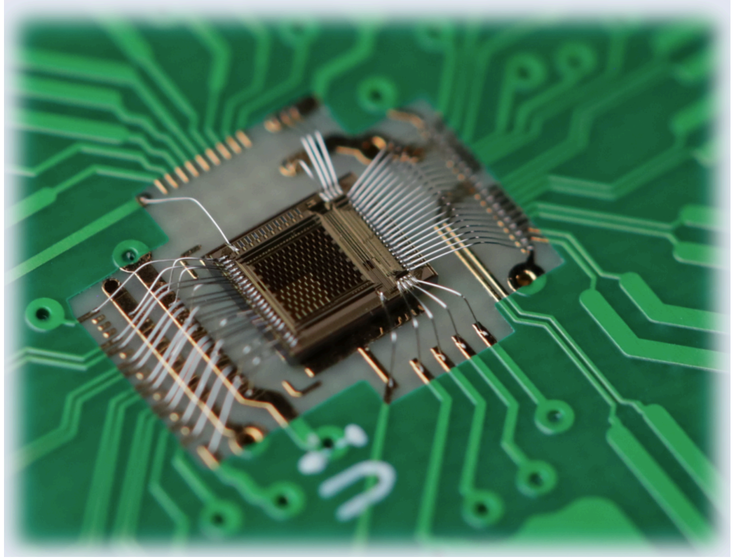
Cd = 80 fF
(100 μm pitch, electronics outside thee pixel)

Monolith Prototype 2 (2022)





hexagonal pixels with ≈ 100µm pitch

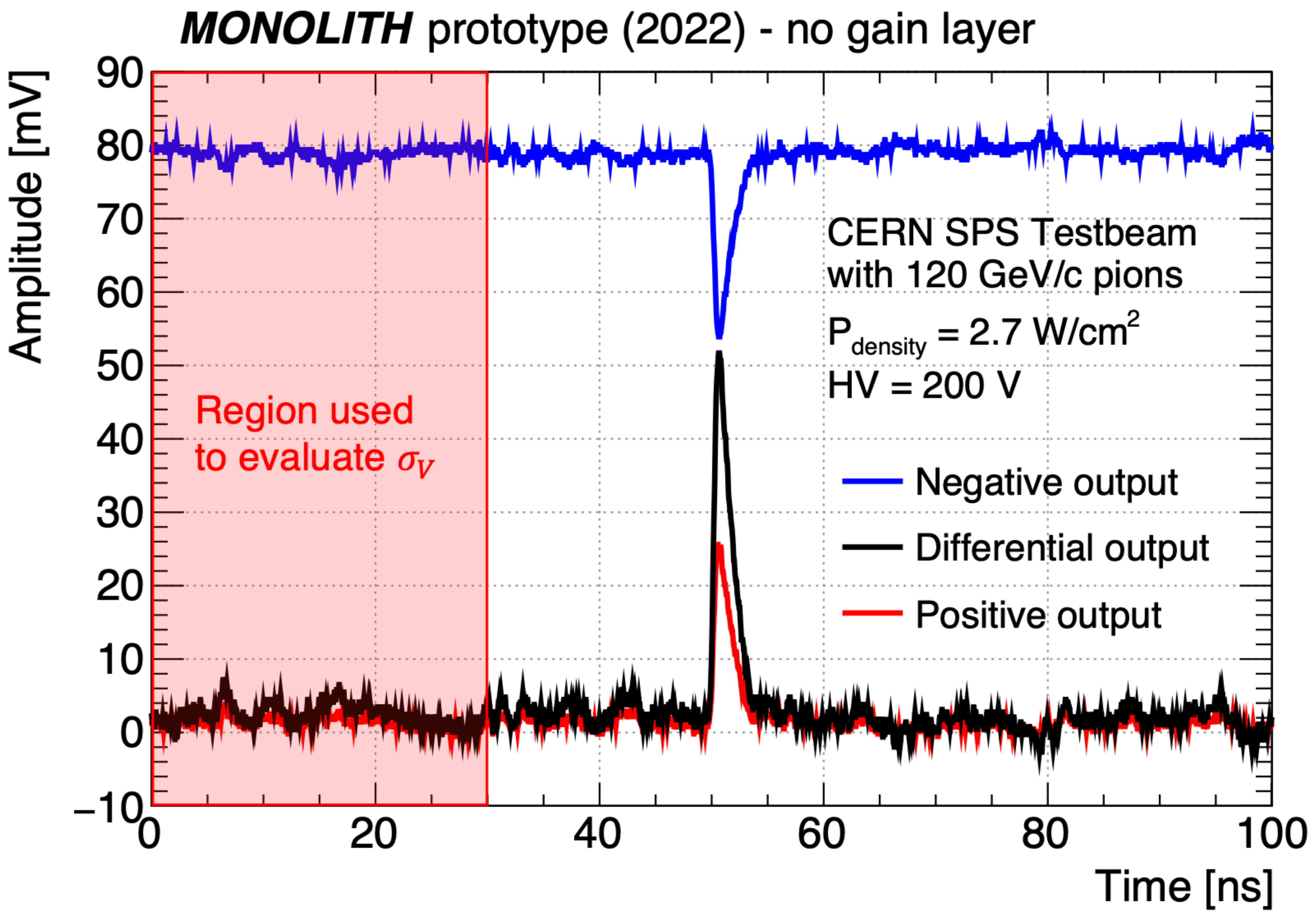


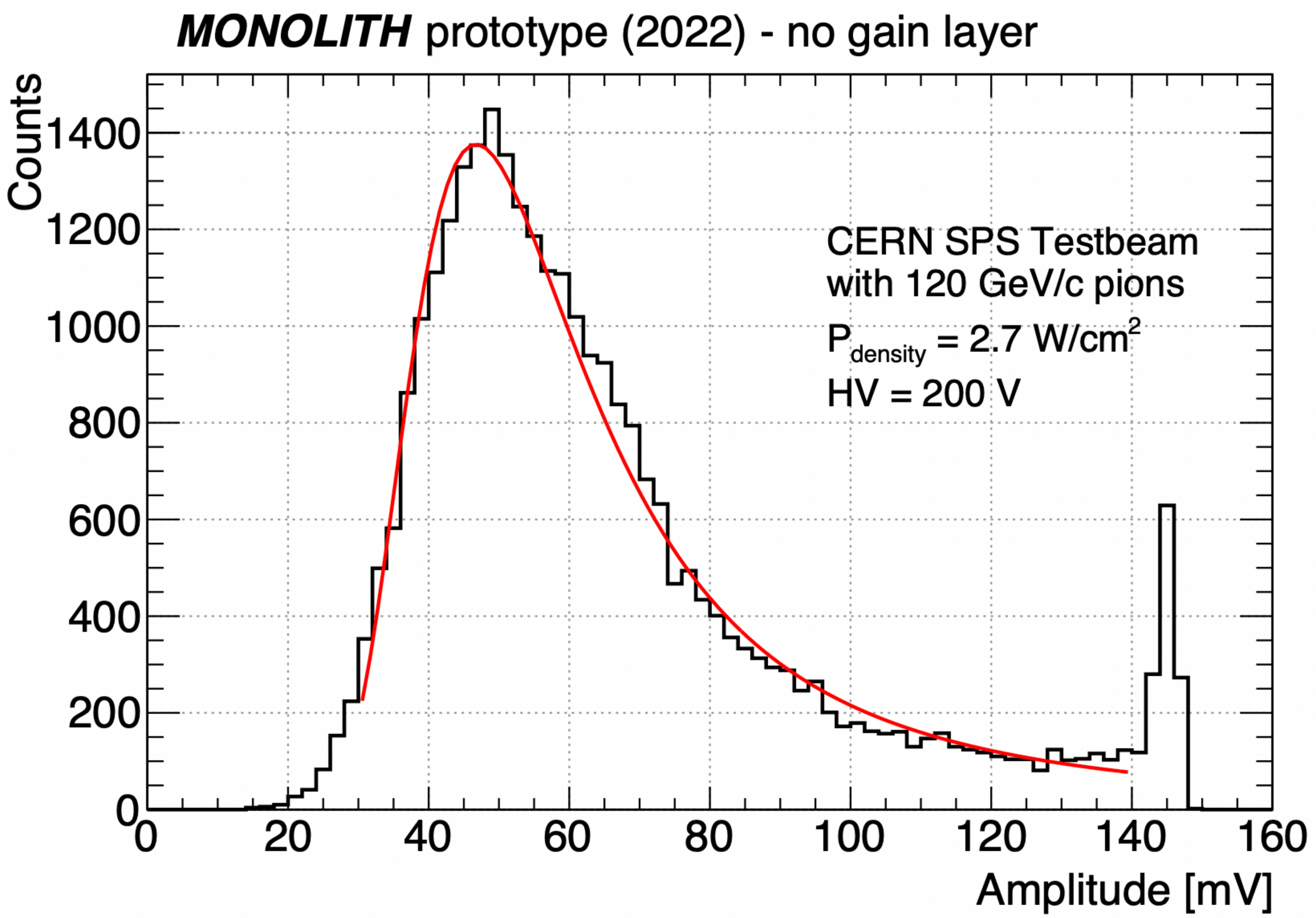
Monolith Prototype 1 (2019) 36 ps time jitter.

Improvements in Prototype 2:

- Substrate: 50Ωcm → 350 Ωcm epilayer, 50µm thick on low-res (1Ωcm) substrate.
  - Smaller pixel capacitance
  - **Depletion 26µm → 50µm**
  - Can operate sensor with **v_{drift} saturated** everywhere
- Preamp and driver voltage decoupled:
  - Increased amplifier gain
  - **Removed cross-talk**
- Analog Differential output, optimized FE layout, high-frequency cables:
  - **Better rise time** (600ps → 300ps)

Monolith Prototype 2 – Analog readout





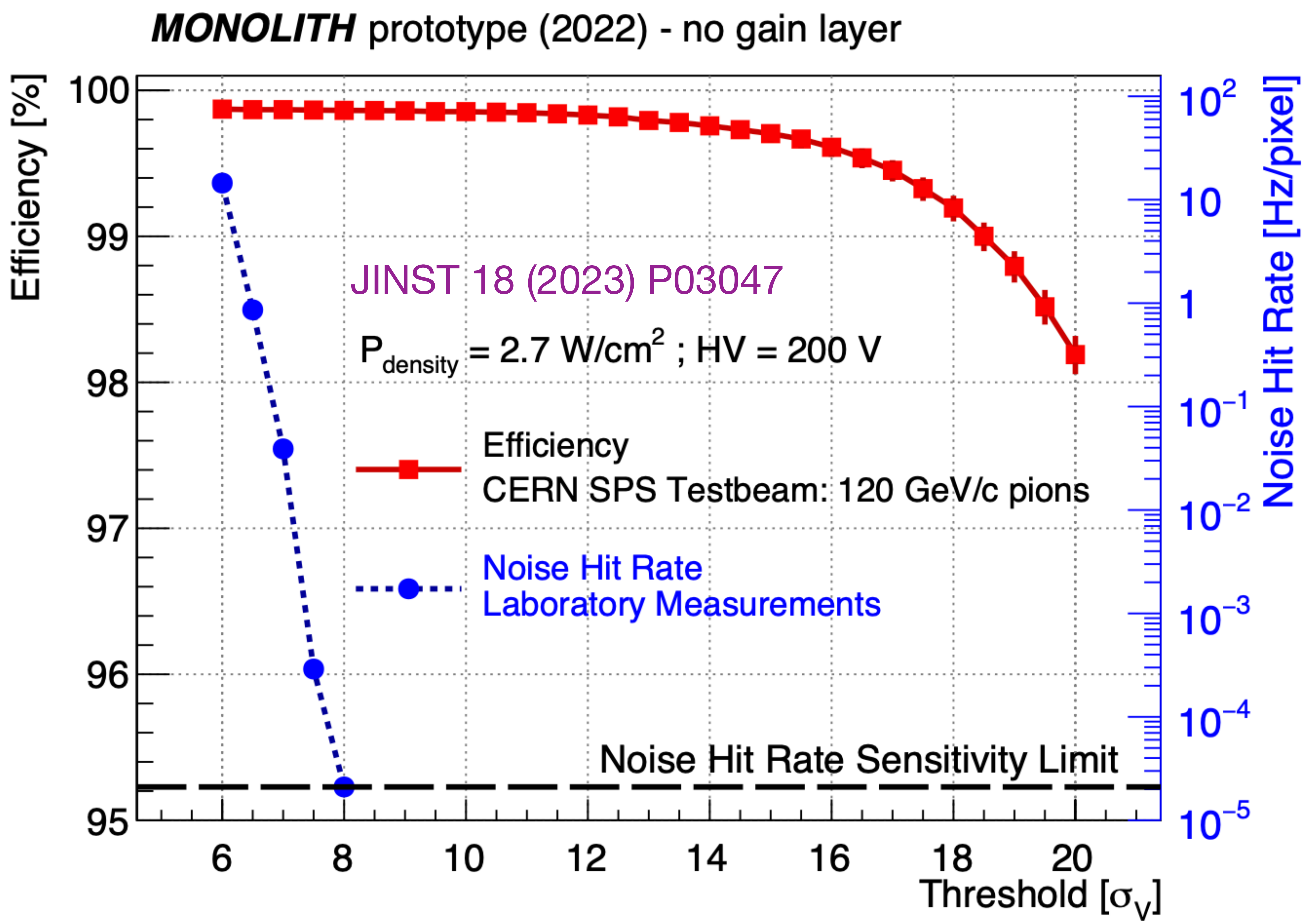
Voltage noise of the differential signal:

$\sigma_V \approx$ 1 mV

Amplitude distribution of differential signal:

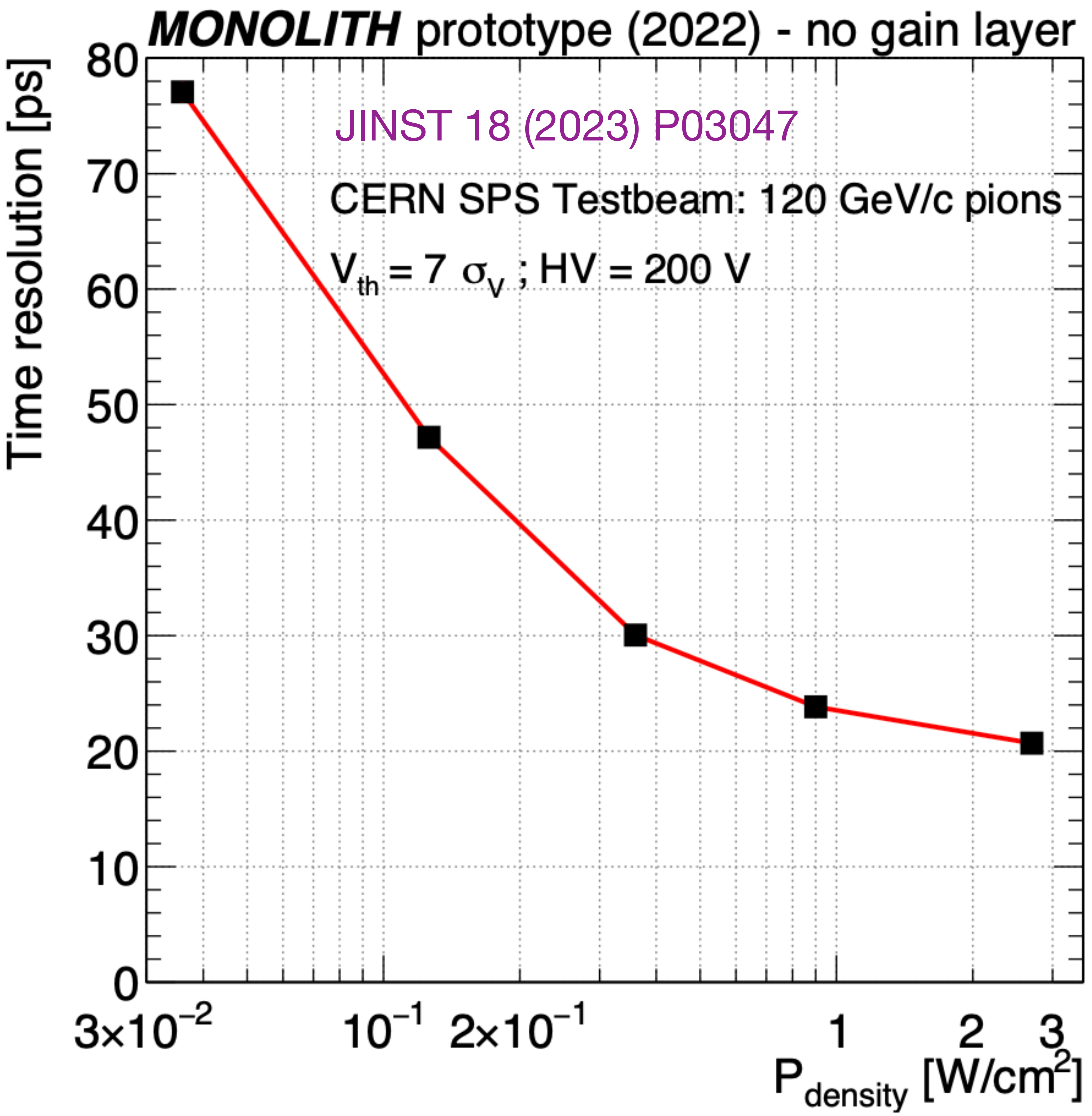
Landau with most probable value ≈ 50 mV

Monolith Prototype 2 – Efficiency and Noise Hit Rate



Large efficiency plateau at ≈ **99.8%**,
that allows operation at very low noise-hit rate

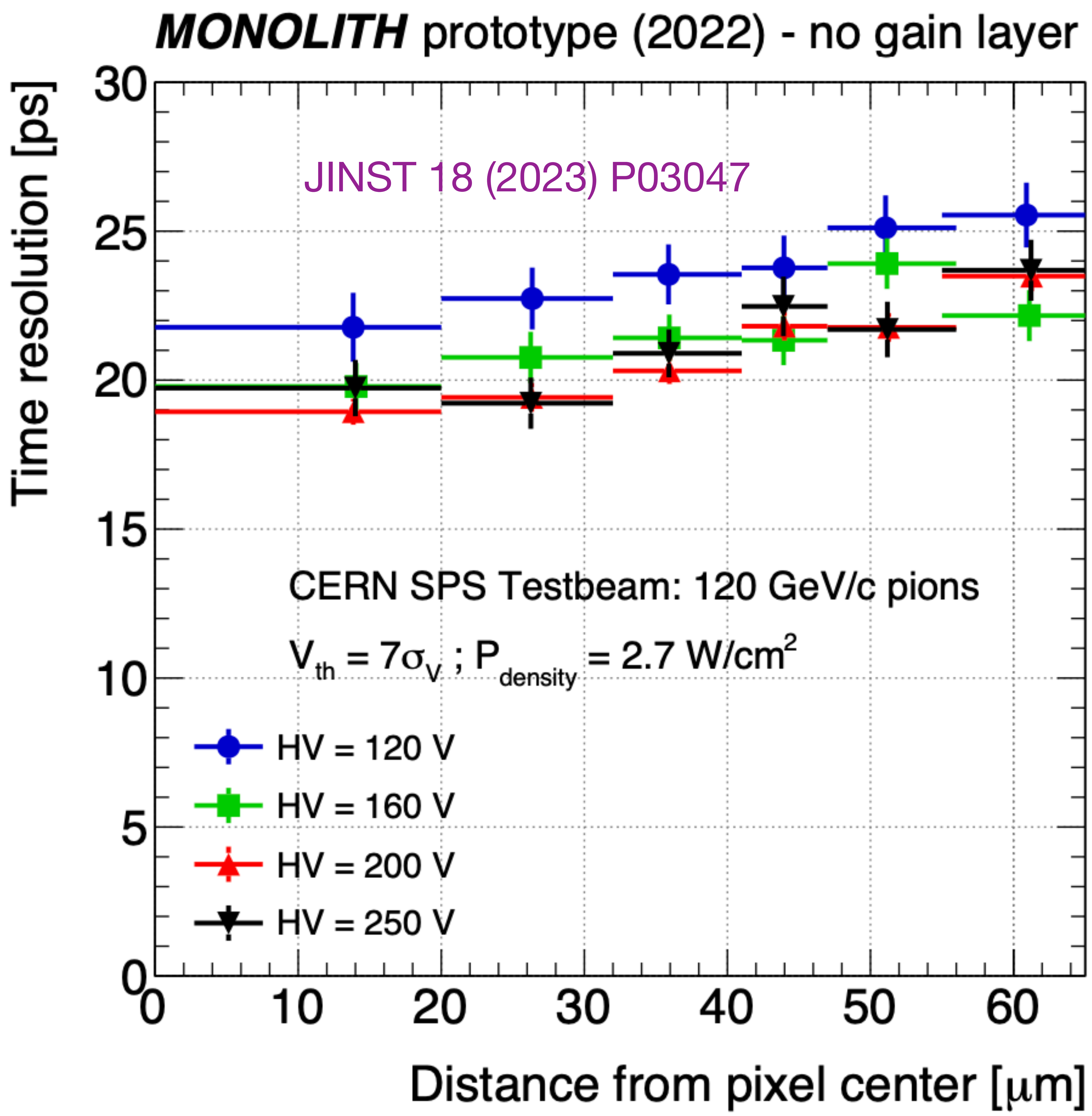
Monolith Prototype 2 – Jitter vs Power



DUT operated at $HV = 200$ V and $V_{th} = 7\sigma_V$		
$P_{density}$ [W/cm^2]	Amplitude MPV [mV]	Time Resolution [ps]
2.7	48.6 ± 0.5	20.7 ± 0.3
0.9	35.8 ± 0.5	23.8 ± 0.3
0.36	22.6 ± 0.4	30.1 ± 0.4
0.13	14.2 ± 0.3	47.2 ± 0.7
0.04	16.2 ± 0.3	77.1 ± 0.9

20 ps at 2.7 W/cm^2
50 ps at 100 mW/cm^2

Monolith Prototype 2 – Jitter vs Position



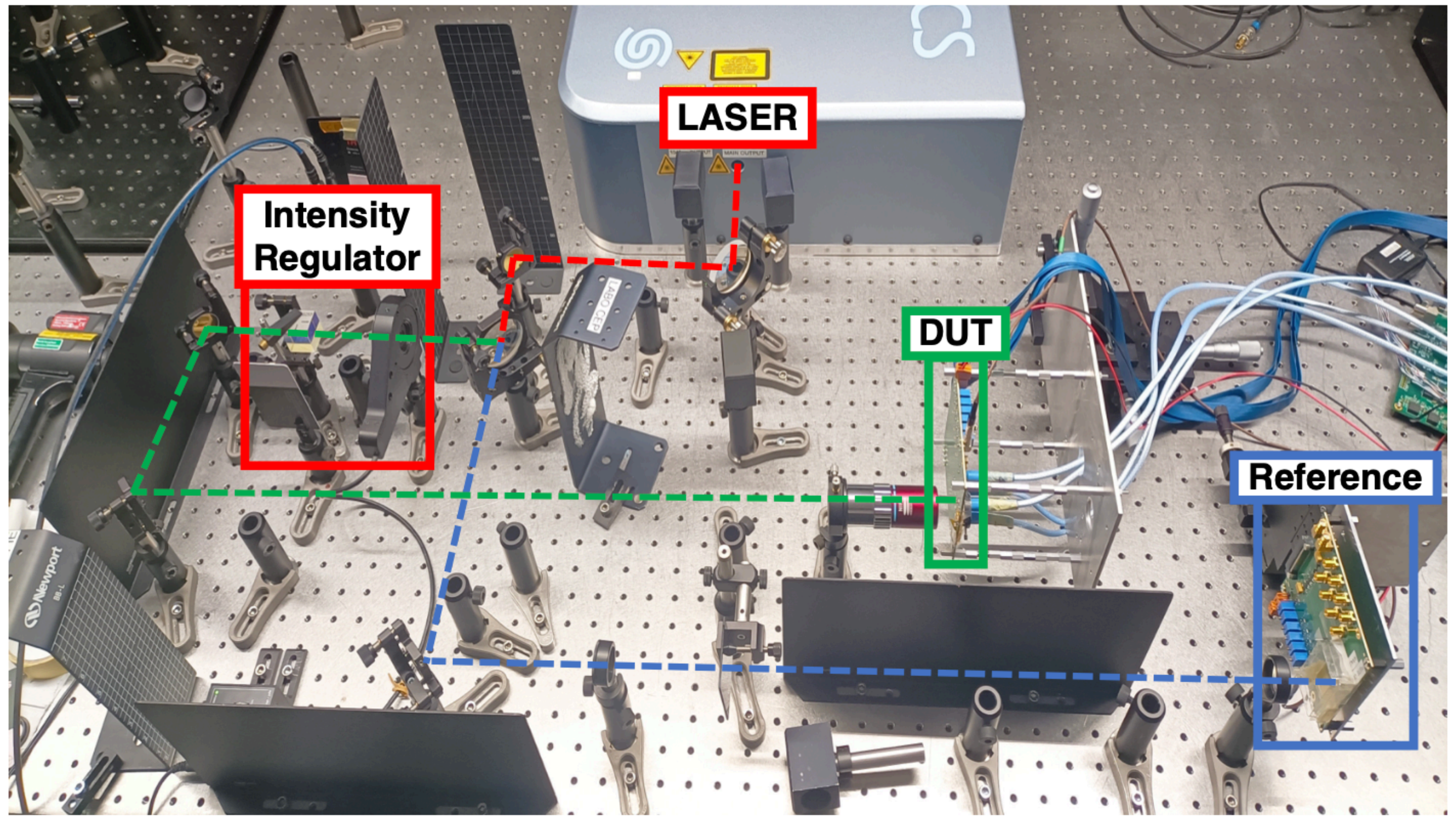
For HV ≥ 160V, time resolution ranges from **≈ 19 ps** at the center

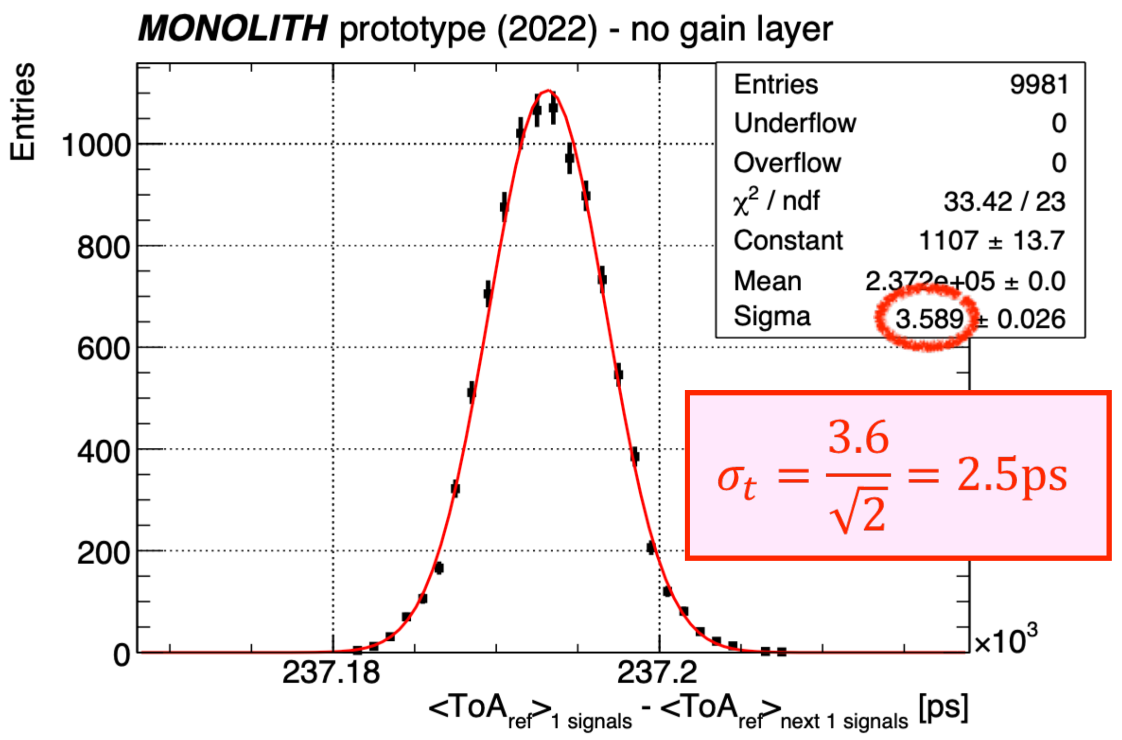
to **≈ 23 ps** at the edge of the pixel

Still something to improve with the weighting field far from pixel center.

For HV = 120 V: ≈ 3 ps worse.

Monolith Prototype 2 - Laser measurement

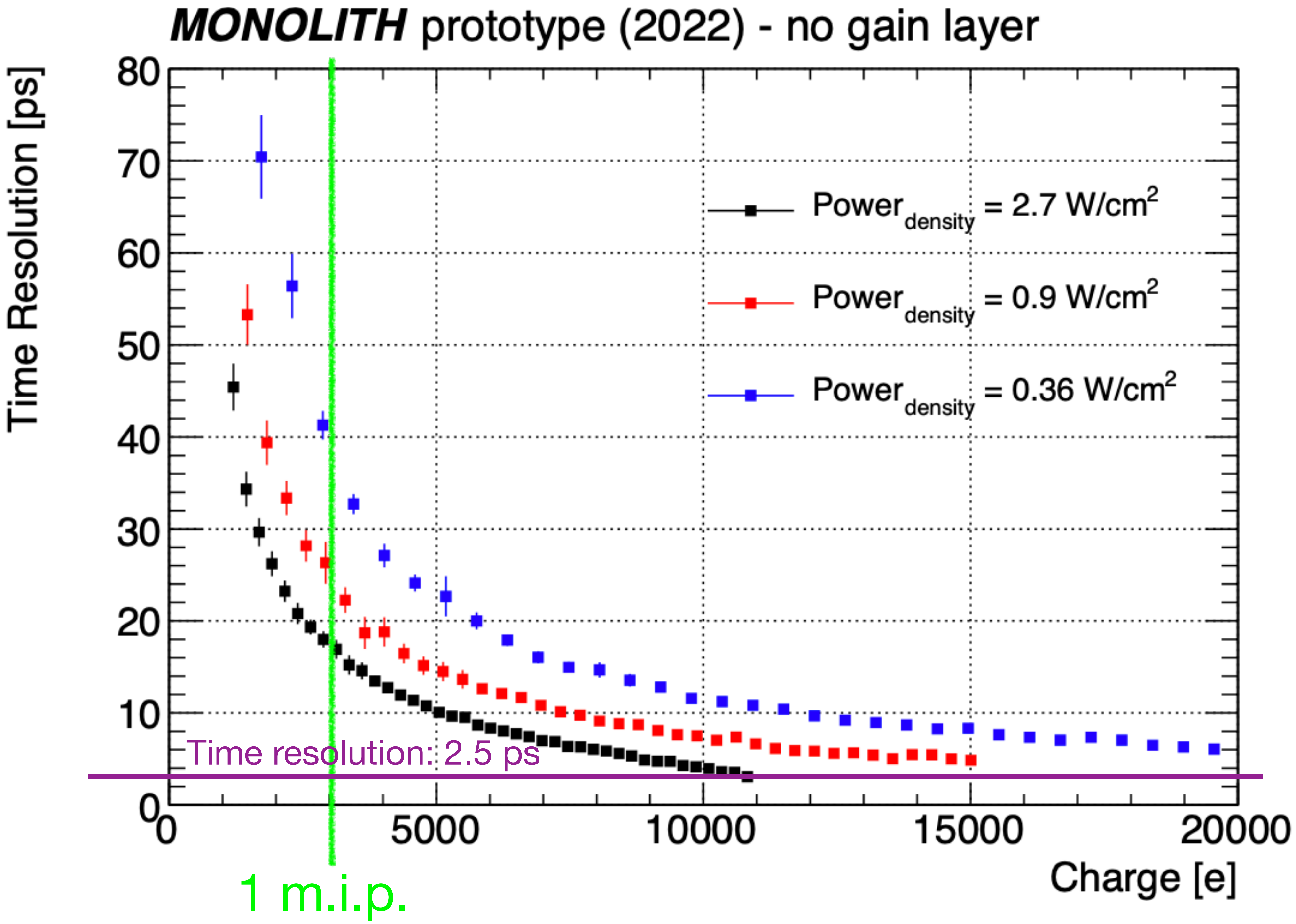




Our prototype "**Reference**":

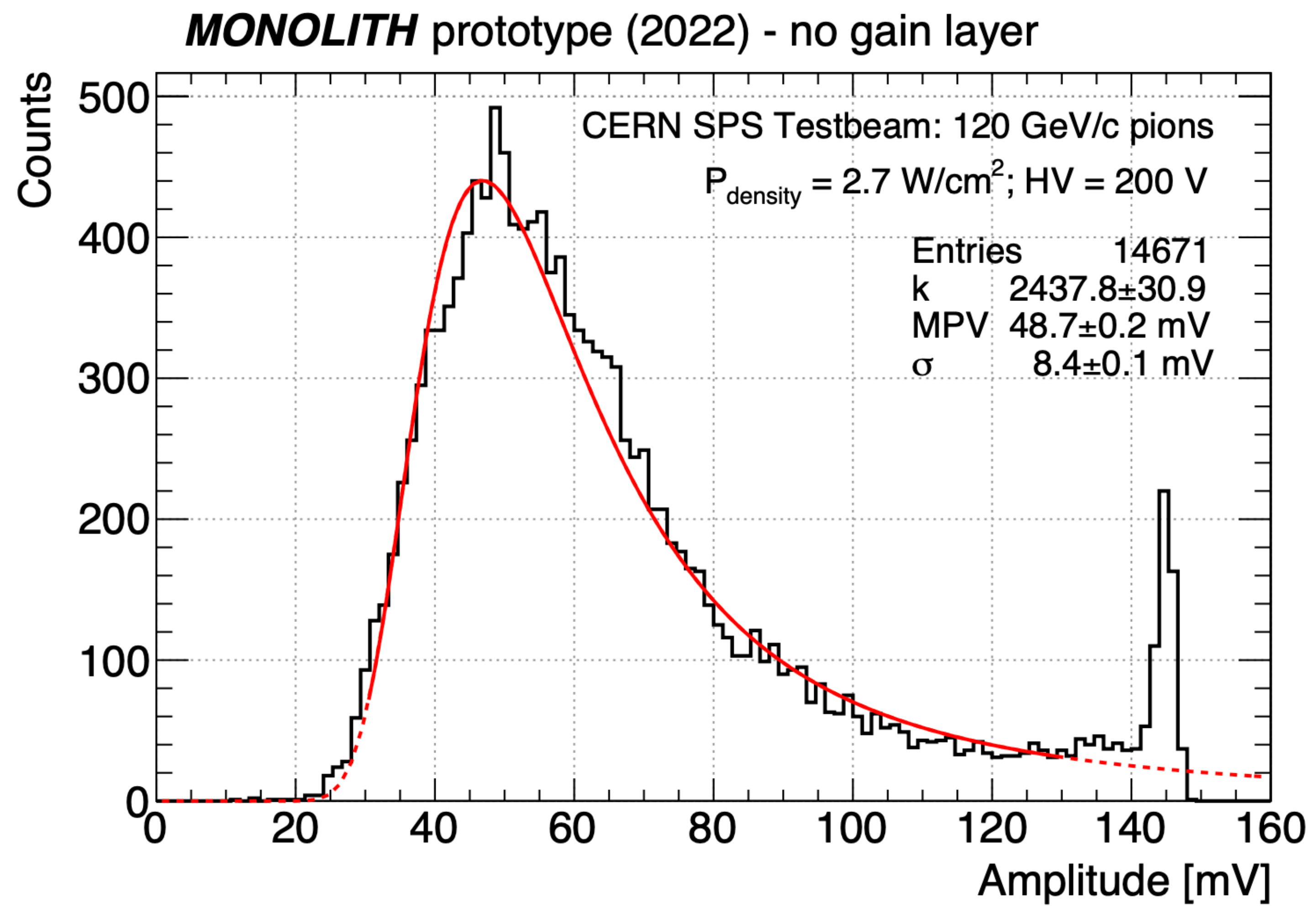
Time resolution = 2.5 ps

with **17k e⁻** (5—6 mips)



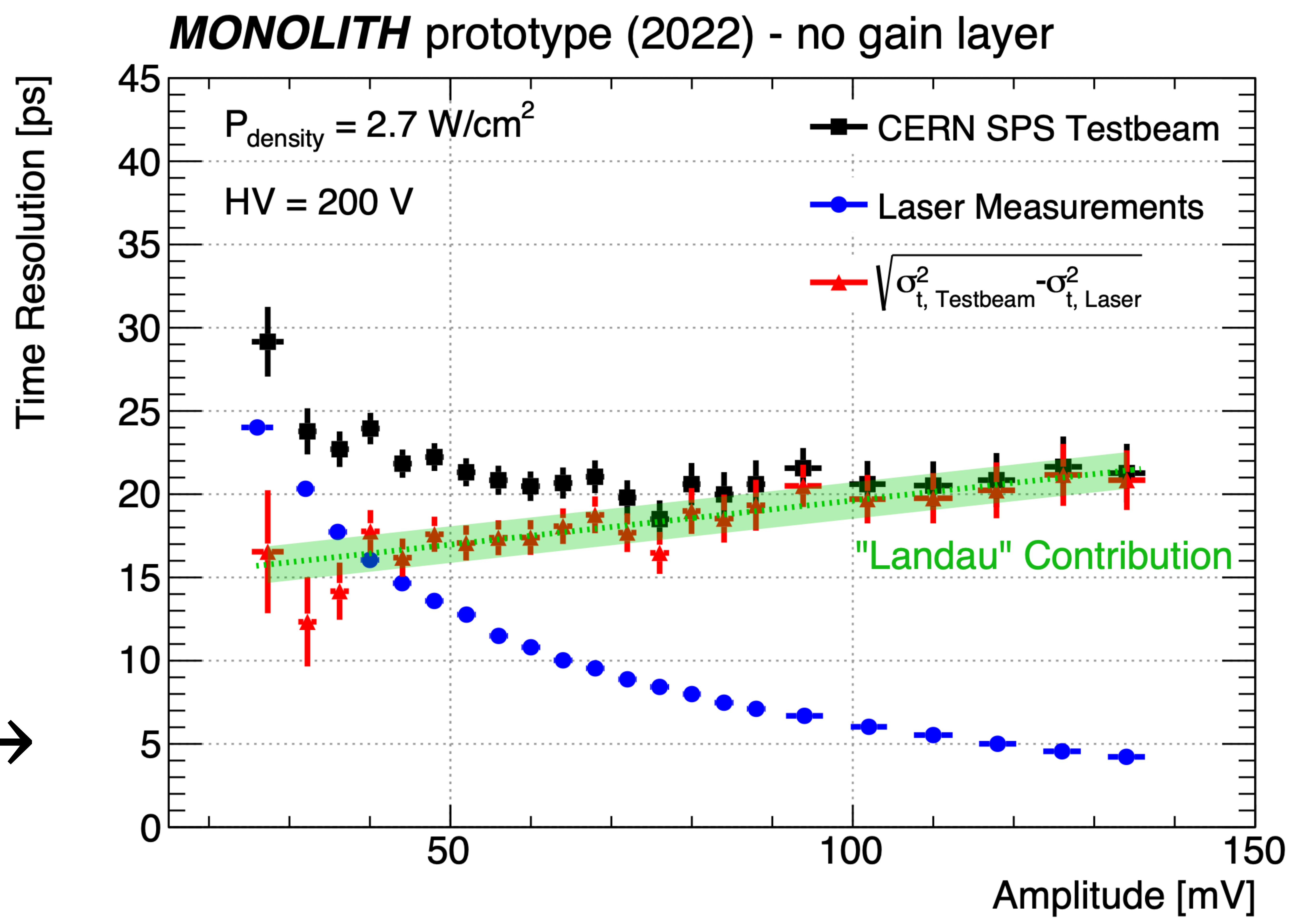
Monolith Prototype 2 – MIP vs Laser

Laser amplitudes were reweighed to the testbeam amplitude distribution:



to estimate the charge-collection ("Landau") noise

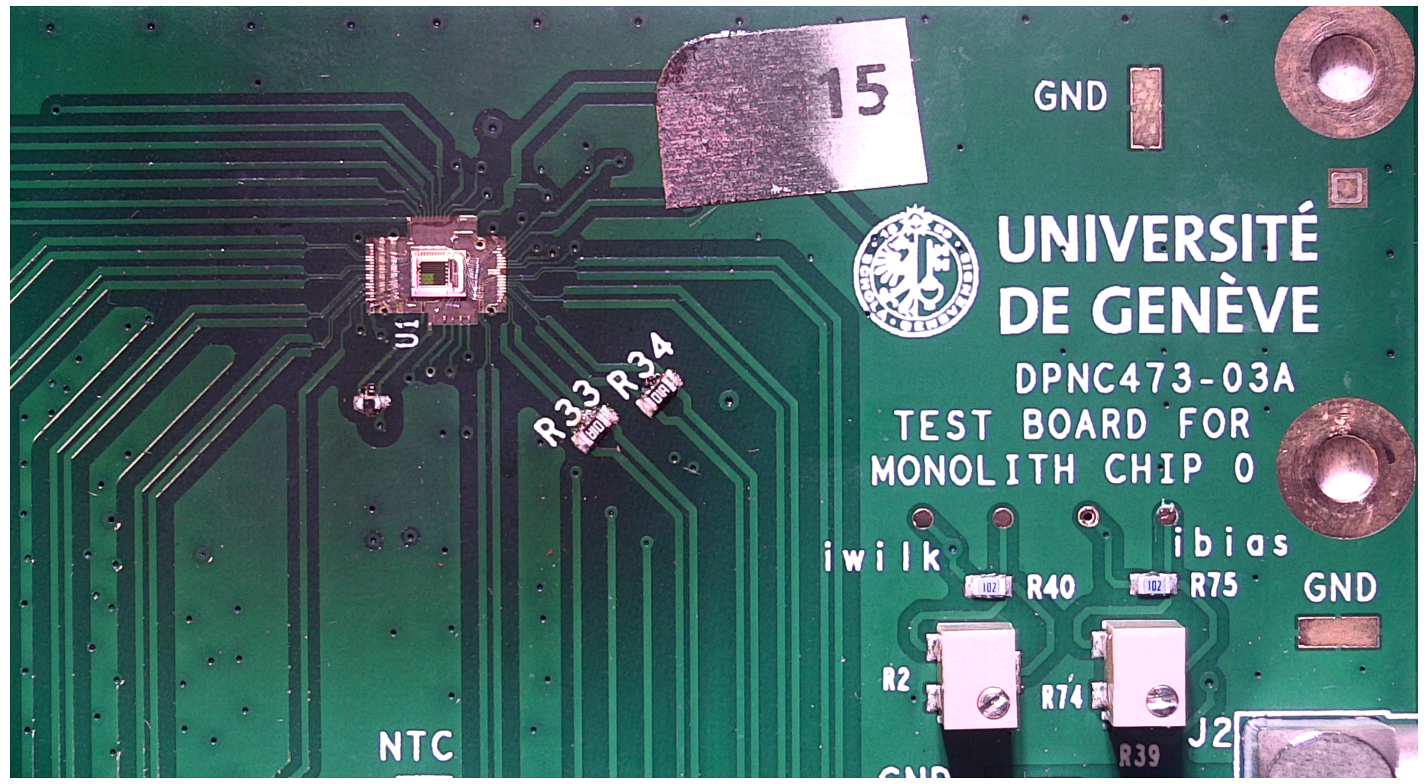
→

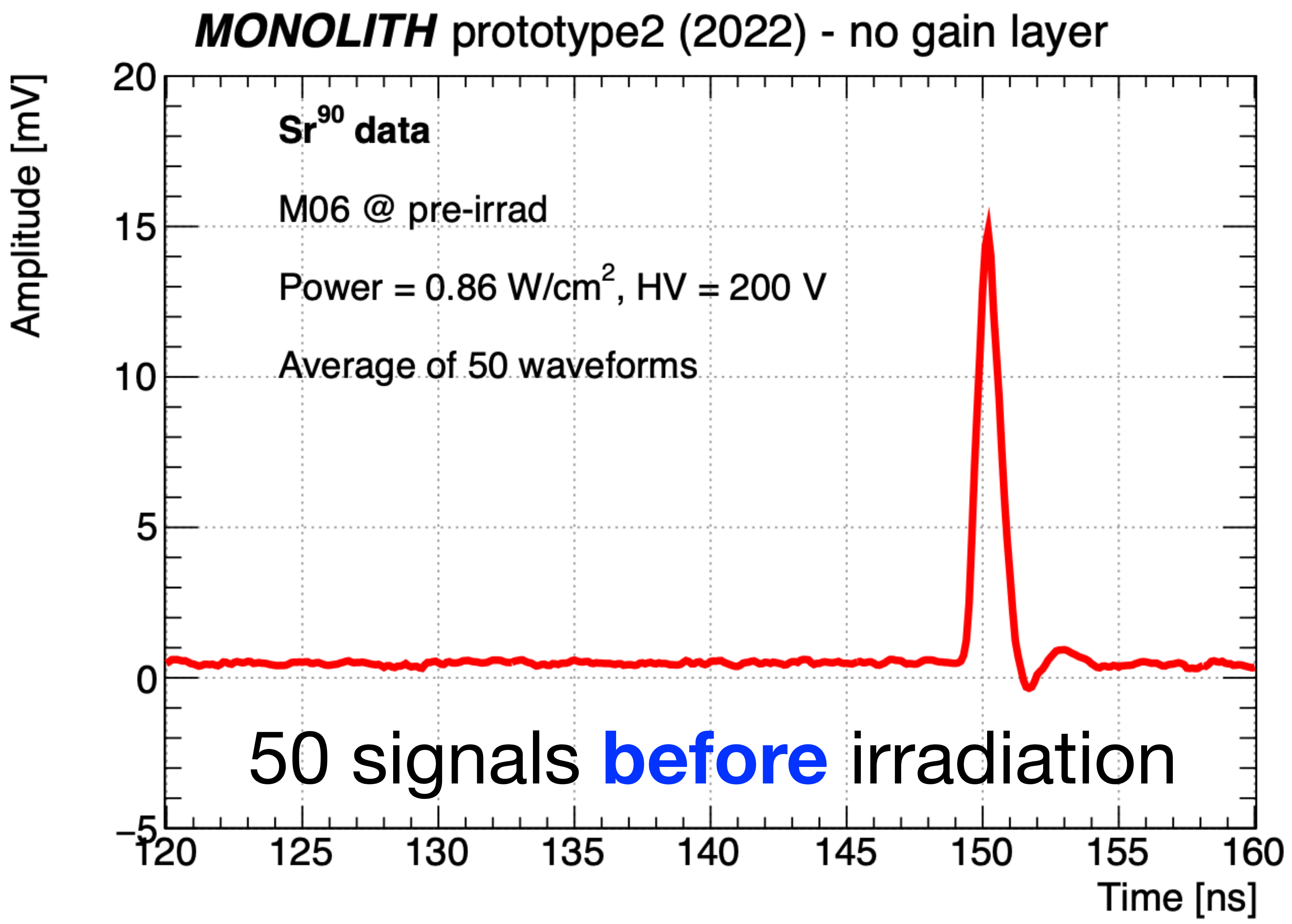


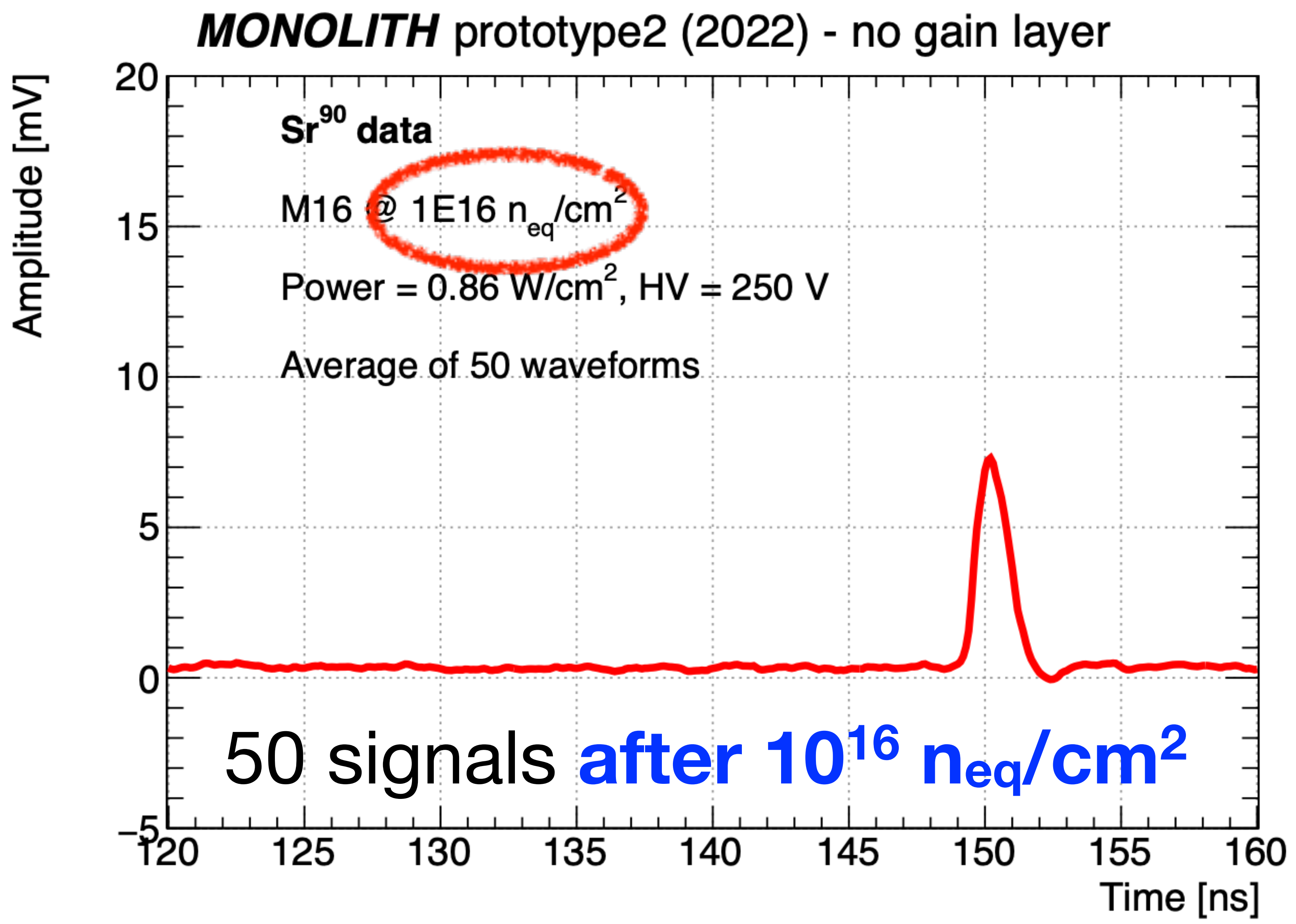
Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
10 samples of prototype2 ASIC were irradiated in Japan up to 1×10^{16} n_{eq}/cm^2.

Very good news:
even after 10^{16} n_{eq}/cm^2 the prototypes work !!!

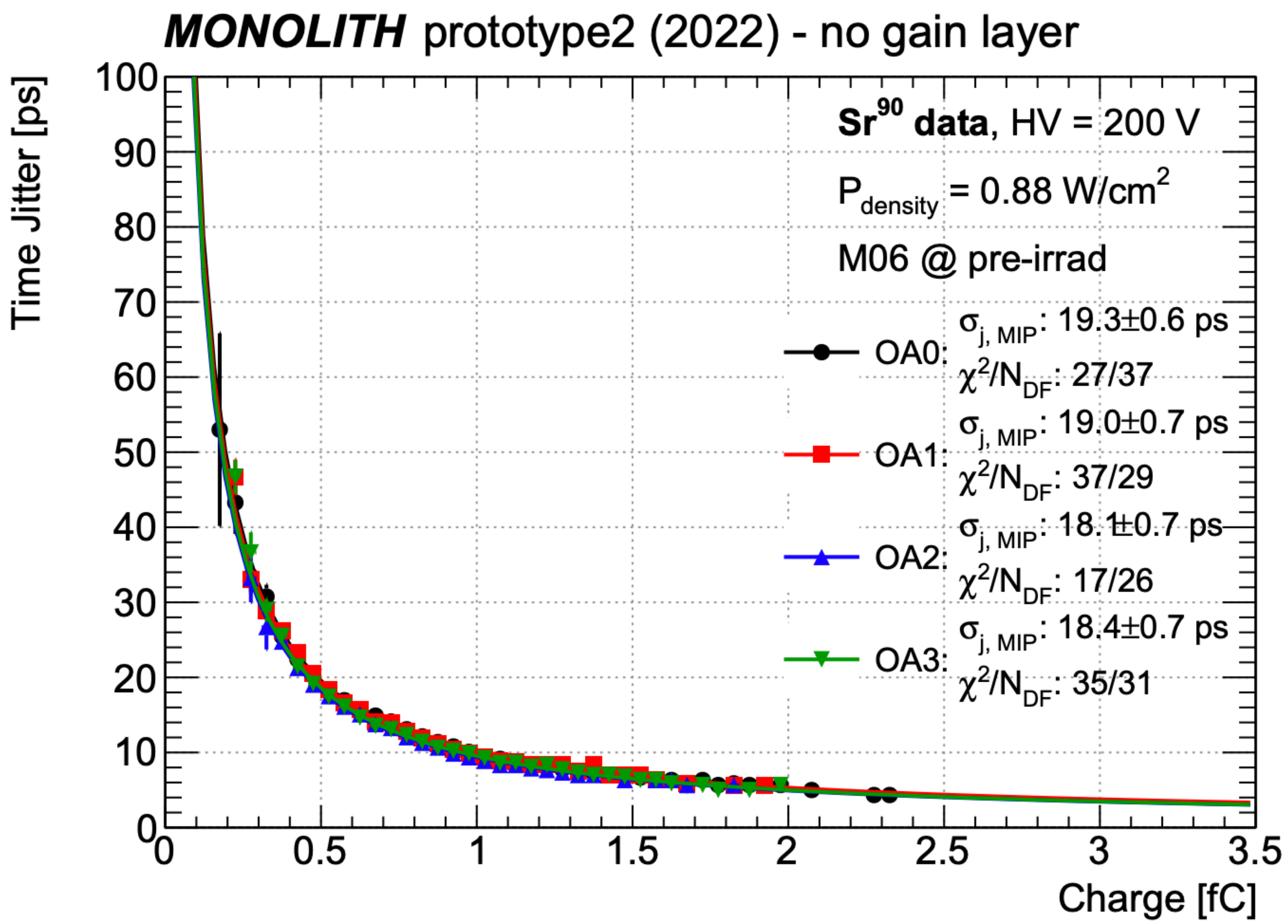




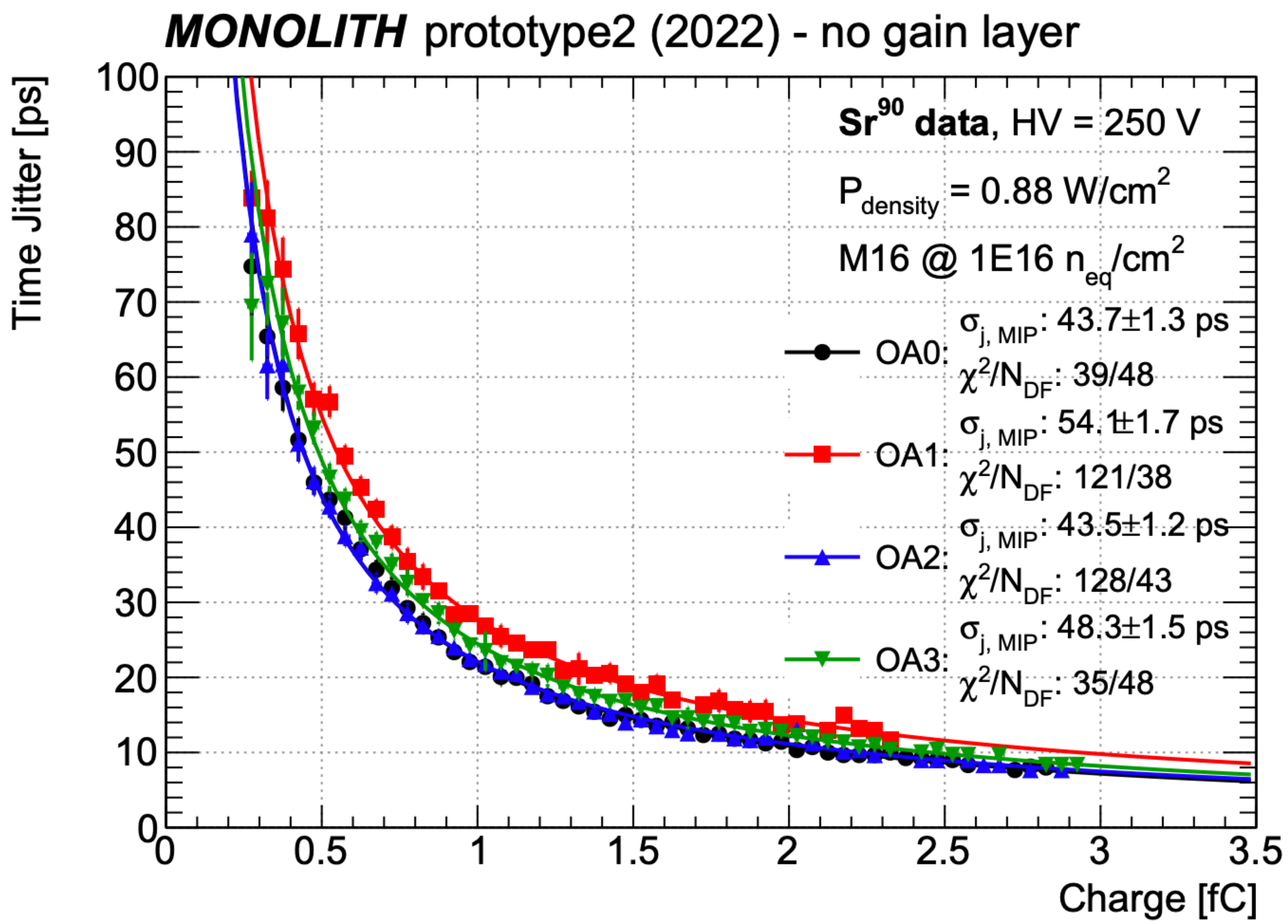


Monolith Prototype 2 Radiation hardness – Jitter vs Qin

pre-rad



after 10^{16} n_{eq}/cm^2



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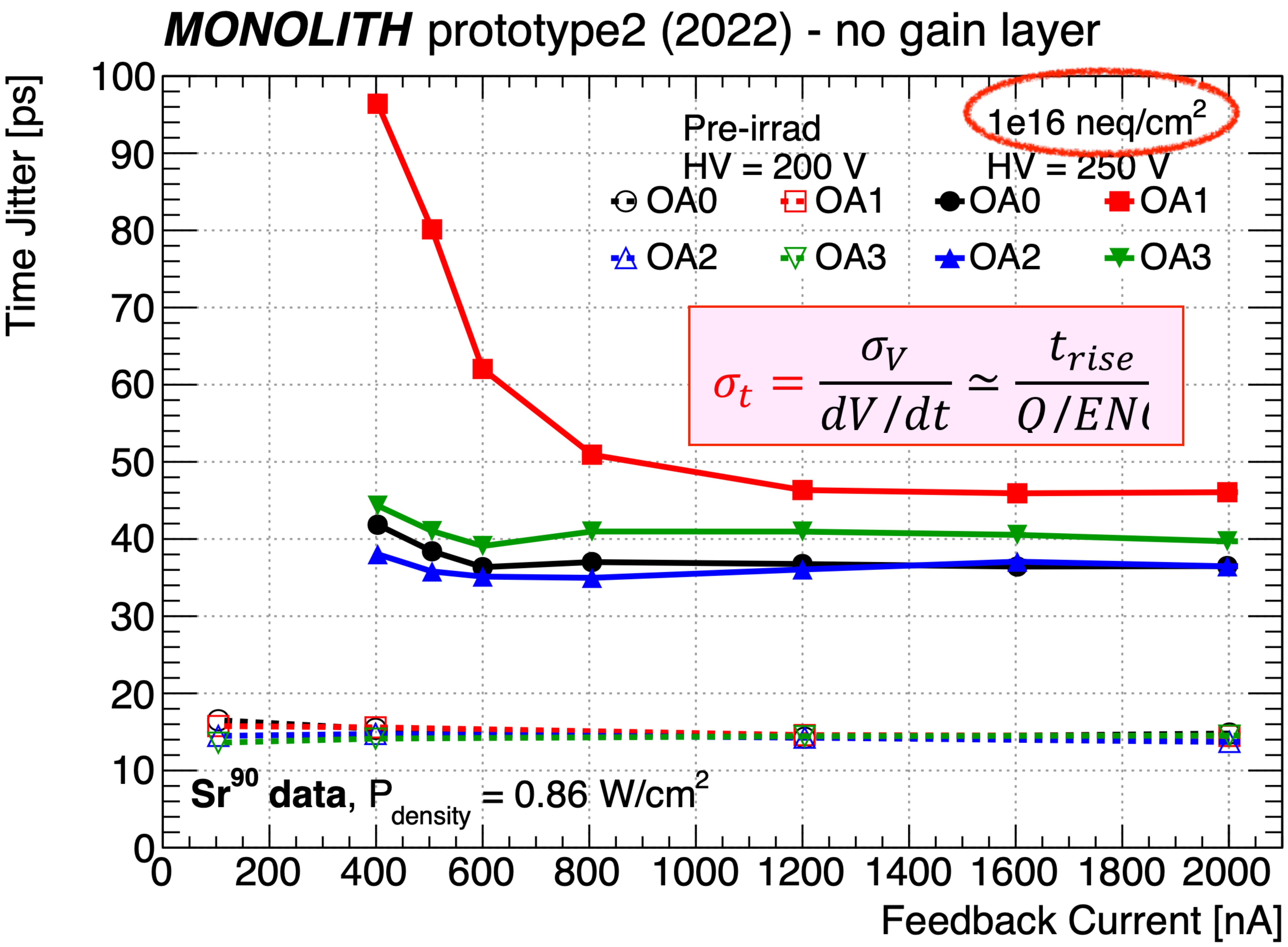


$$\sigma_t = \frac{\sigma_V}{dV/dt} \simeq \frac{t_{rise}}{Q/ENC}$$

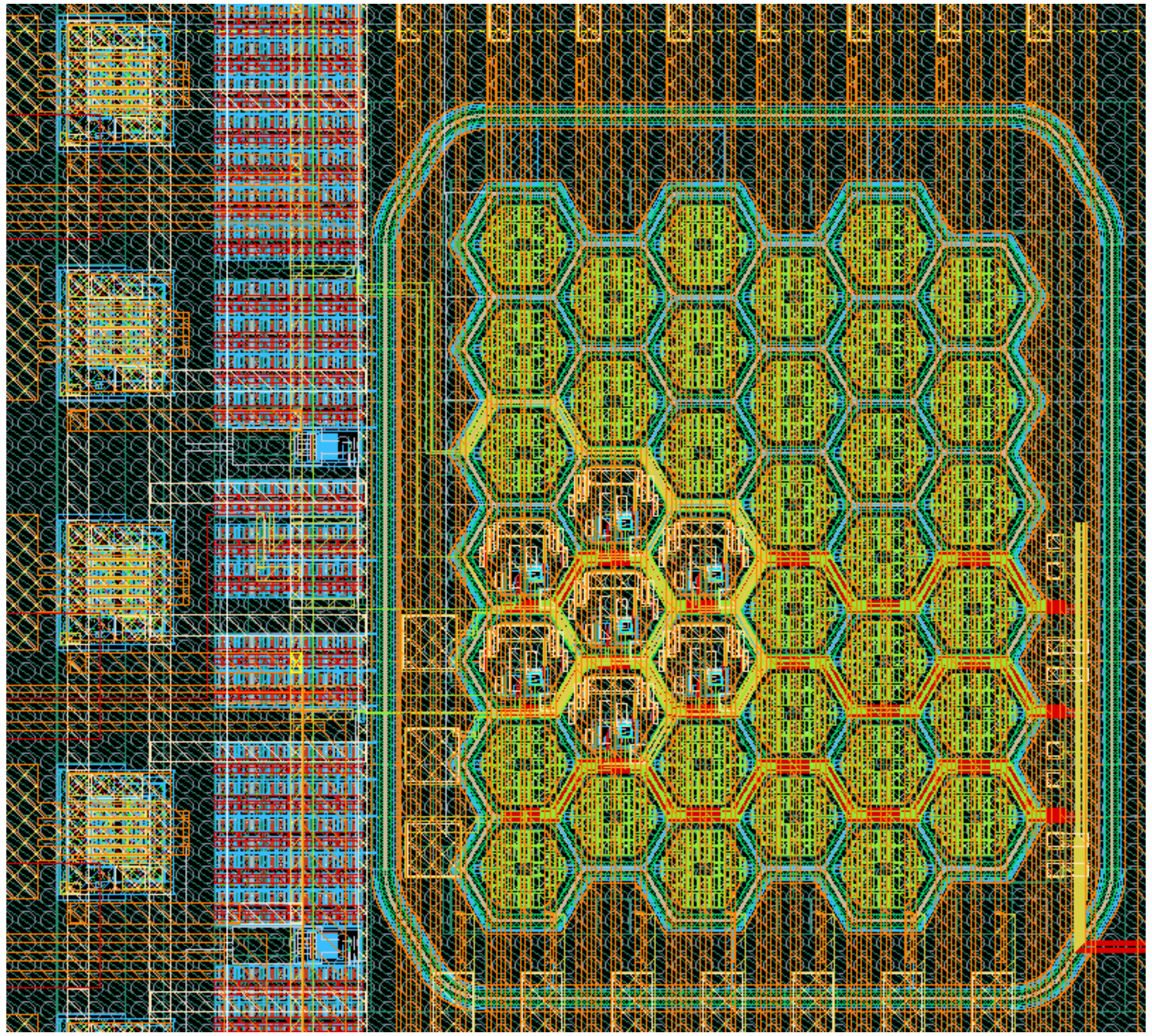
Excellent news from radiation tolerance studies:

ASIC work even at 1×10^{16} n_{eq}/cm^2 and present large $i_{feedback}$ plateaux. The electronics time jitter increases **from ≈16ps to ≈40ps** with HV increased only by 50 V (200→250 V)

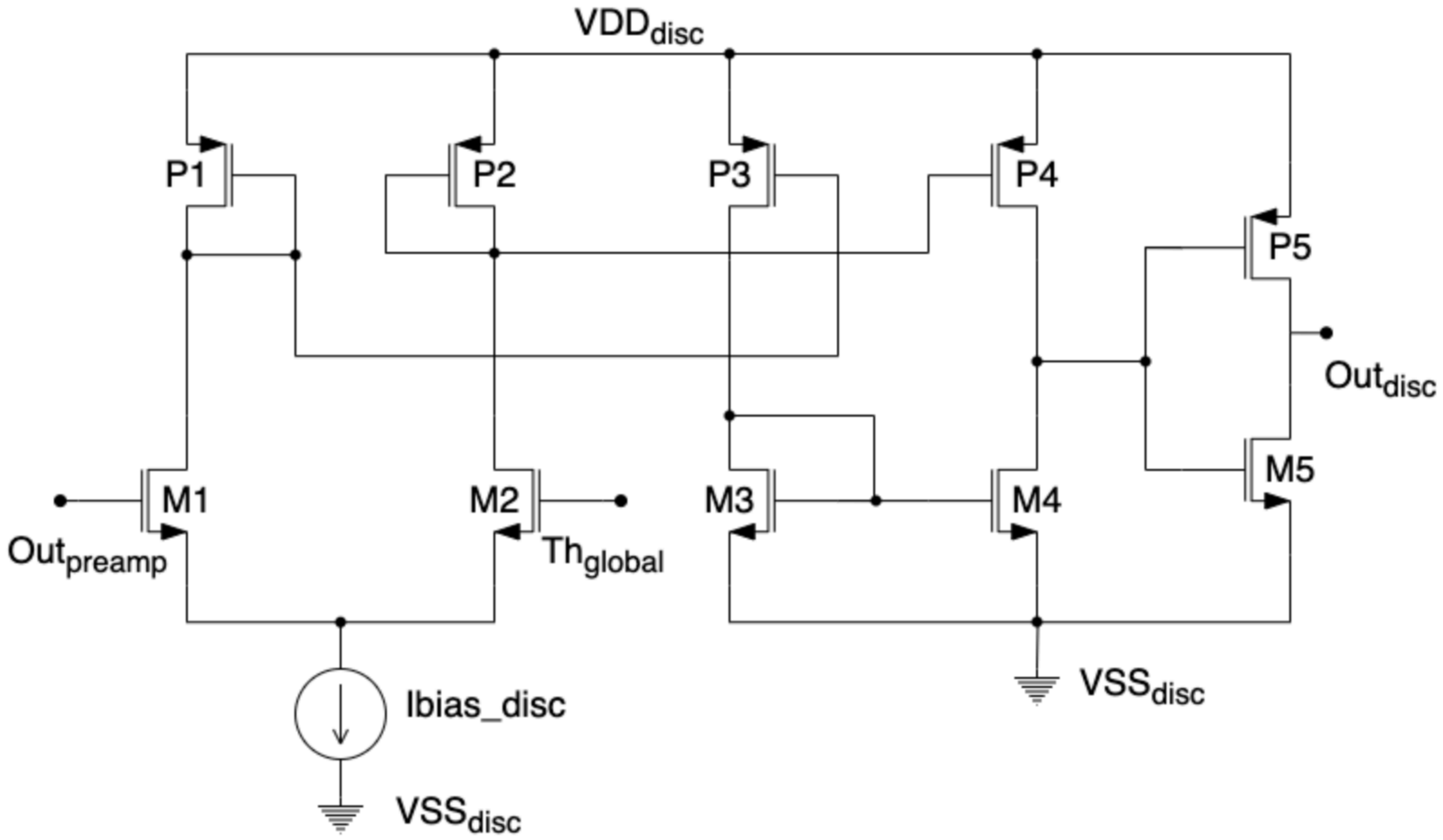
Efficiency & time resolution with mips from testbeam this summer

Monolith Prototype 3 – 50 μm pitch

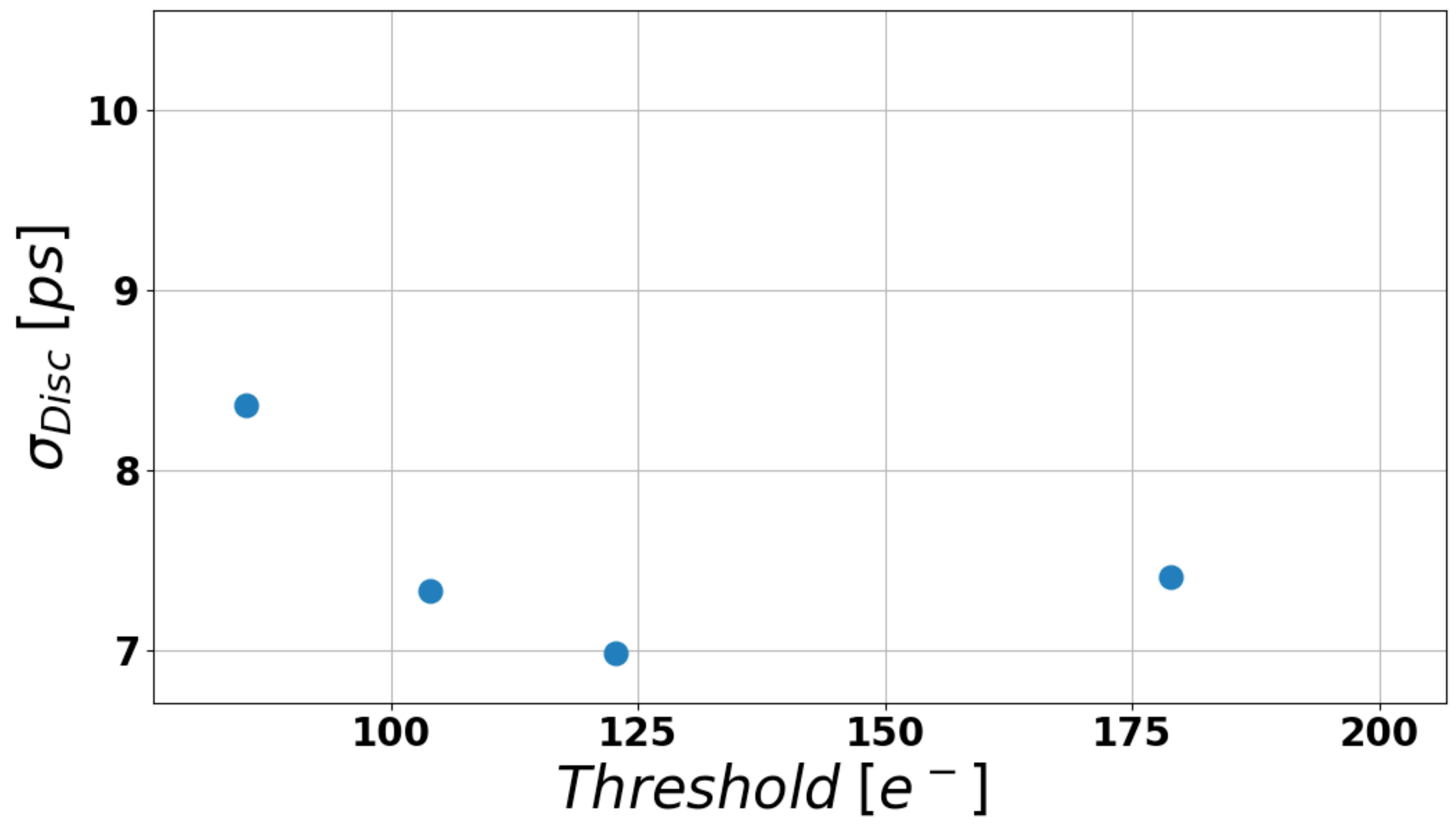
- New prototype: pixels with **50μm pitch**
  - smaller capacitance
  - same timing performance with less power
- **improved FE electronics**
  - 3 different configurations:
    - ➡ analog output with FE in pixel
    - ➡ analog output with FE off pixel
    - ➡ discriminated output with FE and discriminator in pixel
  - reduced inter-pixel distance from 10μm to 6μm to maintain time resolution at pixel edges
- Recently back from the foundry



Monolith Prototype 3 – in pixel discriminator

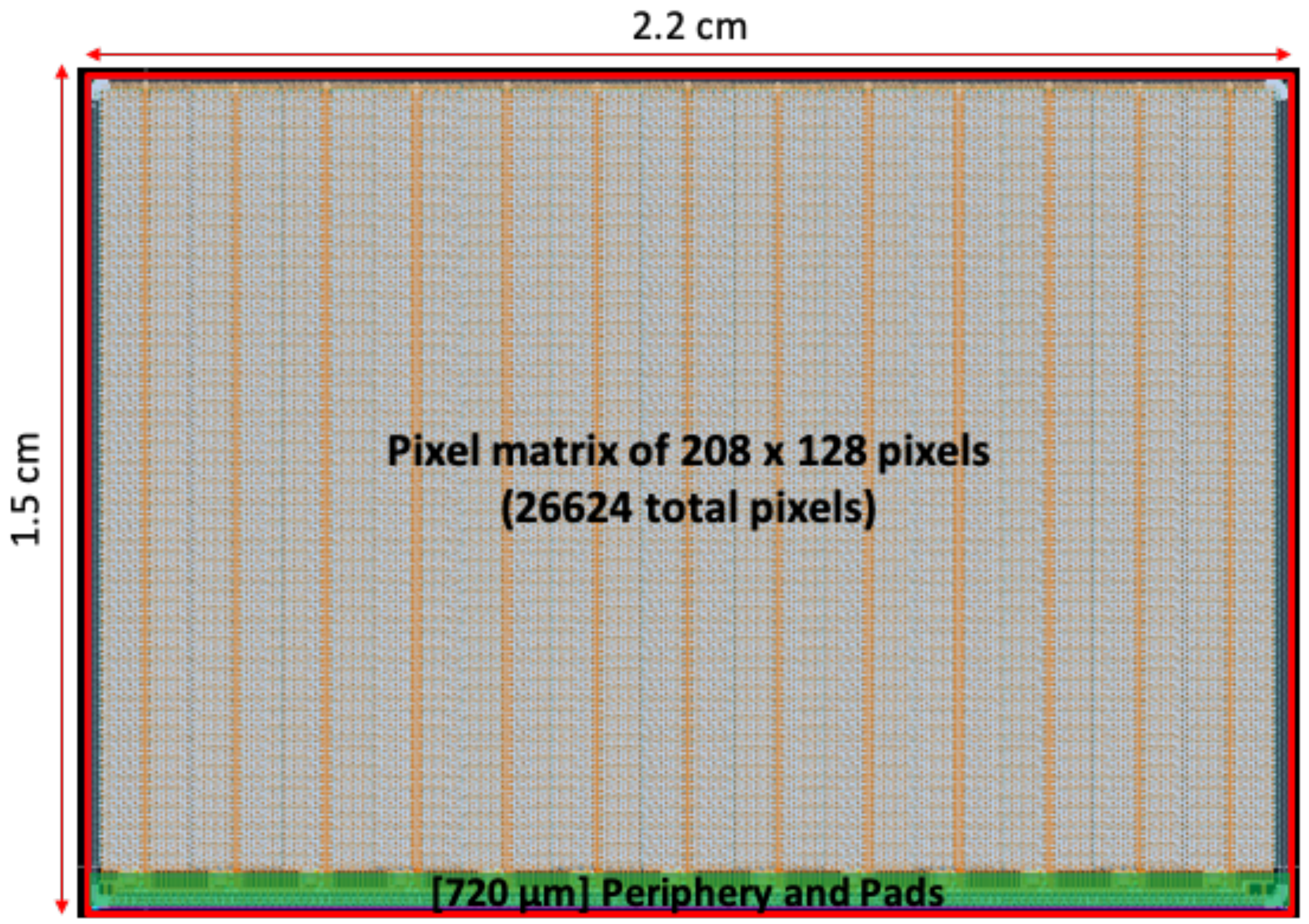


In pixel front-end and discriminator
Simulation expected performance



Cdet = 40 fF
Ipreamp = 50 μA
Ibias_disc = 5μA
Qin = 6250 e

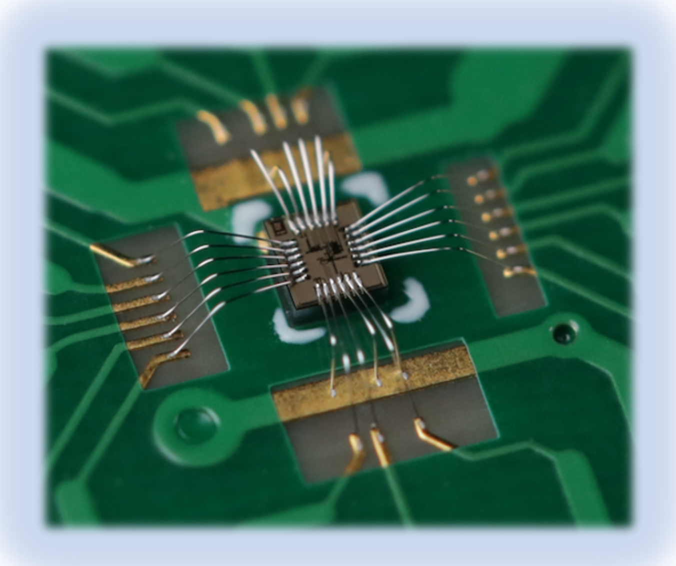
Towards a full reticle size sensor



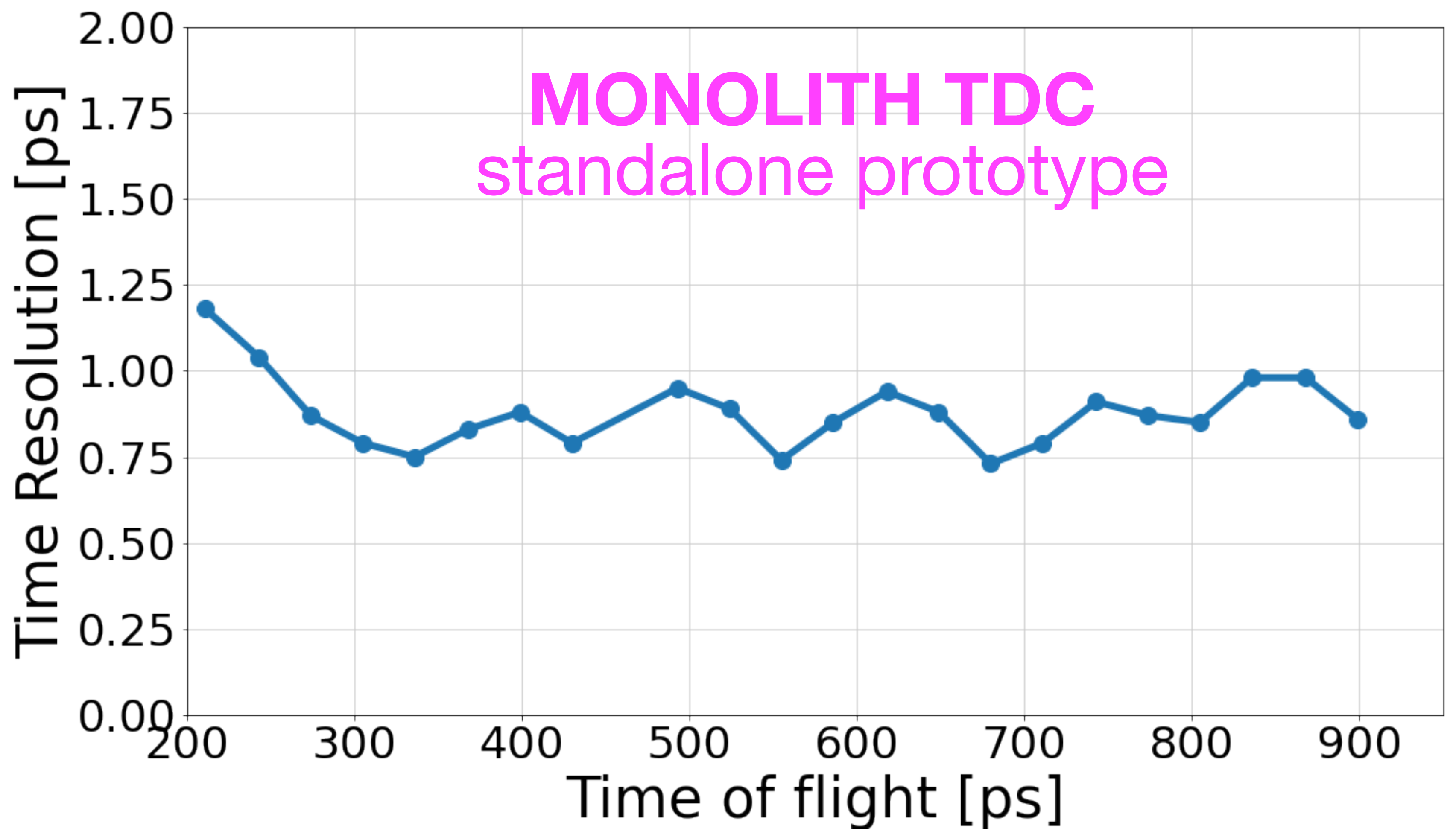
Experience on large scale desing in IHP BiCMOS 130 nm
Imaging chip for electromagnetic showers (FASER experiment at CERN)
Low hit rate application
Power Budget < 150 mW/cm^2
Periphery TDC with 150 ps bin

First prototype of sub-picosecond TDC based on a novel design.
Free running oscillator based on calibration during measurement

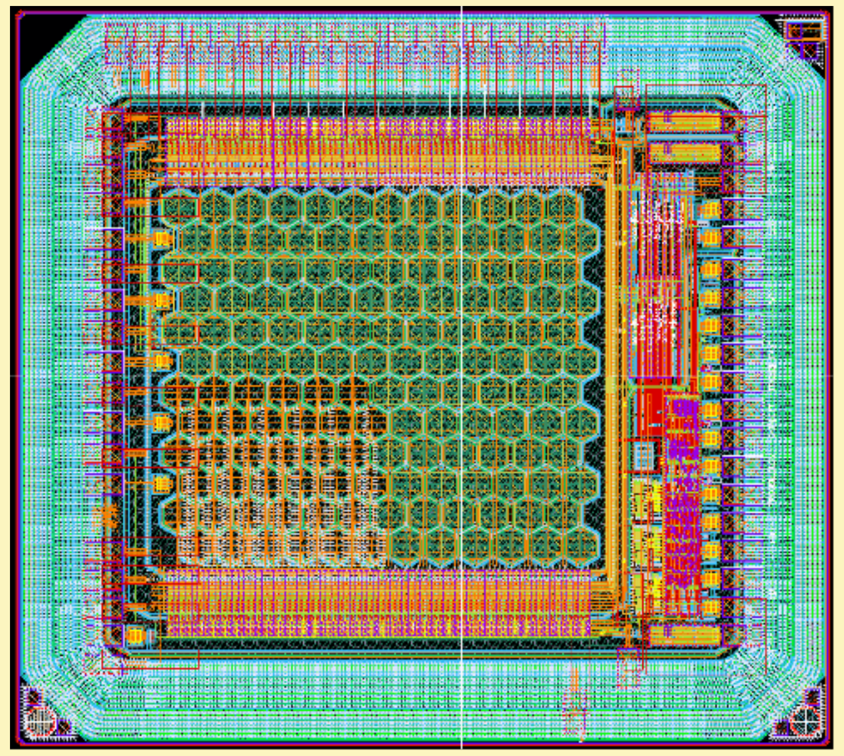
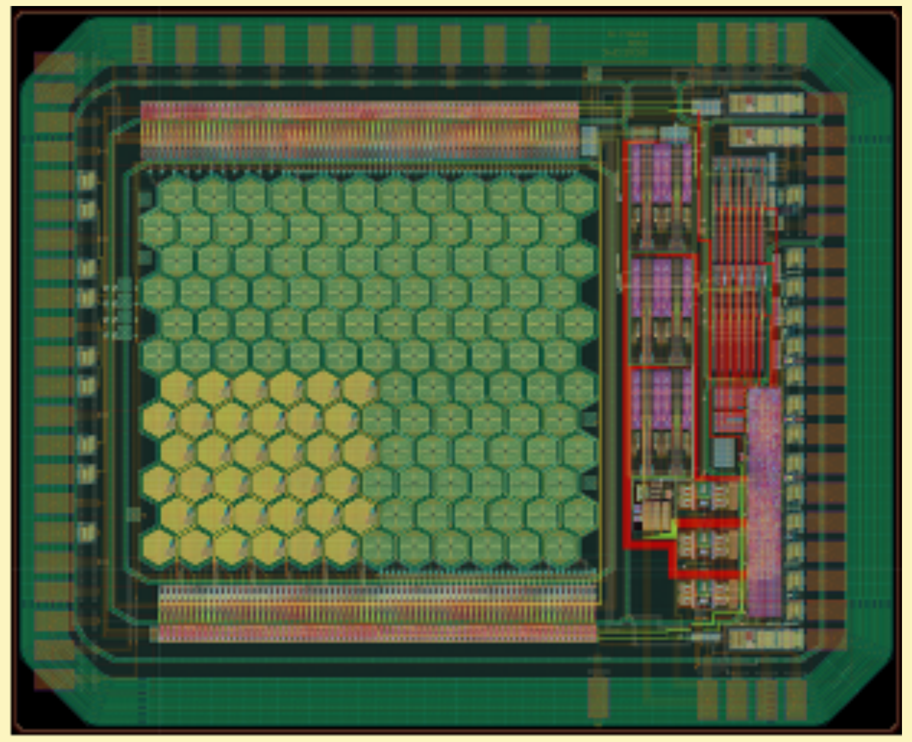
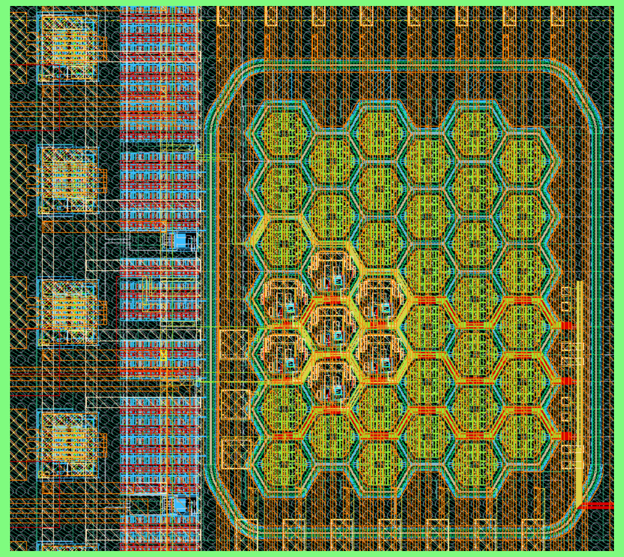
© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.



4 mW/channel



PicoAD Sensor Concept

Prototype 1 - 2020	Prototype 2 - 2022	Prototype 1 - 2023
		
36 ps	**20 ps**	**< 20 ps ?**
• Hexagonal pixels 100µm pitch • 30ps TDC +I/O logic • Analog channels	• Hexagonal pixels 100µm pitch • improved electronics • 50µm epitaxial layer (350Ωcm)	• Hexagonal pixels **50µm pitch** • improved electronics (4 times less power consumption)

BJT radiation hardness demonstrated

PicoAD
special wafers produced internally by IHP
(not optimised yet)

PicoAD Sensor Concept

PicoAD:

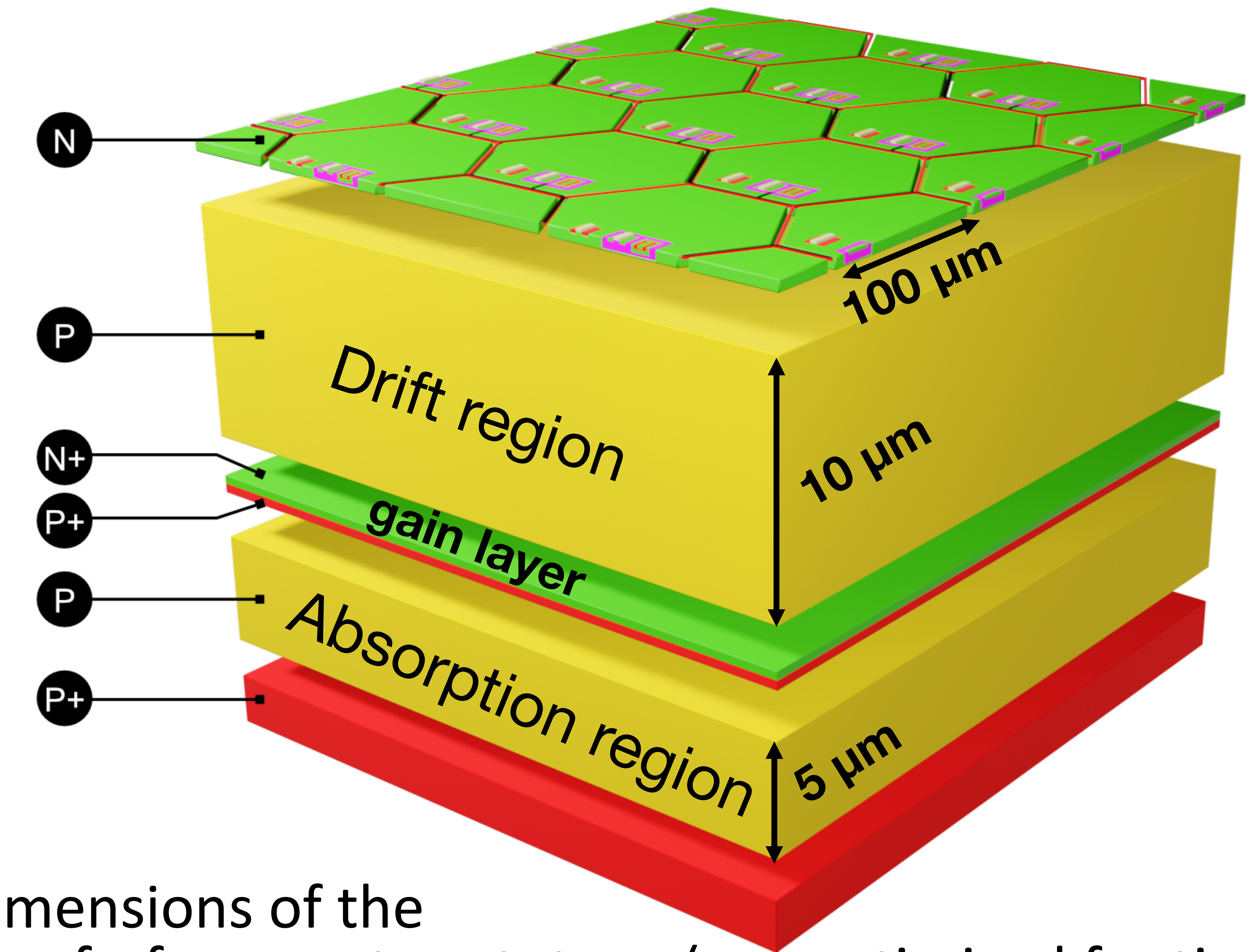
Multi-Junction **Picosecond-Avalanche Detector©**

with continuous and deep gain layer:

- De-correlation from implant size/geometry
  → **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  → **reduced charge-collection noise**
  (enhance timing resolution)

gain 60–70 for a MIP

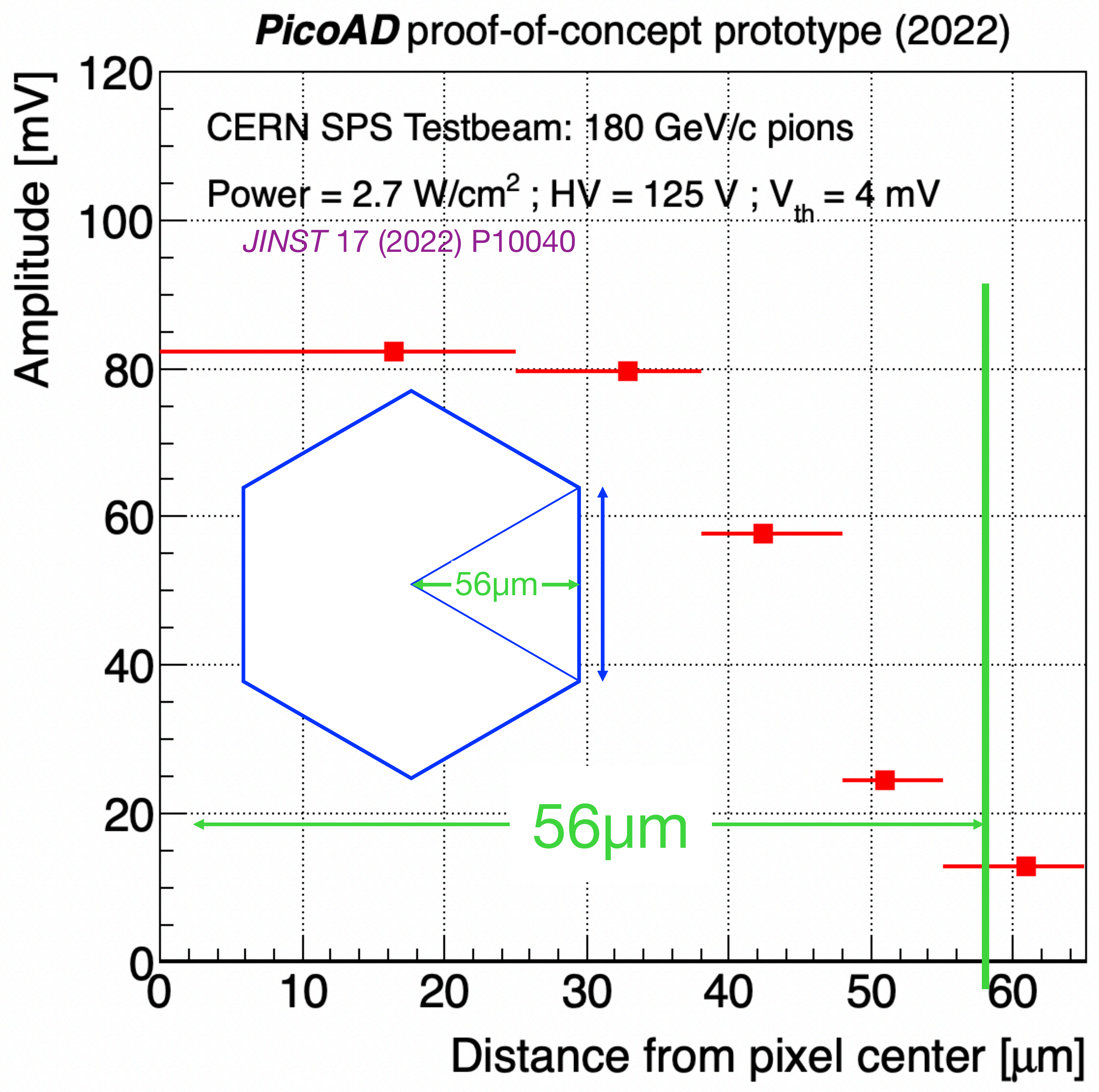
© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018



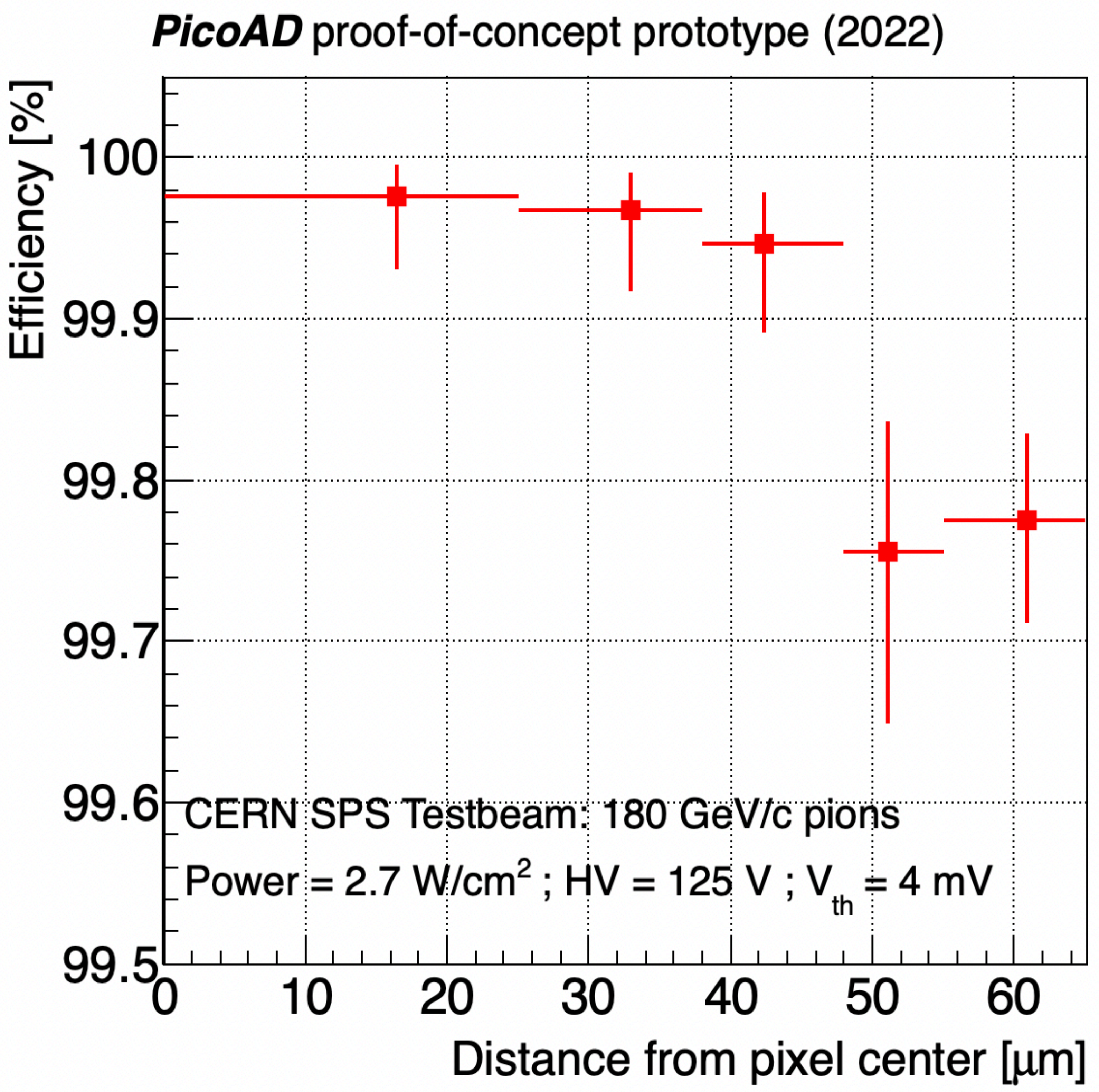
Dimensions of the proof-of-concept prototype (not optimised for timing)

PicoAD Testbeam results: dependence on position

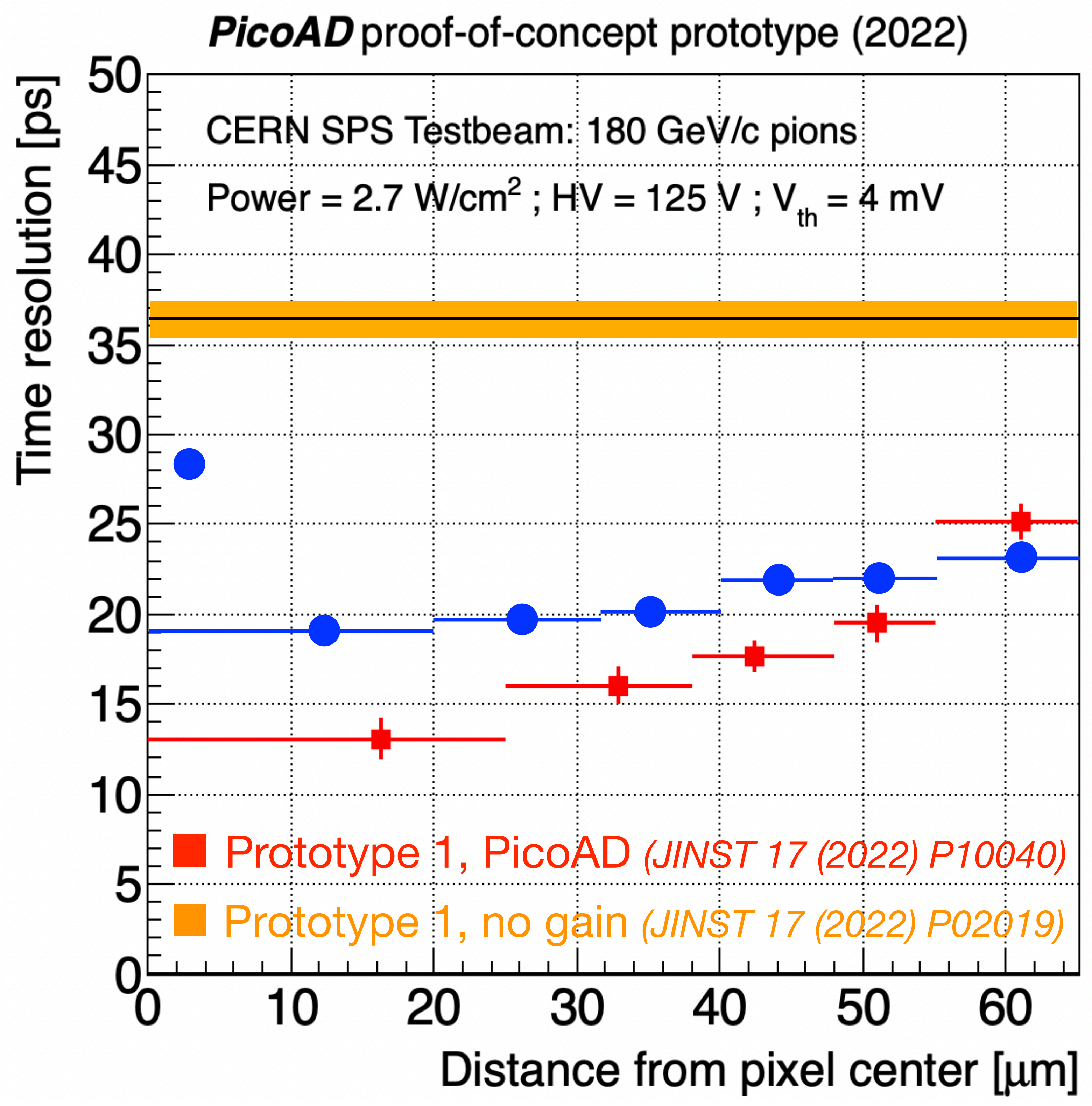
Signal MPV amplitude



Efficiency



Time resolution



PicoAD proof-of-concept: stronger dependence on hit position than for prototype 2

Summary and outlook

The PicoAD© sensor works. Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps : 13 ps** at center and **25 ps** at pixel edge (although sensor not yet optimized for timing)

Testbeam of second prototype ASIC, without gain layer, provided:

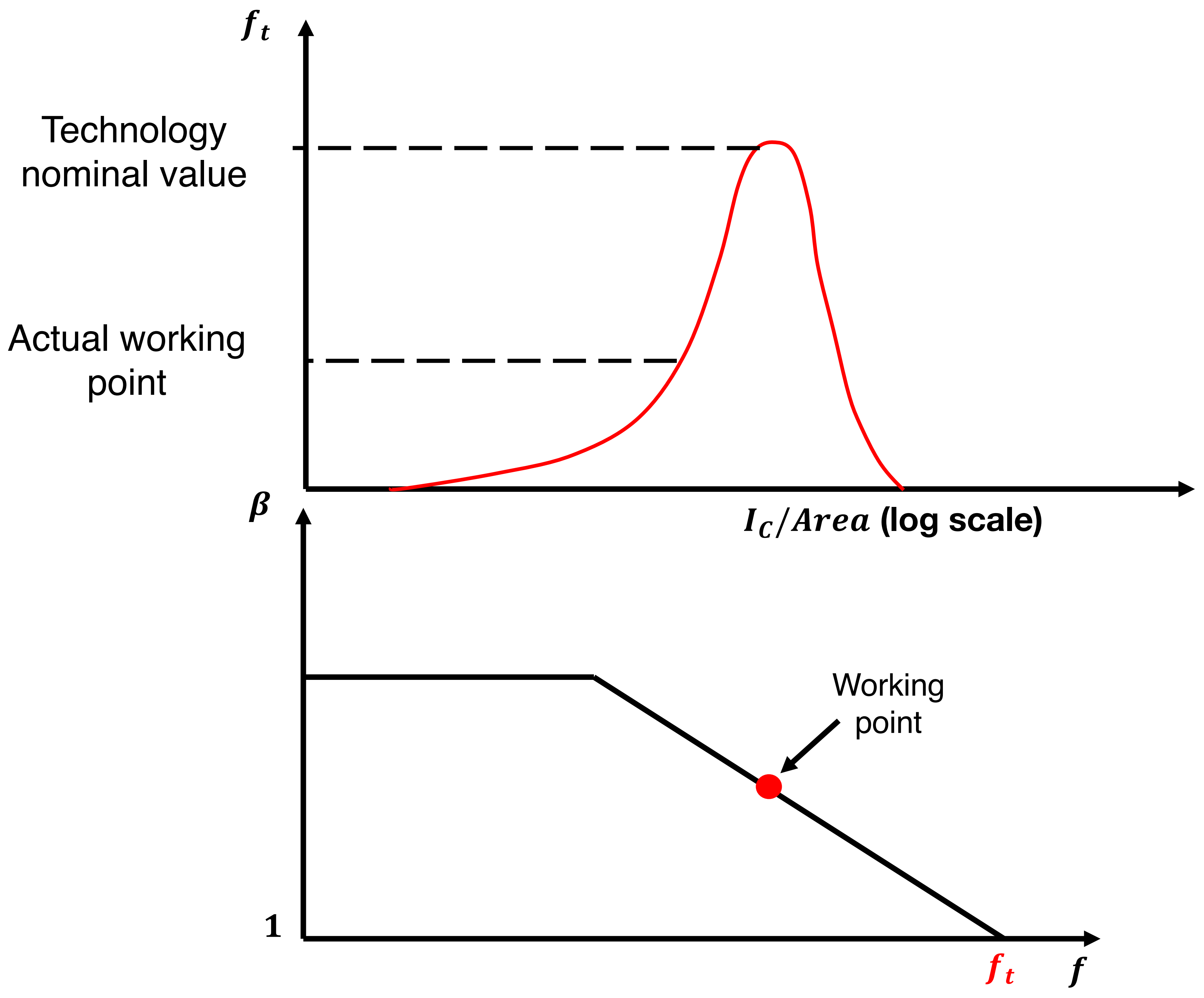
- **Efficiency = 99.8%** and **σ_t = (20.7 ± 0.3) ps**
- Laser measurement: down to 2.5 ps. Contributions from Landau noise studied
- Irradiation with protons (together with KEK) shows **radiation tolerance up to 10^{16} n_{eq}/cm^2**
- **PicoAD** sensor based on this prototype to be delivered in **September 2023**, optimised for timing with TCAD to achieve ≈10 ps (thicker drift layer; improved inter-pixel region)
- **Low power picosecond TDC** development for fully monolithic chip ongoing

Deliverable of MONOLITH ERC project:

- Full-reticle monolithic ASIC in **Summer 2025** with 50μm pitch and sub-10ps timing

Extra Material

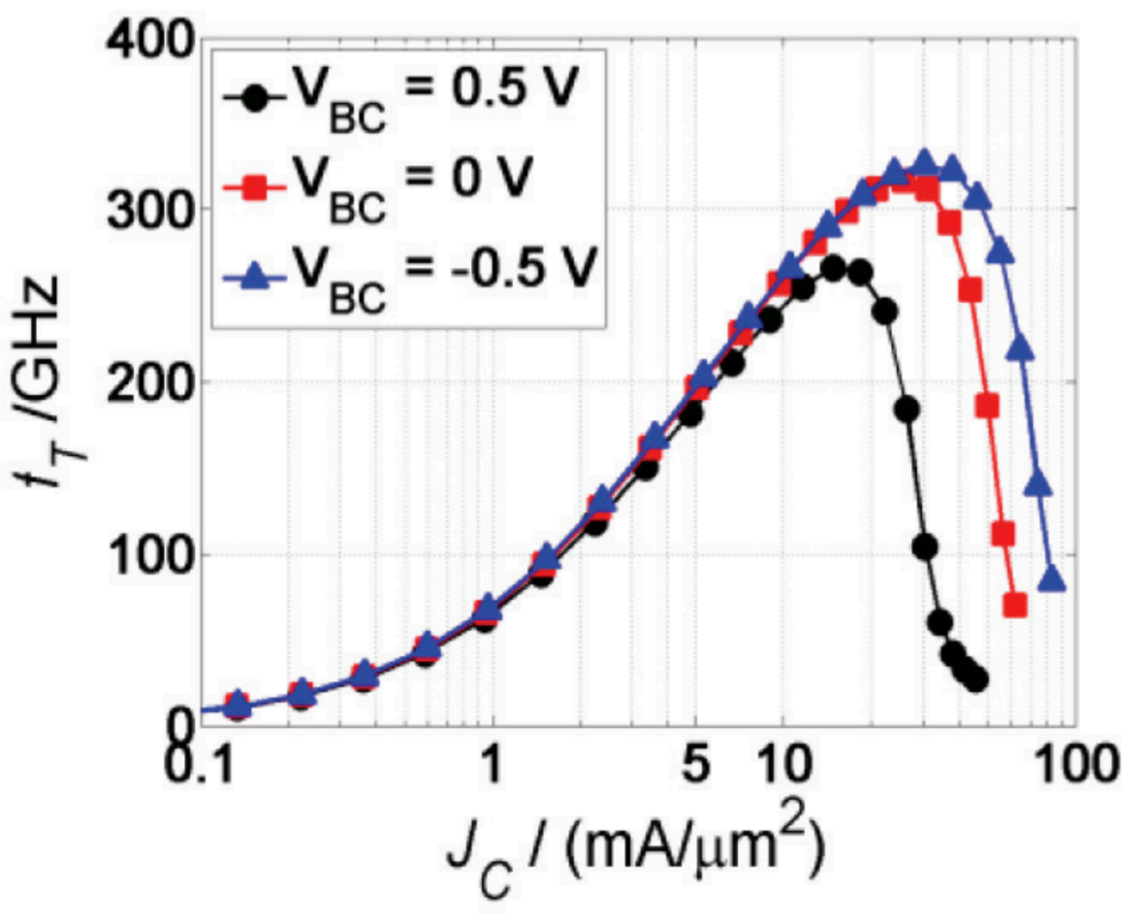
HBT Current gain and power consumption



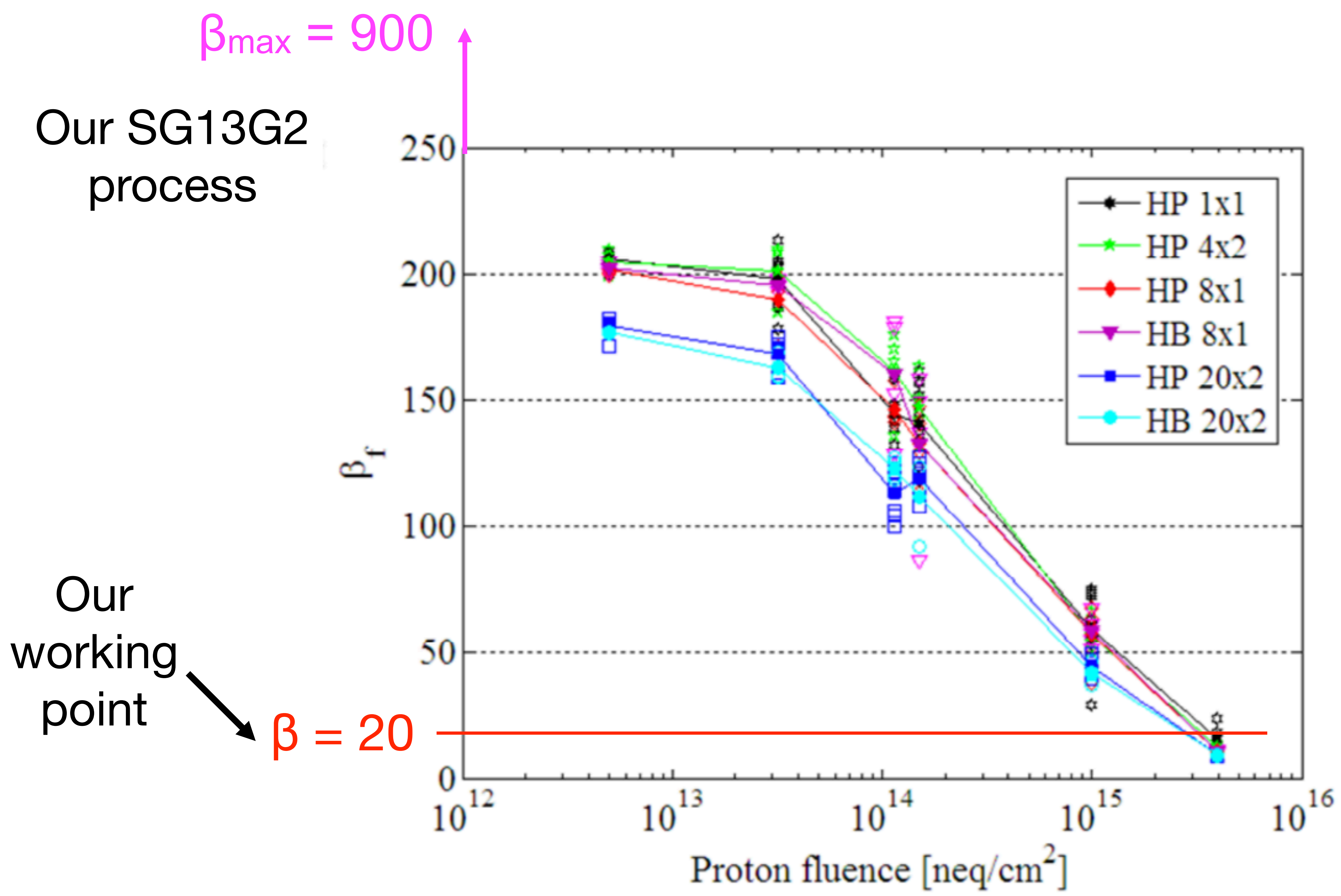
	$f_t = 10\ GHz$	$f_t = 100\ GHz$
β_{max} at 200 MHz	50	500
β_{max} at 1 GHz	10	100
β_{max} at 5 GHz	2	20

Trade-off: **ENC/σ_t** ⇔ **Power Consumption**

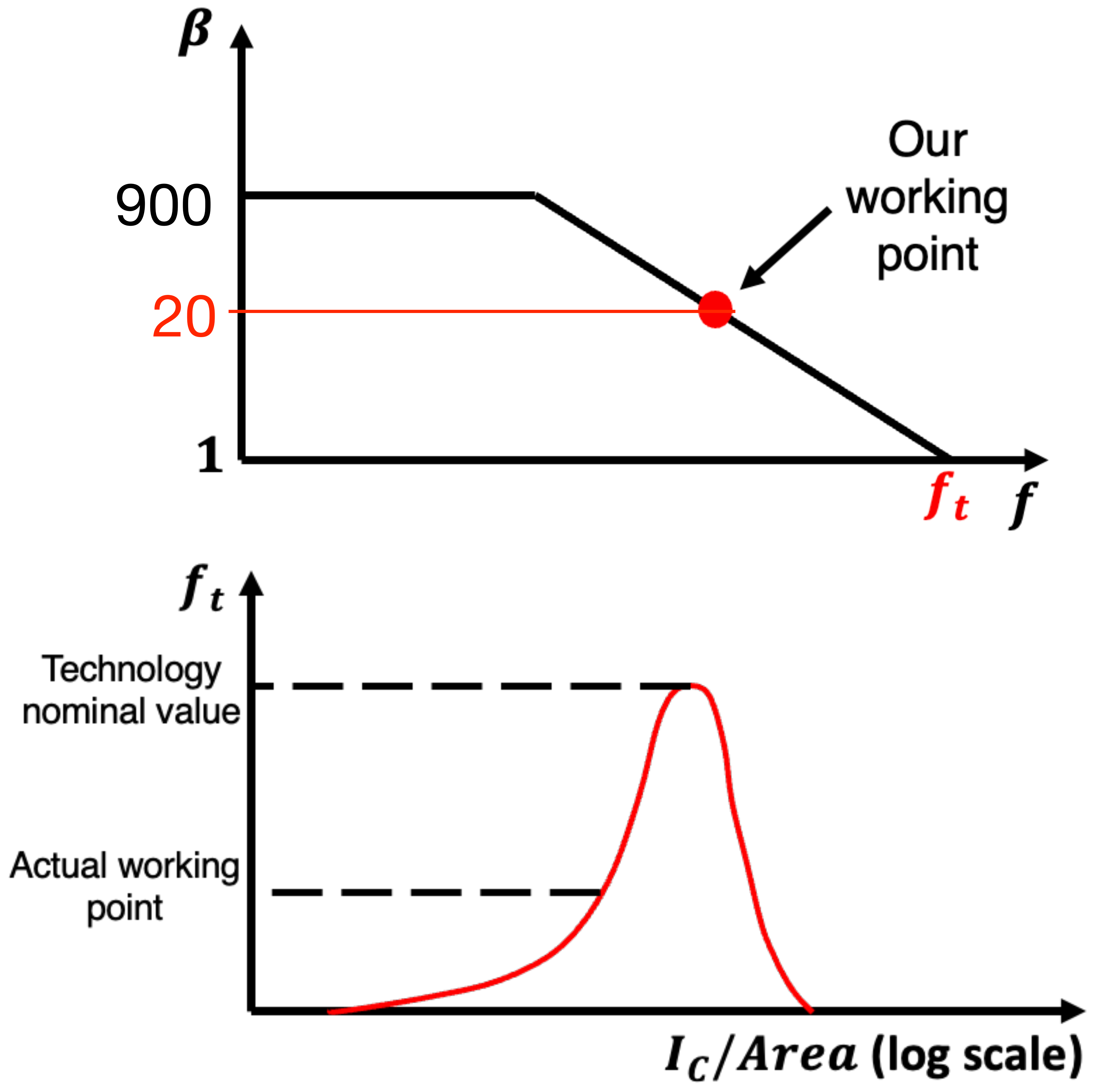
$f_t > 100\ GHz$ technologies are necessary for fast, low-power amplification.



Radiation hardness of SiGe HBTs

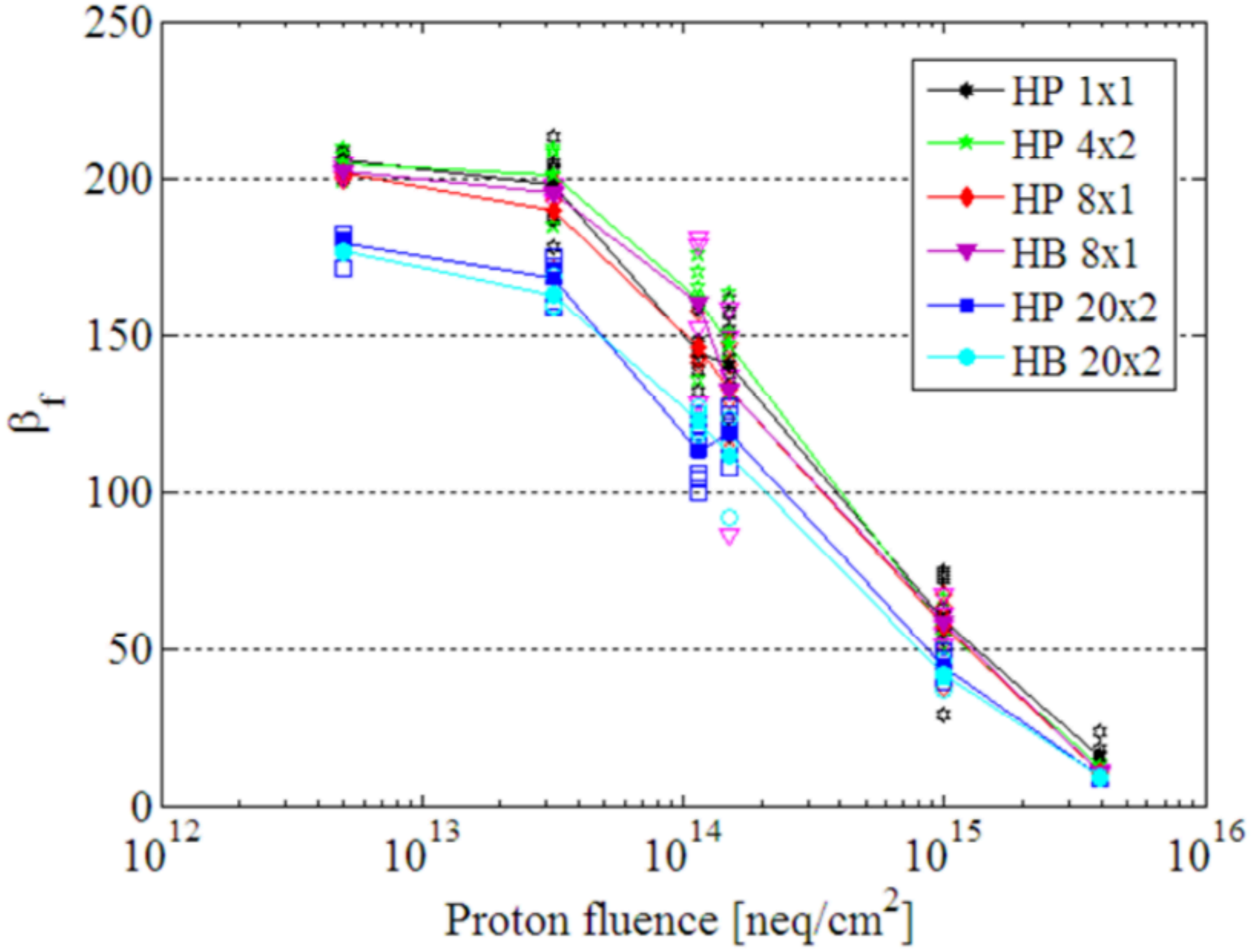


S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.



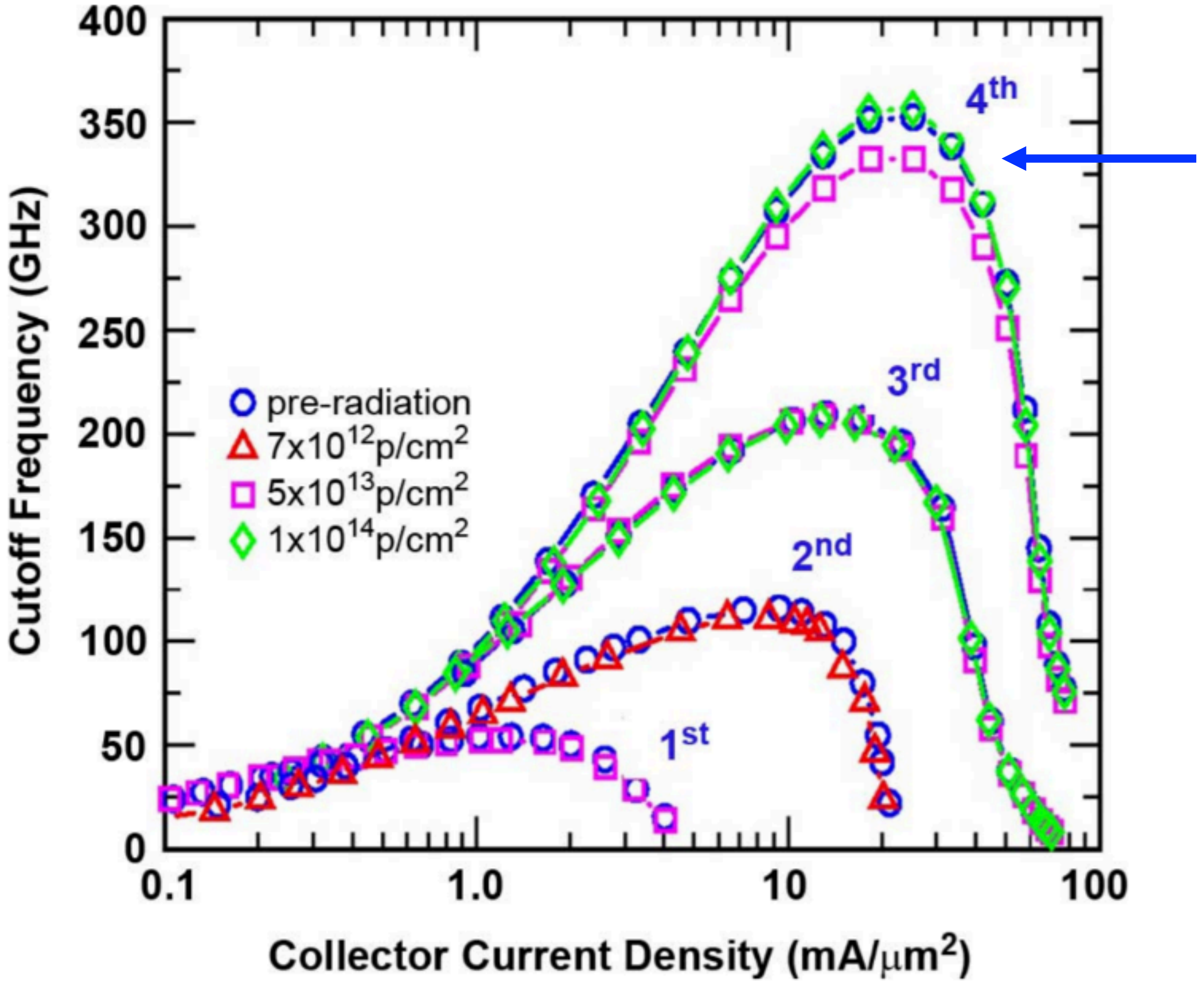
Radiation hardness of SiGe HBTs

DC characteristics



S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.

AC characteristics

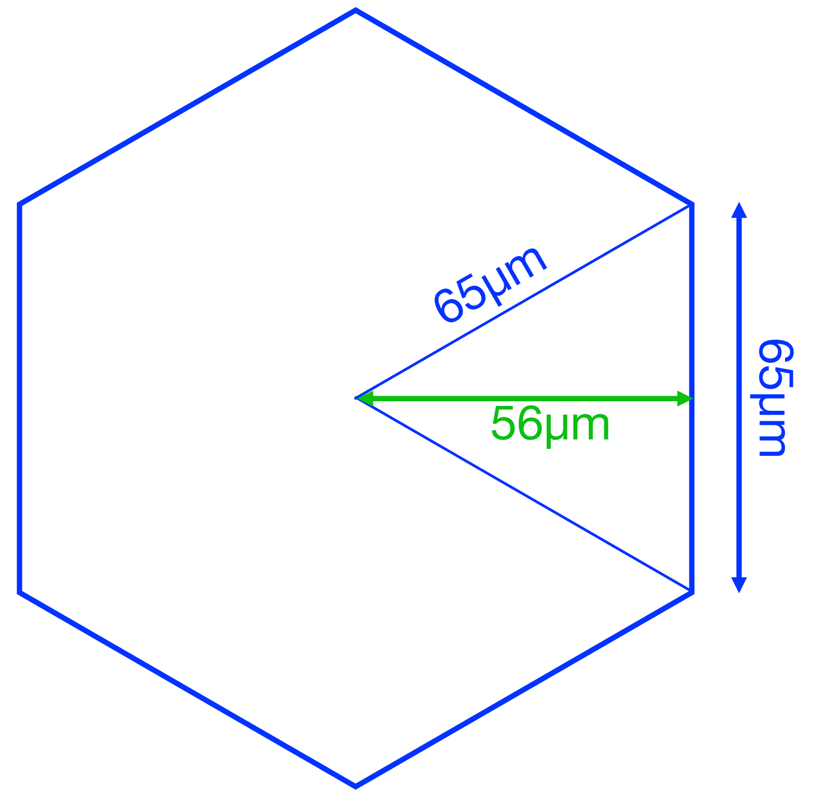


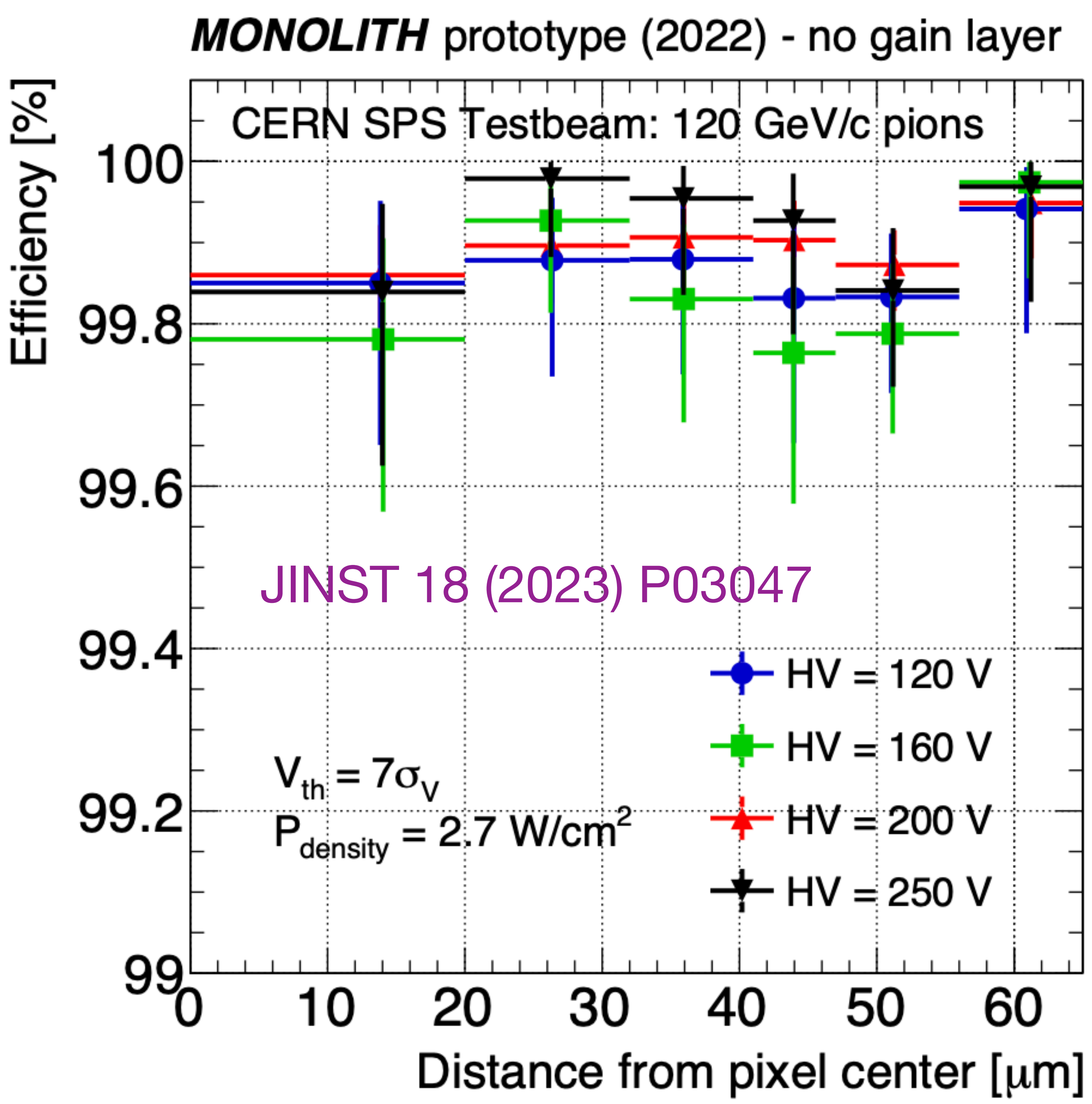
From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

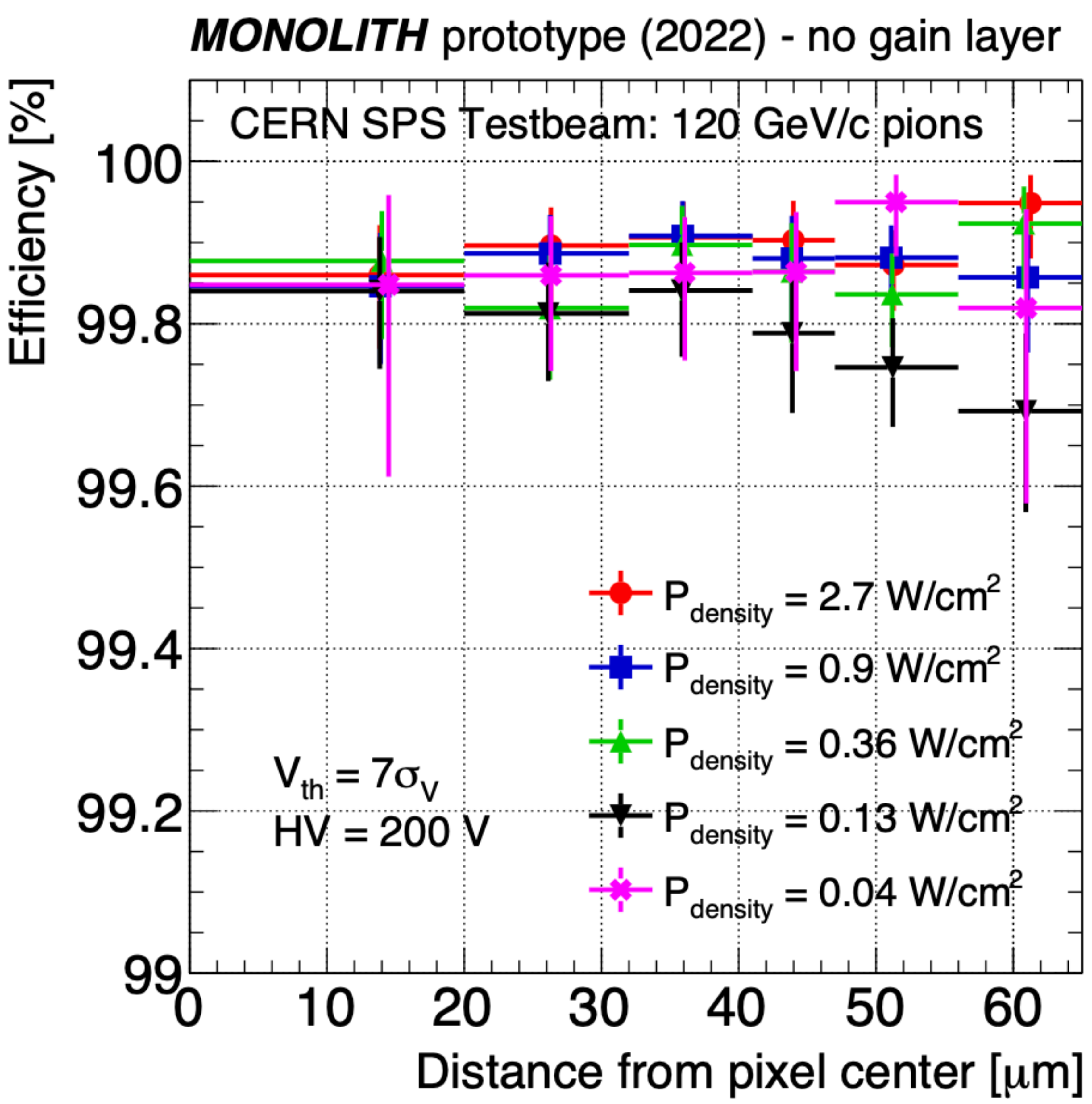
DC characteristics of SiGe BJT: **radiation hard** up to **10^{14} n_{eq}/cm^2**, well above yearly integrated doses of e^+e^- and $\mu^+\mu^-$ colliders.

AC characteristics: **still to be explored** beyond 10^{14} n_{eq}/cm^2

Monolith Prototype 2 – Efficiency vs Position

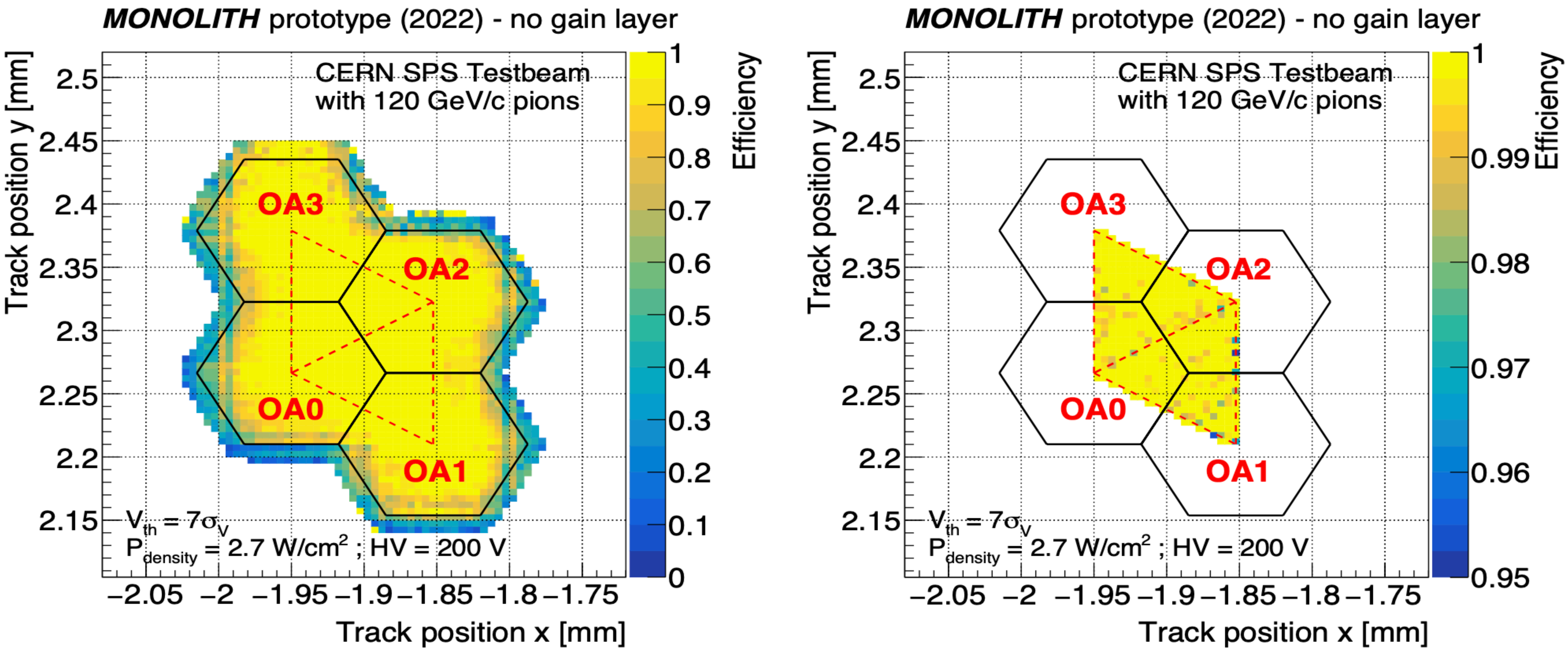






Efficiency ≈ **99.8%** even in the **inter-pixel region**, for all working points

2022 prototype — no gain layer



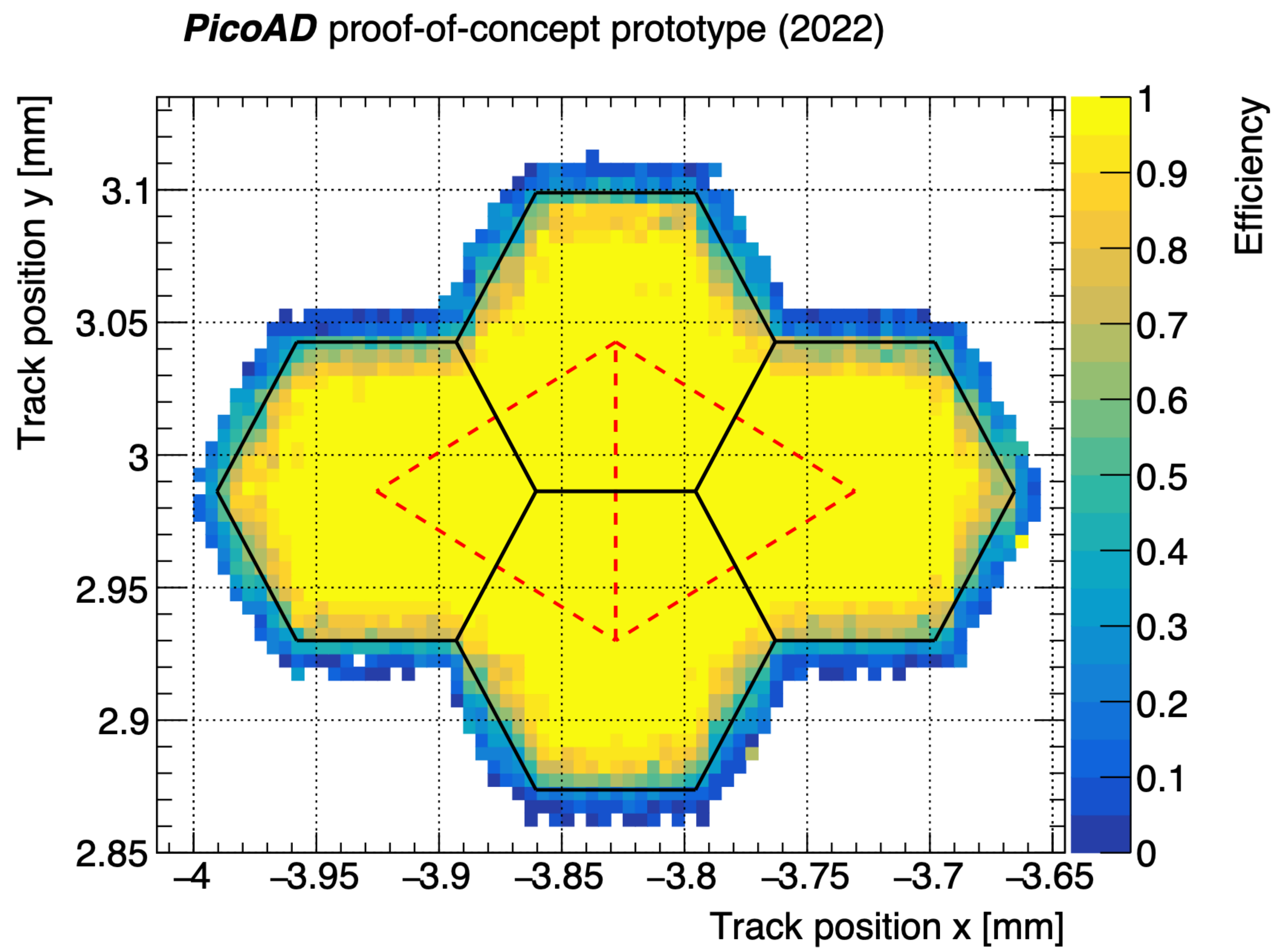
Efficiency at the external edges affected by the telescope resolution of 10 μm

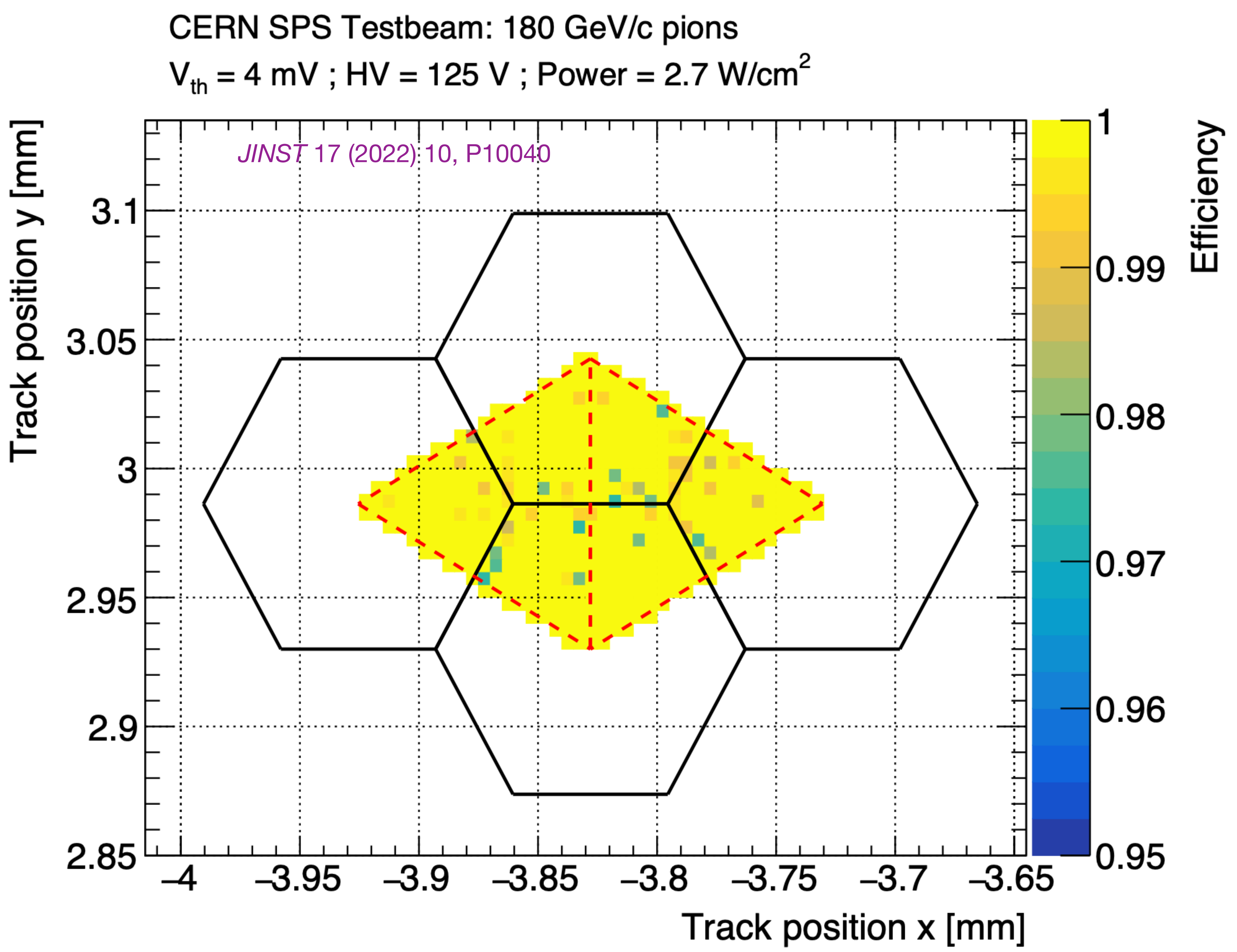
Full efficiency (yellow is 99.8%) in the two triangles unaffected by telescope resolution

$P_{density}$ [W/cm^2]	σ_V [mV]	σ_{scope} [mV]	A_q [mV/fC]	ENC [electrons]
2.7	1.45 ± 0.02	0.39 ± 0.01	89.4 ± 1.1	93 ± 2
0.9	1.06 ± 0.02	0.39 ± 0.01	67.4 ± 0.8	84 ± 1
0.36	0.89 ± 0.01	0.39 ± 0.01	45.3 ± 0.8	97 ± 2
0.13	0.58 ± 0.01	0.16 ± 0.01	26.6 ± 0.5	125 ± 5
0.04	0.67 ± 0.01	0.16 ± 0.01	27.0 ± 0.5	145 ± 8

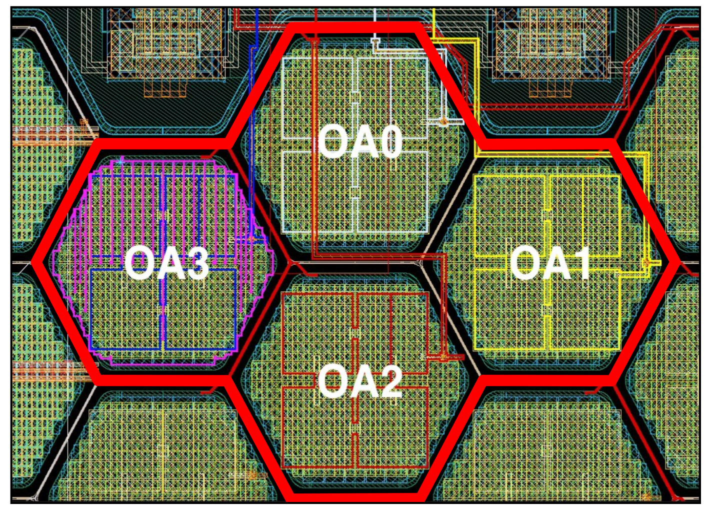
Table 1. Charge gain and ENC measured with a ^{55}Fe source at five different values of the front-end power density. The standard deviations of the voltage noise and of the oscilloscope noise used for the calculation of the ENC are also reported.

Testbeam results: Detection Efficiency





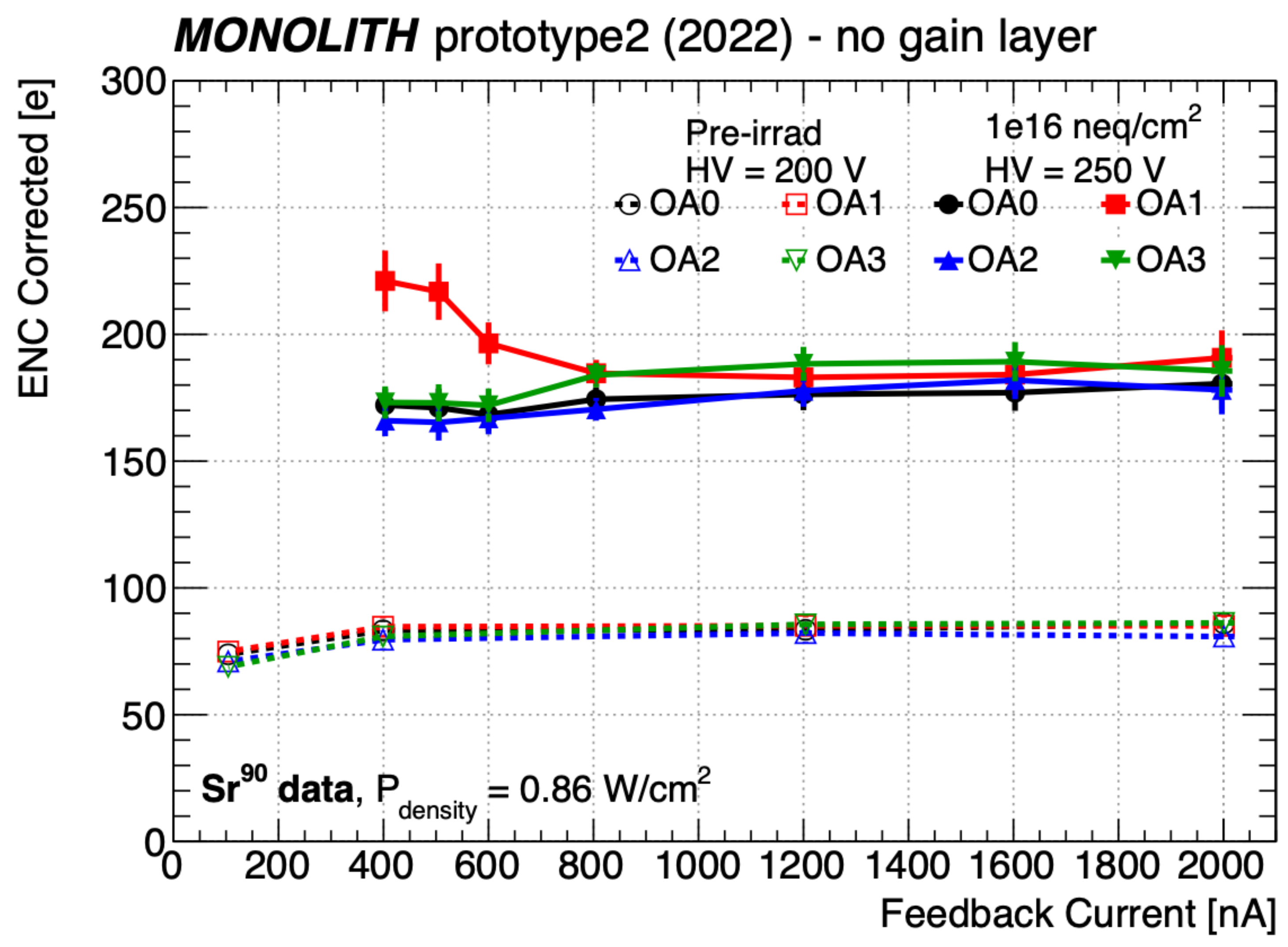
Apparent degradation at the external edges of the four pixels is due to the telescope pointing resolution of ≈10 μm

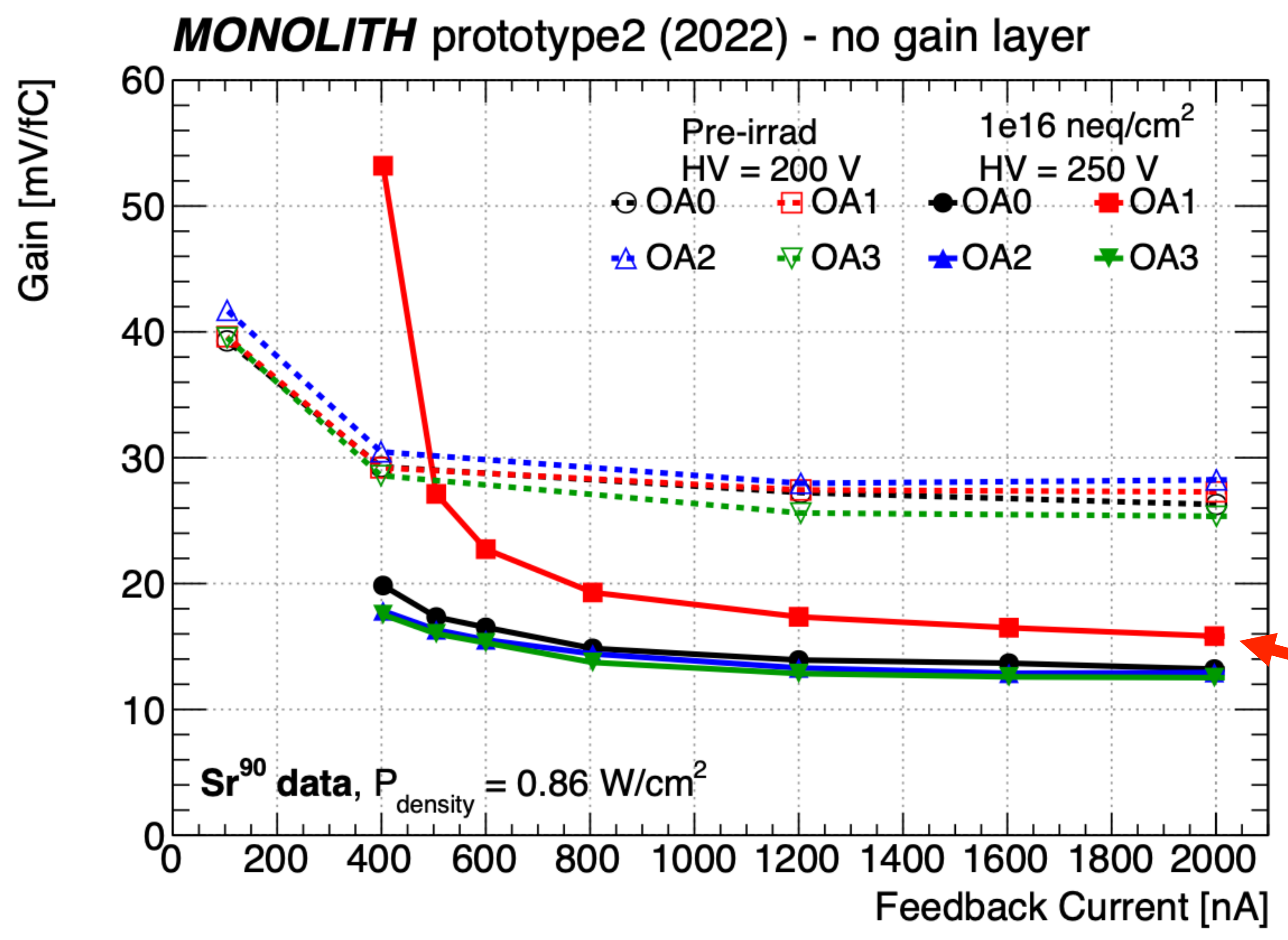


Selection of two **triangles**:

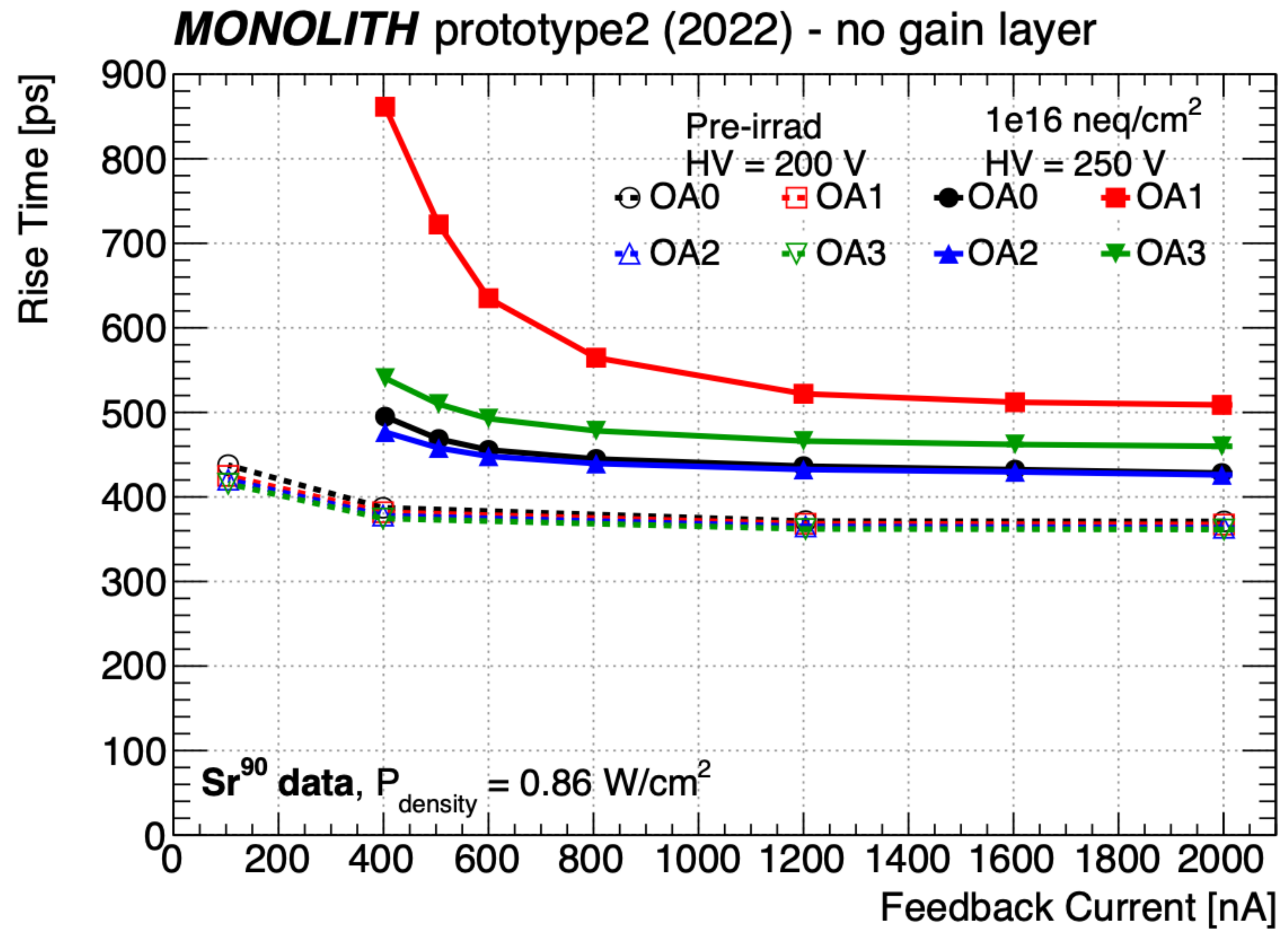
- representative of a whole pixel
- **unbiased by telescope resolution**

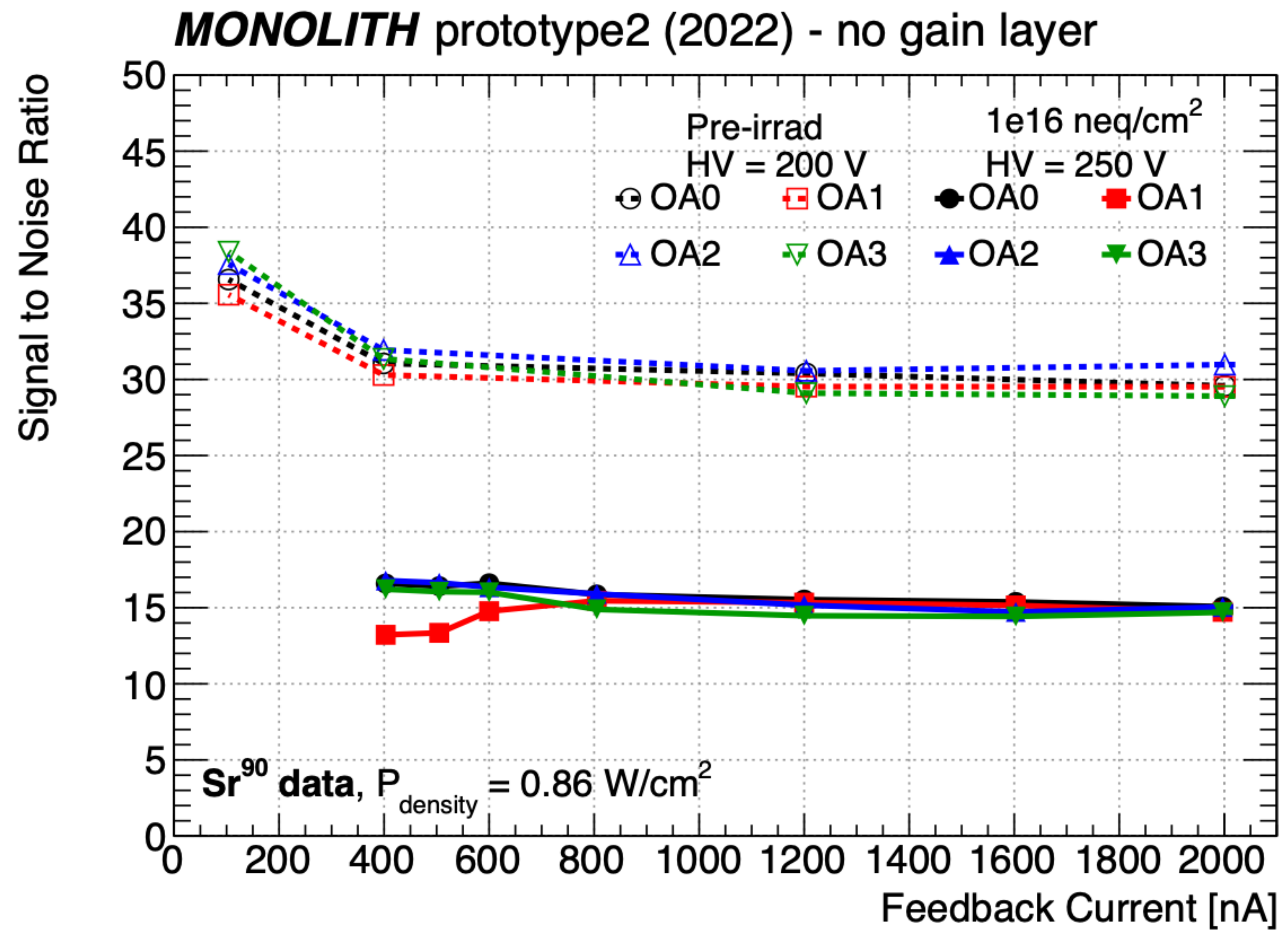
Radiation hardness of SiGe HBTs





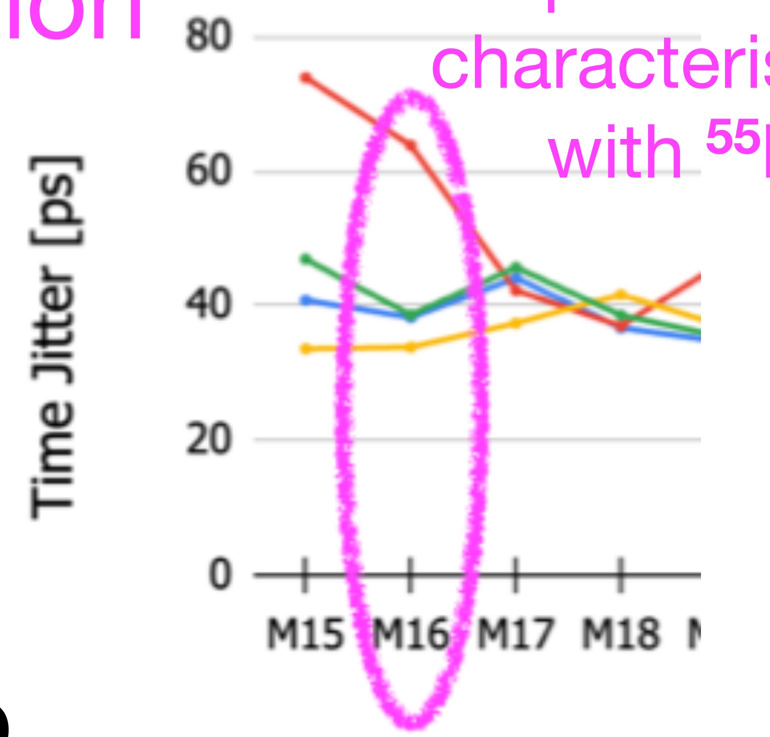
Characterisation with ^{90}**Sr** source of the four pixels of the board M16 irradiated at **10^{16} n_{eq}/cm^2**





The different behaviour of pixel OA0 was present also before irradiation

pre-irrad. characterisation with ^{55}**Fe**



probably due to electronics mismatch
(will be reduced in future submission)

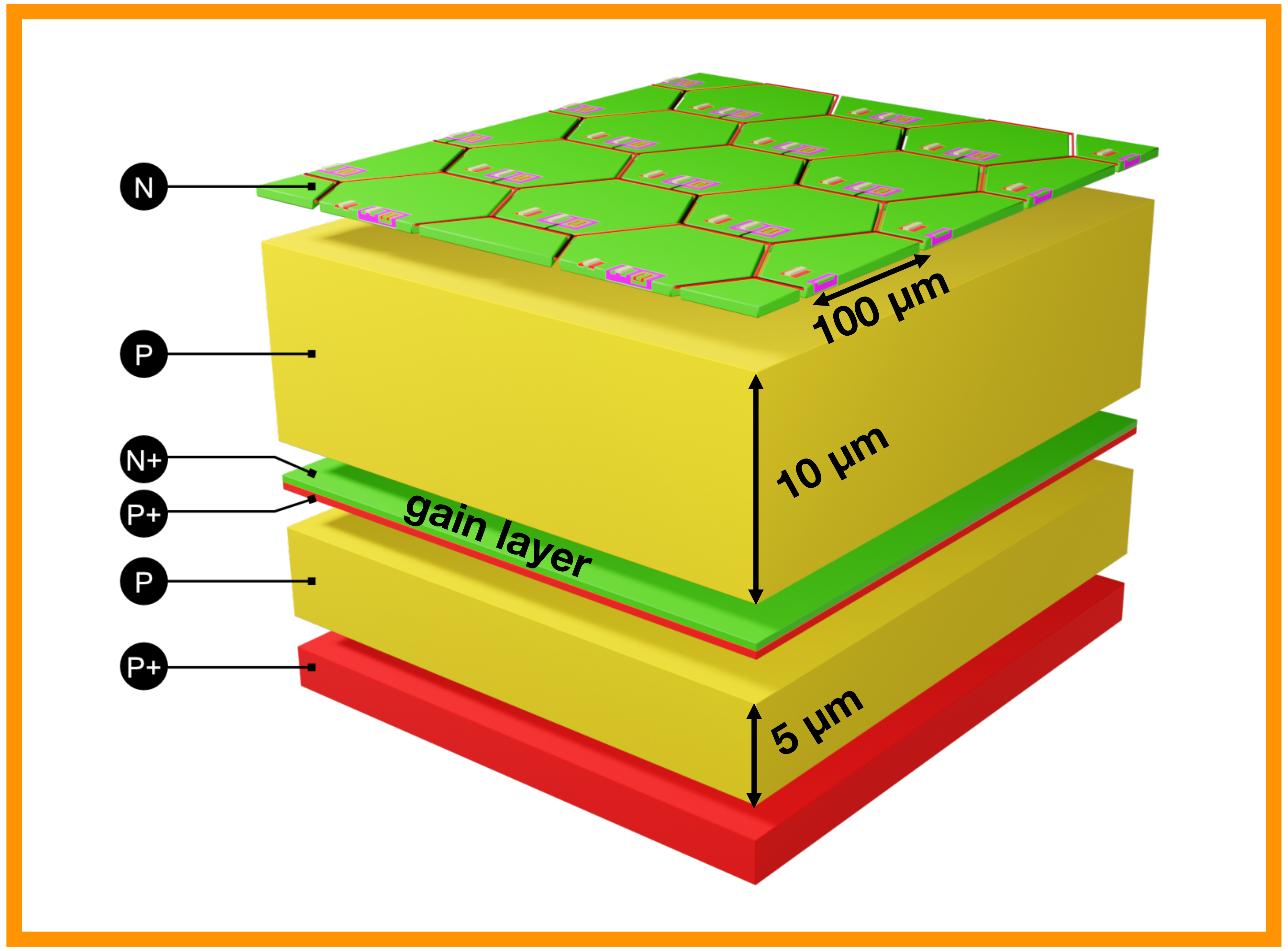
PicoAD Sensor Concept

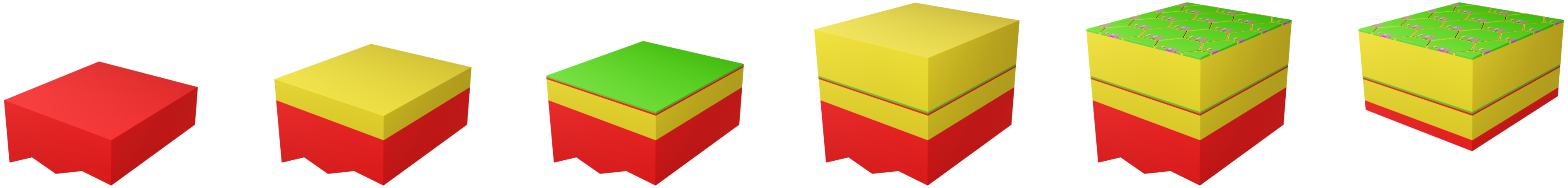
Multi-Junction **Picosecond-Avalanche Detector**

with continuous and deep gain layer:

- De-correlation from implant size/geometry
  → **high pixel granularity and full fill factor**
  (high spatial resolution)
- Only small fraction of charge gets amplified
  → **reduced charge-collection noise**
  (enhance timing resolution)

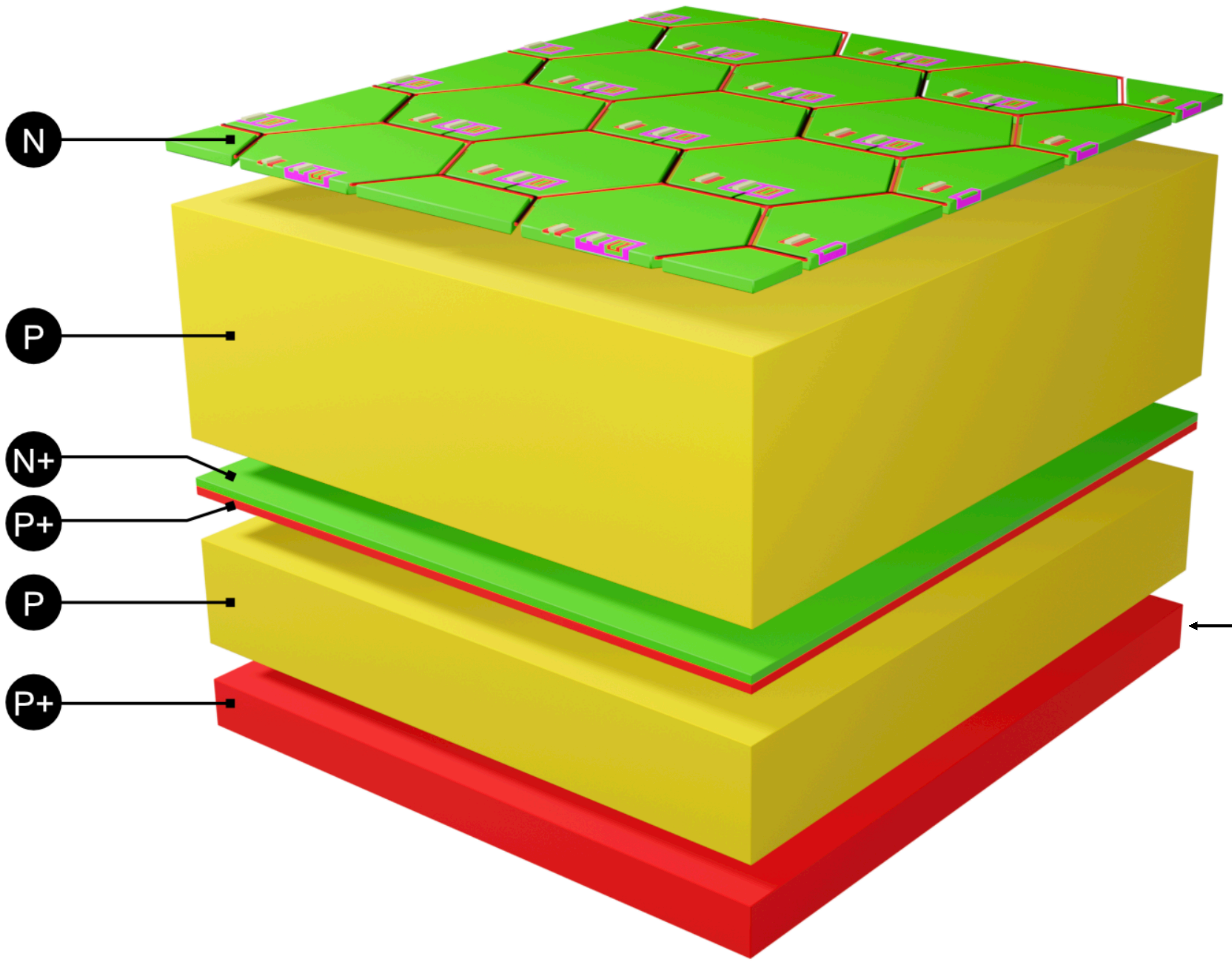
$$\sigma_T \cong \frac{t_{rise}}{Signal/_{Noise}} \cong \frac{ENC}{I_{Ind}}$$





Step 1 Step 2 Step 3 Step 4 Step 5 Step 6

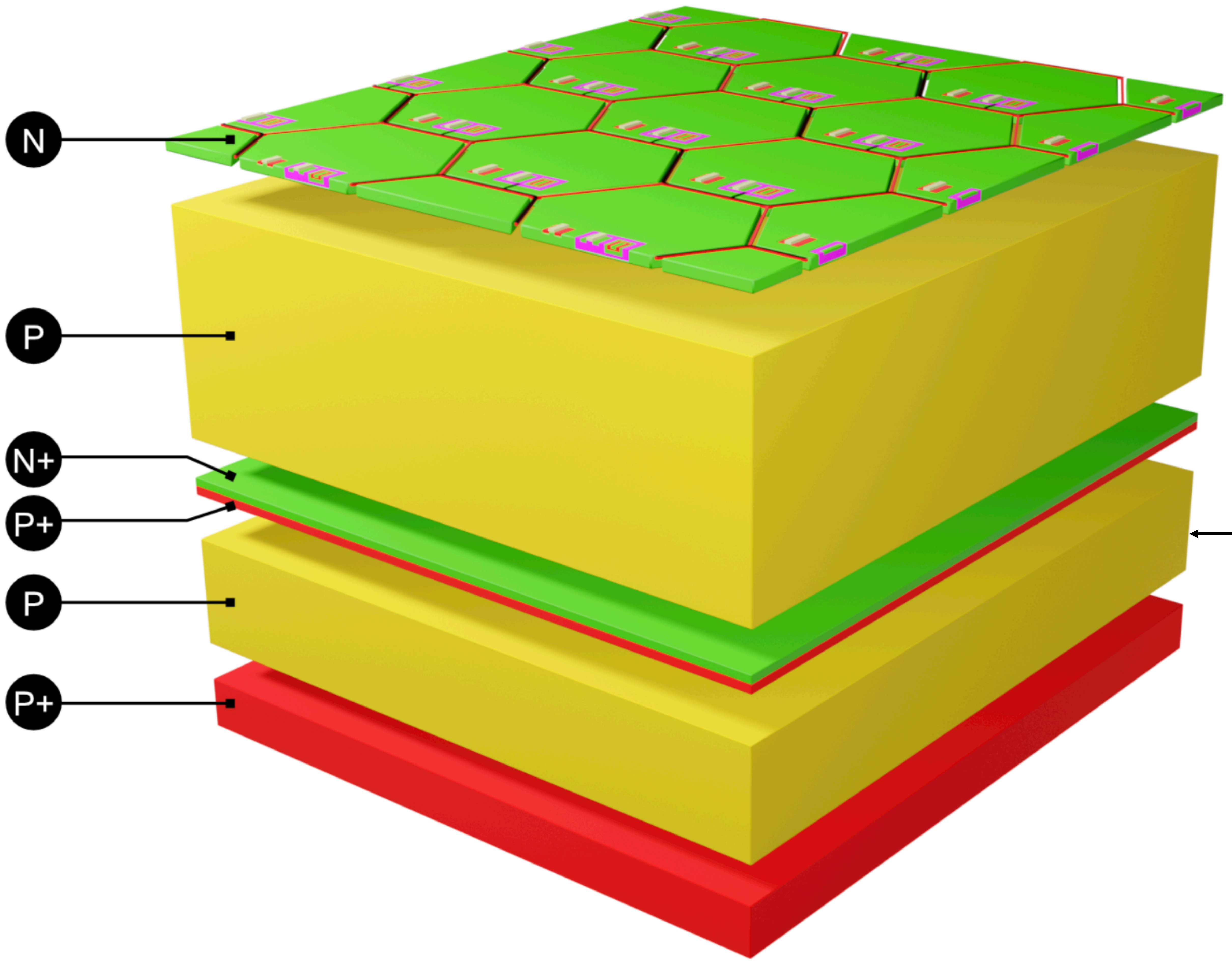
PicoAD Sensor Concept



Sensor growth on low resolitivity wafers:

1. **No dedicated backside processing** needed
2. Low resistivity important to end depleted active region of sensor and minimise coupling to FE integrated in pixel

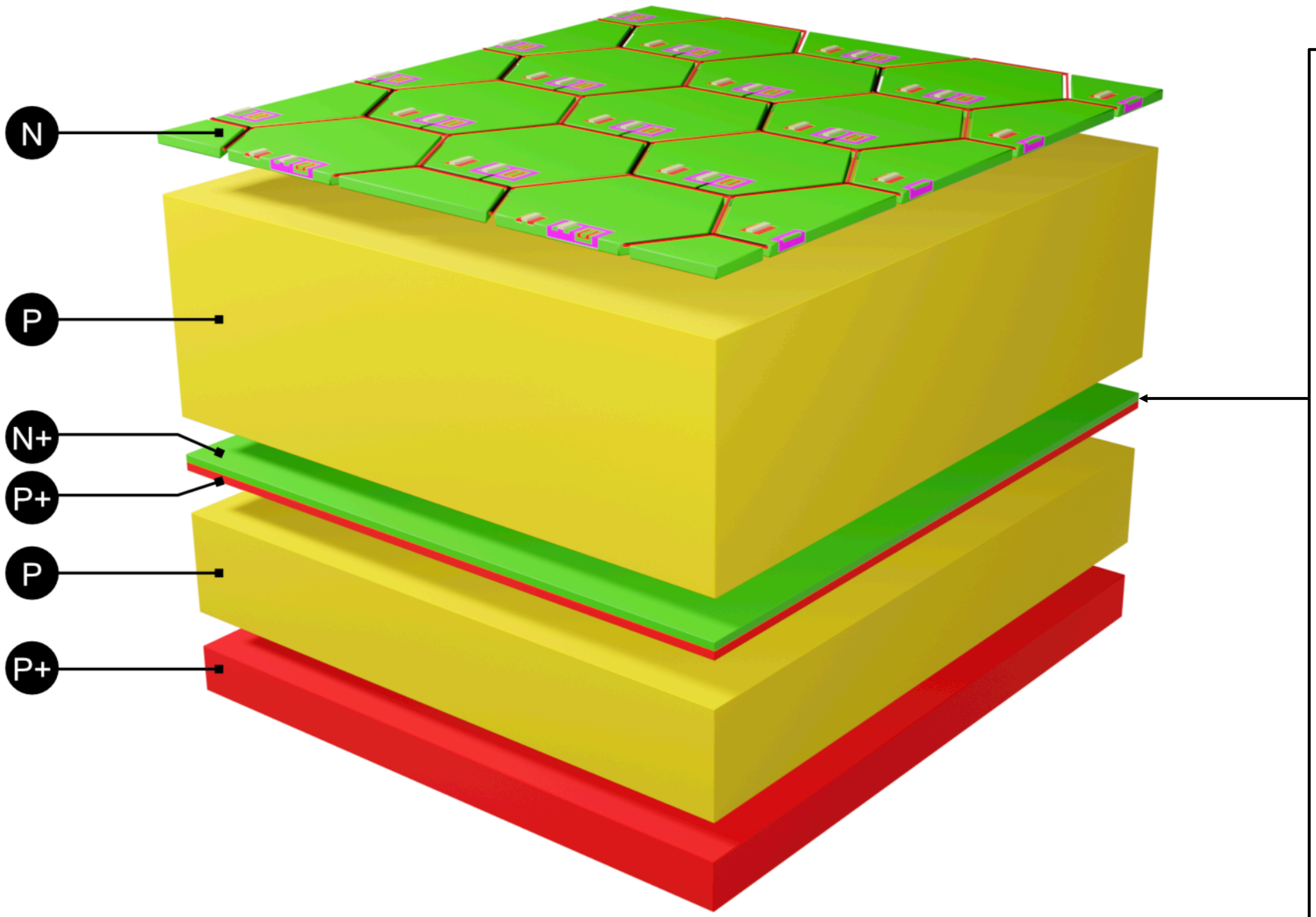
PicoAD Sensor Concept



Thin 'absorbtion region', 1st epitaxial layer:

1. Region where primary charge charge drifting towards topside gets amplified is produced
2. Thin layer (~5µm) to **minimise charge collection noise**

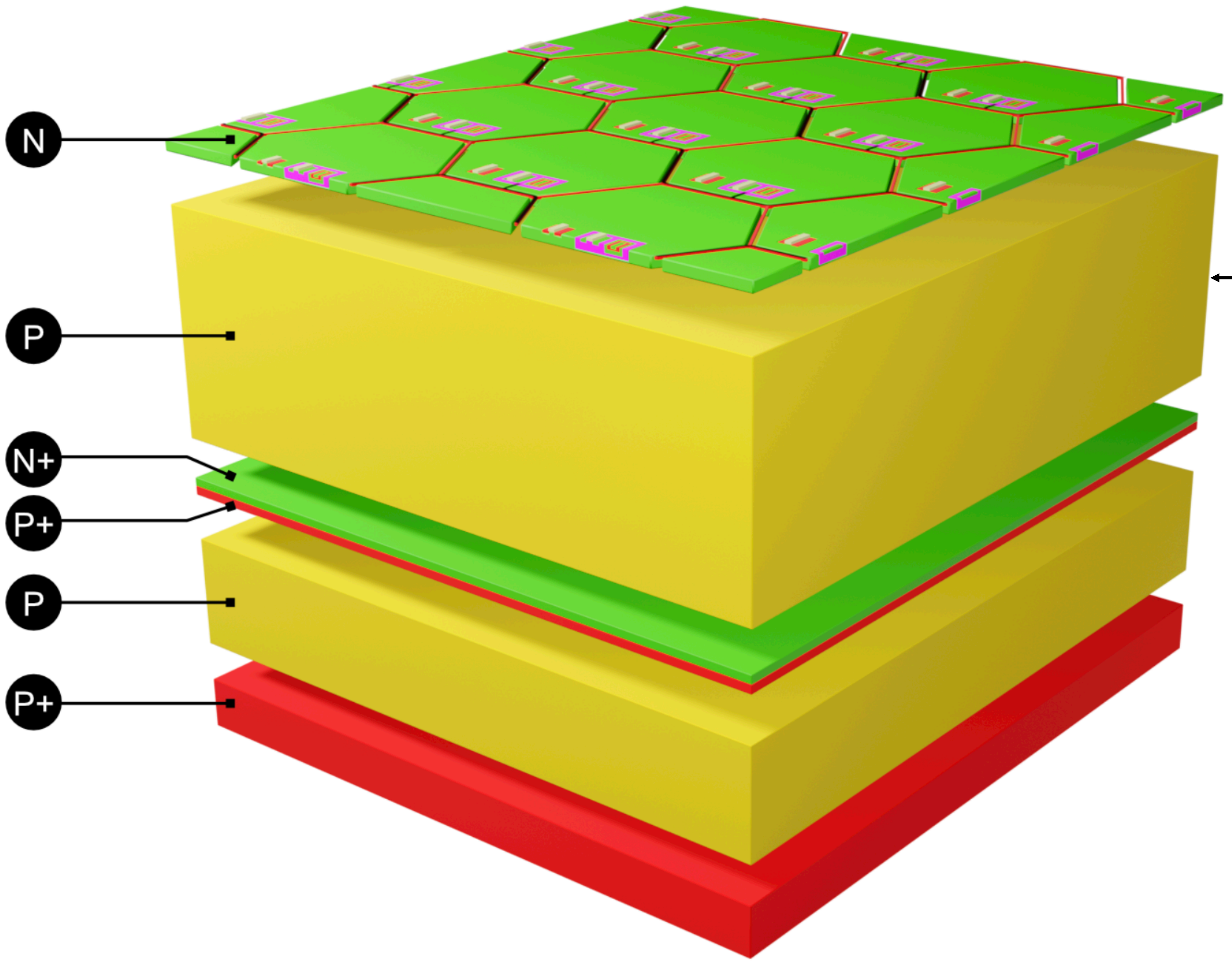
PicoAD Sensor Concept



Thin and uniform deep gain layer:

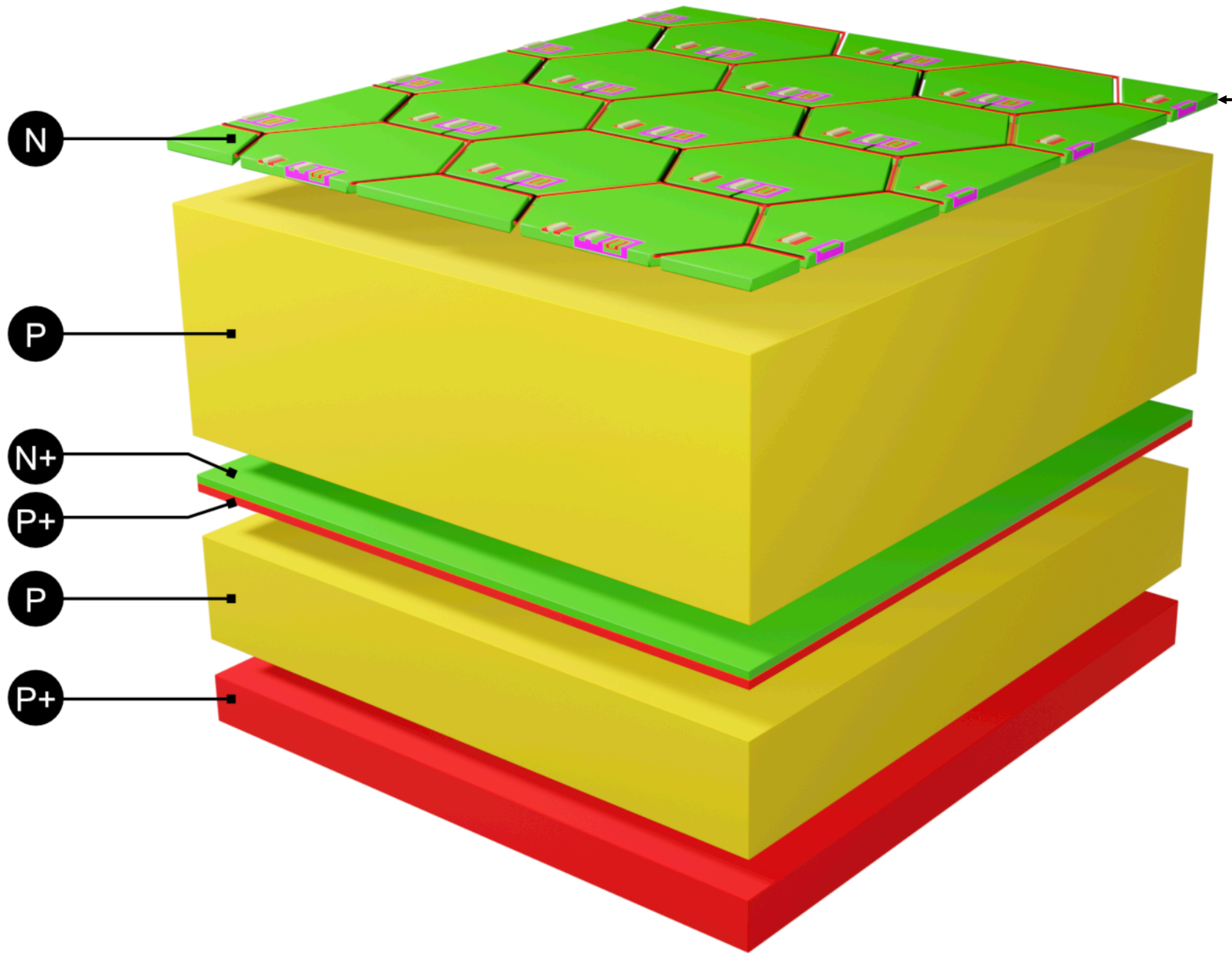
- Same doping of gain layer over full pixel cell (full ‘fill-factor’):
  - **Uniform gain** and minimisation of pixel edge effects
- Gain layer physically seperated from pixel implant:
  - Can decrease absorbtion region to minimise charge collection noise without increasing sensor capacitance (coupling to backside substarte p+)
  - Can integrate FE electronics inside pixel implant (**fully monolithic CMOS**)

PicoAD Sensor Concept



Thicker 'drift region', 2nd epiaxial layer:

- Constrains:
  - Not too thick:
    - Maximise weighting field ($\propto$ 1/depletion)
    - Maximise drift field
  - Not too thin:
    - Minimize capacitance
    - Minimize impact of pixel implants on gain layer uniformity

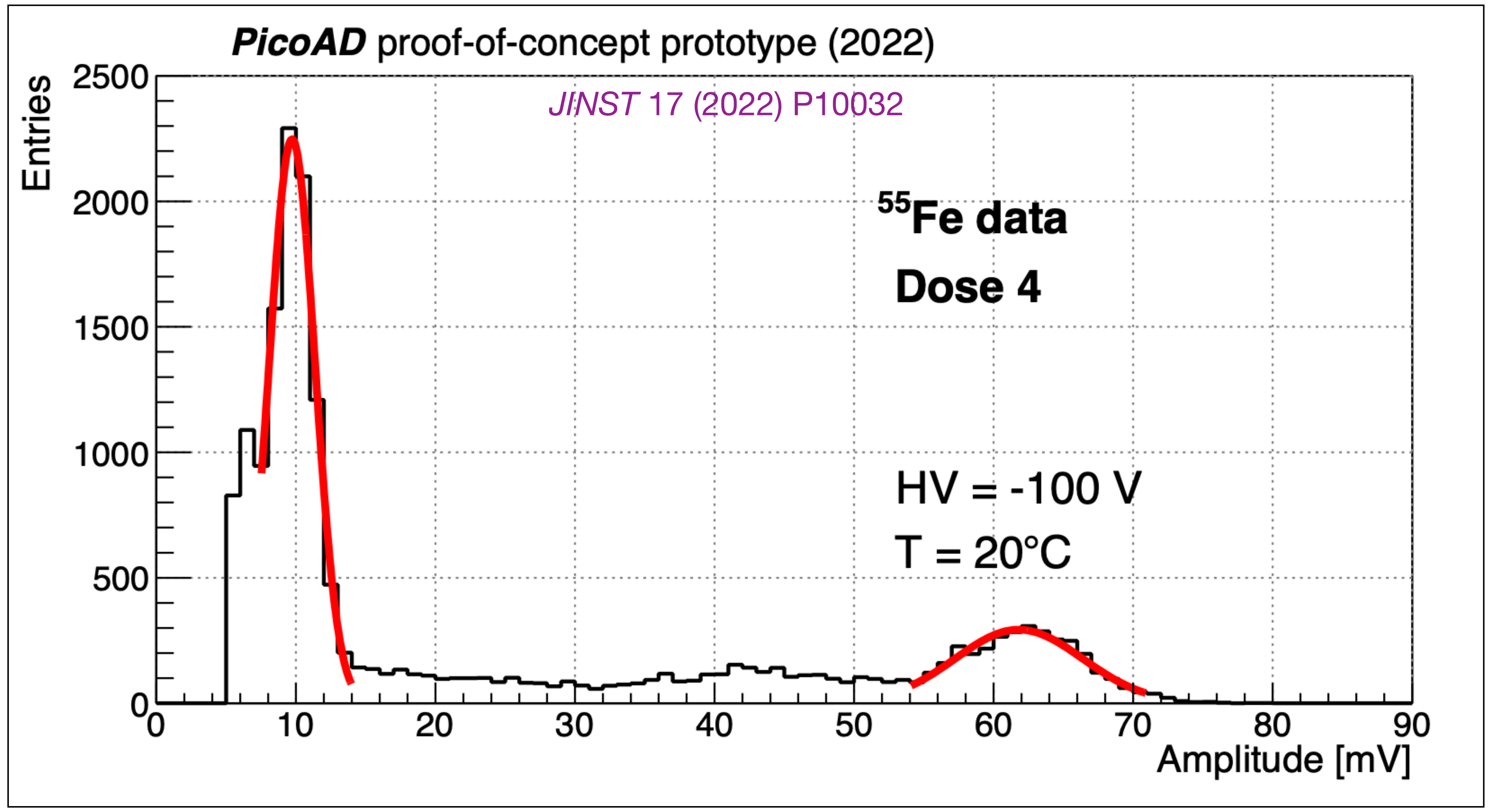


Fully monolithic CMOS processing:

- Implemented in **large collection electrode design to maximise weighting** field over full pixel cell
- **Pixel implant size can be minimised** while maintaining gain layer uniformity!
- **Hexagonal design to minimise edge effects** (impact on gain layer + high field breakdown between pixels)

Gain Measurement with ^{55}Fe source

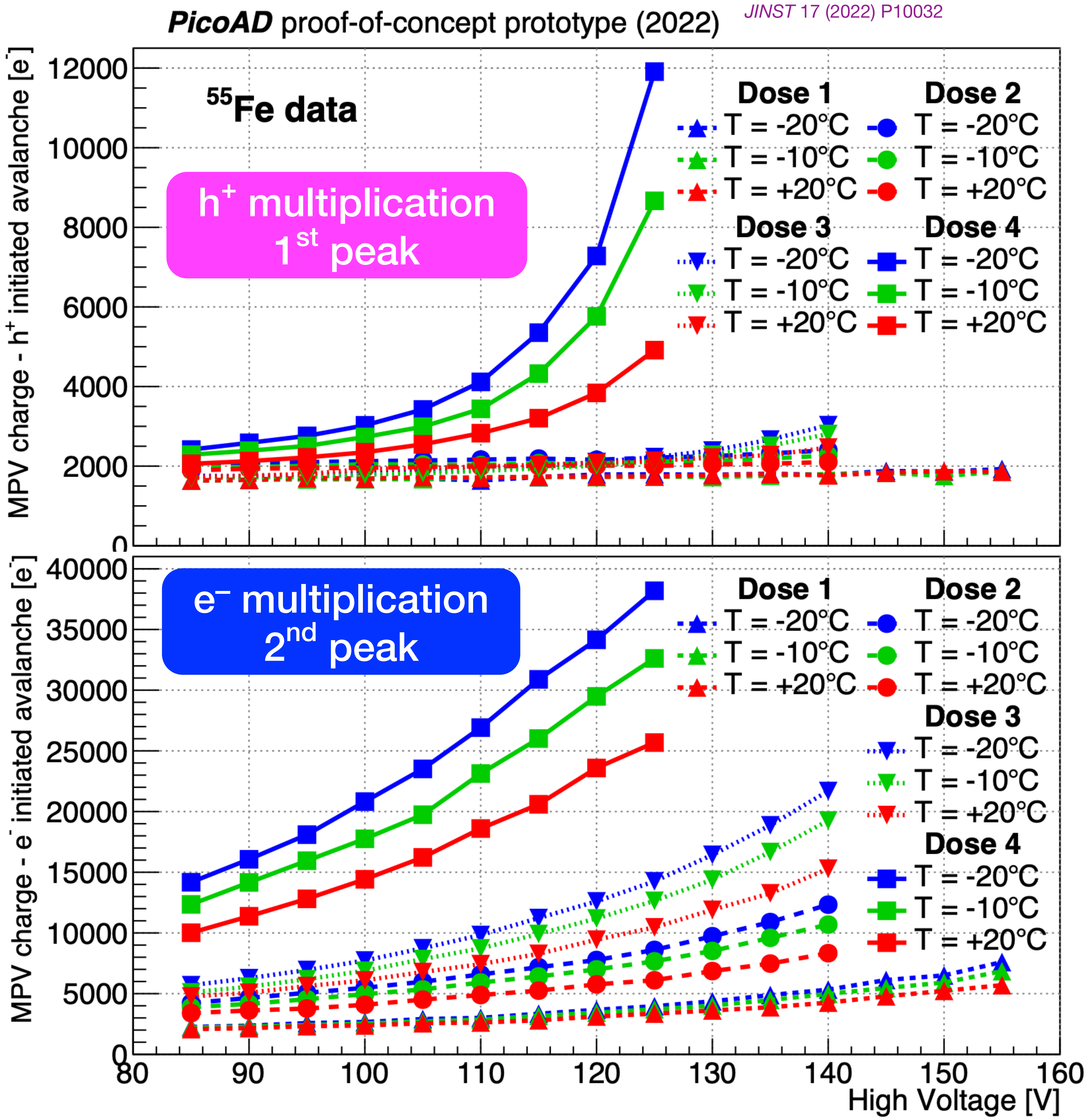
Average amplitudes of h+ and e- gains extracted via gaussian fit around local maxima



Assumption of no gain multiplication when:

- photon absorbed in drift region
- lowest voltage (85 V)
- lowest dose (dose 1)

⇘ **normalization value**



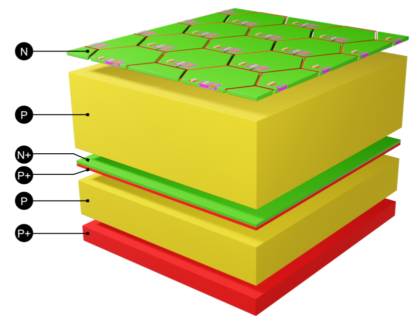
Gain Measurement with ^{55}Fe source

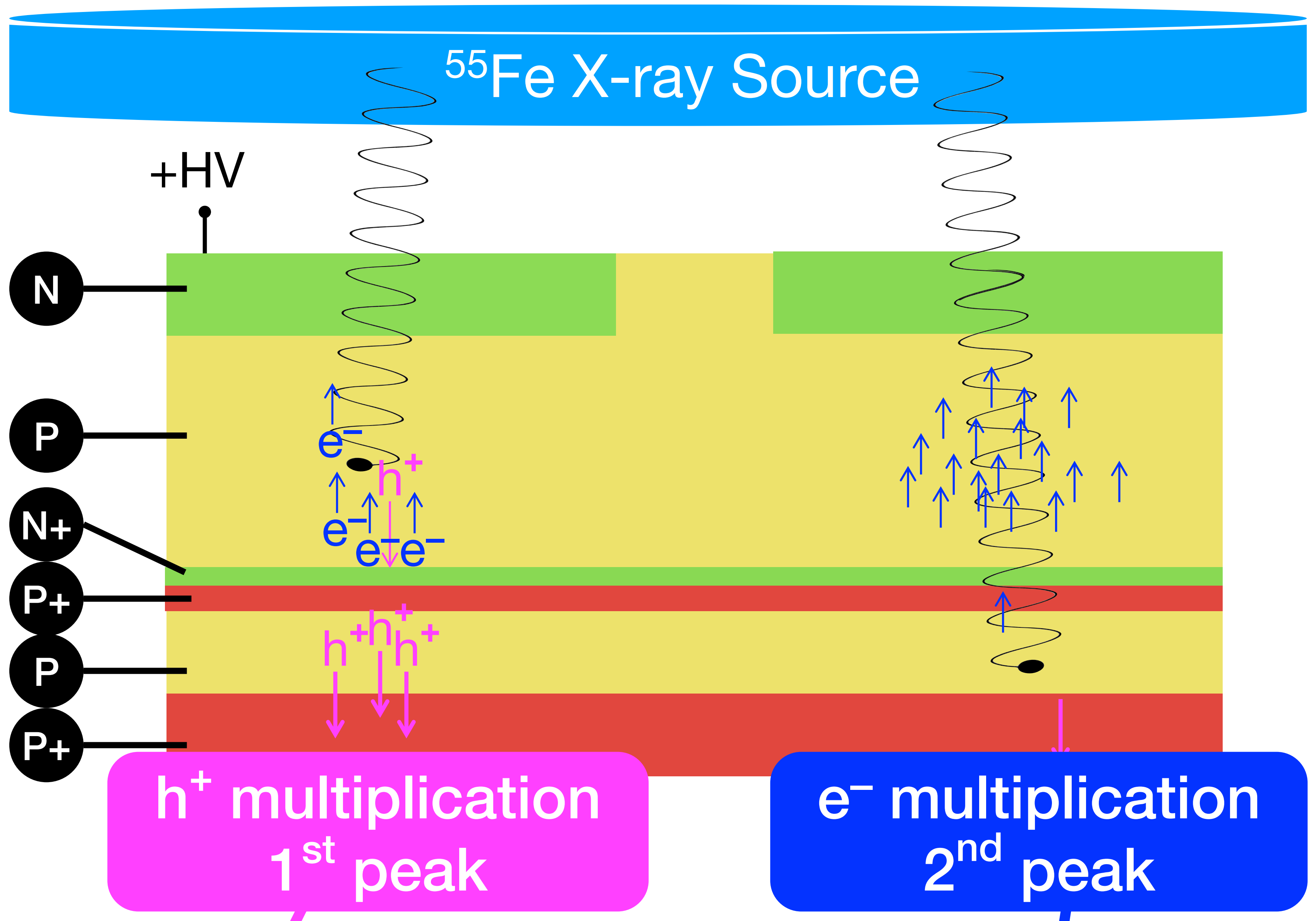
X-rays from 55Fe radioactive source:

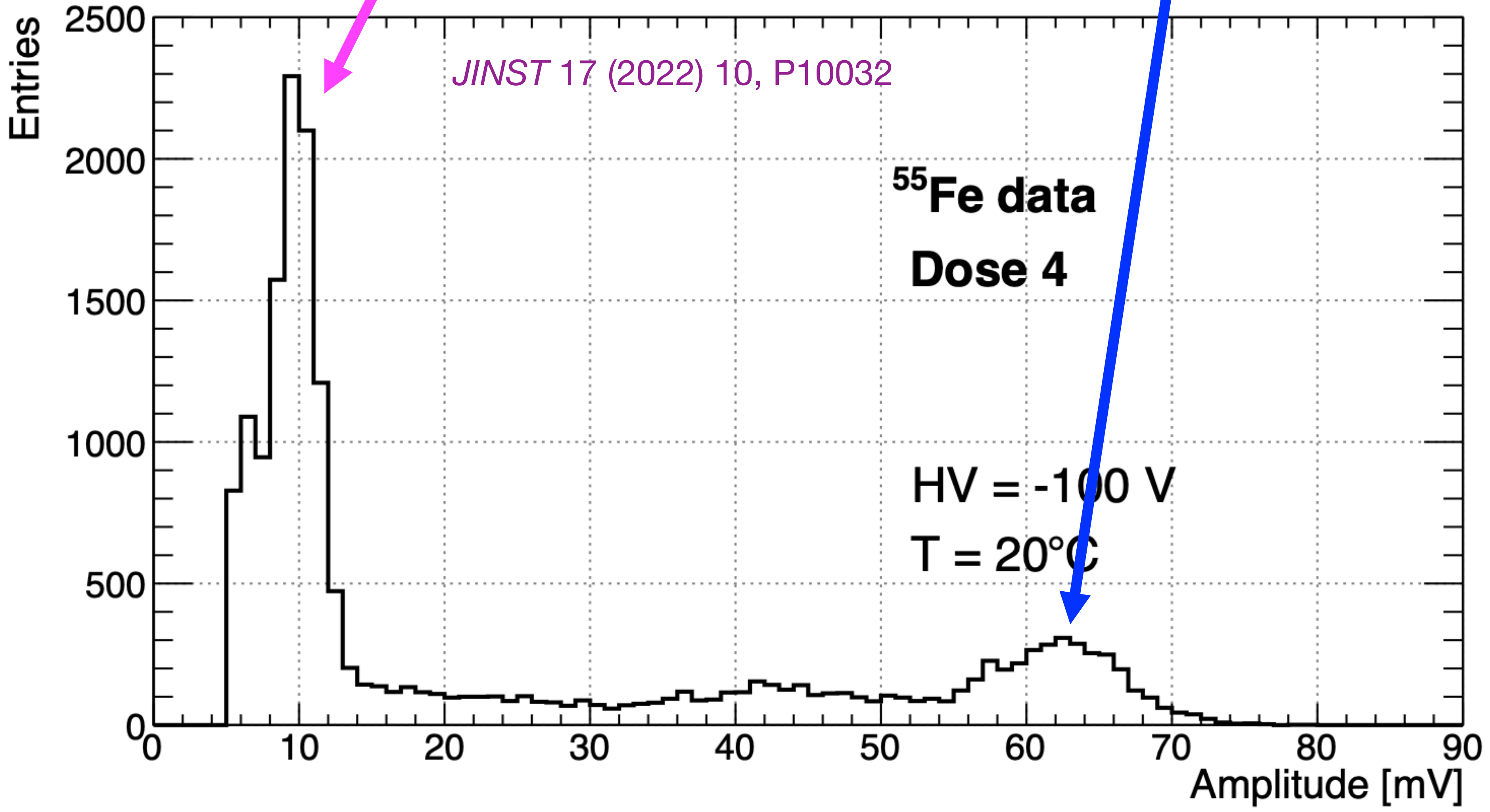
- mainly ~5.9 keV photons
- point-like charge deposition

Characteristic double-peak spectrum

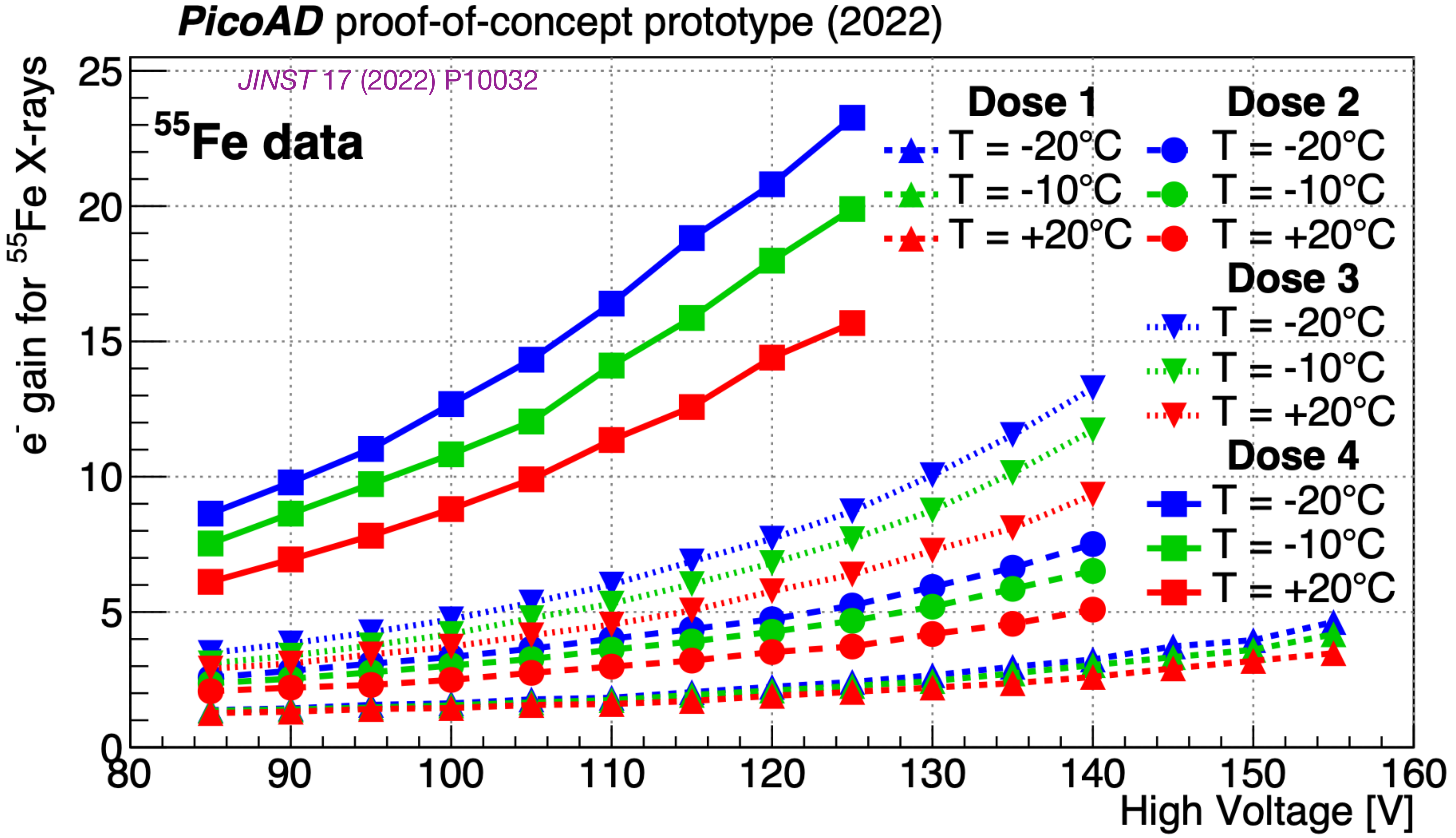
- photon absorbed in **drift region**
  ➡holes drift through gain layer & multiplied
  ➡first peak in the spectrum
- photon absorbed in **absorption region**
  ➡**electrons through gain layer & multiplied**
  ➡second peak in the spectrum





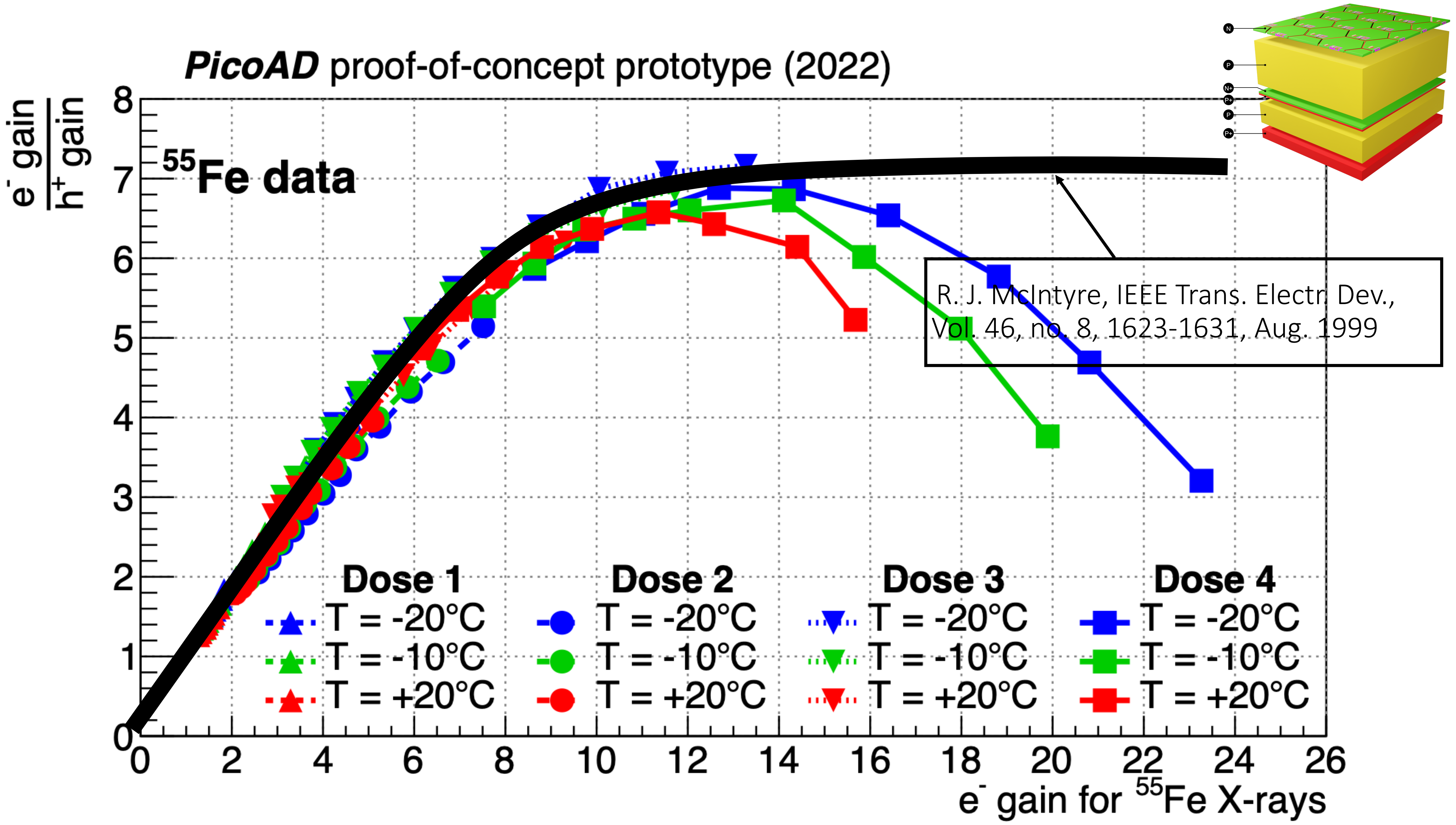


Gain Measurement with ^{55}Fe source



A **gain up to ≈ 20 for ^{55}Fe X-rays**
obtained at HV = 120 V and T = -20 °C

PicoAD



Evidence for **gain suppression**
due to space-charge effects
in the case of ^{55}Fe X-rays

We estimated that ^{55}Fe gain of ≈23 corresponds to **gain 60–70 for a MIP**