Multiple Stages Ring Oscillators Vernier-Based TDC to Optimize Jitter, Power Consumption and Conversion Time

Guillaume Théberge-Dupuis, Robin Scarpellini, Frédérik Dubois, Frédéric Nolet, Nicolas Saint-Jean, Tommy Rossignol, Nicolas Roy, Serge A. Charlebois and Jean-François Pratte

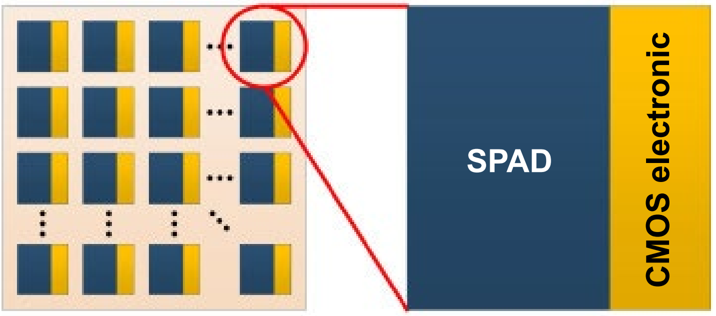
UdS Université de Sherbrooke

GRAMS

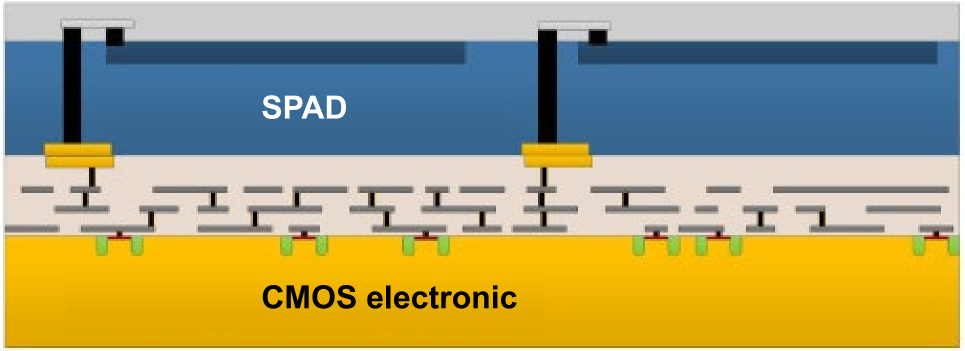
Photon-to-Digital Converter (PDC)

UdS

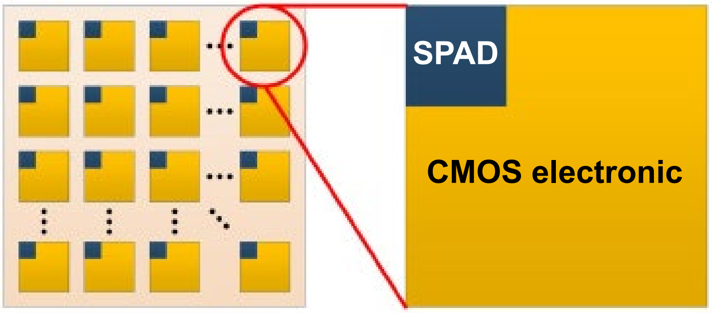
- Pixelated digital SiPM individually quenched
  - 1-to-1 coupling SPAD – Readout electronics
- 3D integration
  - Dedicated process for CMOS and SPAD



2D pixel optimized for SPAD area



3D pixel optimized for SPAD area and electronic functionalities



2D pixel optimized for electronic functionalities

Guillaume.Theberge-Dupuis@USherbrooke.ca

[1] J.-F. Pratte *et al.*, “3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works,” *Sensors (Basel)*, vol. 21, no. 2, p. 598, Jan. 2021, doi: 10.3390/s21020598.

Why the GRAMS needs TDC

UDS

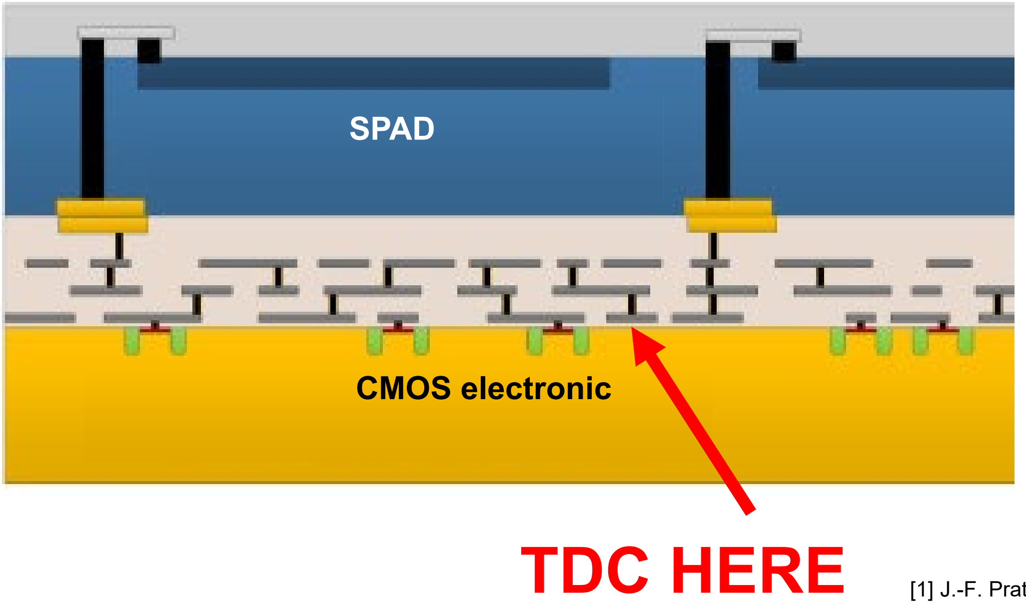
- Particles physics
  - Background rejection (α)
  - To detect cluster of events
- Medical imaging
  - To detect the point of annihilation in PET
  - Time correlated photon counting computed tomography
- Quantum key distribution cryptography
  - Time-bin QKD [2]

[2] S. Carrier, et al., “Towards a Multi-Pixel Photon-to-Digital Converter for Time-Bin Quantum Key Distribution”, Sensors 2023, 23, 3376. https://doi.org/10.3390/s23073376

Guillaume.Theberge-Dupuis@USherbrooke.ca

Precise time of detection for each pixel in the PDC

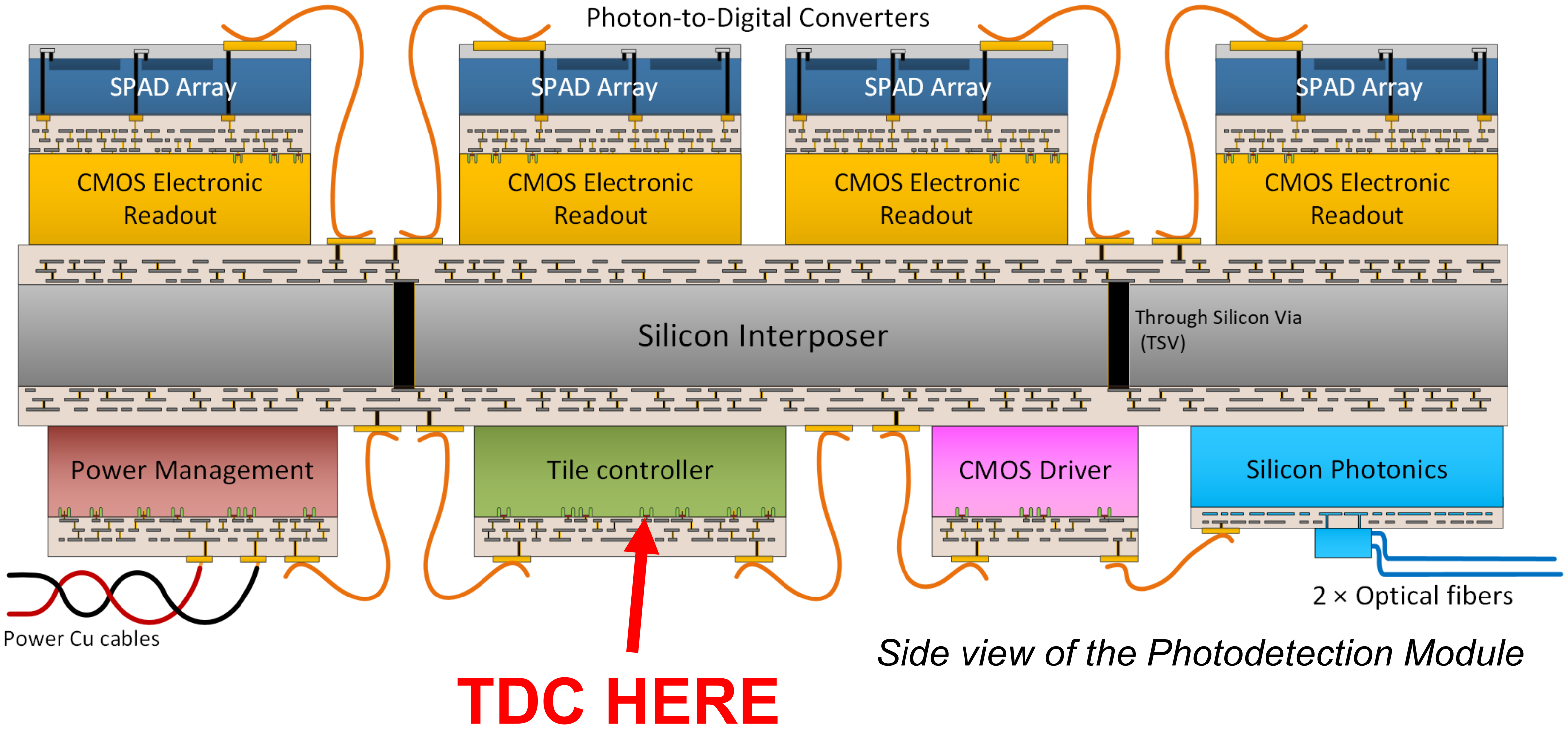
- Quantum Key Distribution (QKD)
- Positron Emission Tomography (PET)
- Time-of-flight computed tomography
- Targeted precision < 4.25 ps RMS



[1] J.-F. Pratte *et al.*, “3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works,” *Sensors (Basel)*, vol. 21, no. 2, p. 598, Jan. 2021, doi: 10.3390/s21020598.

Precise time of detection for each PDC

- Neutron imaging
- Particle physics experiments (nEXO, Argo, etc.)
- Target resolution ≈ 100 ps

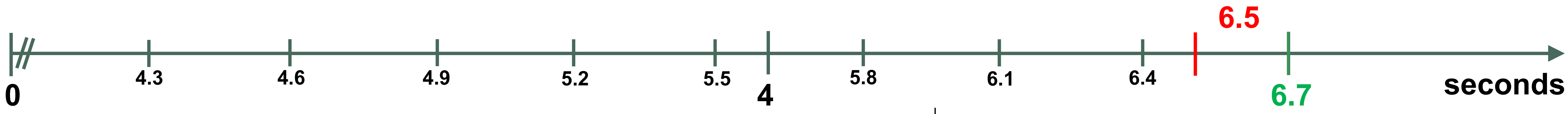


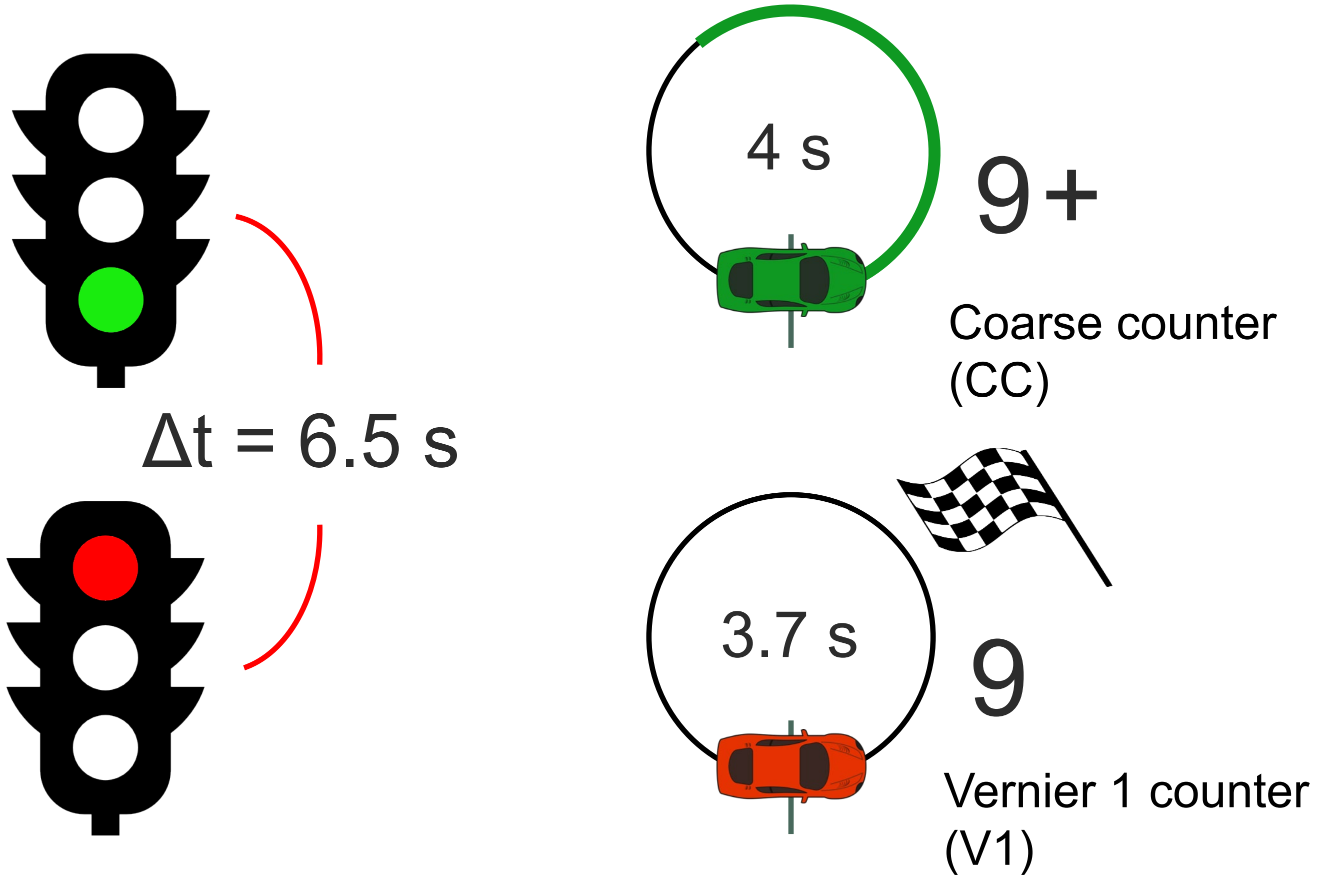
Side view of the Photodetection Module

Guillaume.Theberge-Dupuis@USherbrooke.ca

Vernier-based TDC

Ring Oscillators Vernier-based TDC – Principle





Highlights

- Resolution = $T_{slow} - T_{fast}$ = **0.3 s**

Base equation for Vernier-based TDC

Conversion time = CC × T_{slow}

Coarse time = (CC - V1) × T_{slow}

Vernier time = V1 × Resolution

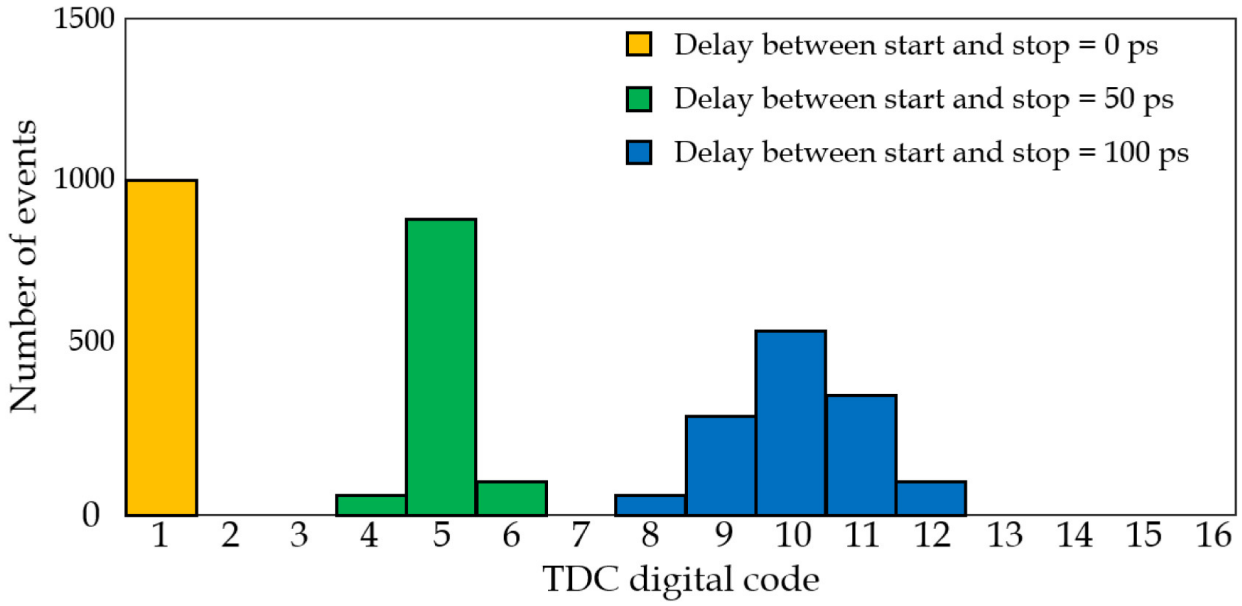
- Conversion time = **40 s**

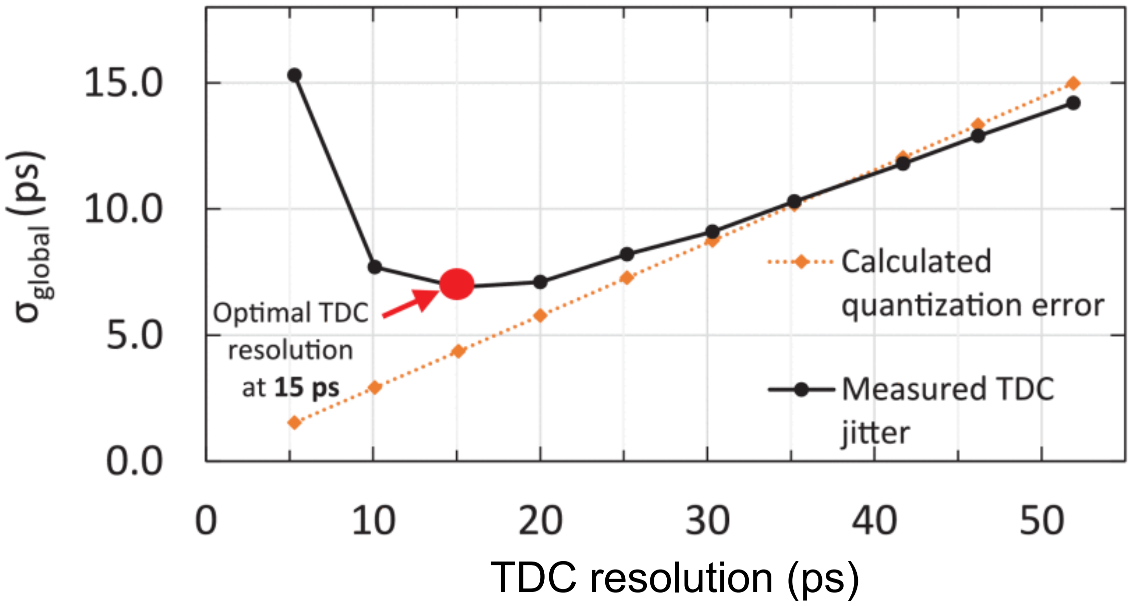
Guillaume.Theberge-Dupuis@USherbrooke.ca

Motivation for a new Ring Oscillators Vernier-Based TDC architecture

UDS

- Finer resolution and larger dynamic range → More cycles
- More cycles induce
  - More jitter accumulation
  - Increased conversion time
  - Increased power consumption





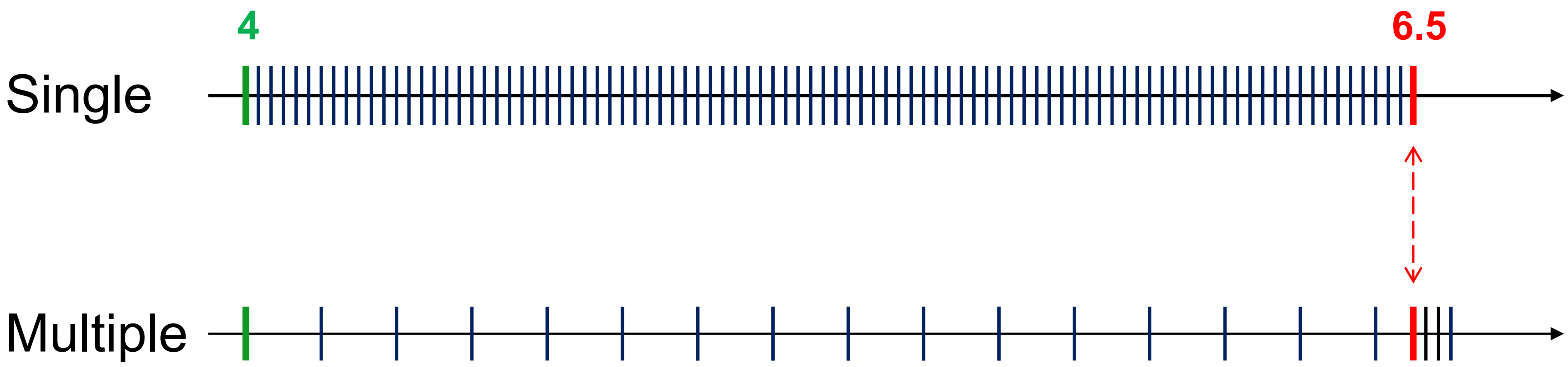
[3] F. Nolet *et al.*, "A 256 Pixelated SPAD readout ASIC with in-Pixel TDC and embedded digital signal processing for uniformity and skew correction," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 949, p. 162891, Jan. 2020, doi: 10.1016/j.nima.2019.162891.

Guillaume.Theberge-Dupuis@USherbrooke.ca

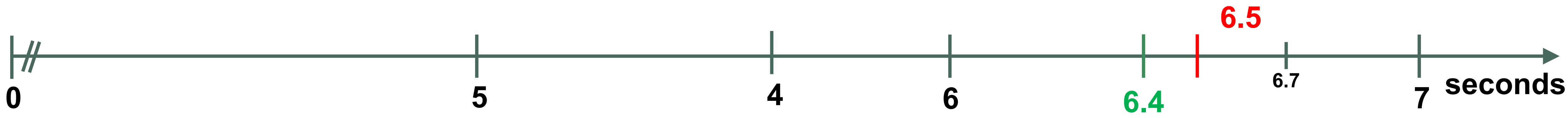
[4] N. Roy *et al.*, "Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM," in *IEEE Transactions on Radiation and Plasma Medical Sciences*, vol. 1, no. 6, pp. 486-494, Nov. 2017, doi: 10.1109/TRPMS.2017.2757444.

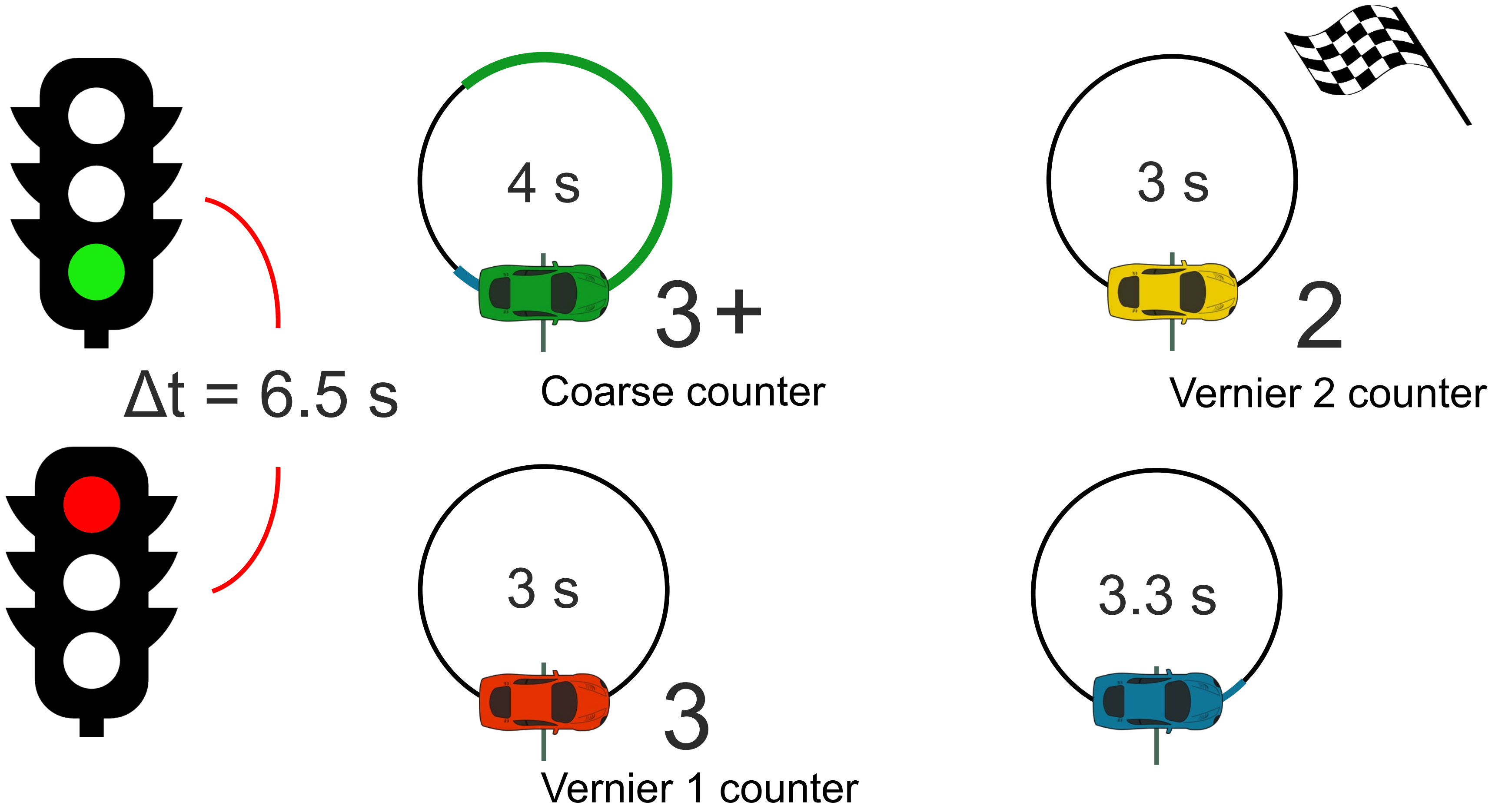
Vernier-based TDC from single to multiple

How to reduce the total cycle count



Consecutive Vernier-based TDC – Principle





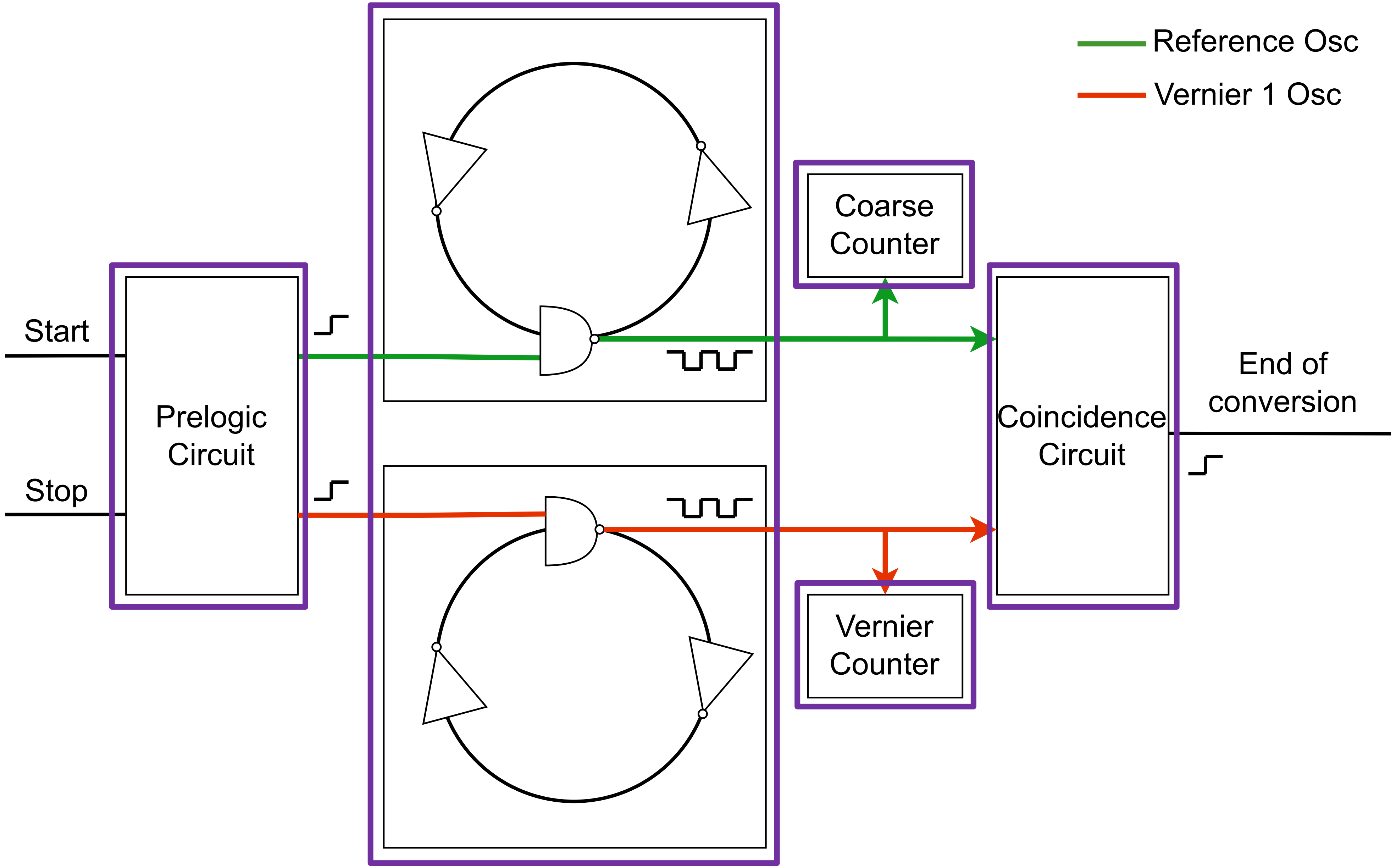
Highlights

- $\text{Resolution}_{V1} = T_{ref} - T_{fast}$ = **1 s**
- $\text{Resolution}_{V2} = T_{slow} - T_{ref}$ = **0.3 s**

➢ Conversion time = **22 s**
  ➢ Single Vernier = **40 s**

Guillaume.Theberge-Dupuis@USherbrooke.ca

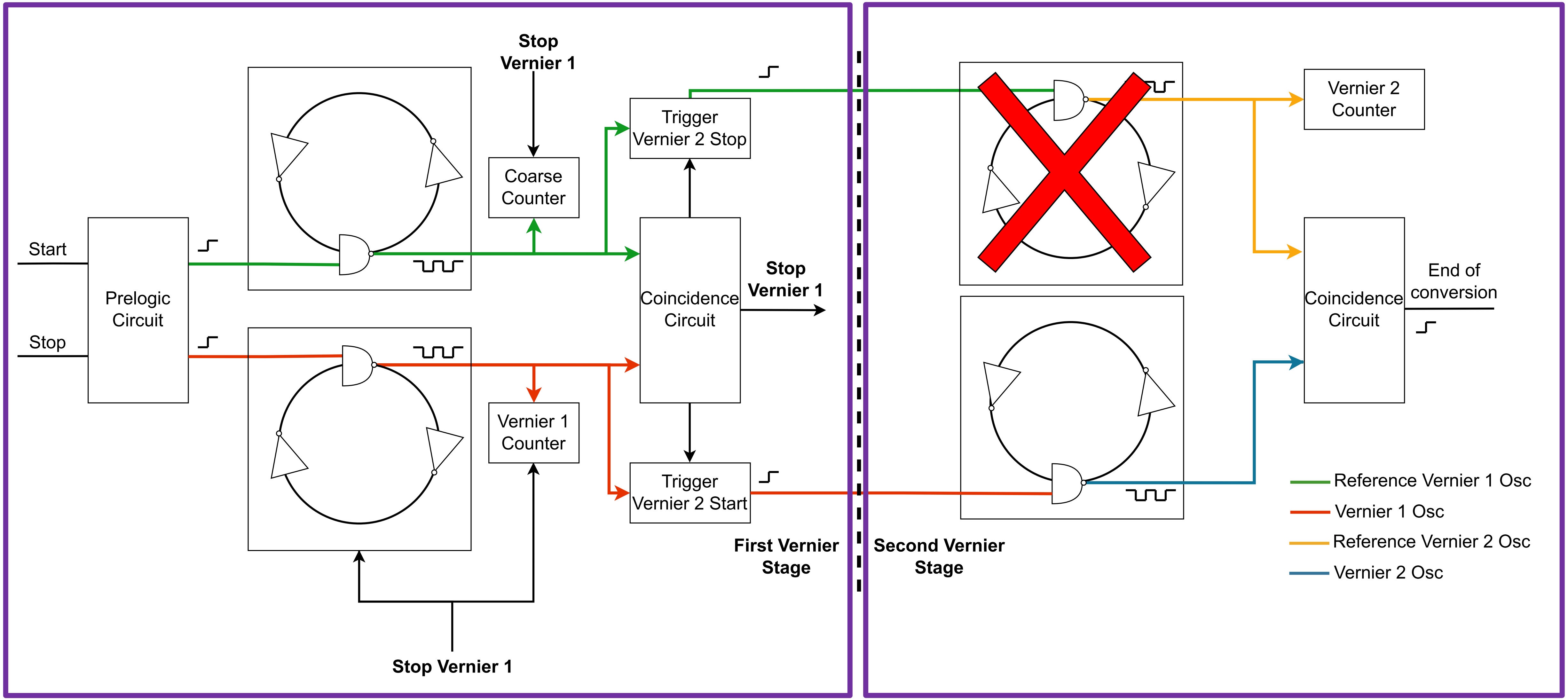
Ring Oscillators Vernier-based TDC – Single Vernier



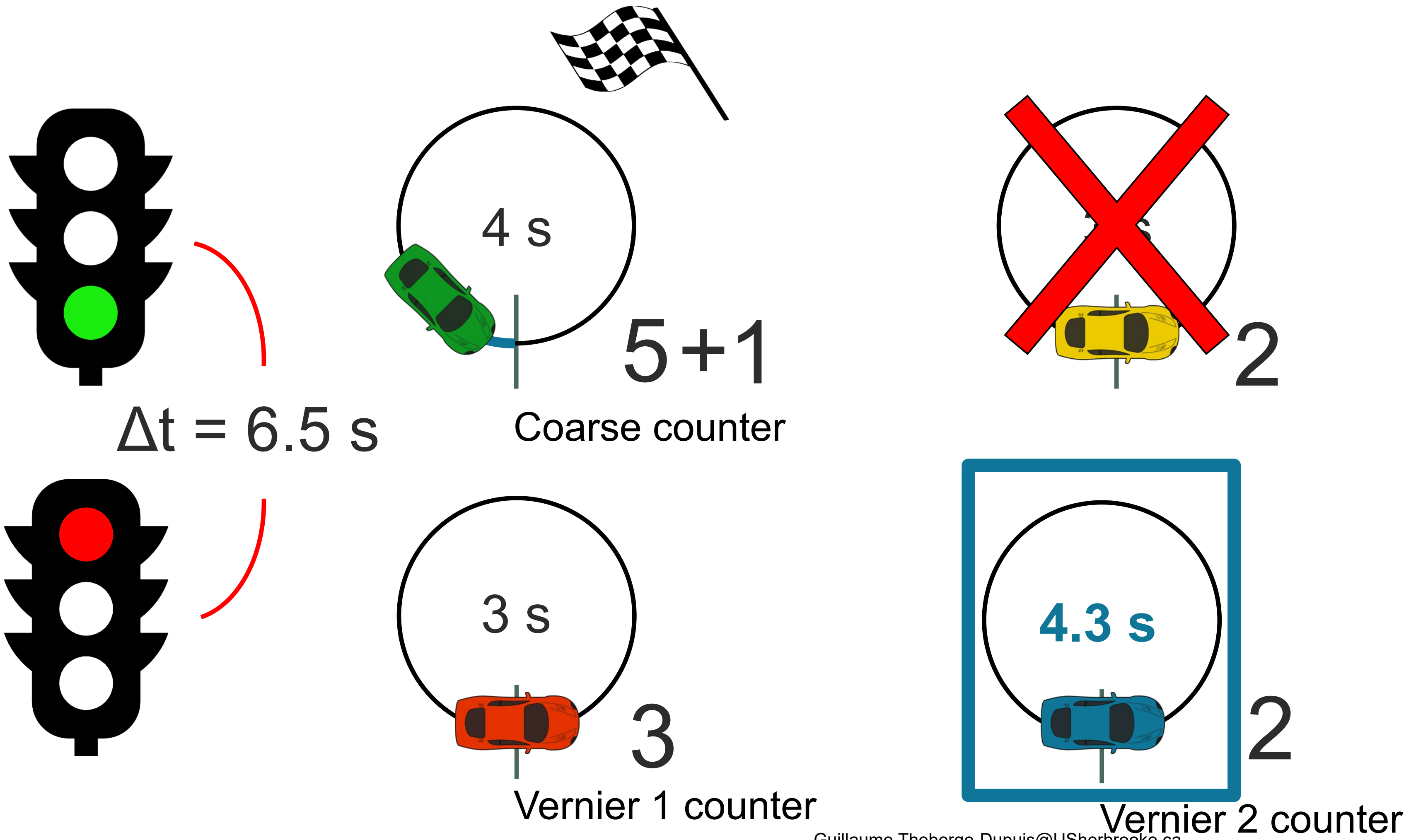
Guillaume.Theberge-Dupuis@USherbrooke.ca

Ring Oscillators Vernier-based TDC – Consecutive Vernier

The LSB of the first Vernier is the dynamic range of the second Vernier



Guillaume.Theberge-Dupuis@USherbrooke.ca



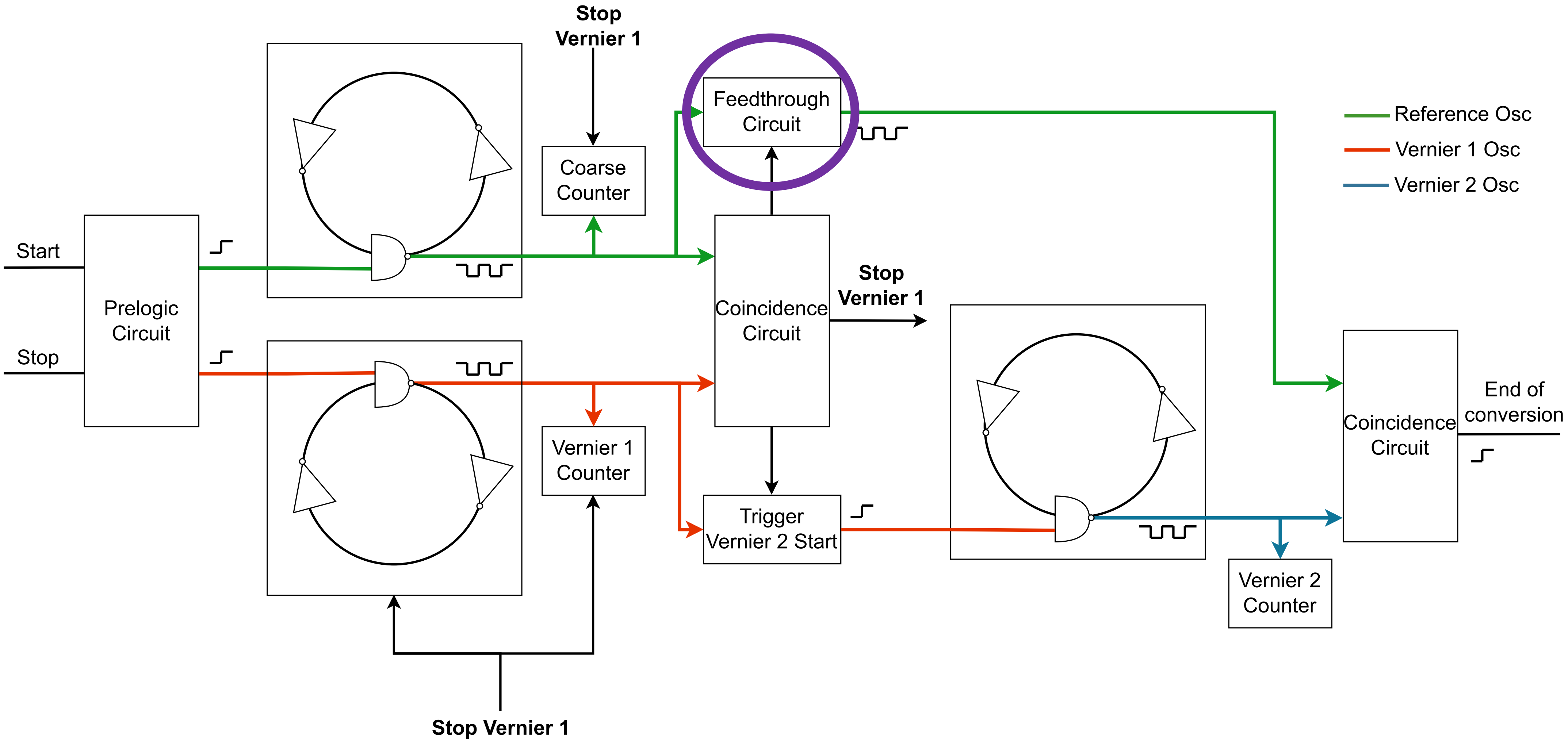
Highlights

- $\text{Resolution}_{V1} = T_{ref} - T_{fast}$ = **1 s**
- $\text{Resolution}_{V2} = T_{slow} - T_{ref}$ = **0.3 s**

➢ Conversion time = **24 s**
  ➢ Single Vernier = **40 s**

Guillaume.Theberge-Dupuis@USherbrooke.ca

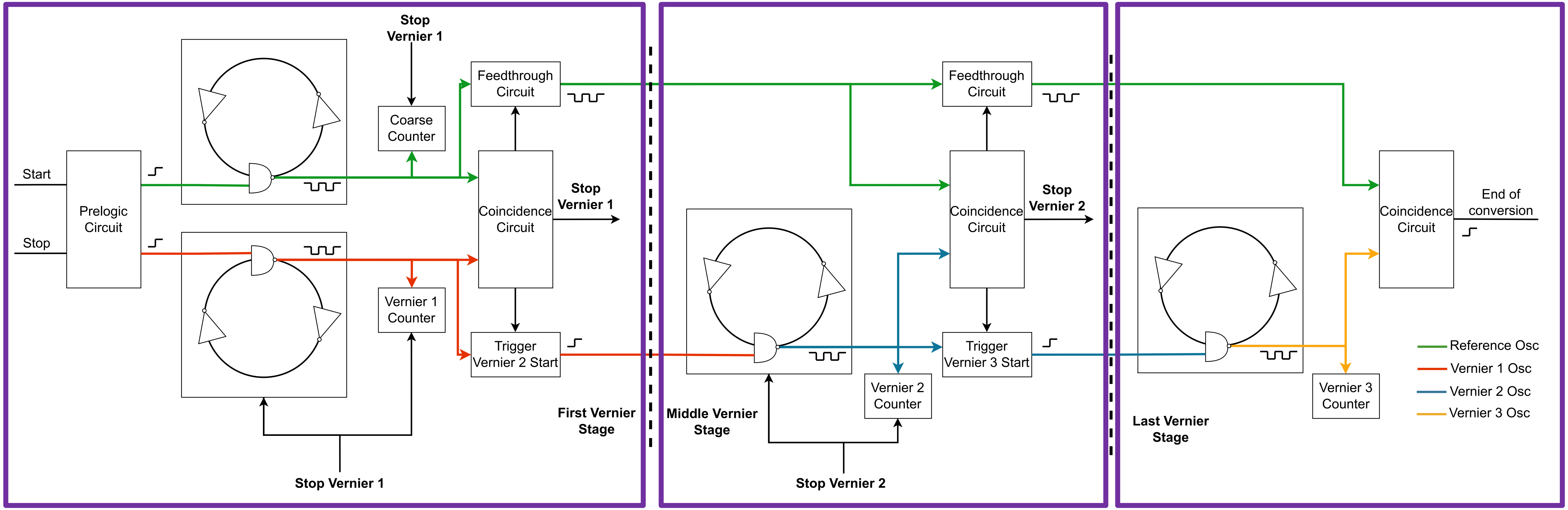
From consecutive Vernier to the patented cascaded Vernier TDC – Schematic



Guillaume.Theberge-Dupuis@USherbrooke.ca

Generalisation of the architecture

UdS



Guillaume.Theberge-Dupuis@USherbrooke.ca

Is there an optimal number of stages?

- Dynamic Range to Resolution Ratio (DR_3)

$$\mathrm{DR_3} = \frac{\text{Dynamic Range}}{\text{Resolution}} = \text{Number of different timestamps}$$

- Minimize the total cycle count ⇒ Each stage has the same cycle count

$$\text{Optimal cycle count per stage} = \sqrt[(\text{VernierStages}+1)]{\mathrm{DR_3}}$$

$$\text{Total reference cycles} = (\text{VernierStages} + 1) \times \text{Optimal cycle count per stage}$$

Guillaume.Theberge-Dupuis@USherbrooke.ca

How to optimize the total cycle count? – Examples

UdS

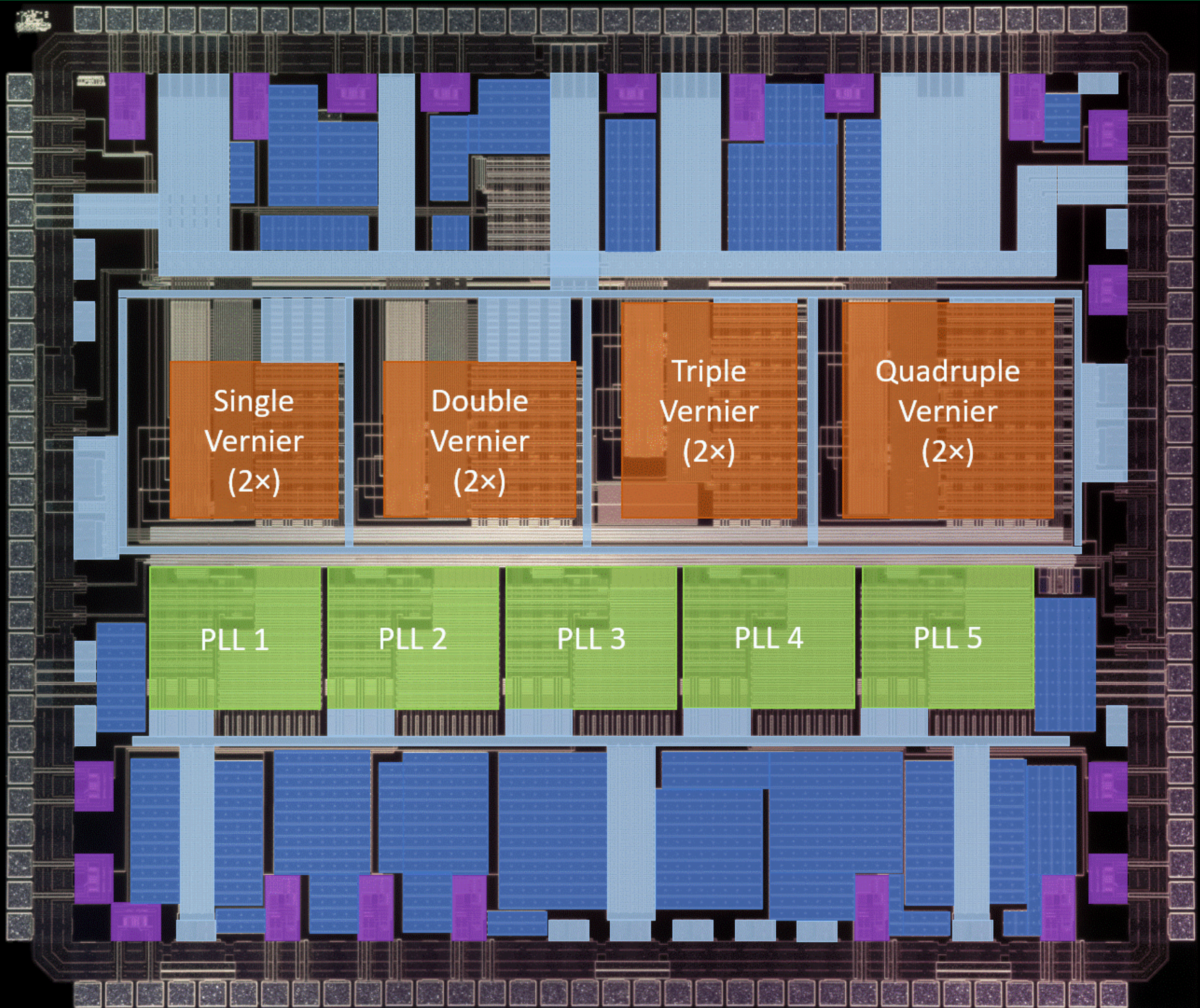
- Case 1:
  Dynamic range of 4 ns and resolution of 50 ps ⇒ Dynamic range to resolution ratio = 80
- Case 2:
  Dynamic range of 20 ns and resolution of 50 ps ⇒ DR_3= 400
  Dynamic range of 4 ns and resolution of 10 ps ⇒ DR_3= 400
- Case 3:
  Dynamic range of 100 ns and resolution of 10 ps ⇒ DR_3= 10 000

DR_3	80		400		10,000	
	Cycles		Cycles		Cycles	
Single Vernier	18	-28%	40	-43%	200	-68%
Double Vernier	13	-8%	23	-22%	64	-38%
Triple Vernier	12	+8%	18	-6%	40	-20%
Quadruple Vernier	13		17		32	

Guillaume.Theberge-Dupuis@USherbrooke.ca

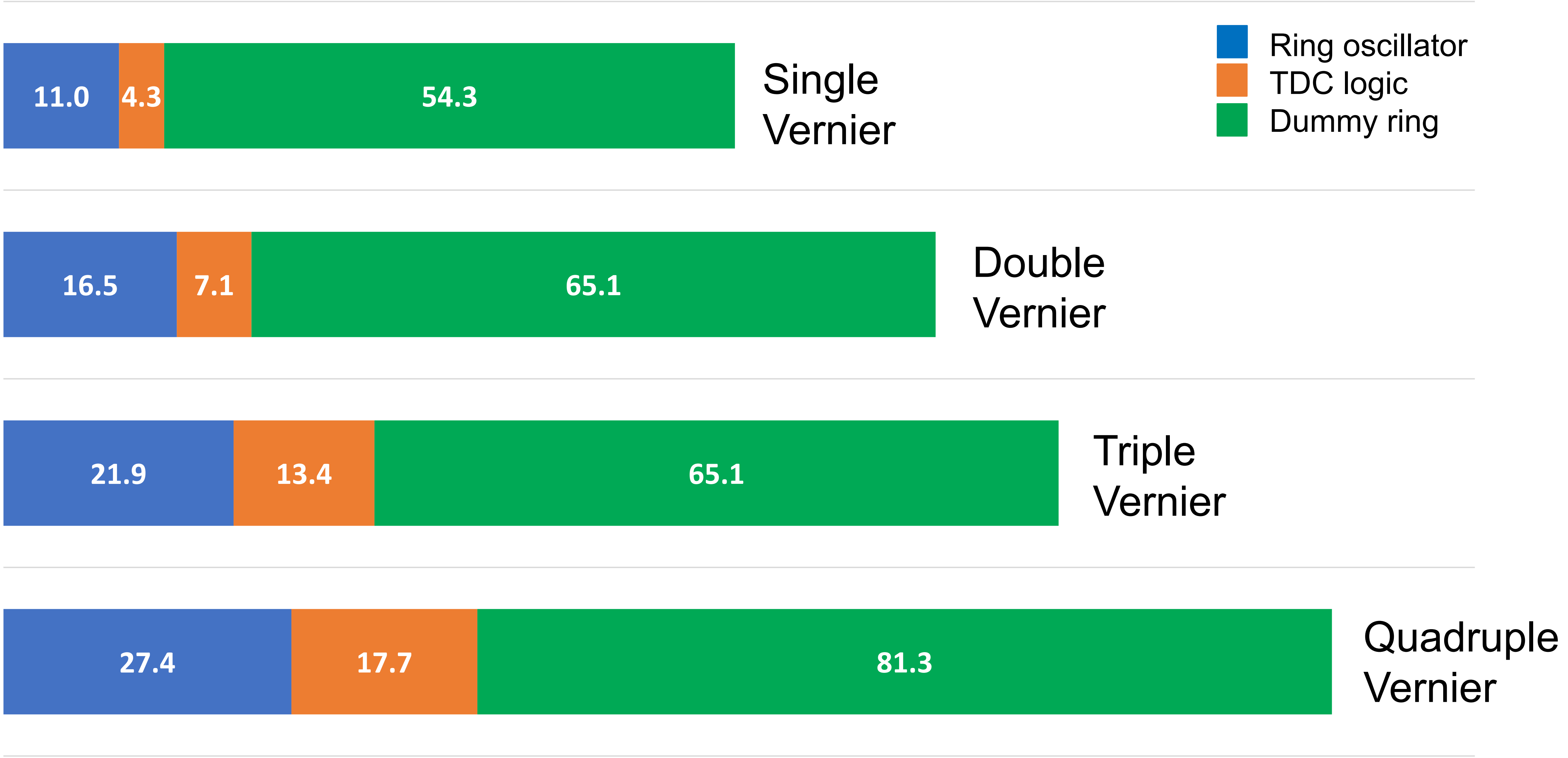
Implementation in TSMC 180 nm

System implementation



- TDC
- PLL
- Driver LVDS
- Power Rail
- Decoupling Cap

Size comparison of the TDC – Area in thousand μm²

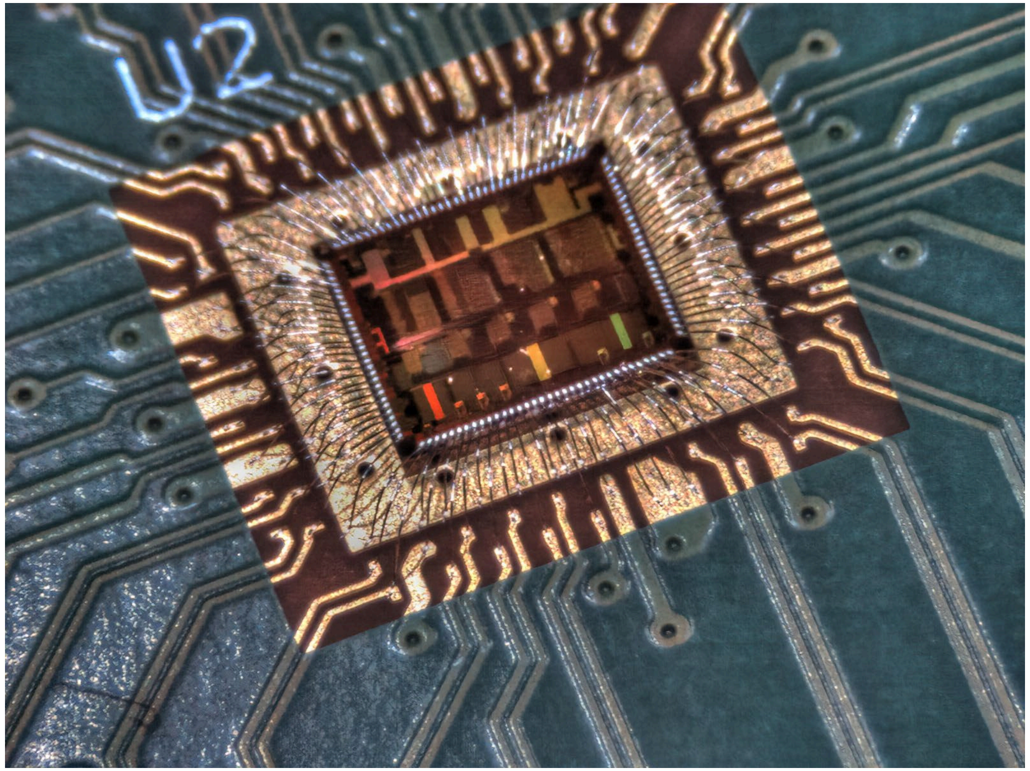


Guillaume.Theberge-Dupuis@USherbrooke.ca

Xilinx Zynq-7000 System on chip

Five (5) reference oscillators for phase locked-loop

Correlated and uncorrelated Start and Stop



Results

Uncorrelated measurement – Histogram at LSB = 50 ps and dynamic range = 20 ns

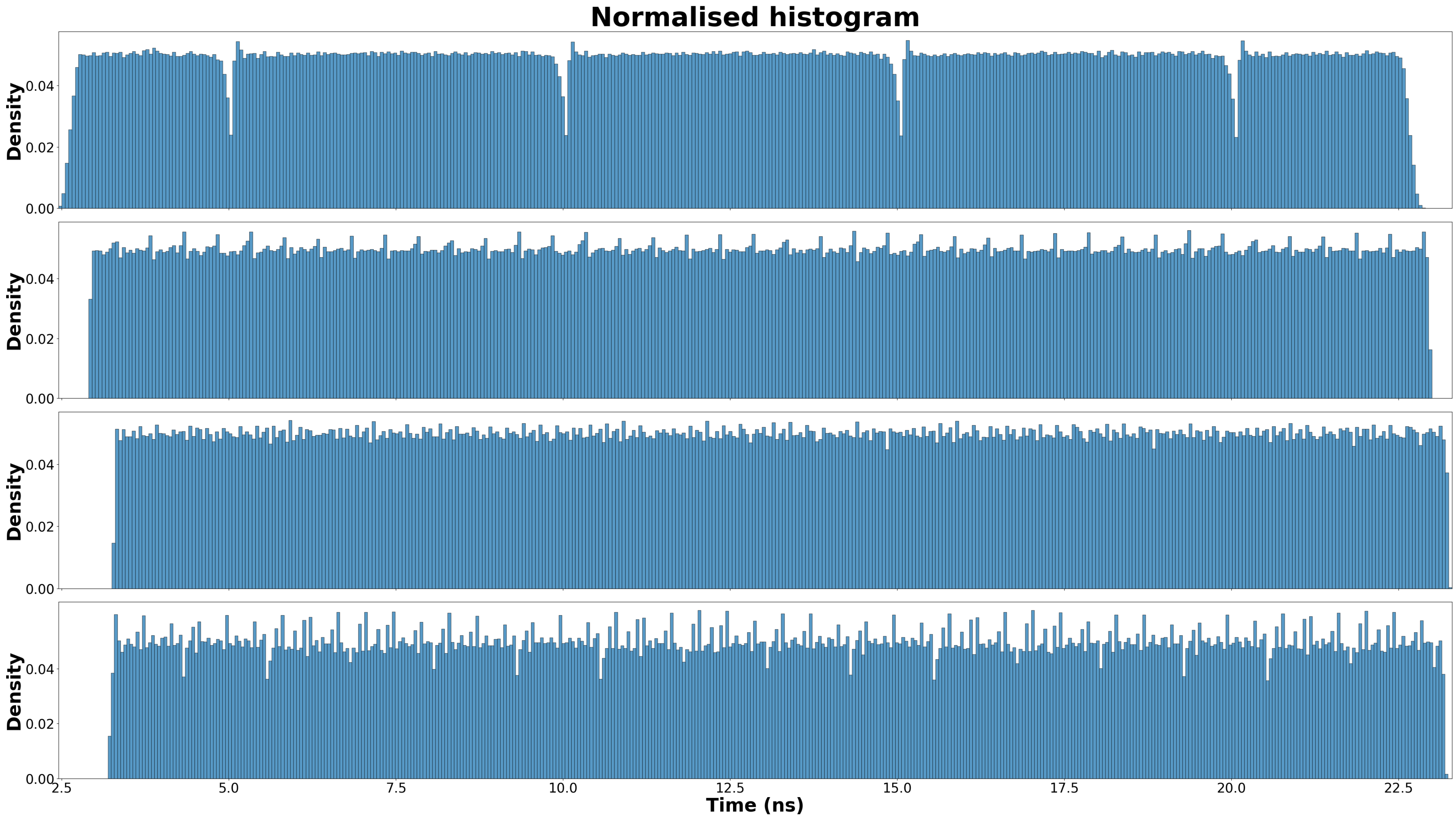
UdS

Single Vernier

Double Vernier

Triple Vernier

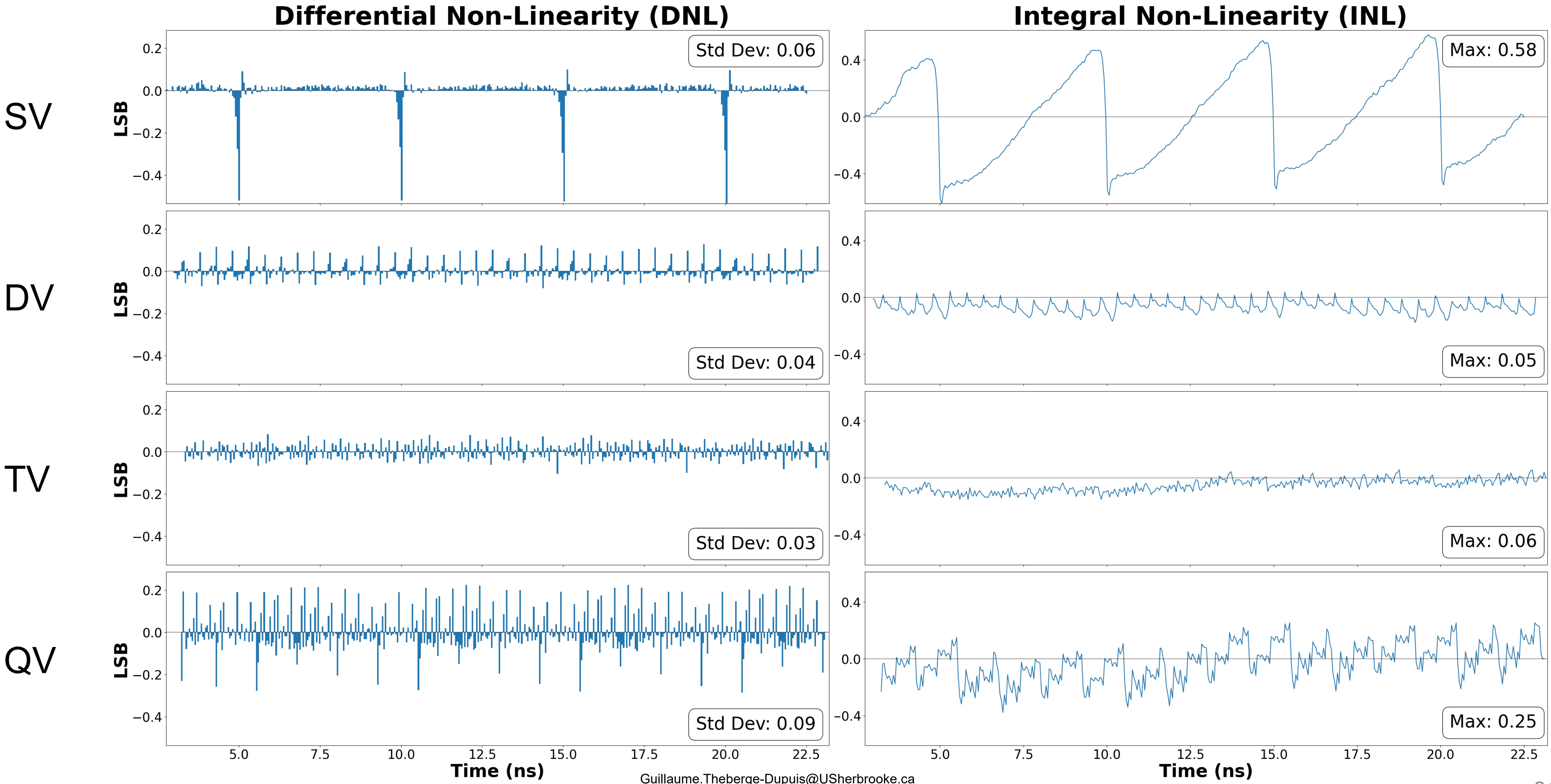
Quadruple Vernier



Guillaume.Theberge-Dupuis@USherbrooke.ca

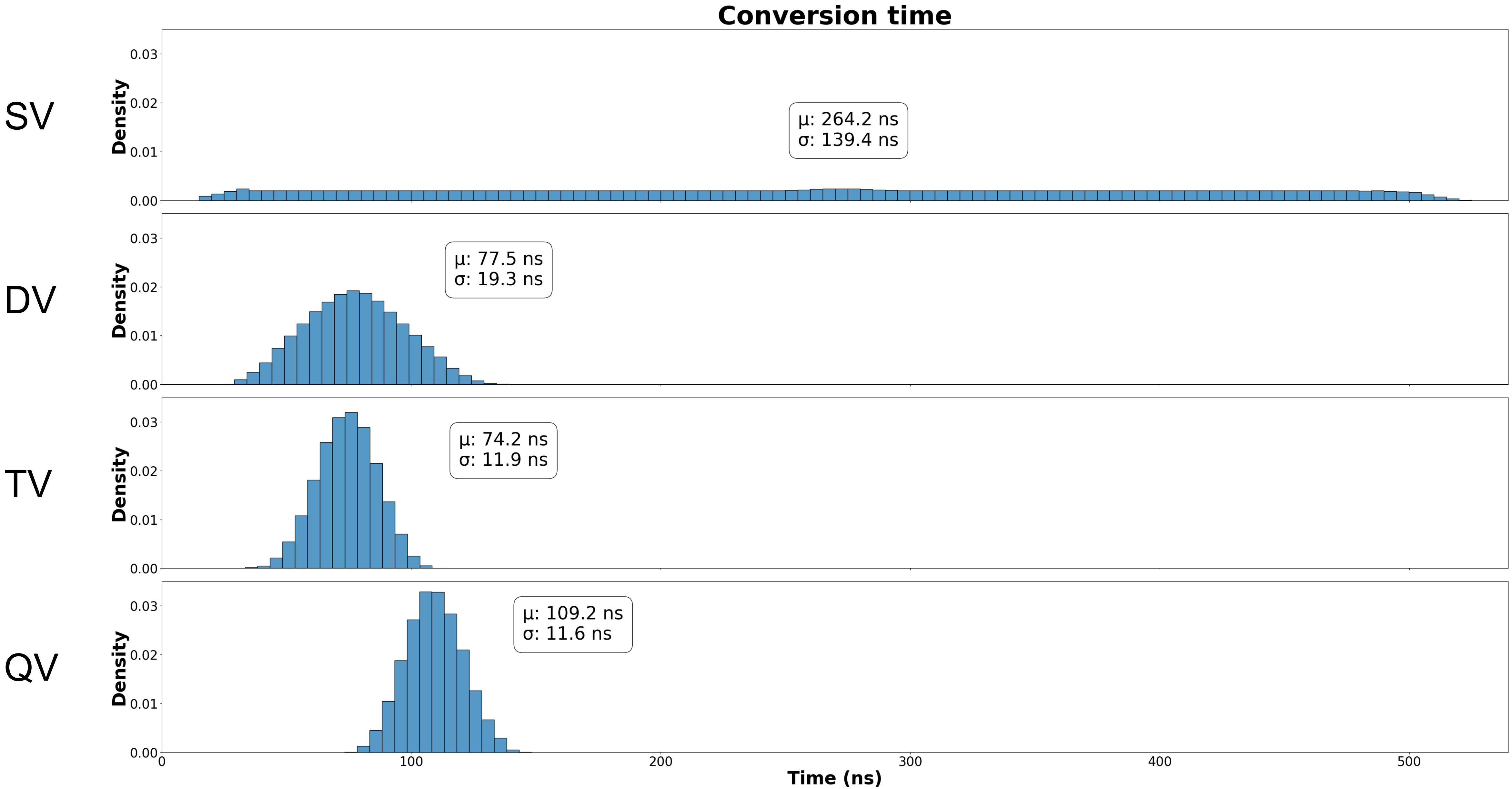
Uncorrelated measurement – Linearity at LSB = 50 ps and dynamic range = 20 ns

UdS



Guillaume.Theberge-Dupuis@USherbrooke.ca

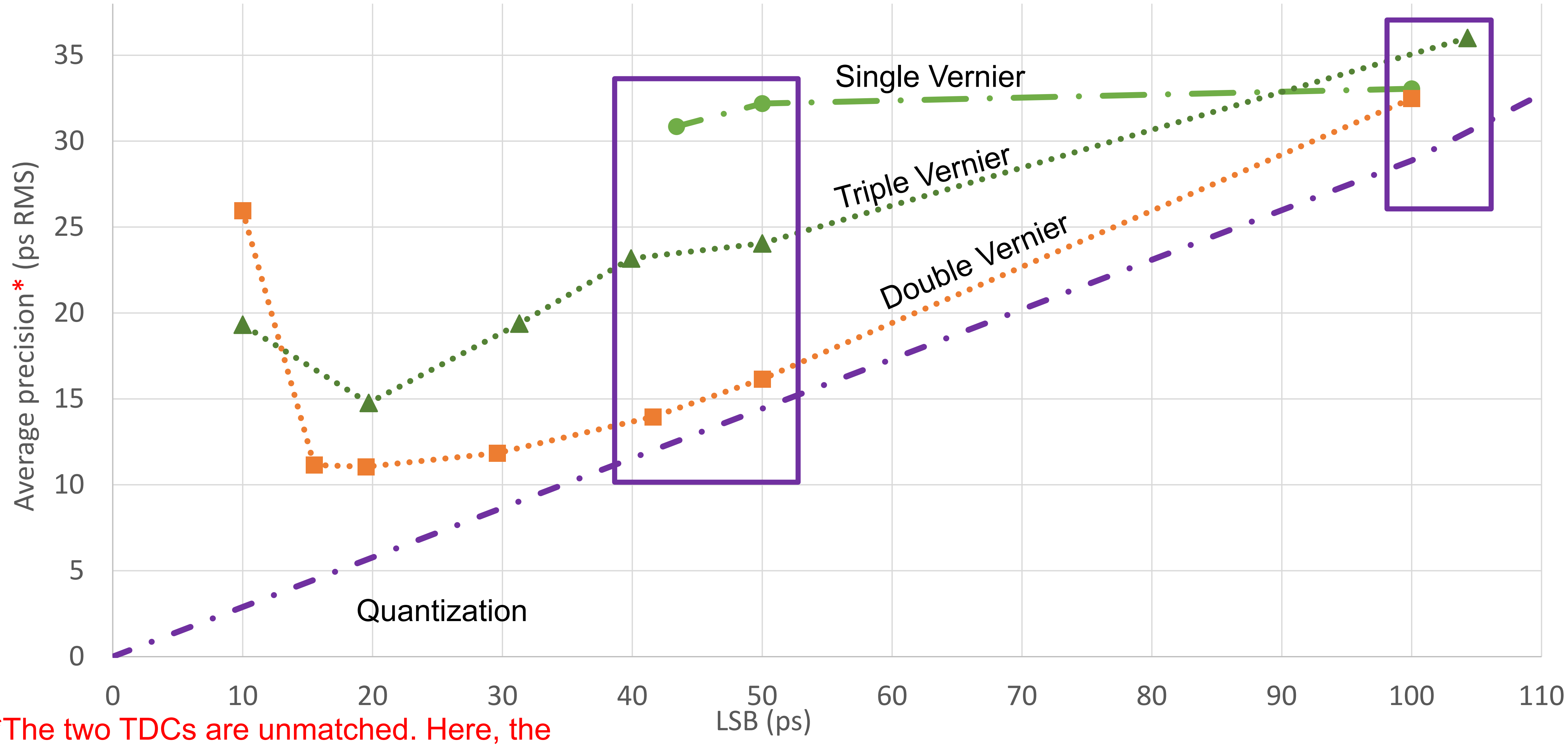
Uncorrelated measurement – Conversion time at LSB = 50 ps and dynamic range = 20 ns



Guillaume.Theberge-Dupuis@USherbrooke.ca

Improvement for the cascaded Vernier (dynamic range = 20 ns)

UdS

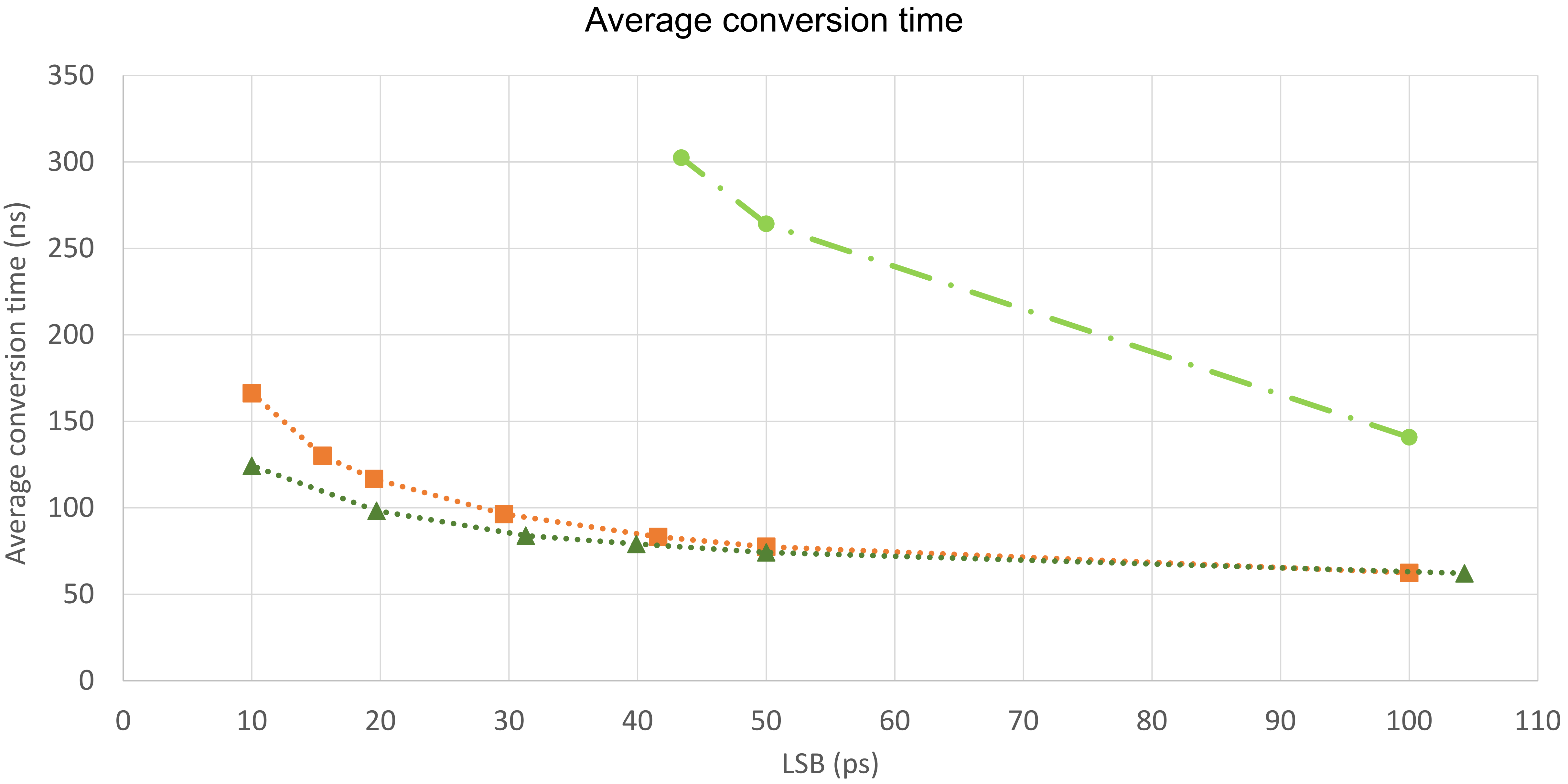


*The two TDCs are unmatched. Here, the precision is the average of both. See *Slide 36* for more details.

Guillaume.Theberge-Dupuis@USherbrooke.ca

Dependence of the average conversion time for the different architectures on resolution (DR = 20ns)

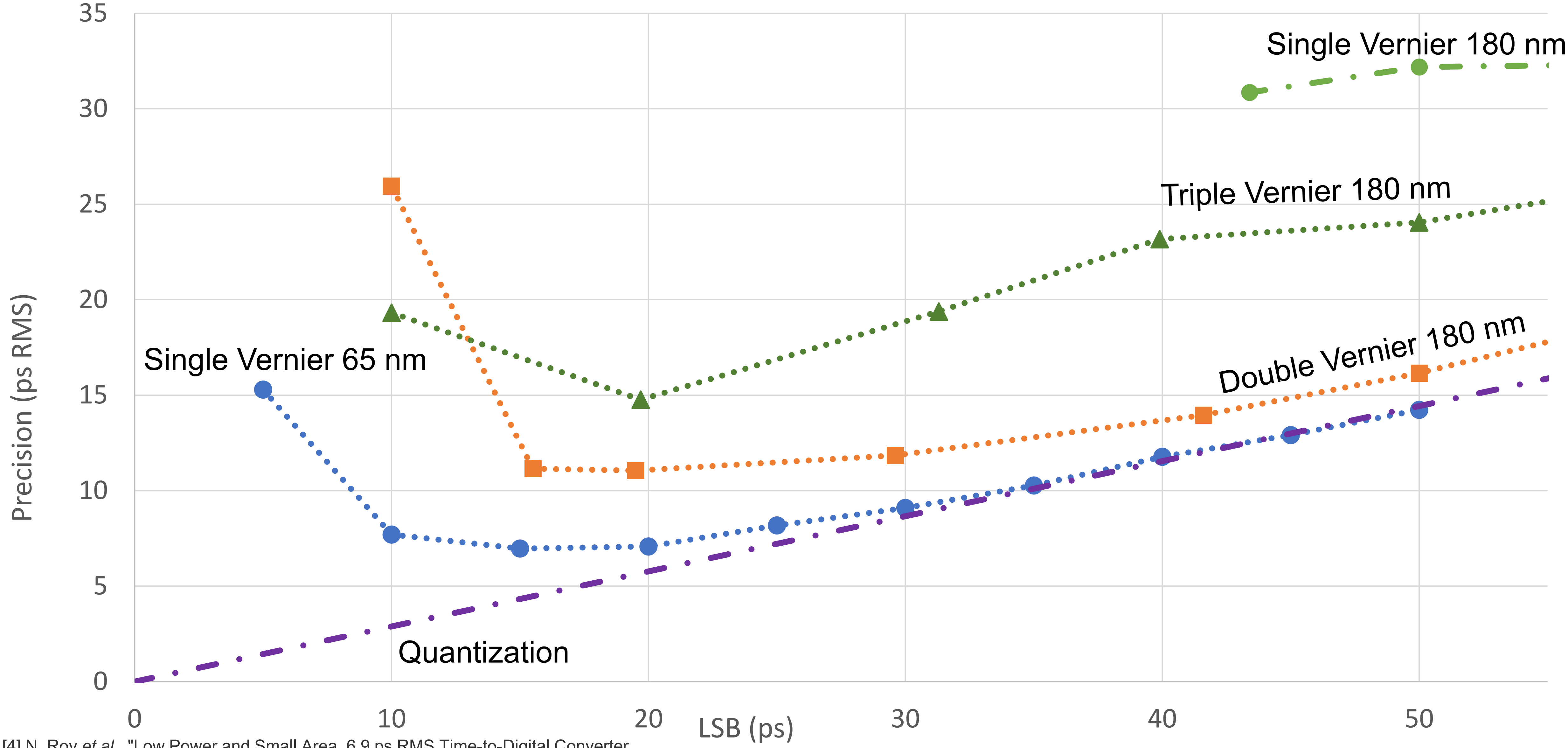
UdS



Guillaume.Theberge-Dupuis@USherbrooke.ca

Relation between precision and resolution (65 nm[1] vs 180 nm[2])

UdS

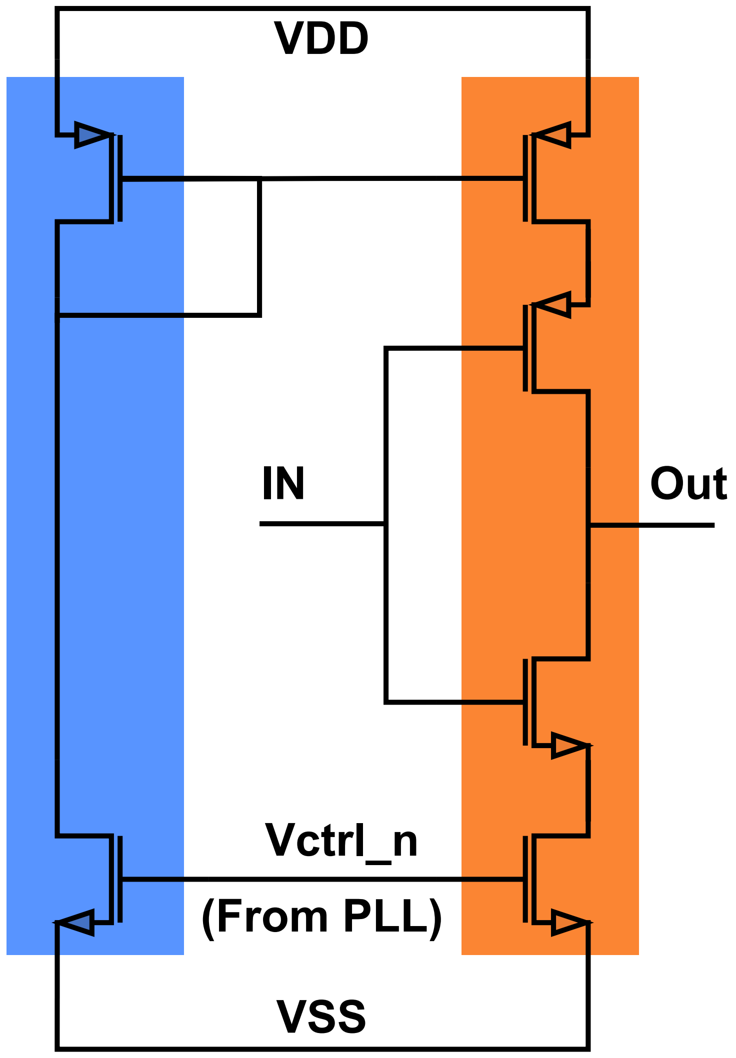


1 [4] N. Roy *et al.*, "Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM," in *IEEE Transactions on Radiation and Plasma Medical Sciences*, vol. 1, no. 6, pp. 486-494, Nov. 2017, doi: 10.1109/TRPMS.2017.2757444.

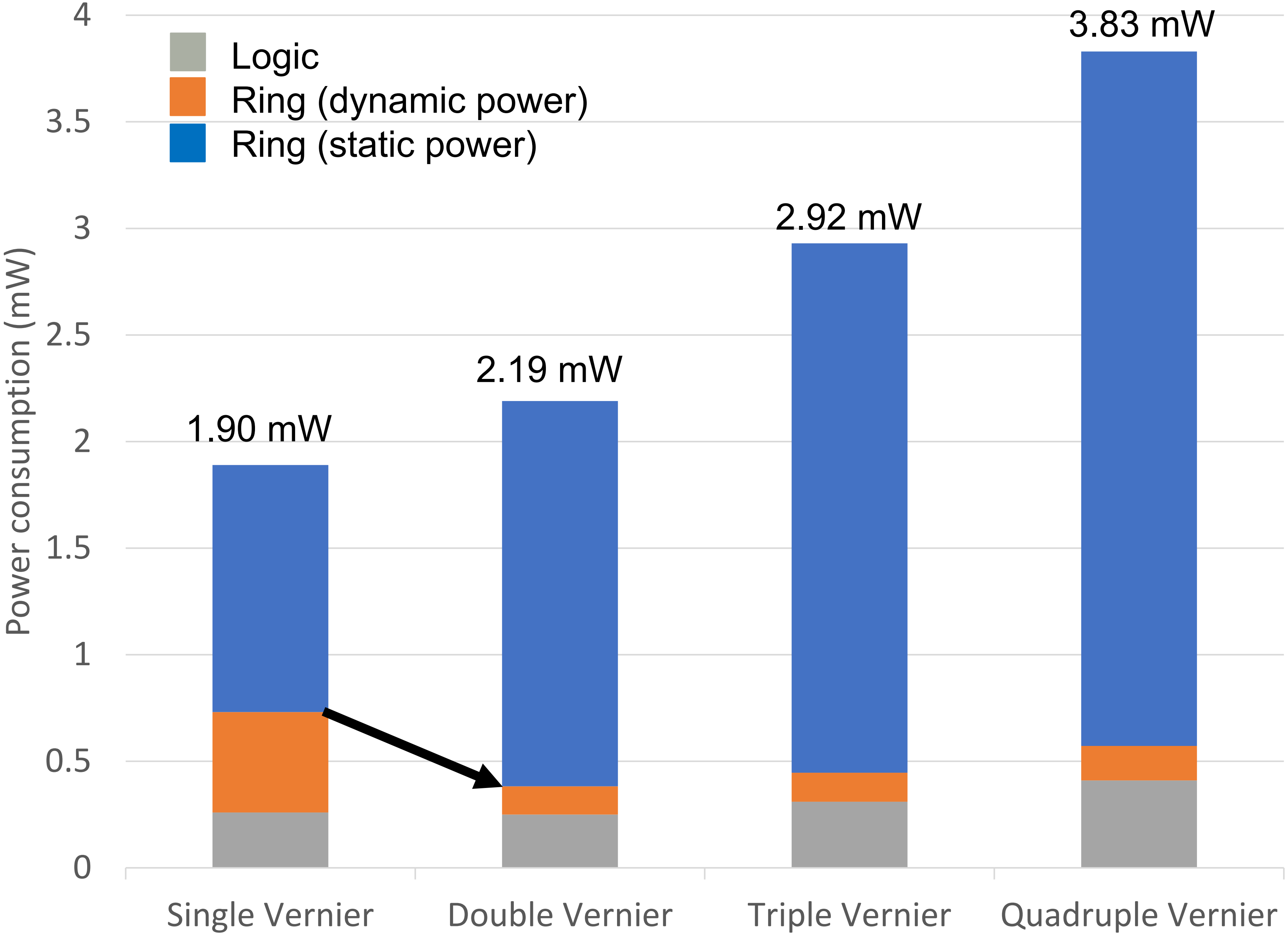
2 The precision of the 180 nm results is the averaged precision of 2 TDC.

Guillaume.Theberge-Dupuis@USherbrooke.ca

Origin of the power consumption for different implementations (simulation at 1 Mcps and LSB = 50 ps)



Schematic of the ring oscillator delay element



Guillaume.Theberge-Dupuis@USherbrooke.ca

Main features and drawbacks of the architecture

- Flexible architecture that can be optimized for
  - Dynamic range to resolution ratio
  - Available area
- Each stage requires a calibration system
  - PLL or DAC
  - Other solutions are under investigation
- More stages = more logic power consumption
- Reduce the number of cycles
  - Reduce conversion time
  - Less cycles = less accumulated jitter
  - Reduce dynamic power consumption

Guillaume.Theberge-Dupuis@USherbrooke.ca

- Cascaded double Vernier for array integration
  - Design in 65 nm
  - 4096 SPAD array
  - 1024 TDC
  - Sub-4.25 ps RMS precision
  - SPAD pitch of 78 μm
  - ASIC size 5.3×5.85 mm²
  - Rad-Hard (quantum key distribution – low earth orbit satellite)

Guillaume.Theberge-Dupuis@USherbrooke.ca

Acknowledgment

Philippe Marcoux[1]
Caroline Paulin[1]
Gabriel Martin-Hardy[1]
Nicolas Viscogliosi[1]
Julien Rossignol[1]
Charles Bourcier-Guérette[1]
Lorenzo Fabris[2]
Paul Hausladen[2]

[1] Université de Sherbrooke
[2] Oak Ridge National Laboratory

Thank you for your attention

Linked articles

UDS

[1] J.-F. Pratte *et al.*, “3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works,” *Sensors (Basel)*, vol. 21, no. 2, p. 598, Jan. 2021, doi: 10.3390/s21020598.

[2] S. Carrier, et al., “Towards a Multi-Pixel Photon-to-Digital Converter for Time-Bin Quantum Key Distribution”, *Sensors* **2023**, *23*, 3376. https://doi.org/10.3390/s23073376

[3] F. Nolet et al., “A 256 Pixelated SPAD readout ASIC with in-Pixel TDC and embedded digital signal processing for uniformity and skew correction,” Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 949, p. 162891, 2020, doi: 10.1016/j.nima.2019.162891.

[4] N. Roy, *et al*., “Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM,” *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 1, no. 6, pp. 486–494, 2017, doi: 10.1109/TRPMS.2017.2757444.

[5] F. Nolet *et al*., “22 μW, 5.1 ps LSB, 5.5 ps RMS jitter Vernier time-to-digital converter in CMOS 65 nm for single photon avalanche diode array,” Electronics Letters, vol. 56, no. 9, pp. 424–426, 2020, doi: 10.1049/el.2019.4105.

[6] F. Nolet, *et al*., “Time to Digital Conversion,” Dec. 09, 2021 Accessed: Mar. 07, 2022. [Online]. Available: https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2021243451&_cid=P12-L0H3AU-76121-1

[7] V. Sesta, *et al.*, "A novel sub-10 ps resolution TDC for CMOS SPAD array," 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Bordeaux, France, 2018, pp. 5-8, doi: 10.1109/ICECS.2018.8617859.

Backup

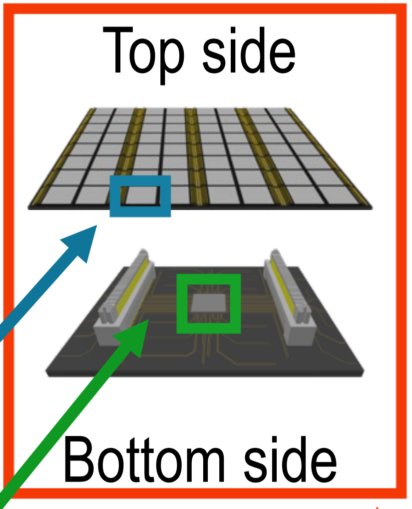
Technique used to obtain precision

1. Subtract the results of the two TDCs
   - Remove the common noise of the acquisition chain
2. Extract the distribution of the subtractions
   - The standard deviation is the combine jitter of the two TDCs
3. Calculate the quadratic average from the combine jitters to get the average precision of the two TDCs

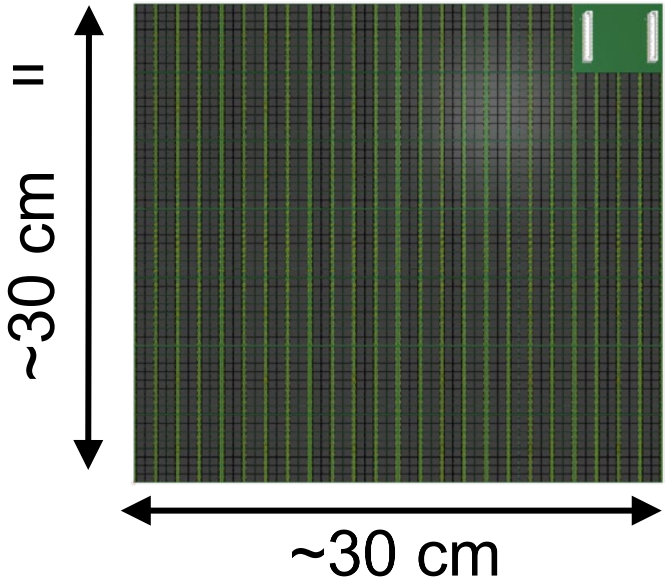
$$\text{Average precision} = \frac{\sqrt{\sigma_1^2 + \sigma_2^2}}{\sqrt{2}} = \frac{\sigma_{global}}{\sqrt{2}}$$

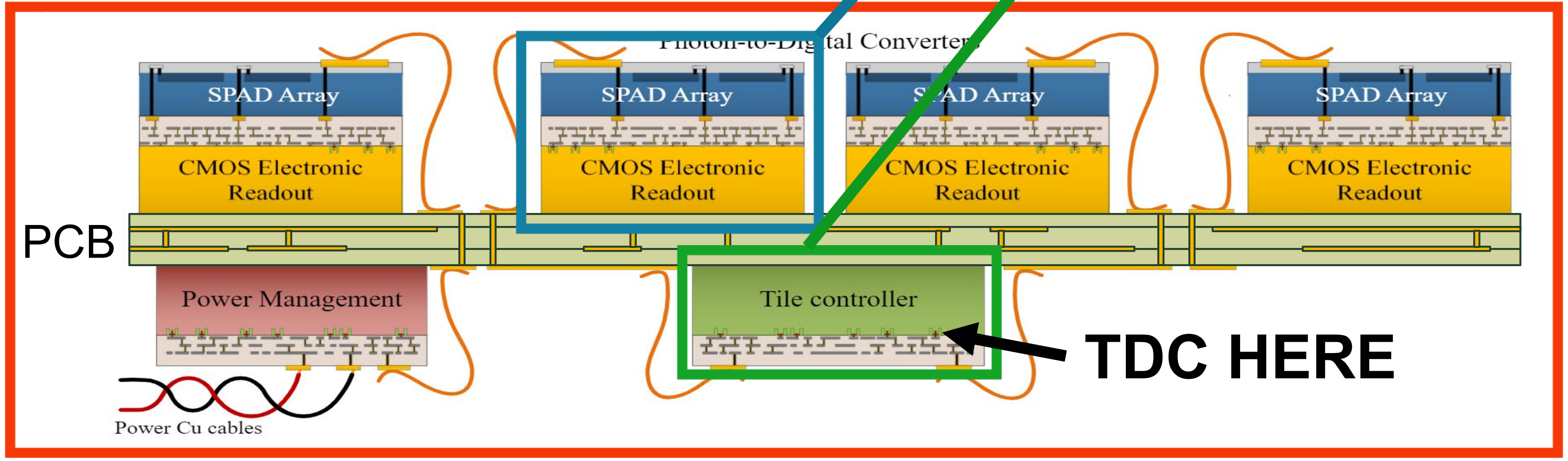
Guillaume.Theberge-Dupuis@USherbrooke.ca

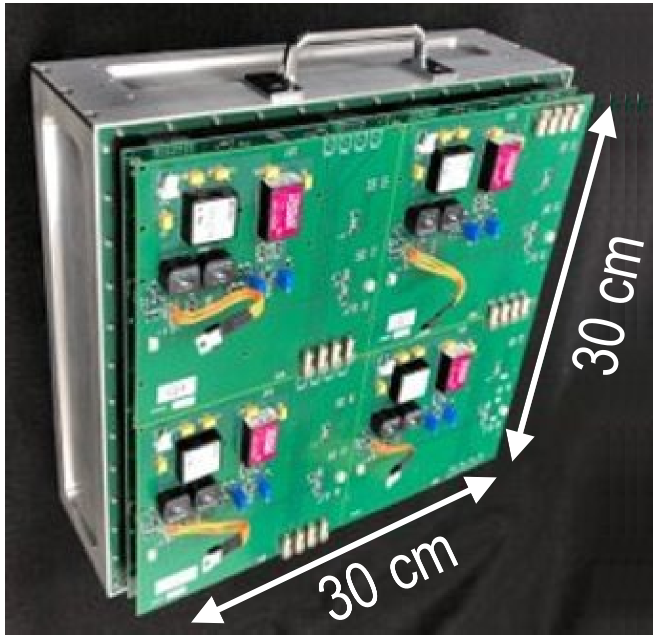
- Difference between gamma ray and neutron
  - Array time of detection on photons ≈ 100 ps
  - Conversion time
- Power consumption



× 42 =



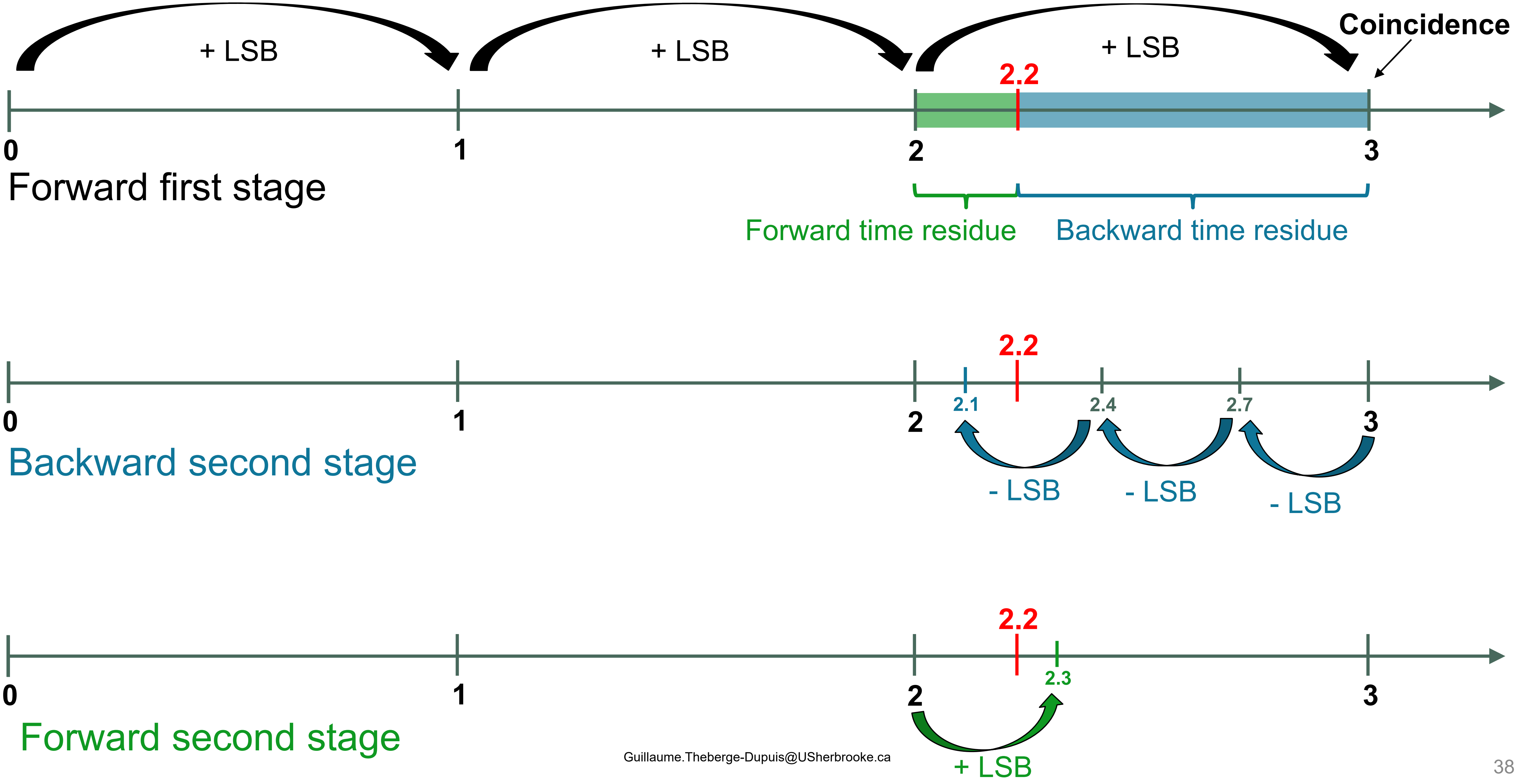




ORNL-developed panel, PMT based (100s W power)

Multiple Stages Vernier-based TDC – Forward Vs Backward

UDS



Guillaume.Theberge-Dupuis@USherbrooke.ca

Uncorrelated results – Comparison at a resolution of 50 ps

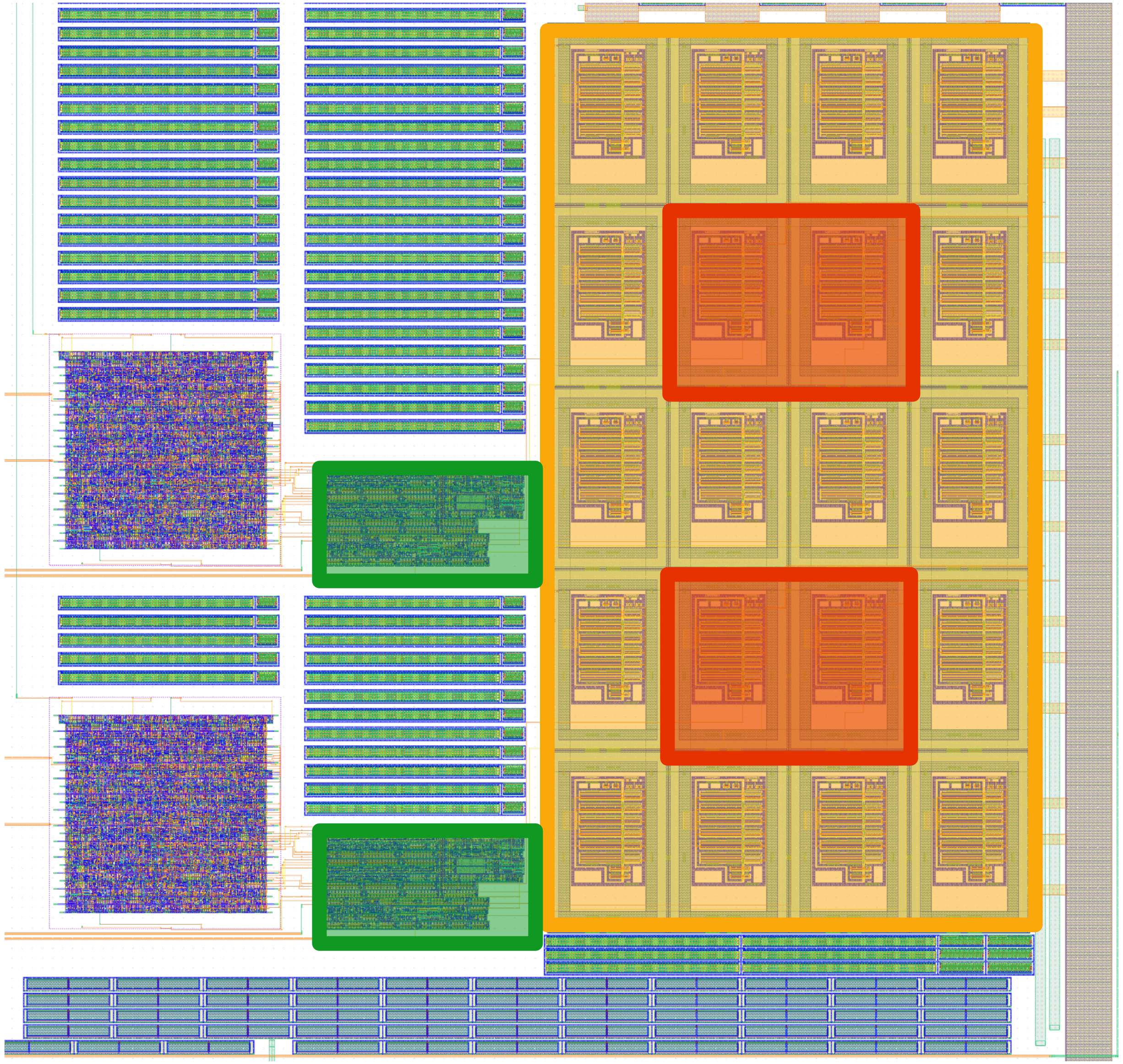
UdS

	LSB (ps)	DNL (LSB) Max	DNL (LSB) RMS	INL (LSB) Max	INL (LSB) RMS	Precision (ps RMS)	Jitter (ps RMS)	Quantization (ps RMS)	Conversion time (ns) Average	Conversion time (ns) Sigma
Single	50	0.53	0.08	1.23	0.08	32.19	28.77	14.43	264.2	139.4
Double	50	0.13	0.04	0.14	0.05	16.16	7.26	14.43	77.5	19.3
Triple	50	0.10	0.03	0.14	0.04	24.05	19.24	14.43	74.2	11.9
Quadruple	46.4	0.32	0.09	0.36	0.14	17.27	10.91	13.39	109.2	11.6

Guillaume.Theberge-Dupuis@USherbrooke.ca

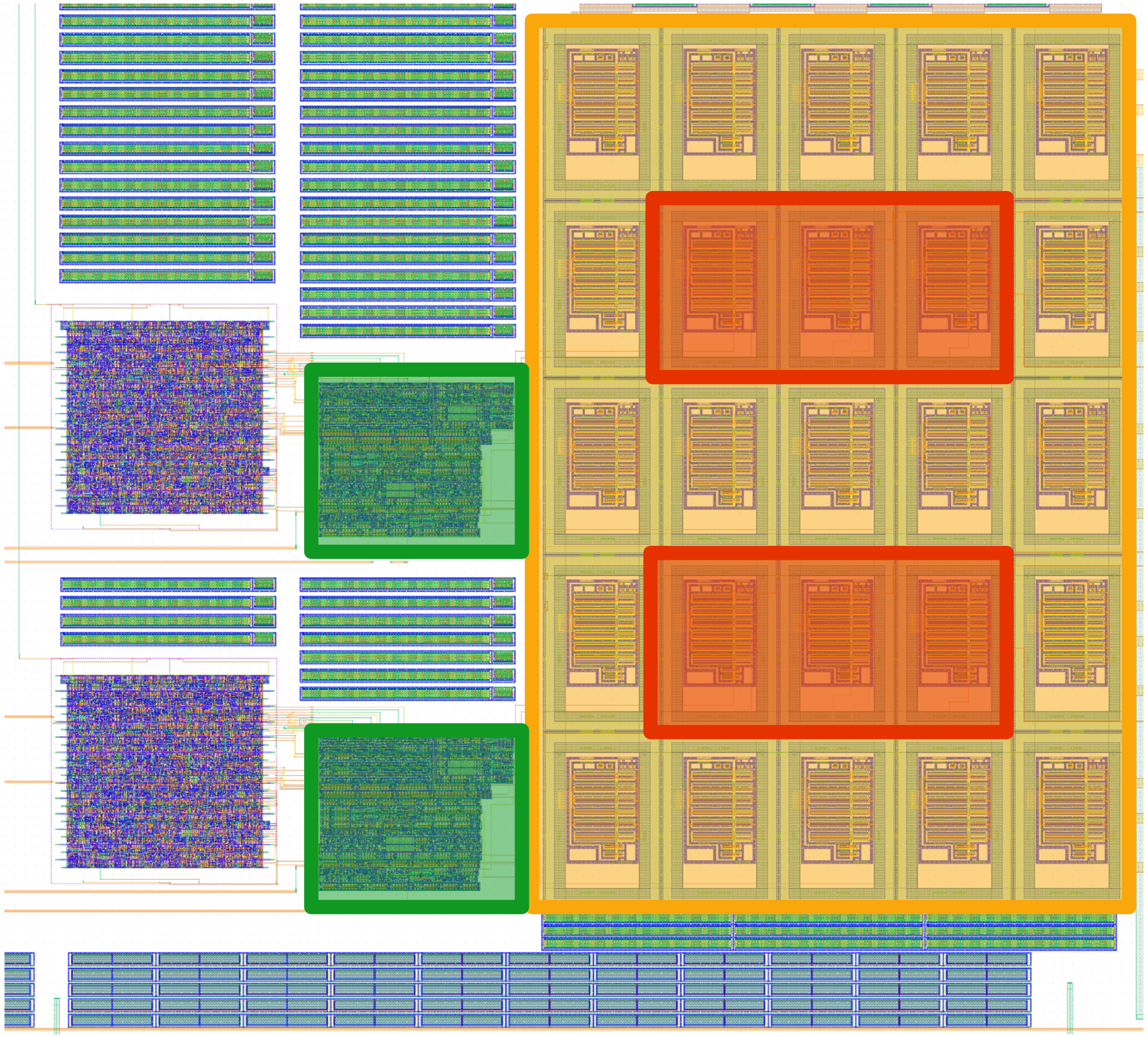
Implementation in TSMC 180 nm - Single Vernier stage

Single Vernier	Area (µm²)
Ring oscillators	10 975
Dummy ring oscillators	54 322
TDC logic	4 334
Area for 1 TDC	



Guillaume.Theberge-Dupuis@USherbrooke.ca

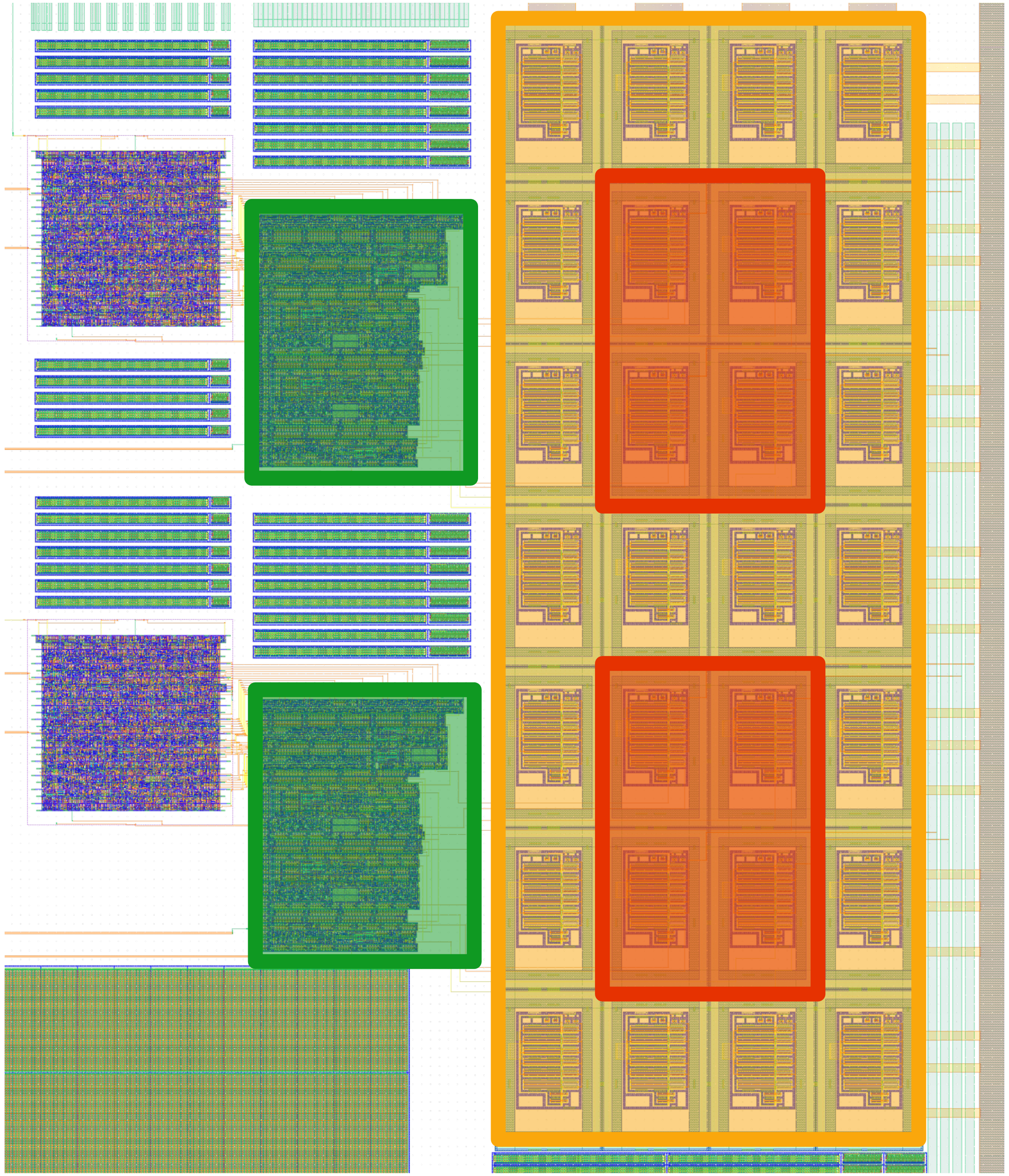
Double Vernier	Area (µm²)
Ring oscillators	16 463
Dummy ring oscillators	65 131
TDC logic	7 067
Area for 1 TDC	



Guillaume.Theberge-Dupuis@USherbrooke.ca

UDS

Single Vernier	Area (µm²)
Ring oscillators	21 952
Dummy ring oscillators	65 069
TDC logic	13 410
Area for 1 TDC	

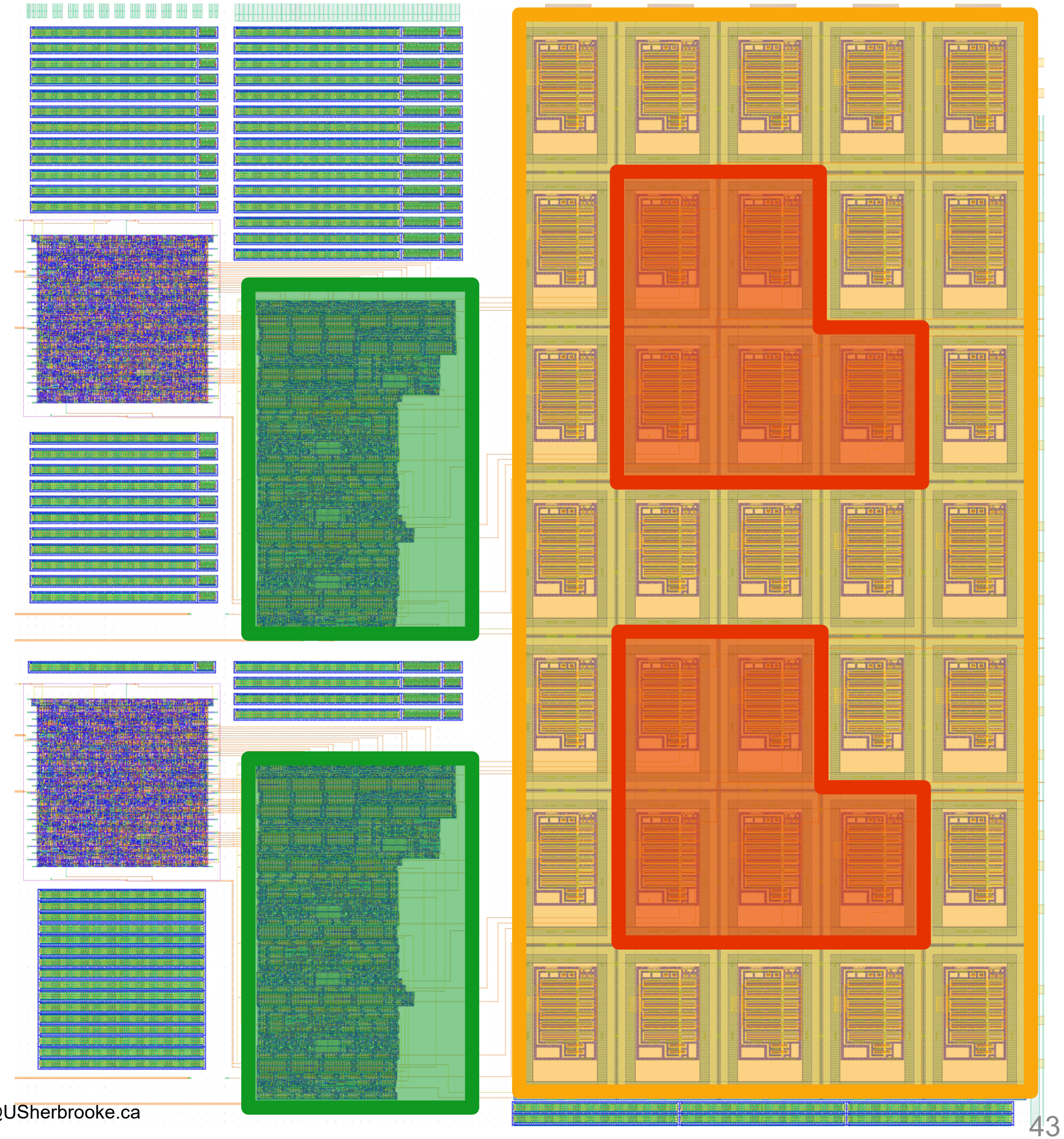


Guillaume.Theberge-Dupuis@USherbrooke.ca

Implementation in TSMC 180 nm - Single Vernier stage

UDS

Single Vernier	Area (μm²)
Ring oscillators	27 438
Dummy ring oscillators	81 306
TDC logic	17 709
Area for 1 TDC	



Guillaume.Theberge-Dupuis@USherbrooke.ca

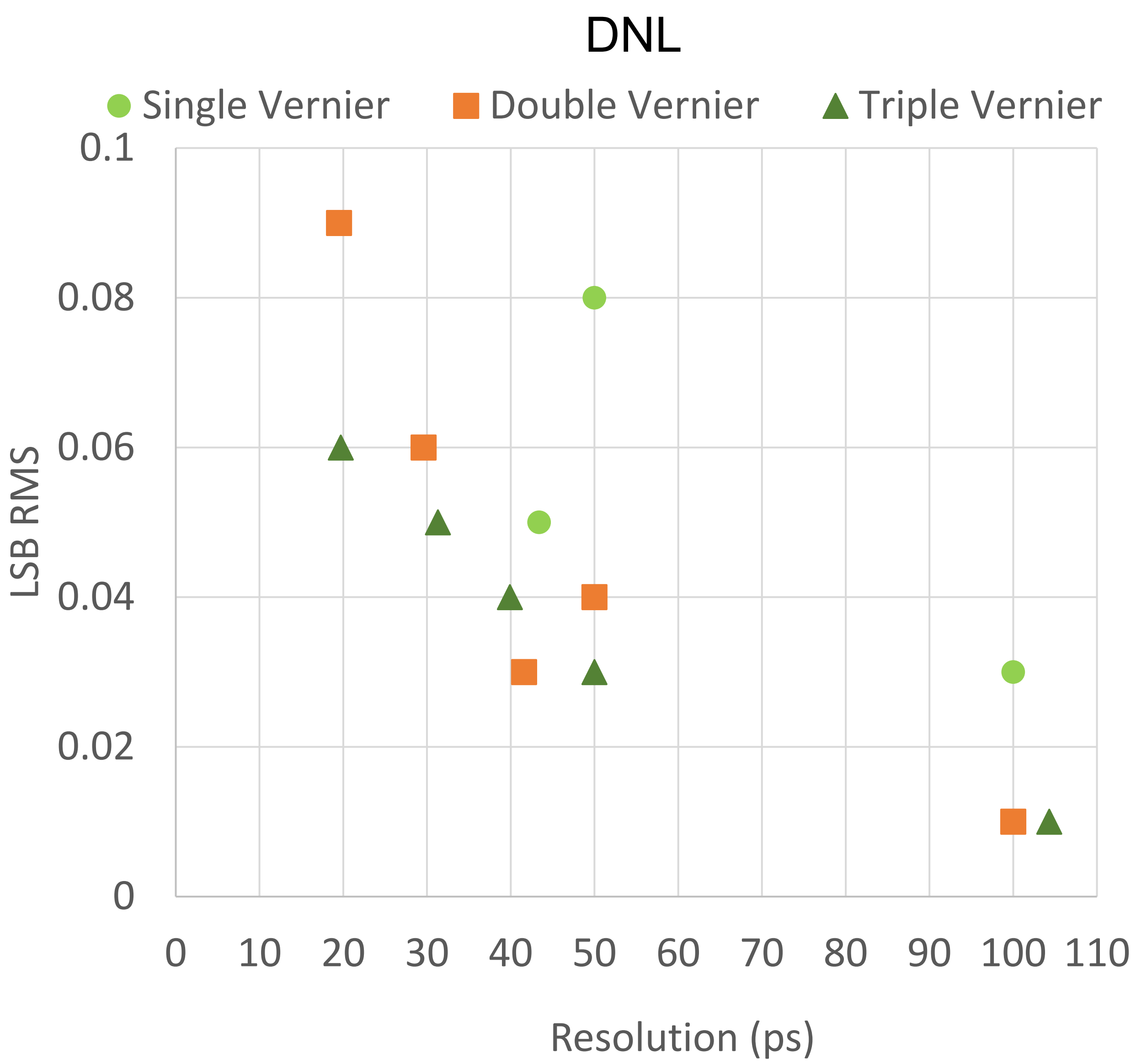
Size of each TDC

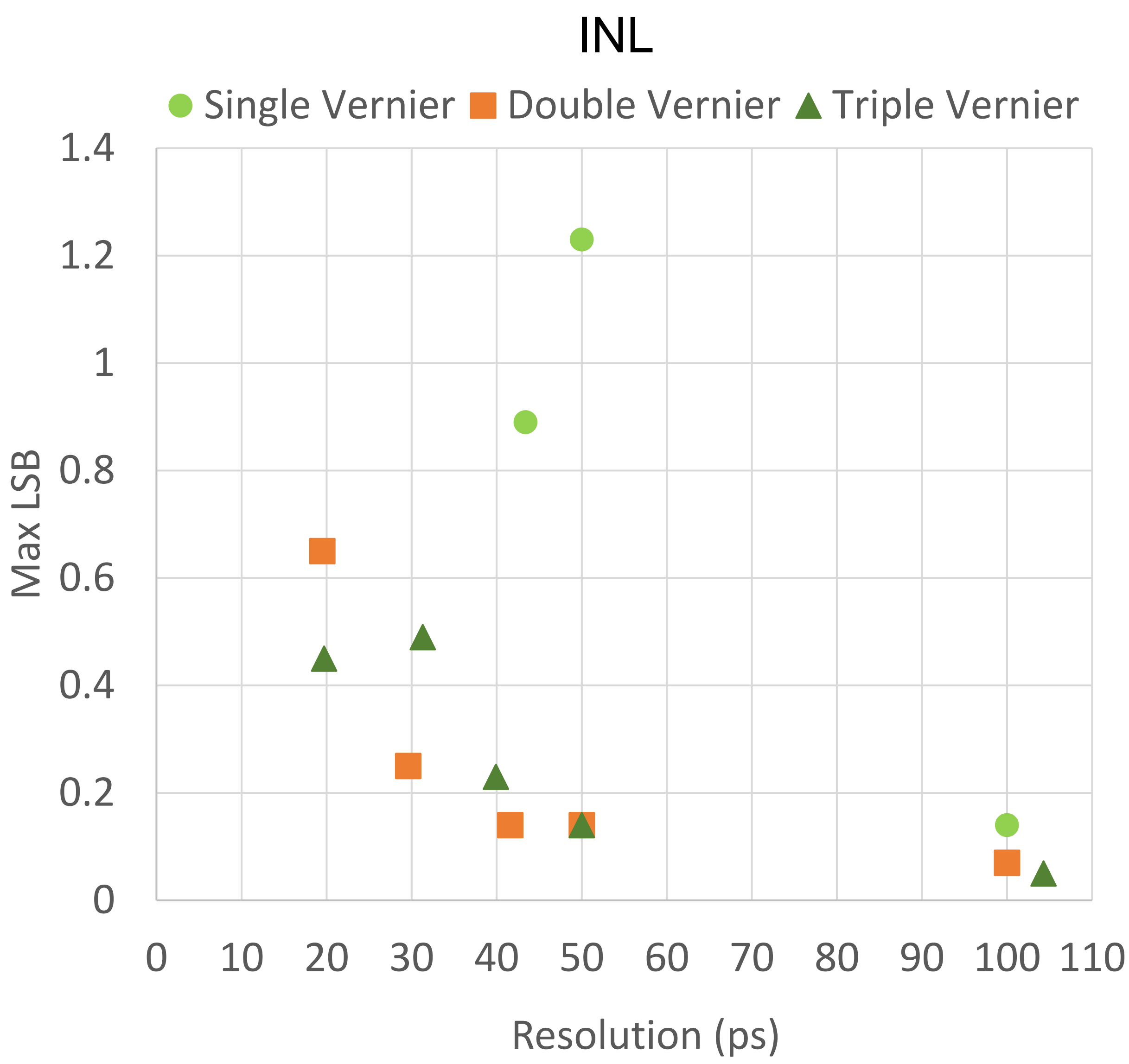
UdS

	Active					+	Dummy ring (µm²)	=	Total (µm²)
	Ring oscillator (µm²)	+	TDC logic (µm²)	=	Subtotal (µm²)				
Single Vernier	10 975		4 334		15 309		54 322		69 631
Double Vernier	16 463		7 067		23 530		65 131		88 661
Triple Vernier	21 952		13 410		35 360		65 069		100 429
Quadruple Vernier	27 438		17 709		45 470		81 306		126 453

Evolution of DNL and INL on resolution for the different architectures (dynamic range = 20ns)

UdS

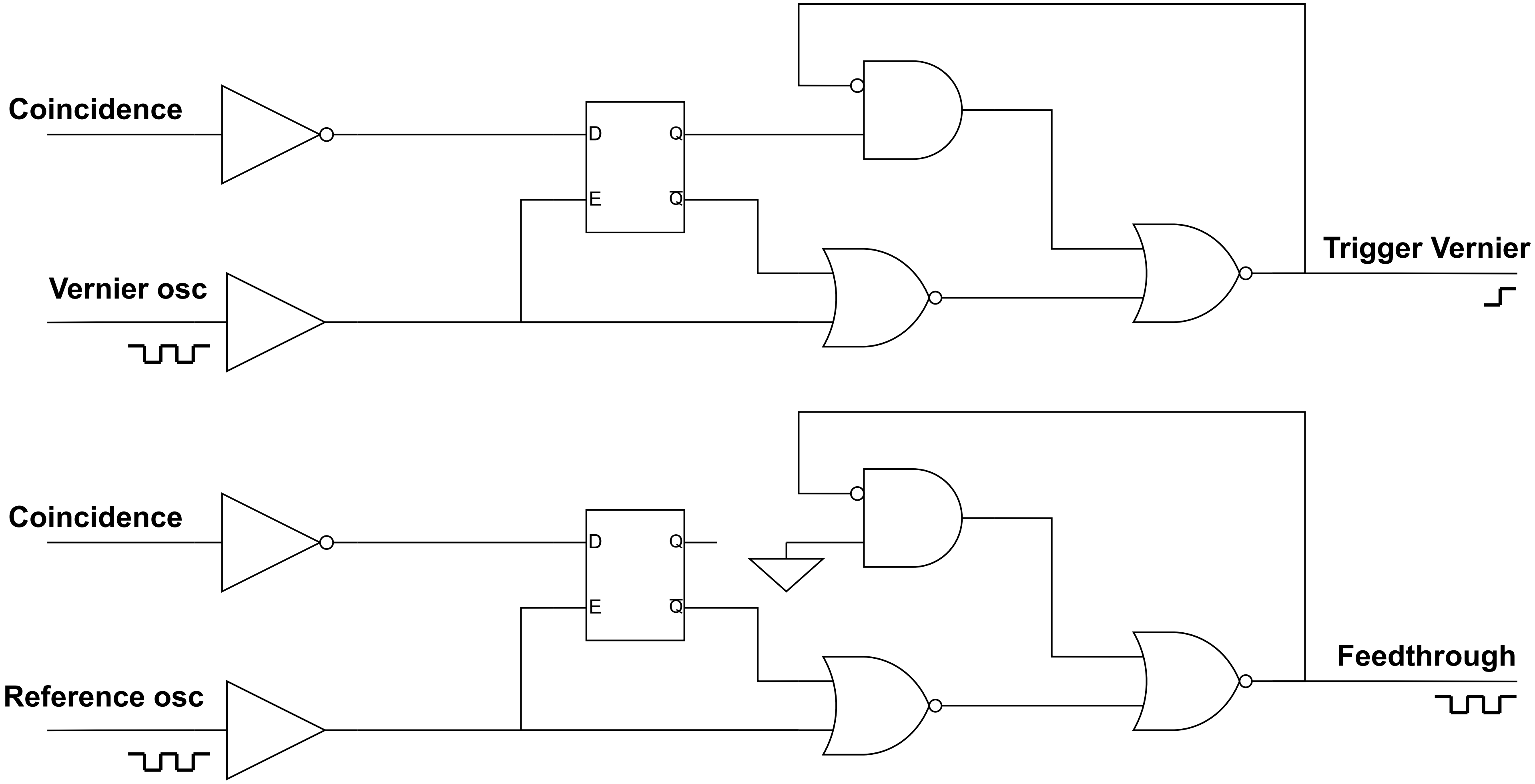




Guillaume.Theberge-Dupuis@USherbrooke.ca

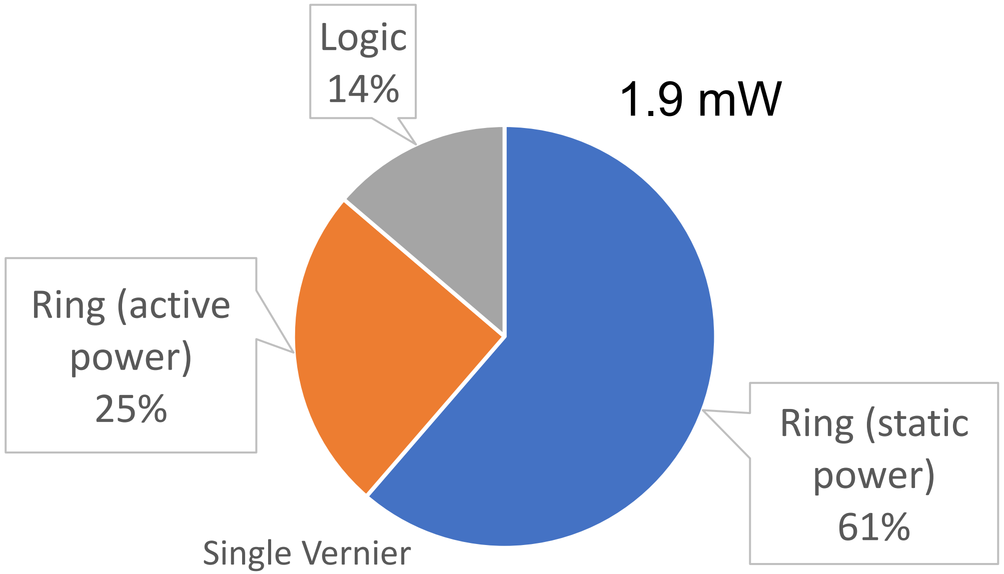
Feedthrough and Trigger

UdS

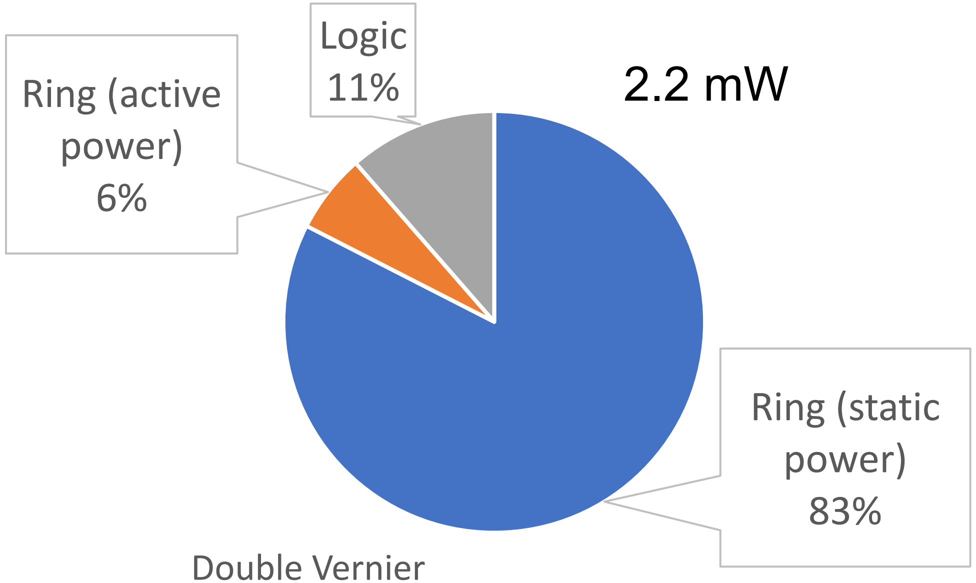


Guillaume.Theberge-Dupuis@USherbrooke.ca

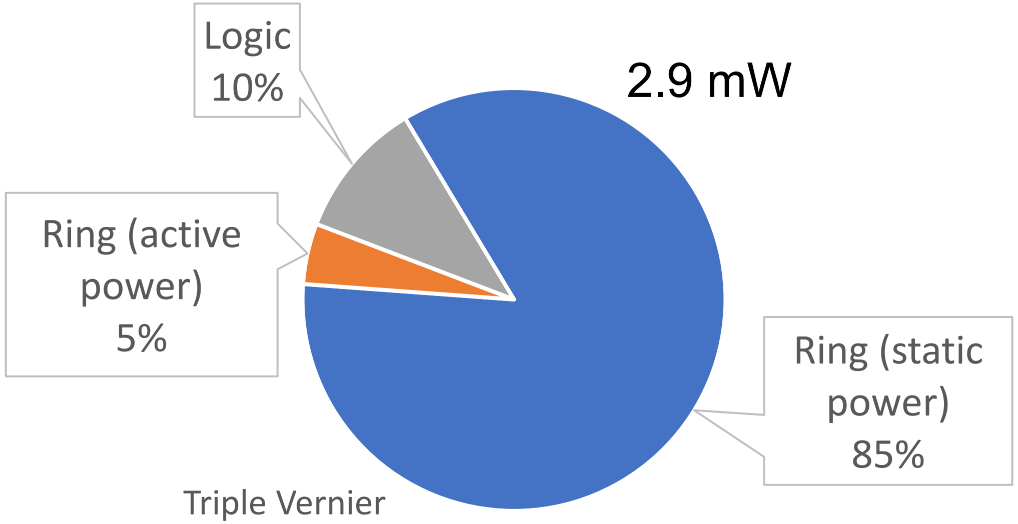
Origin of the power consumption



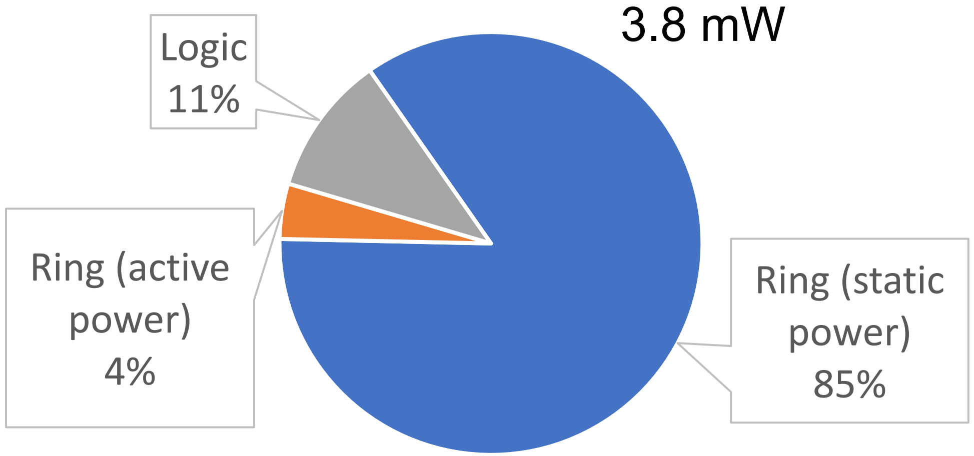
Single Vernier



Double Vernier



Triple Vernier



Quadruple Vernier

Guillaume.Theberge-Dupuis@USherbrooke.ca

Origin of the power consumption – Table

Power (mW)	Logic	Ring oscillator (active)	Ring oscillator (static)	Total (active)	Total
Single Vernier	0.26	0.47	1.16	0.73	1.89
Double Vernier	0.25	0.13	1.81	0.38	2.19
Triple Vernier	0.31	0.14	2.48	0.45	2.93
Quadruple Vernier	0.41	0.16	3.26	0.57	3.83

UdS

The constraint we want to minimize is the summation of turns of each stage, so we have:

$$f(x, y, z, \cdots, n) = x + y + z + \cdots + n$$

where each variable is the cycle count of the stage

The other constraint is the total different codes (C), which is given by:

$$g(x, y, z, \cdots, n) = x \times y \times z \times \cdots \times n = C$$

By the Lagrange theorem, we know that we are at a maxima or minima when:

$$\nabla f = \lambda \nabla g$$

For 2 stages and 1 coarse counter (3 total stages) we have:

$$\nabla f = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \lambda \begin{bmatrix} yz \\ xz \\ xy \end{bmatrix} and\ xyz = C$$

To minimize $f(x, y, z)$, we have $x = y = z = \sqrt[3]{C}$

Lagrange multiplier – Other examples

UDS

For 3 stages and 1 coarse counter (4 total stages) we have:

$$\nabla f = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} = \lambda \begin{bmatrix} xyz \\ wyz \\ wxz \\ xyw \end{bmatrix} and\ wxyz = C$$

To minimize $f(x, y, z)$, we have w $= x = y = z = \sqrt[4]{C}$

For 4 stages and 1 coarse counter (5 total stages) we have:

$$\nabla f = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} = \lambda \begin{bmatrix} wxyz \\ vxyz \\ vwyz \\ vwxz \\ vxyw \end{bmatrix} and\ vwxyz = C$$

To minimize $f(x, y, z)$, we have w $= x = y = z = \sqrt[5]{C}$

Guillaume.Theberge-Dupuis@USherbrooke.ca