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Low power, high accuracy ADCs and TDCs

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Outline

- 10b ADC in CMOS 130nm and 65nm
  - Motivation
  - Architecture considerations
  - ADC design
  - Measurement results
    - Static and dynamic metrics
    - Power consumption
    - Radiation hardness

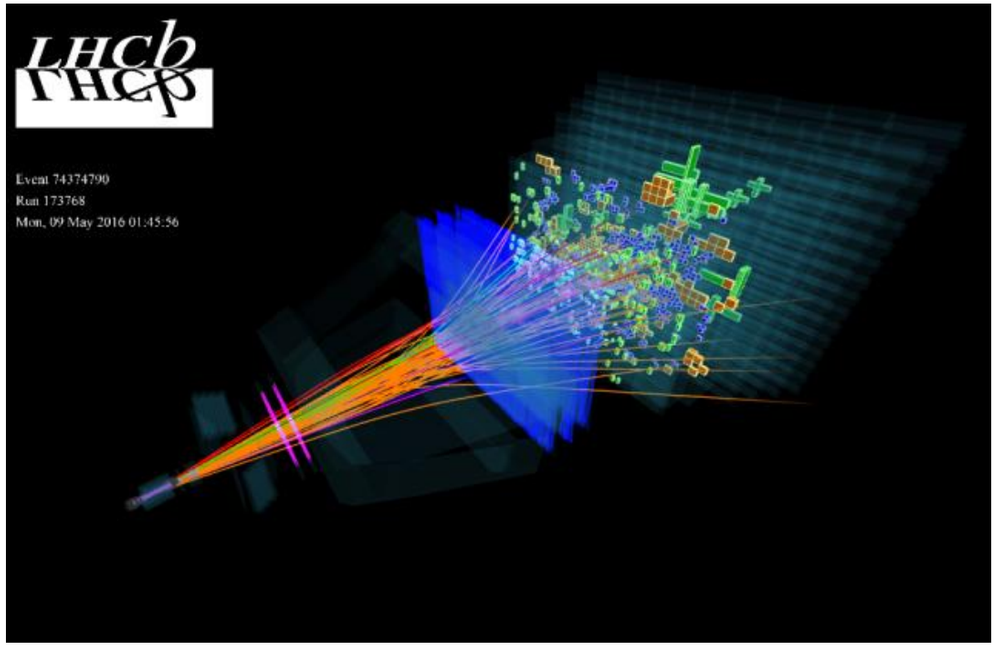
- TAC (Time to Analogue Converter)-based TDC
  - Architecture and design
  - Post-layout simulation results
  - ~~Measurement results~~ (*no data yet…)*

- Summary

Motivation – High Energy Physics experiments

Demands for readout electronics in high energy physics experiments are constantly rising:

- Higher luminosity – more events – more data
- Calorimetry – needs amplitude measurement and digitization:
  - ADC (FE pulse maximum)
  - TDC (FE pulse time over threshold)



- Increasing complexity of event reconstruction starts to require:
  - Amplitude measurements in trackers (e.g. Upstream Tracker in LHCb)
  - 4-D detectors (pixel detector with precise timing measurement) *not in scope of this talk*

- Putting an ADC in each readout channel fairly not possible in the past:
  - Large power consumption (much higher than analogue FE)
  - Large die area

ADC

ADC FoMs (Figure of Merit)

Various features/parameters are important in ADC design/applications: effective resolution (ENOB), power, sampling frequency, area, etc... and can be used to create the “Figure Of Merit” (FOM) for ADC

- Walden FoM [Walden, 1999)

$$FoM_W = \frac{P}{f_s \cdot 2^{ENOB}}$$

- Schreier FoM (DR) [Schreier, 2005]

$$FoM_{S,DR} = DR + 10log\left(\frac{BW}{P}\right)$$

- Schreier FoM (SNDR) [Ali, 2010]

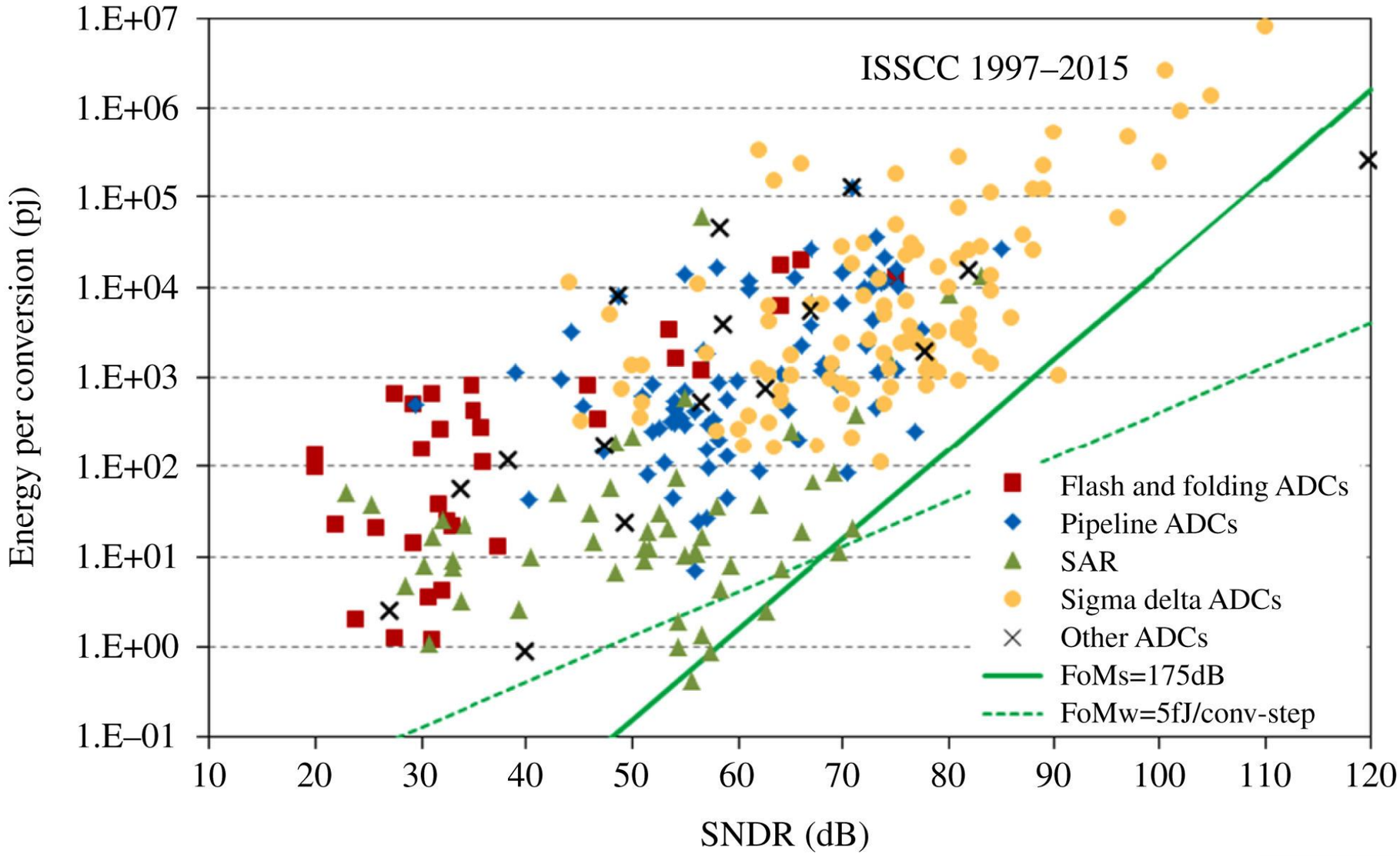
$$FoM_S = SNDR + 10log\left(\frac{f_s/2}{P}\right)$$

FoM_W is often given as:

- FoM_W^{hf}, measured at input sine with almost Nyquist frequency
- FoM_W^{lf}, measured at lower input frequency

Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications, Boris Murmann
https://github.com/bmurmann/ADC-survey/blob/main/pdf/ISSCC2022-Short%20Course-Murmann.pdf

ADC architectures State of the Art – FoM

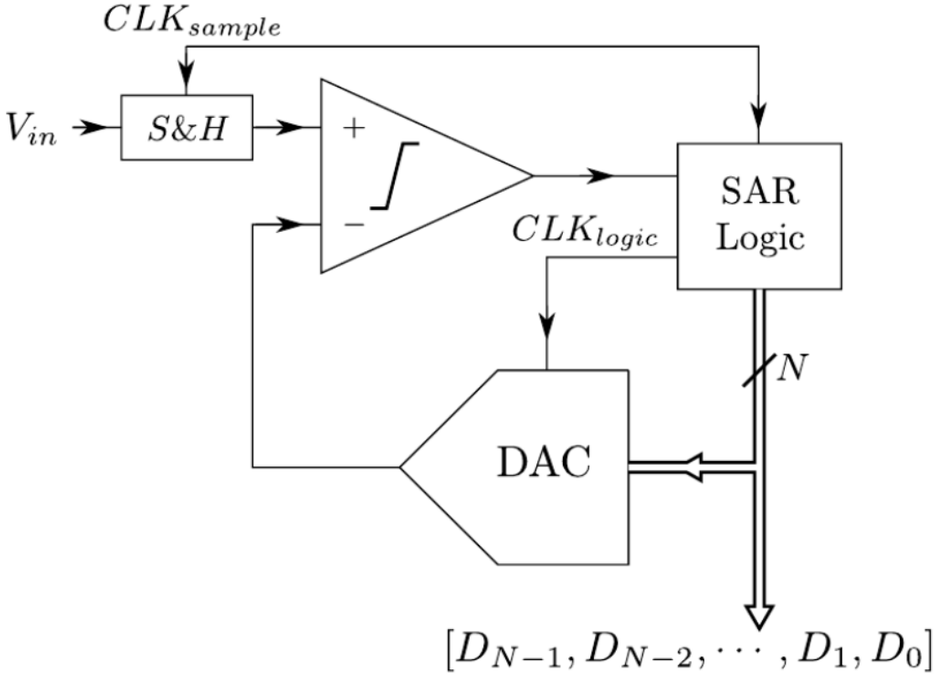


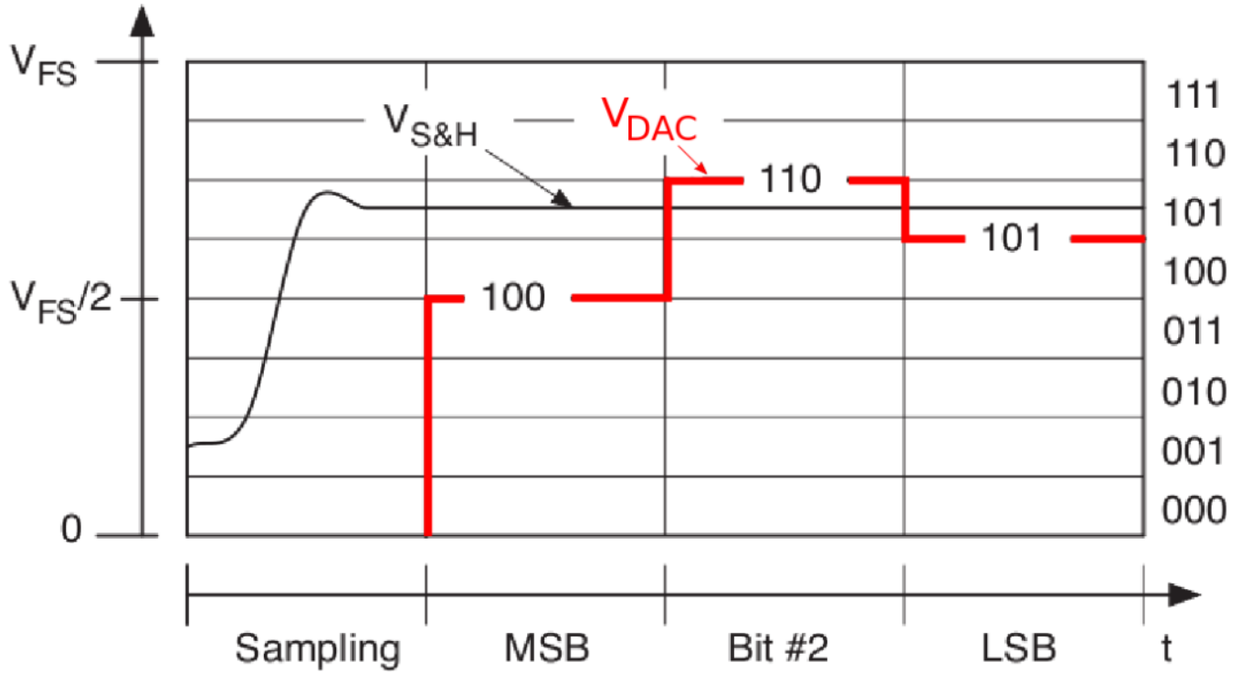
3b 6b 8b 10b 13b 16b

ENOB

ADC Performance Survey 1997-2015, B. Murmann
http://web.stanford.edu/~murmann/adcsurvey.html

SAR – principles of operation





- Comparison between sampled input voltage and DAC output voltage
- Comparison result → changes DAC output voltage closer to the input sample
- Each consecutive voltage change is half of the previous one
- Operation repeated N times for N-bit ADC

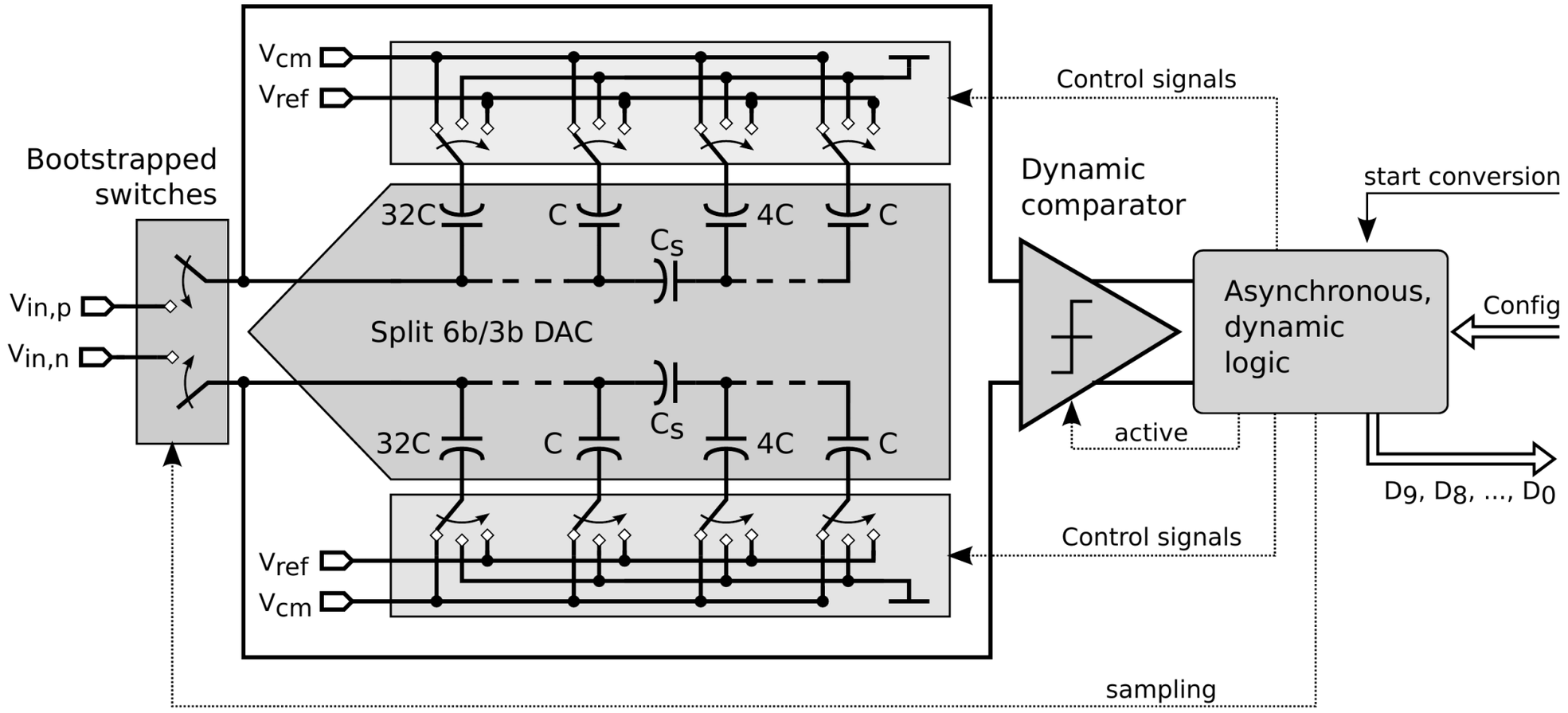
\+ Power and area-efficient architecture – same circuitry used in loop N-times

\+ Contains: one comparator, two DACs (differential) and SAR logic – fits well to modern digital CMOS

\+ DAC network usually capacitive - no static power, serves also as S/H circuit

\- Limited conversion rate

SAR ADC architecture

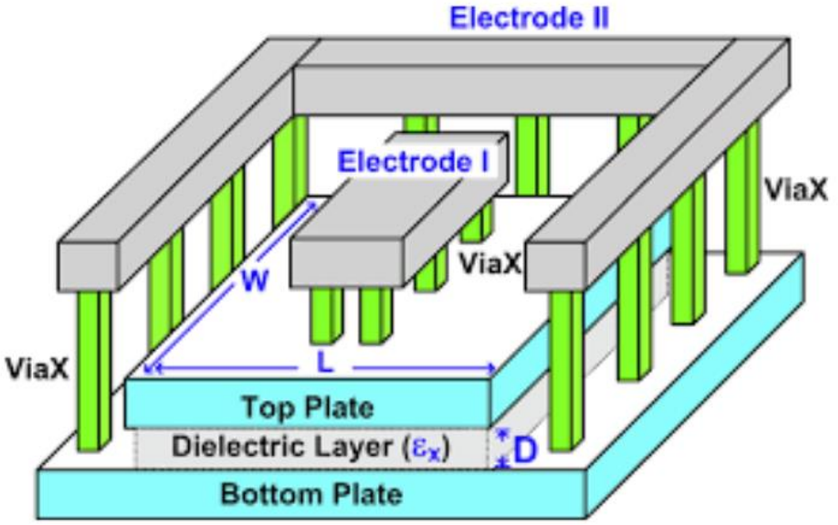


Architecture of 10-bit ADC

- Differential segmented/split DAC with MCS switching scheme – ultra low power
- Dynamic comparator – no static power consumption, power pulsing for free
- Asynchronous logic – no clock tree – power saving, allows asynchronous sampling

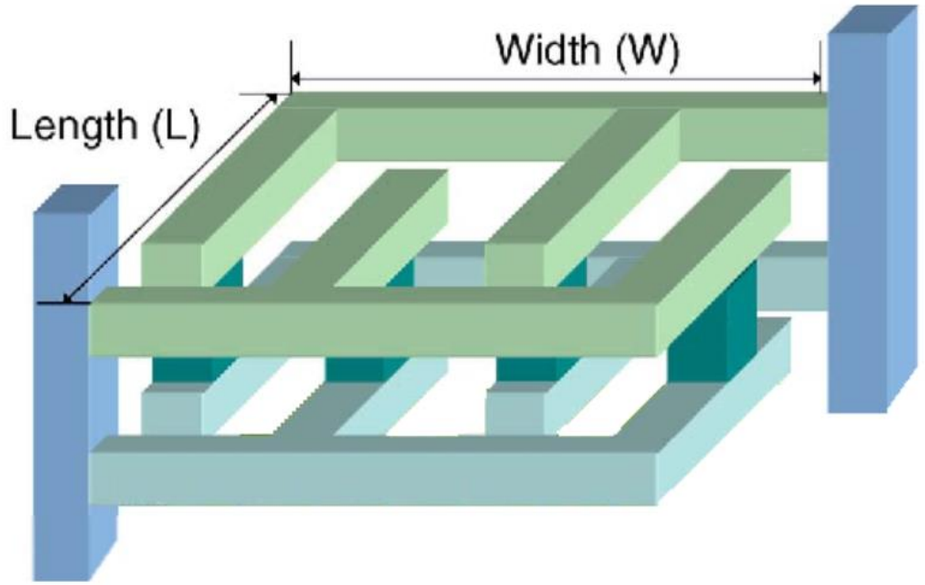
Capacitive DAC design – capacitance selection

Planar capacitor – MIMcap



- Available in both technologies
- Lower capacitance density
- Well defined matching parameters
- Smaller parasitics (especially to bulk)
- Minimal capacitance
  - 26.2 fF in CMOS 130 nm
  - 9.9 fF in CMOS 65 nm

Vertical capacitor – MOM



- Available only in CMOS 65 nm
- Higher capacitance density
- Matching given by MC simulations
- Large parasitics (especially to bulk)
- Minimal capacitance of 2.5 fF

Capacitive DAC design – thermal noise

Two subjects have to be considered in terms of capacitive DAC design:

- Thermal noise
- Matching

Thermal noise is given by

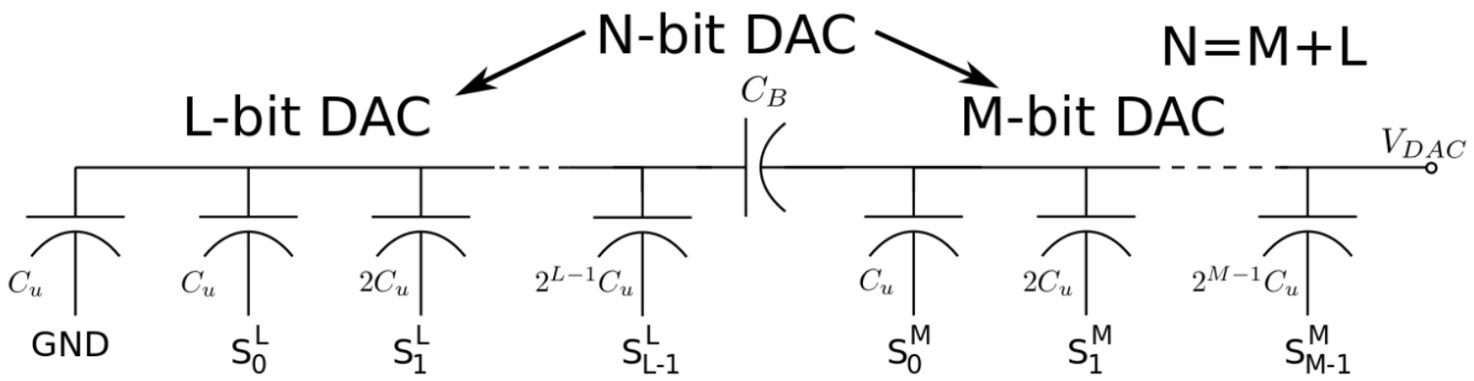
$$\frac{kT}{C_{total}} < \frac{\sigma^2}{12}, \qquad \sigma = \frac{V_{ref}}{2^N} \qquad \Rightarrow \qquad C_{total} > 12kT\left(\frac{2^N}{V_{ref}}\right)^2$$

For V_{ref} = 1 V, T = 293 K

- N = 6b, C > 0.2 fF
- N = 8b, C > 3.2 fF
- N = 10b, C > 51 fF
- N = 12b, C > 815 fF
- N = 16b, C > 209 pF

Thermal noise is negligible for medium resolution ADC

Capacitive DAC design – split DAC



To reduce total capacitance, N-bit DAC can be split into two sub-DACs, connected via series unit capacitor

$$C_u > \frac{9}{2\sqrt{2}\sigma_{Limit}^2} 2^{2L}(2^M - 1)K_\sigma^2 K_C$$

$K_\sigma\ [\%\mu m]$ Matching parameter

$K_C \left[\frac{fF}{\mu m^2}\right]$ Capacitance density

C_u – minimal unit capacitance ensuring $3\sigma_{DNL} < \sigma_{Limit}$ (0.5 LSB assumed)

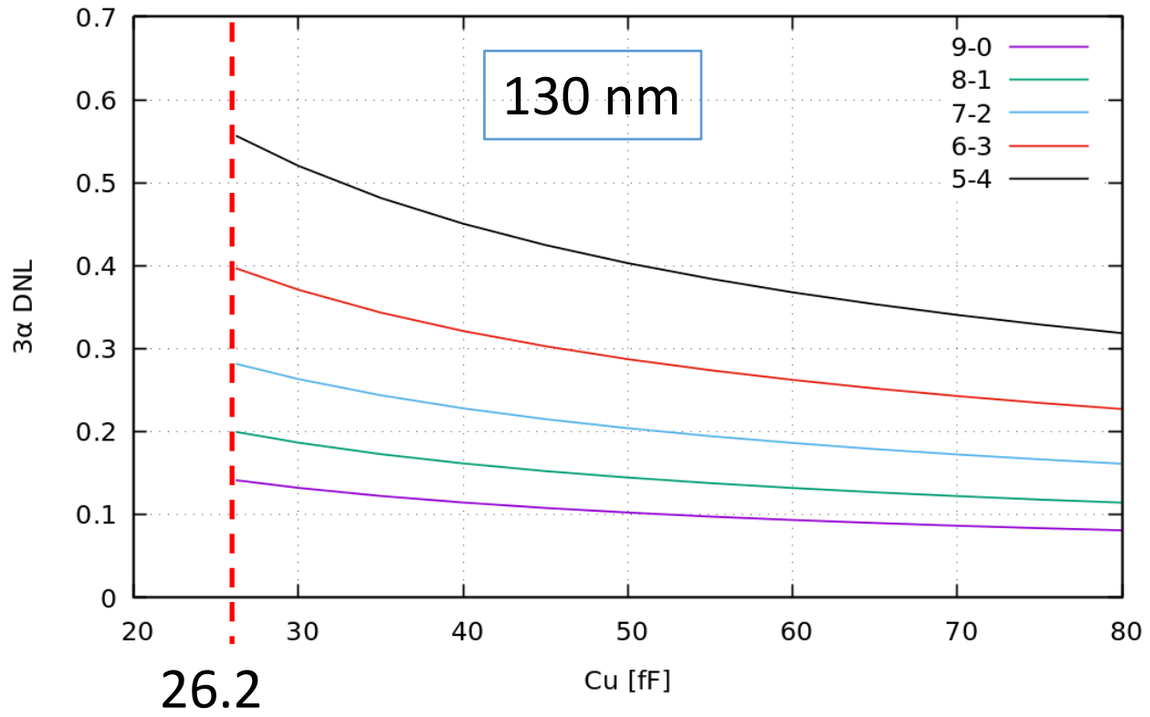
C_u cannot be smaller, than the technology limit

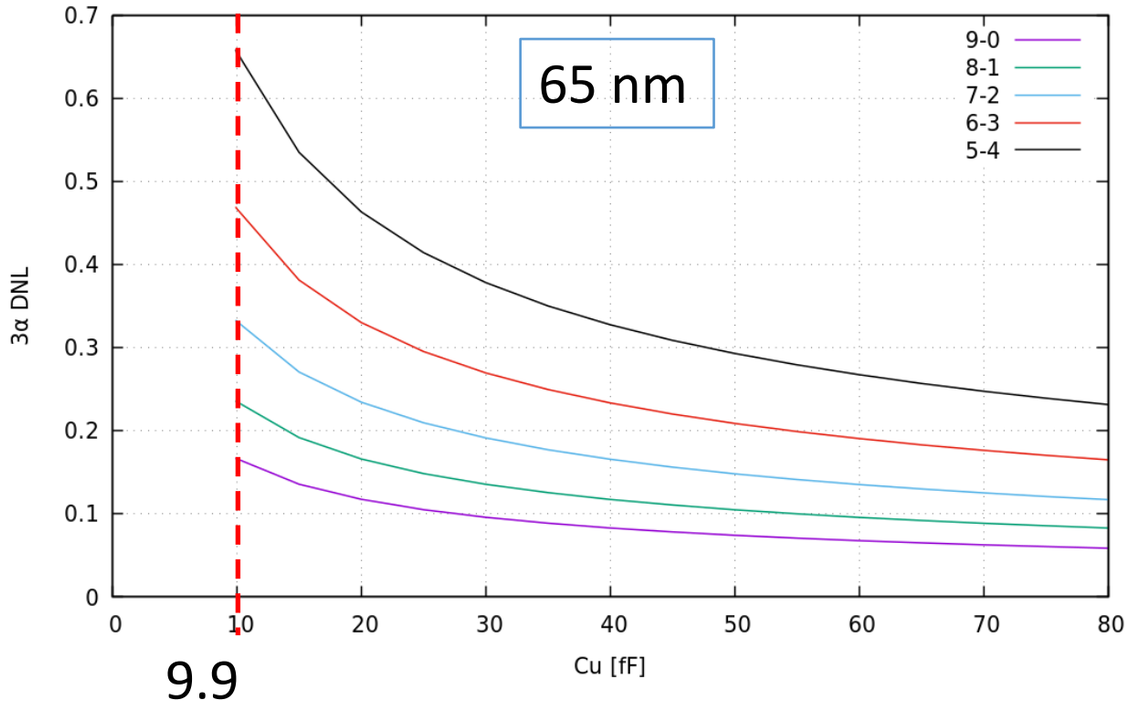
D. Zhang, Design of Ultra-Low-Power Analog-to-Digital Converters. Linköping University, 2012.

Capacitive DAC design – matching

65 nm offers ~2.5 smaller minimal capacitance (9.9 fF vs 26.2 fF)
130 nm offers a slightly better matching

- 6-1-3 and 5-1-4, both with minimal 26.2 fF capacitor as C_u configurations selected for 130 nm
- 6-1-3 with minimal 9.9 fF capacitor as C_u selected for 65 nm



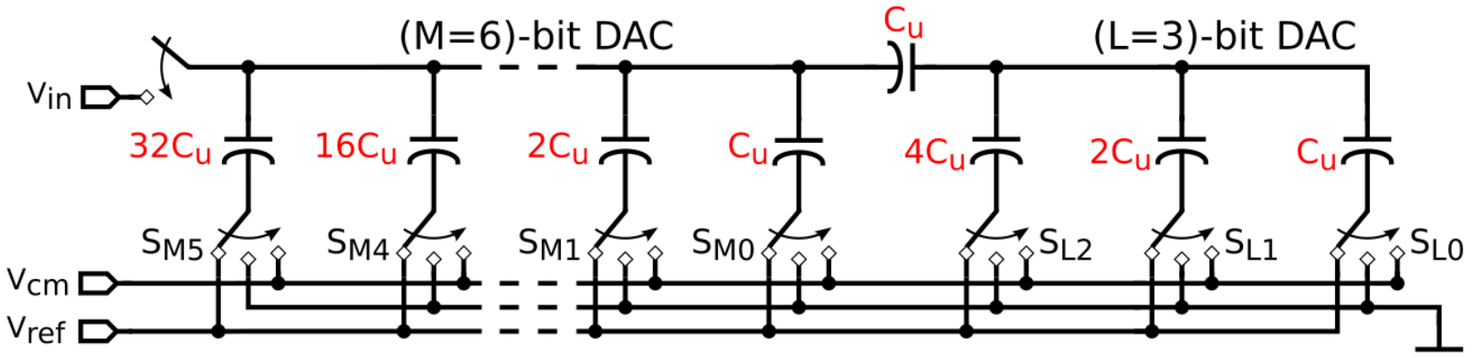


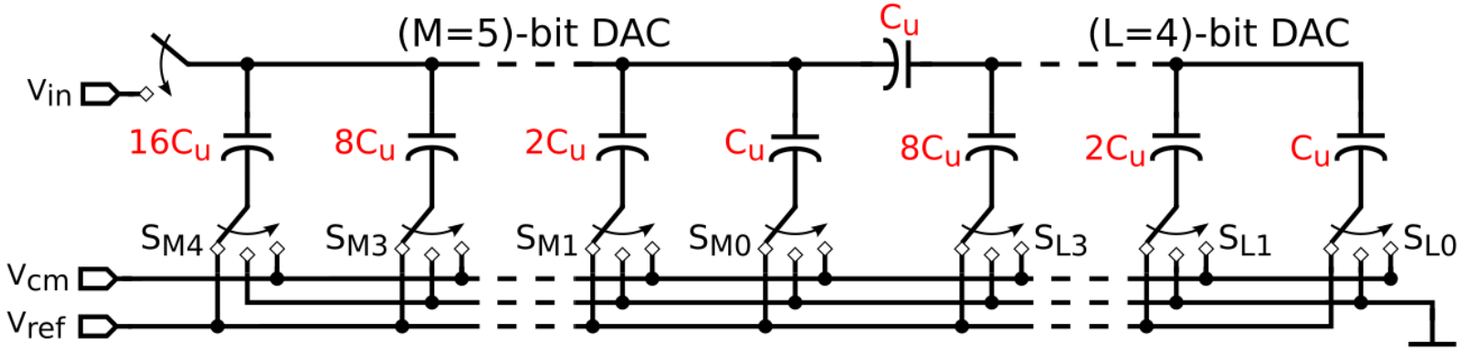
Selected capacitive DAC architectures

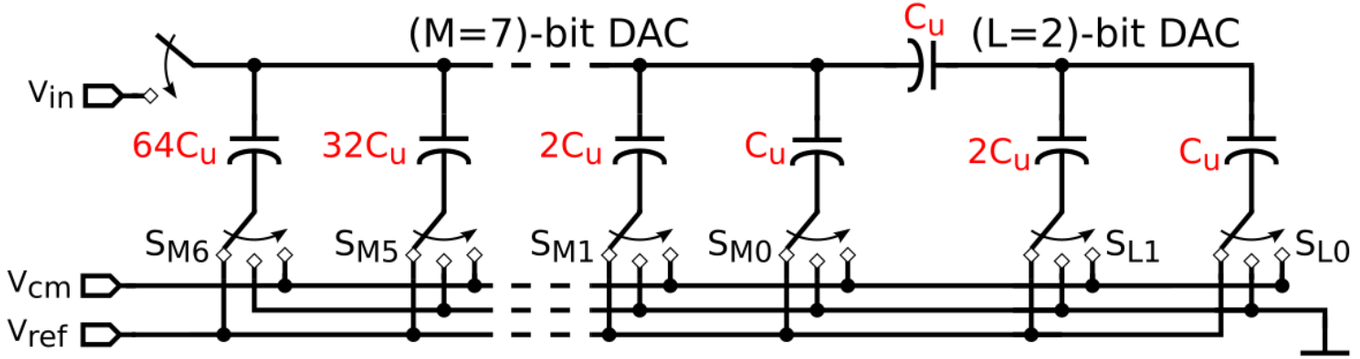
- **DAC 613 MIMcap**
  130nm / 65nm
  C_u = 26.2 / 9.9 fF
  C_{in} = 1.68 / 0.64 pF

- **DAC 514 MIMcap**
  130nm only
  C_u = 26.2 fF
  C_{in} = 0.84 pF

- **DAC 712 MOMcap**
  65nm only
  C_u = 4.6 fF
  C_{in} = 0.59 pF



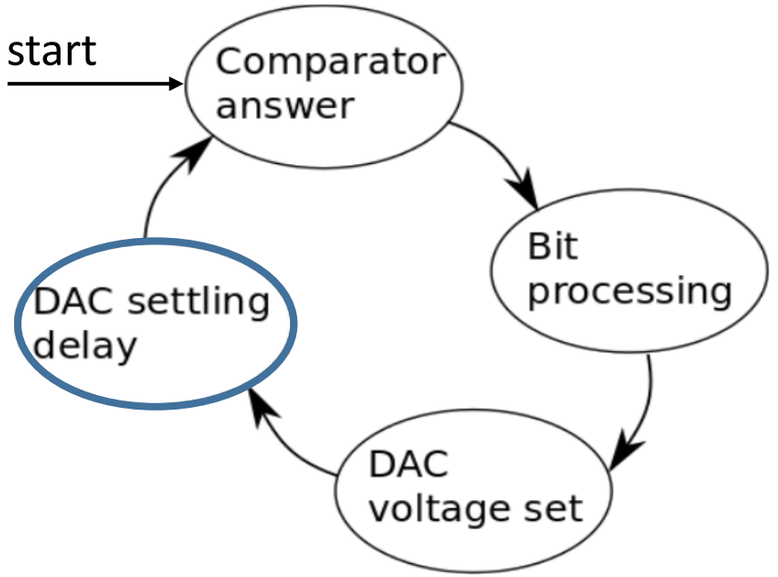




SAR asynchronous logic

"Typical" SAR ADC requires bit cycling clock

- For 10b ADC working at 50 MSps, at least 500 MHz (1 GHz in reality) needed



Such bit cycling clock have to be generated (PLL) and distributed in the ASIC – large power consumption.

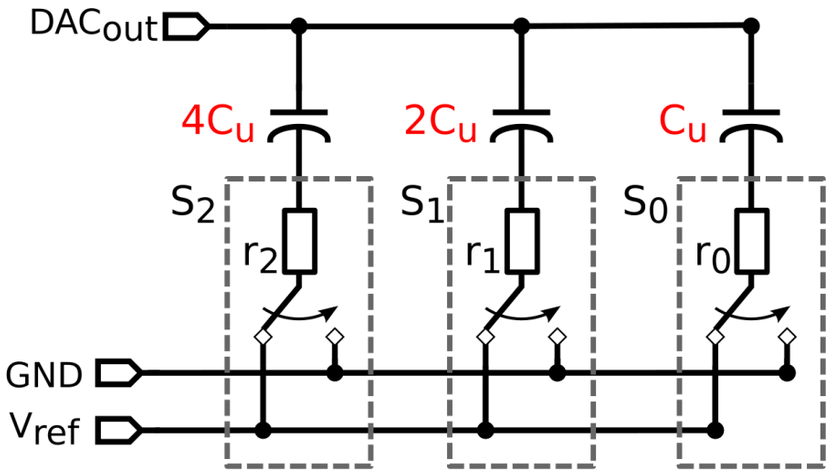
Asynchronous, "event-driven" logic does not need bit cycling clock, so can save a lot of power.

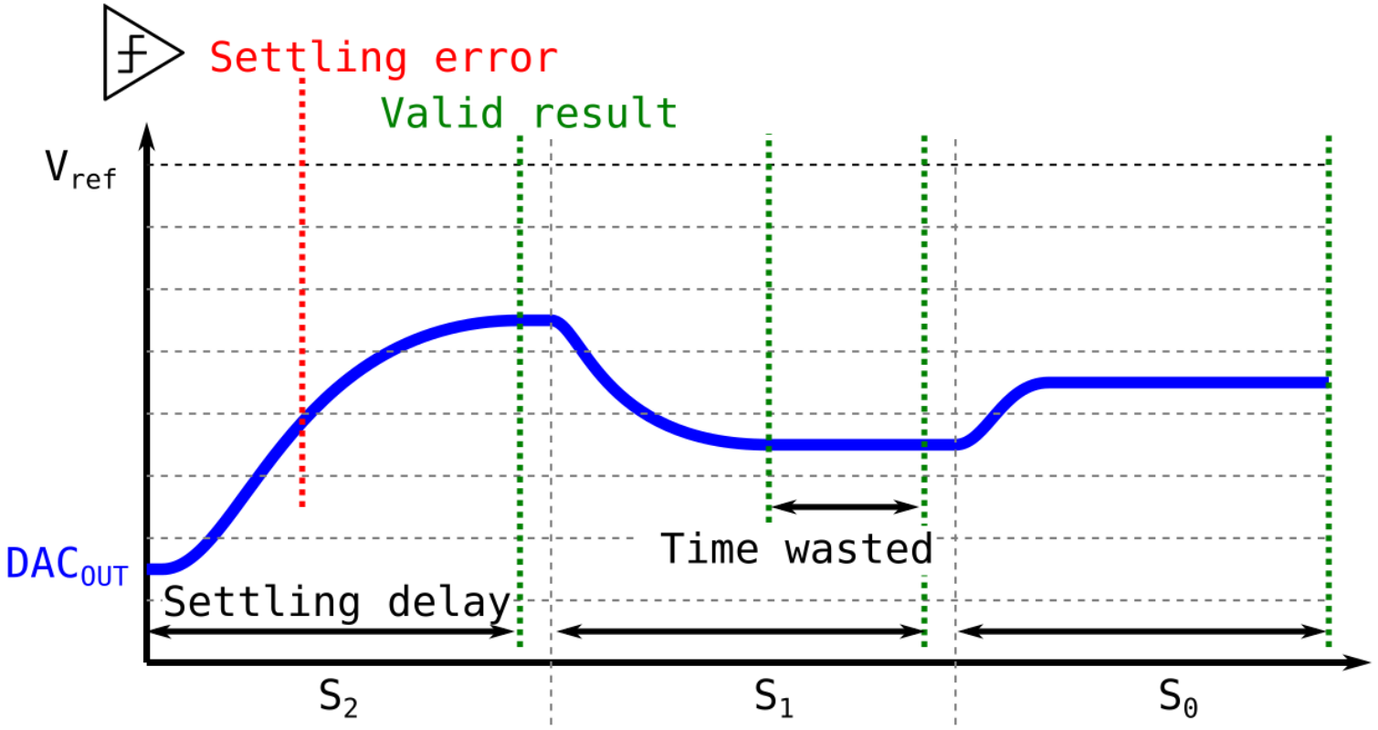
Additionally, asynchronous logic requires a "start conversion" signal, not a sampling clock, so ADC can sample input signal asynchronously.

There are two downsides of the asynchronous logic:

- It have to be designed and simulated manually (no automatic synthesis and implementation)
- It needs to have a "settling delay" (see next slide) implemented

SAR asynchronous logic – settling delay



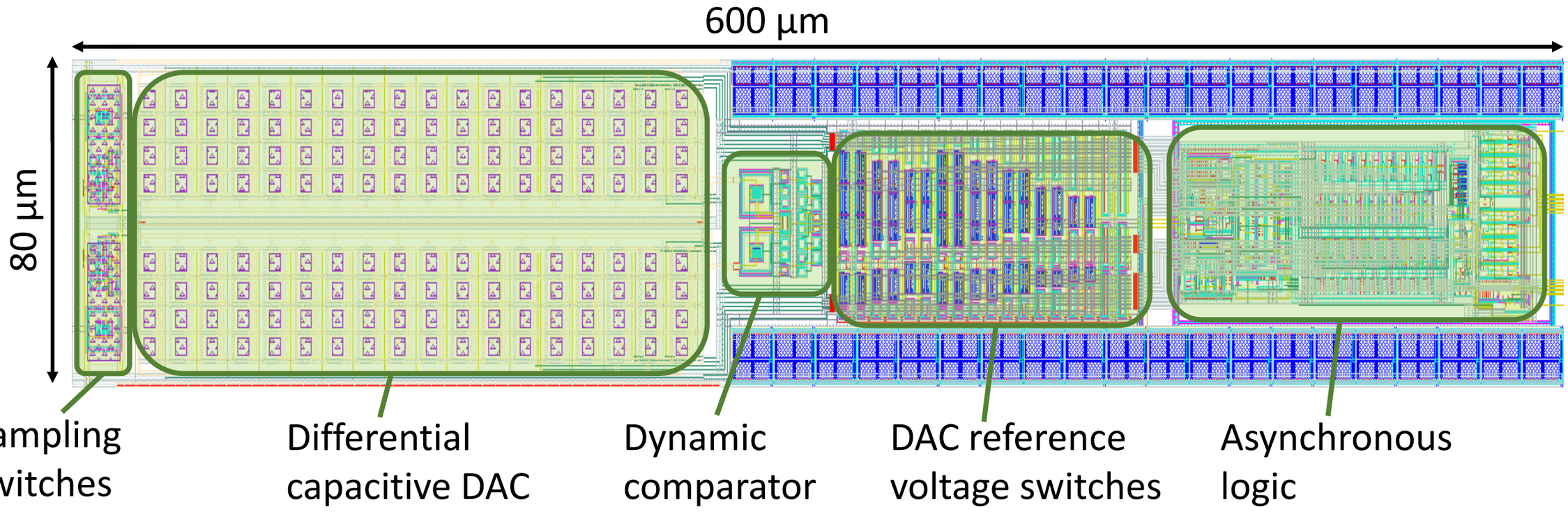


- Making settling time equal for each bit almost impossible
- Constant settling delay for each bit → a lot of time wasted...
- Variable (and configurable) settling delay implemented

Bit no.	9	8	7	6	5	4	3	2	1
Group	D9	D87		D65		D41			

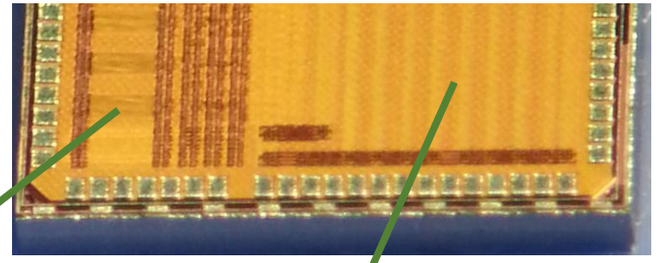
Delay for each group set individually via slow control 3-bit register, with 175 ps/bit resolution in 130nm, ~120 ps/bit in 65nm

SAR ADC layout – 130nm CMOS technology

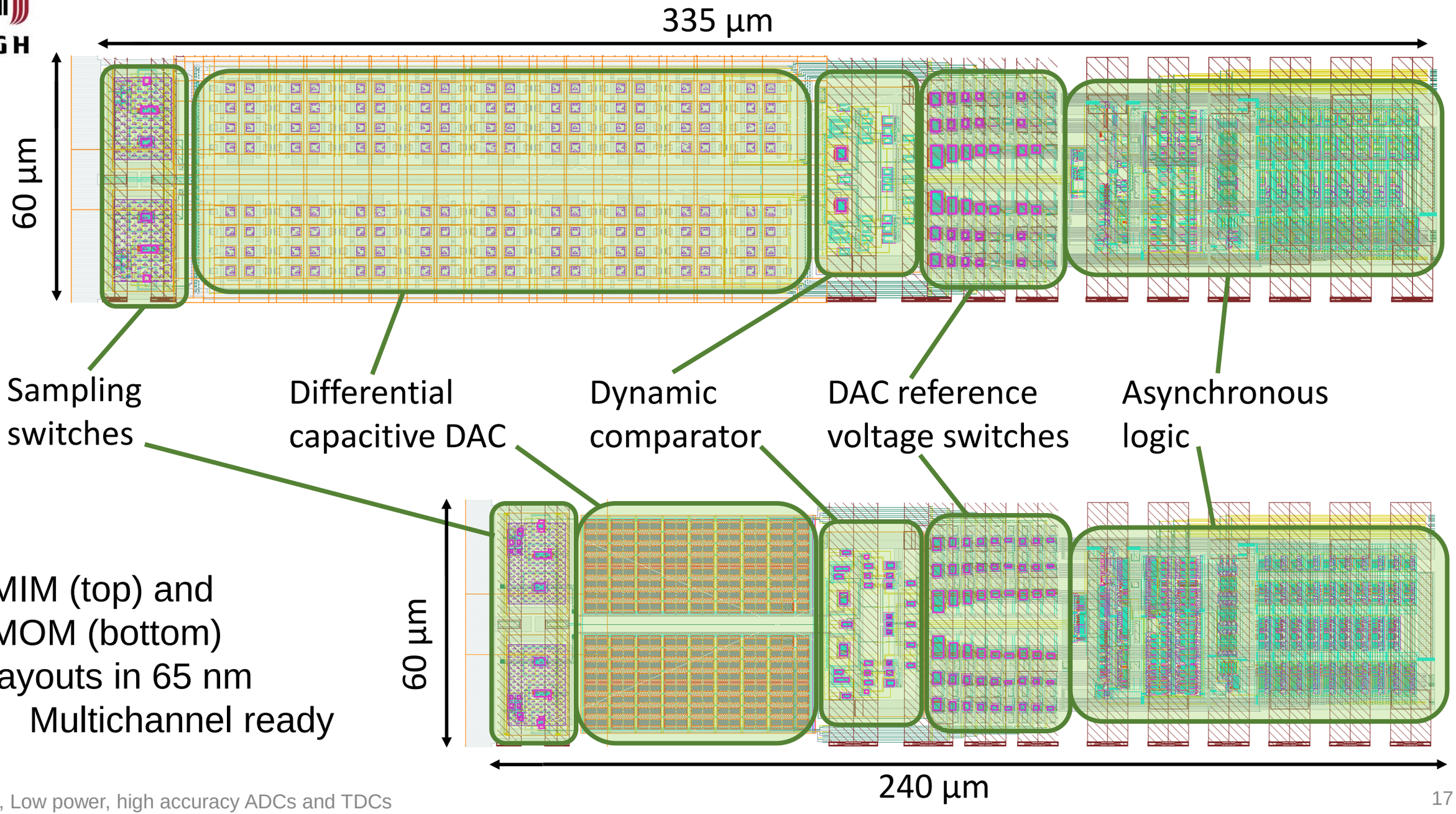


MIM 613 (514 is nearly identical) layout in 130 nm

- Designs ready for multichannel ASIC with pitch 160µm (80µm ADC core + 80µm decoupling)



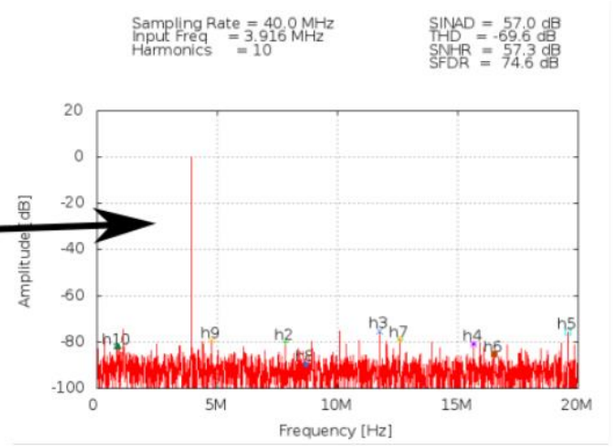
SAR ADC layouts – 65nm CMOS technology



MIM (top) and MOM (bottom) layouts in 65 nm

- Multichannel ready

ADC measurement setup



Agilent 81160A
differential generator

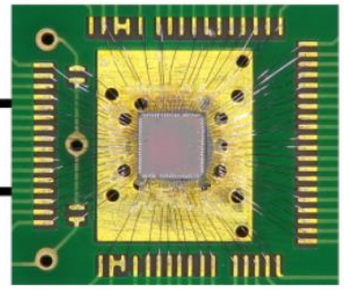
Power supply,
reference
voltages

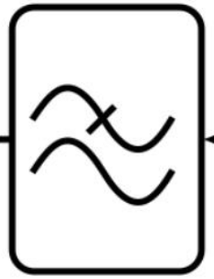
ADC data and
measurement control
(Ethernet)

Input sine
(differential)

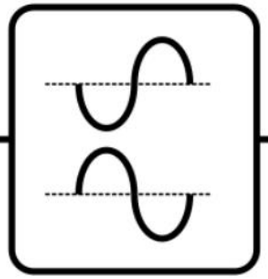
FPGA-based DAQ
(Xilinx Virtex-5)

ADC data
output (SLVS):
parallel or serial

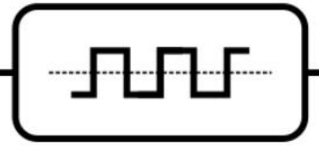




Differential
low pass filter

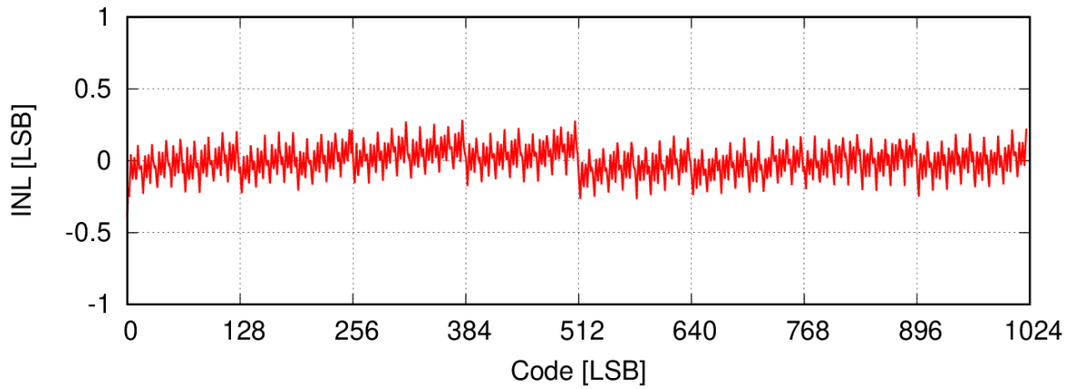


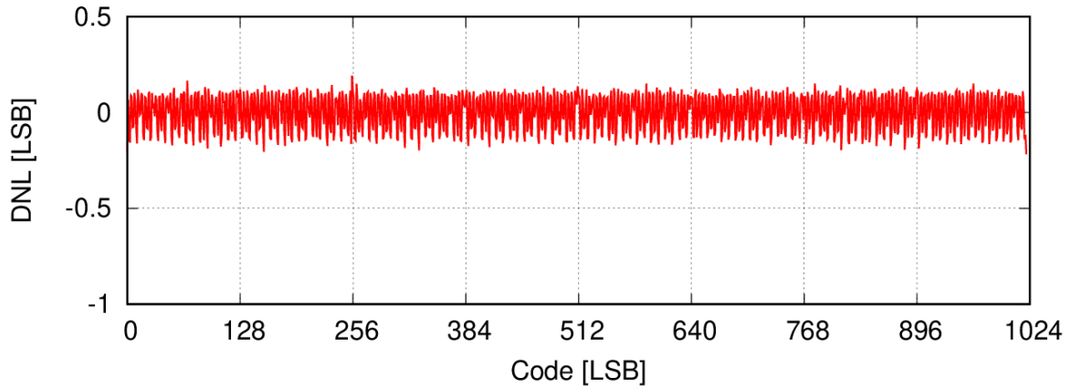
Sampling clock



Measurements: ADC static metric – 130nm CMOS technology

130 nm MIM 613



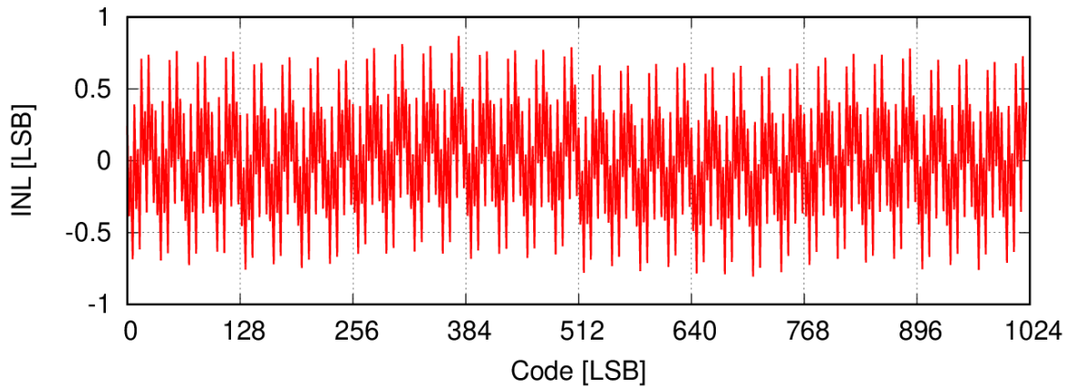


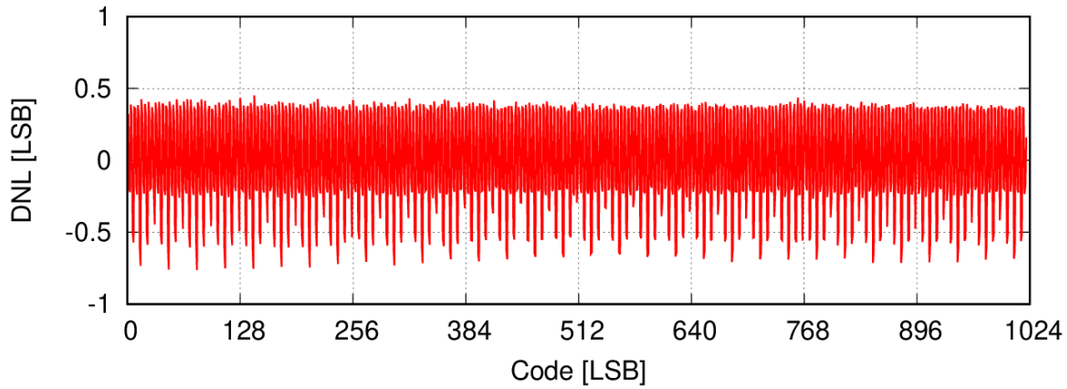
-0.22 < **DNL** < 0.20

-0.30 < **INL** < 0.40

Static **ENOB** = 9.92

130 nm MIM 514





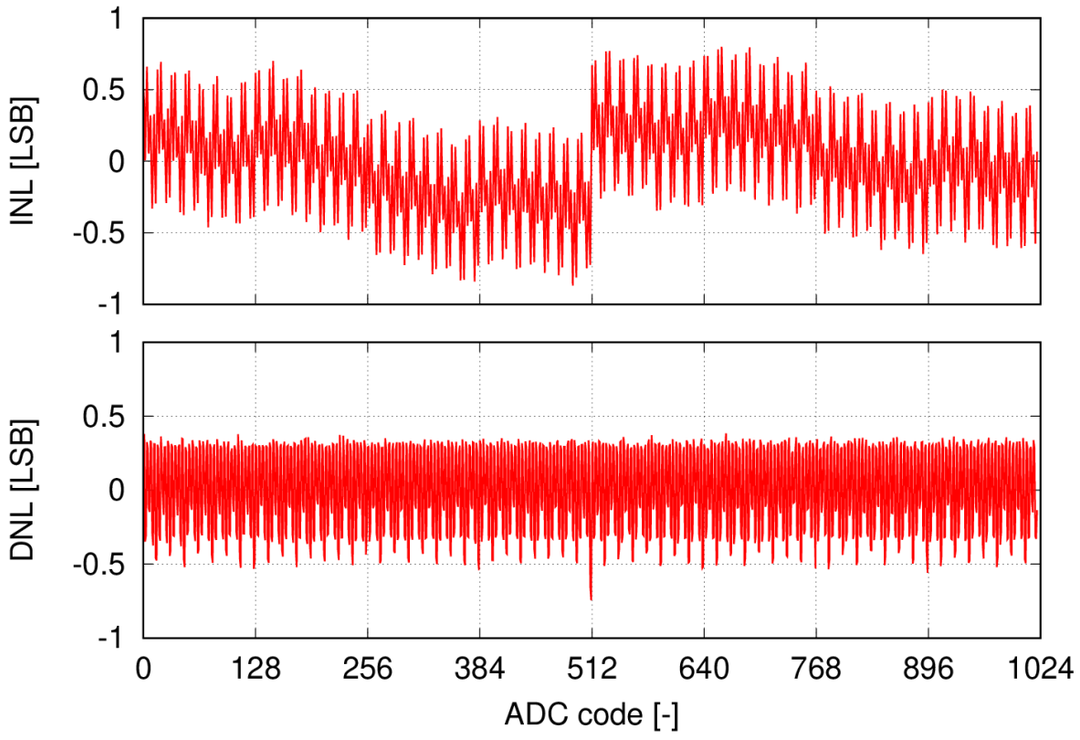
-0.70 < **DNL** < 0.44

-0.87 < **INL** < 0.81

Static **ENOB** = 9.37

Measurements: ADC static metrics – 65nm CMOS technology

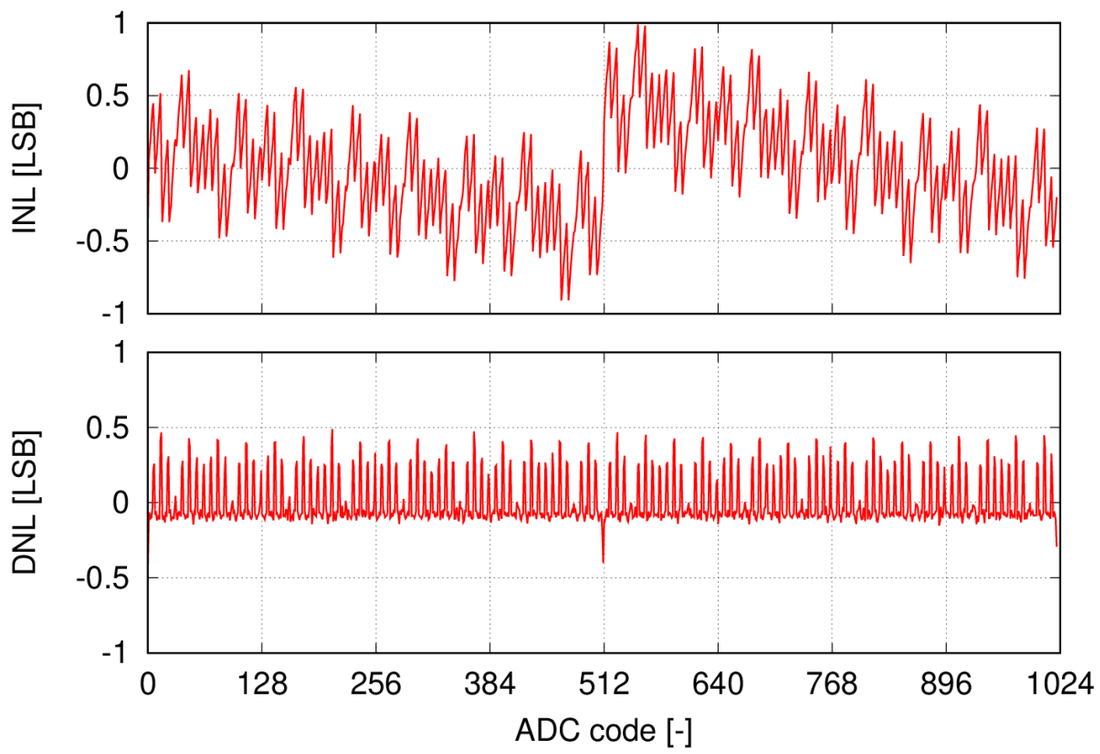
65 nm MIM 613



-0.75 < **DNL** < 0.40
-0.80 < **INL** < 0.82
Static **ENOB** = 9.40

Unexpected large INL step in the middle due to the overlooked parasitic capacitance

65 nm MOM 712

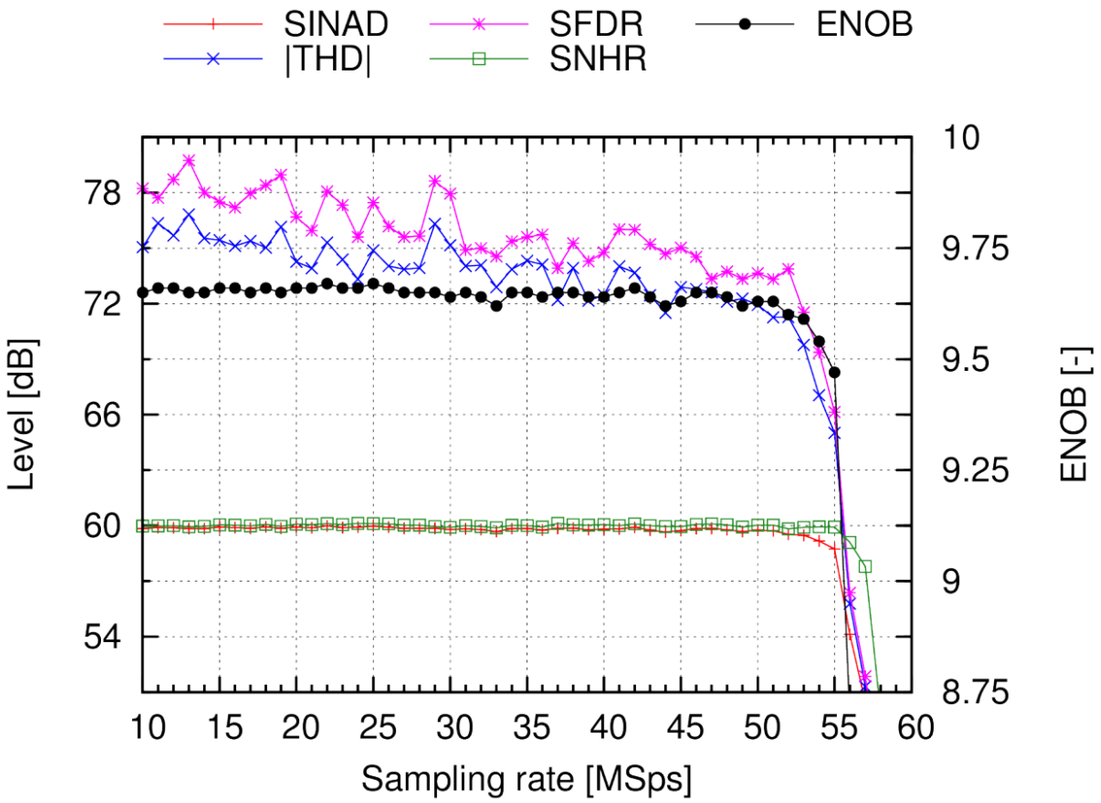


-0.42 < **DNL** < 0.52
-0.98 < **INL** < 0.94
Static **ENOB** = 9.35

Result somehow expected due to the large parasitics and lack of matching parameters

Measurements: ADC dynamic metrics – 130nm CMOS technology

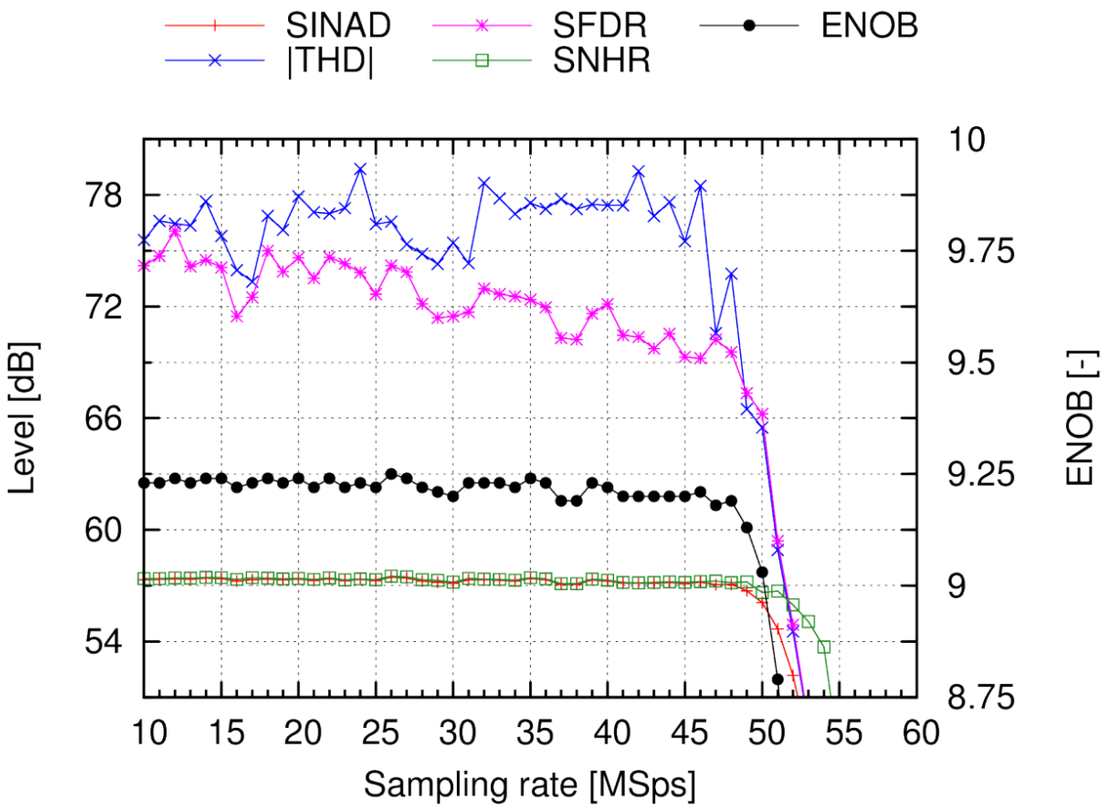
130 nm MIM 613



Sampling rate ≤ **55 MSps**

ENOB > 9.65 up to 50 MSps
ENOB ≈ 9.5 at 55 MSps

130 nm MIM 514

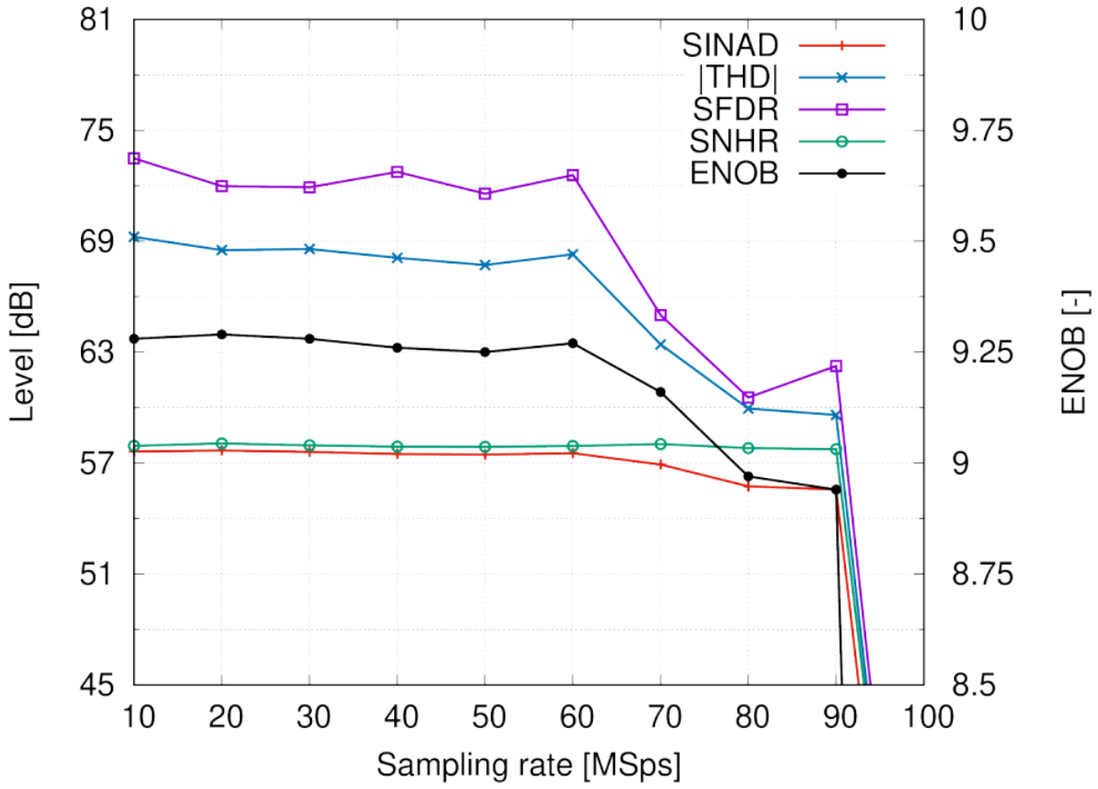


Sampling rate ≤ **50 MSps**

ENOB > 9.2 up to 45 MSps
ENOB ≈ 9.0 at 50 MSps

Measurements: ADC dynamic metrics – 65nm CMOS technology

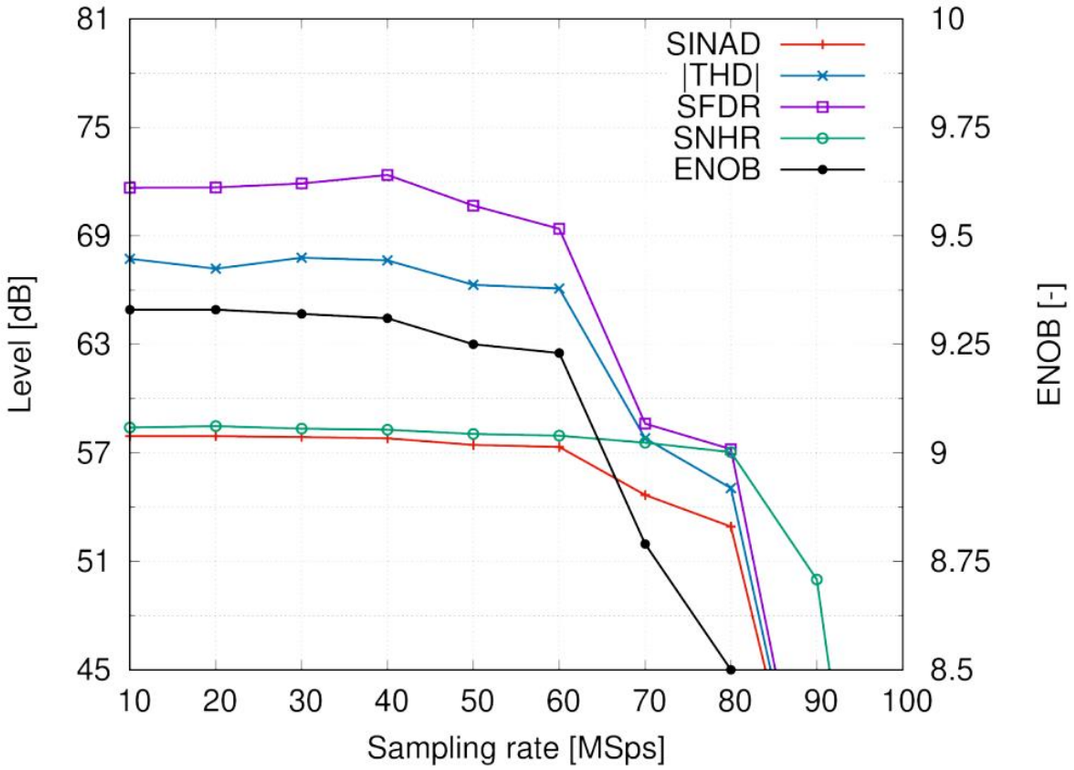
65 nm MIM 613



Sampling rate ≤ **90 MSps**

ENOB > 9.3 up to 60 MSps
ENOB ≈ 8.9 at 90 MSps

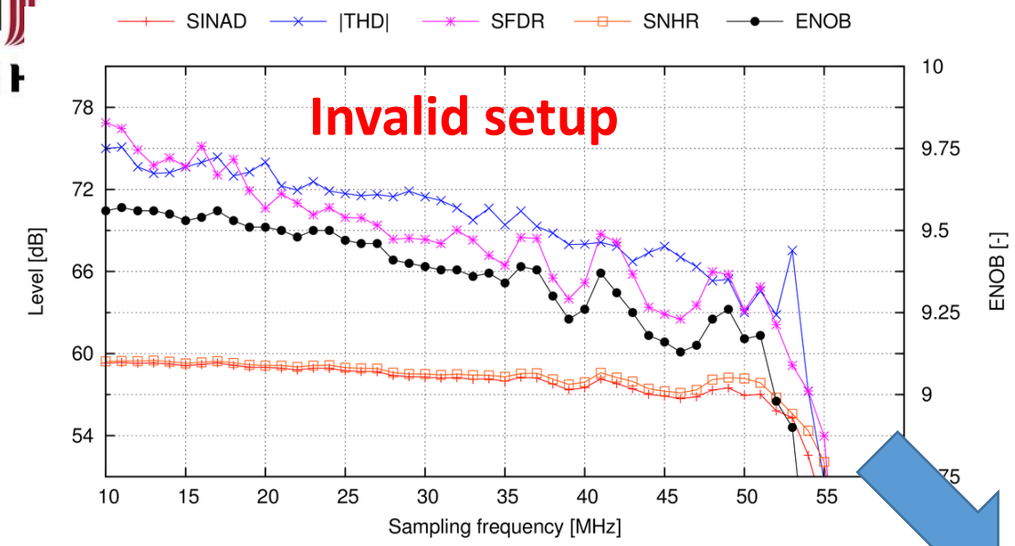
65 nm MOM 712



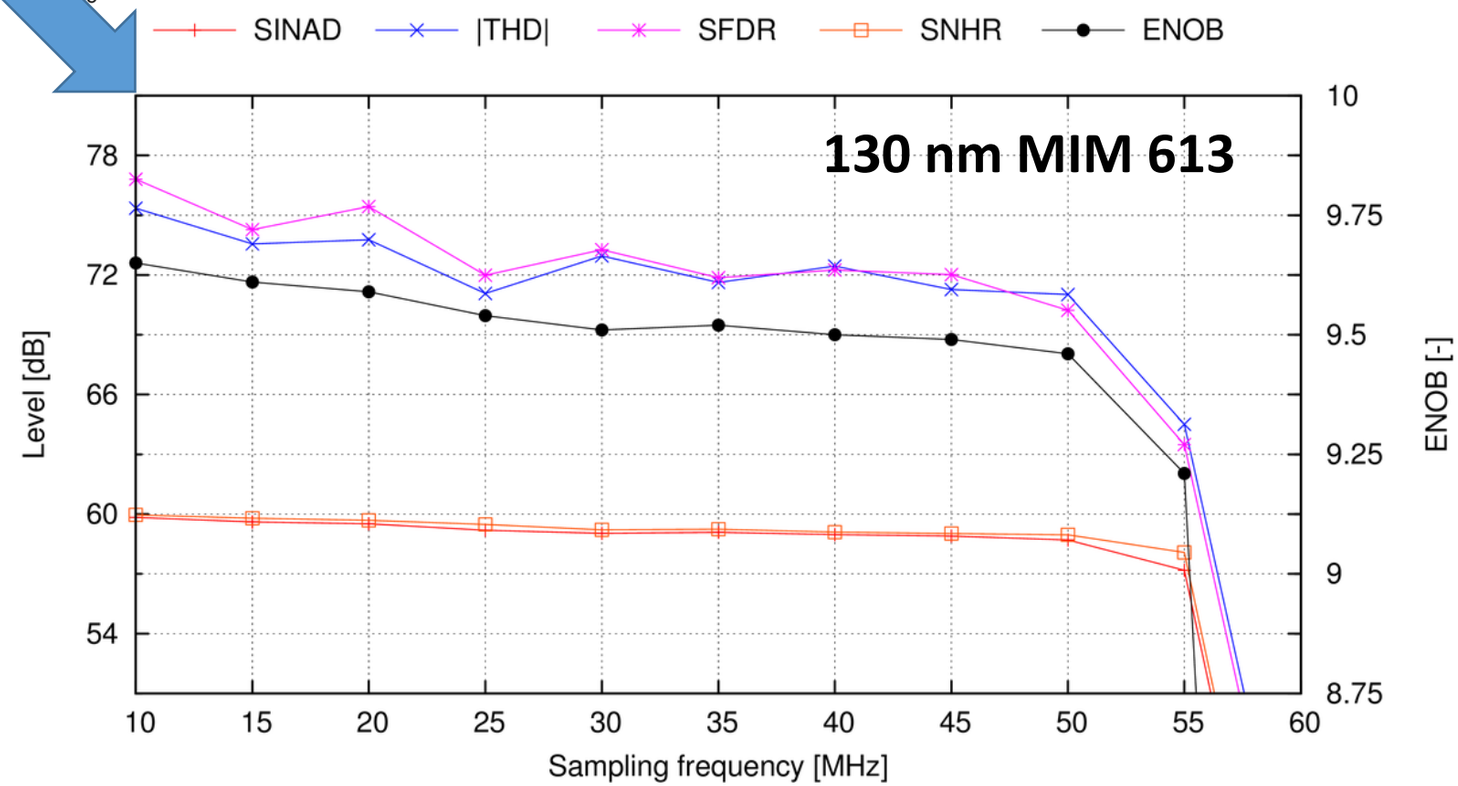
Sampling rate ≤ **70 MSps**

ENOB > 9.3 up to 60 MSps
ENOB ≈ 8.7 at 70 MSps

Measurements: ADC dynamic metrics at Nyquist – 130nm CMOS technology



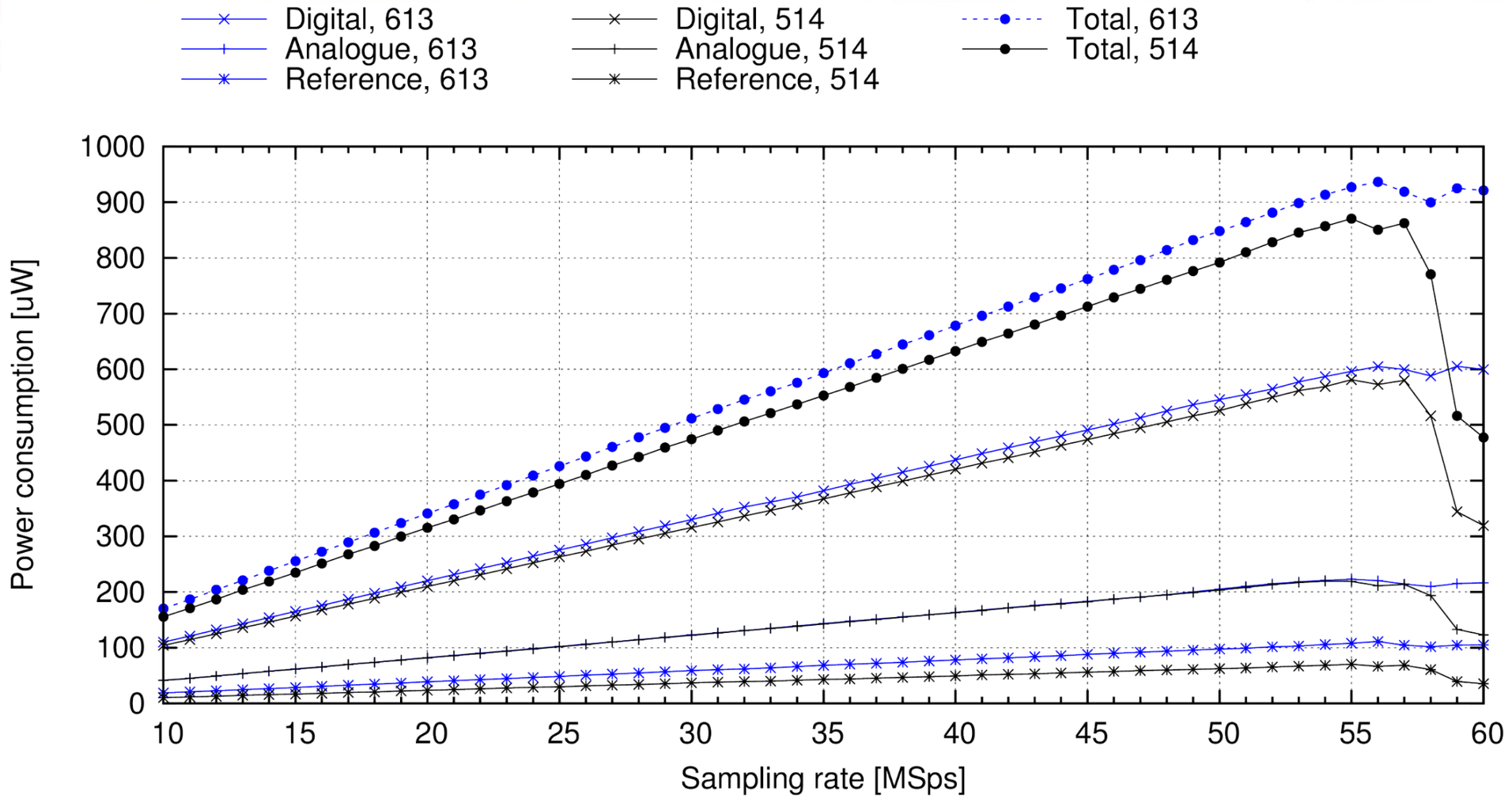
Measurements at Nyquist are challenging…

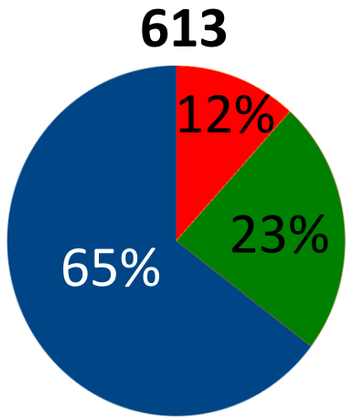


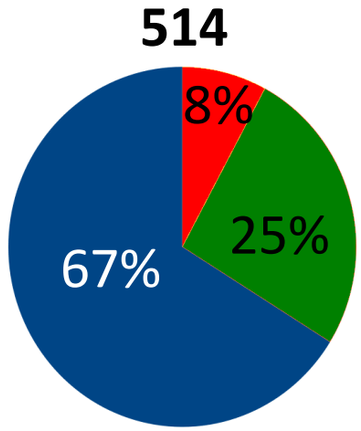
Sampling rate ≤ **55 MSps**

ENOB > 9.5 up to 40 MSps
ENOB ≈ 9.2 at 55 MSps

Measurements: ADC power consumption – 130nm CMOS technology



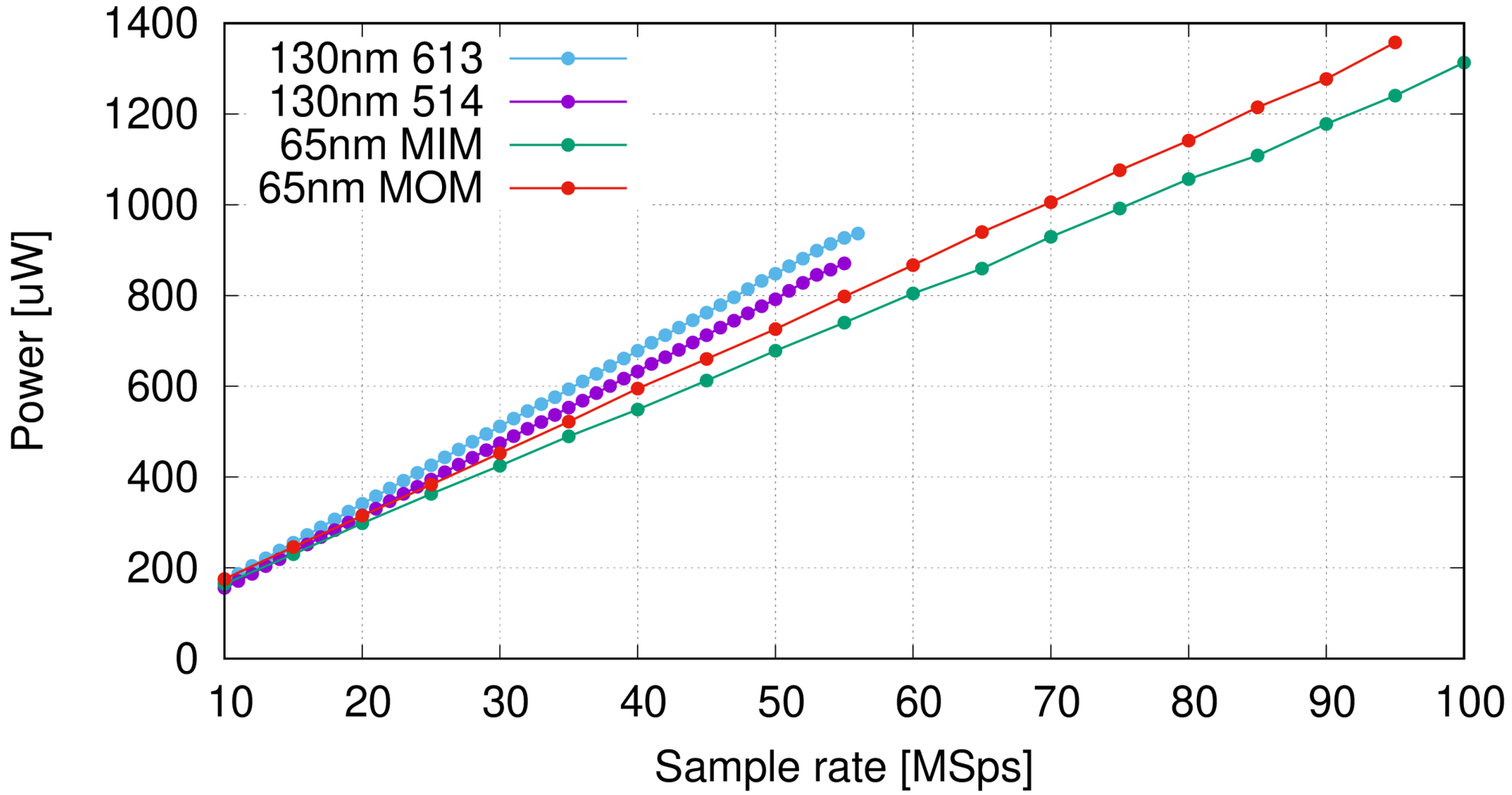




(digital + analogue + reference)

130nm power consumption at 40 MSps:
- 613: **680 µW** (440 + 160 + 80) µW
- 514: **635 µW** (425 + 160 + 50) µW

Measurements: ADC power consumption – 65nm and 130nm comparison

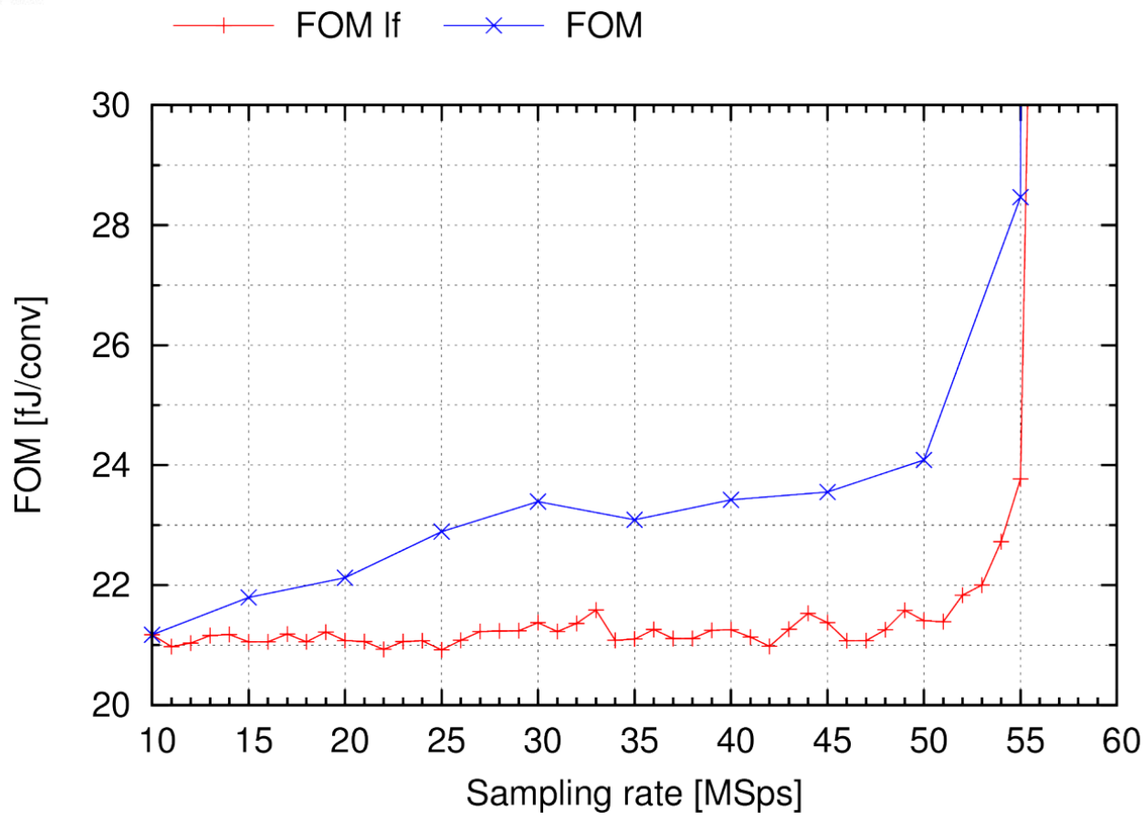


Power consumption at 40 MSps:

- 130nm 613: **680 µW**
- 130nm 514: **635 µW**
- 65nm MIM : **550 µW**
- 65nm MOM: **600 µW**

Measurements: ADC FoM – 130nm CMOS technology

130 nm MIM 613

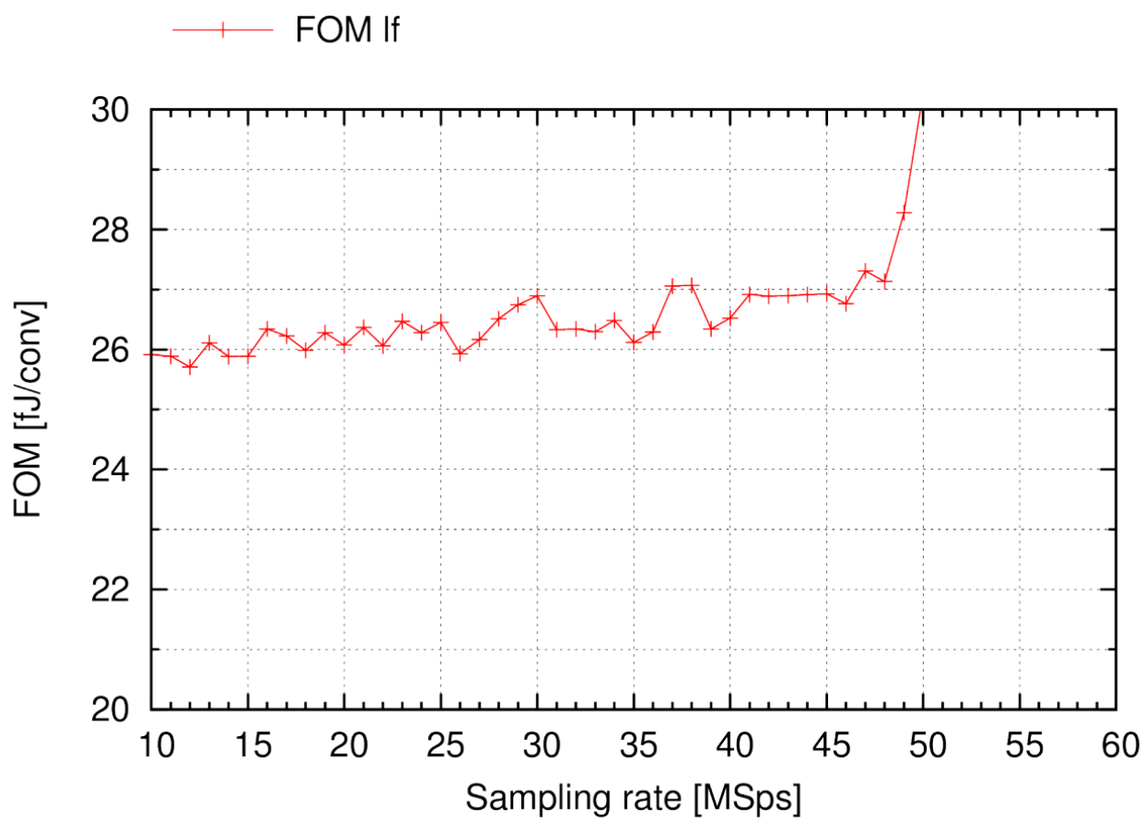


$FoM_{lf} \leq$ **21** fJ/conv up to 50 MSps

FoM $\leq$ **24** fJ/conv up to 50 MSps

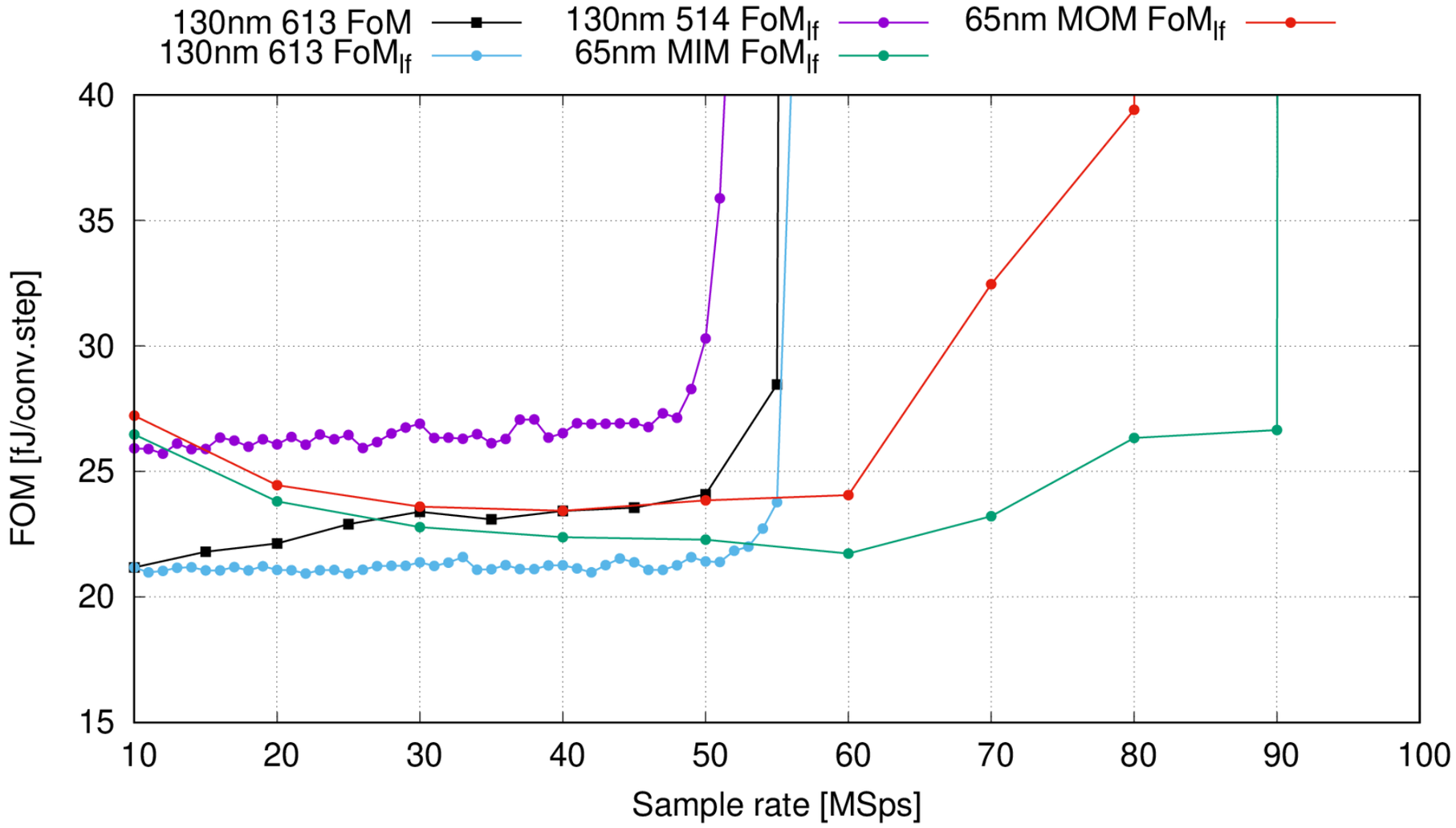
One of the best results so far among State of the Art ADCs in similar technology

130 nm MIM 514



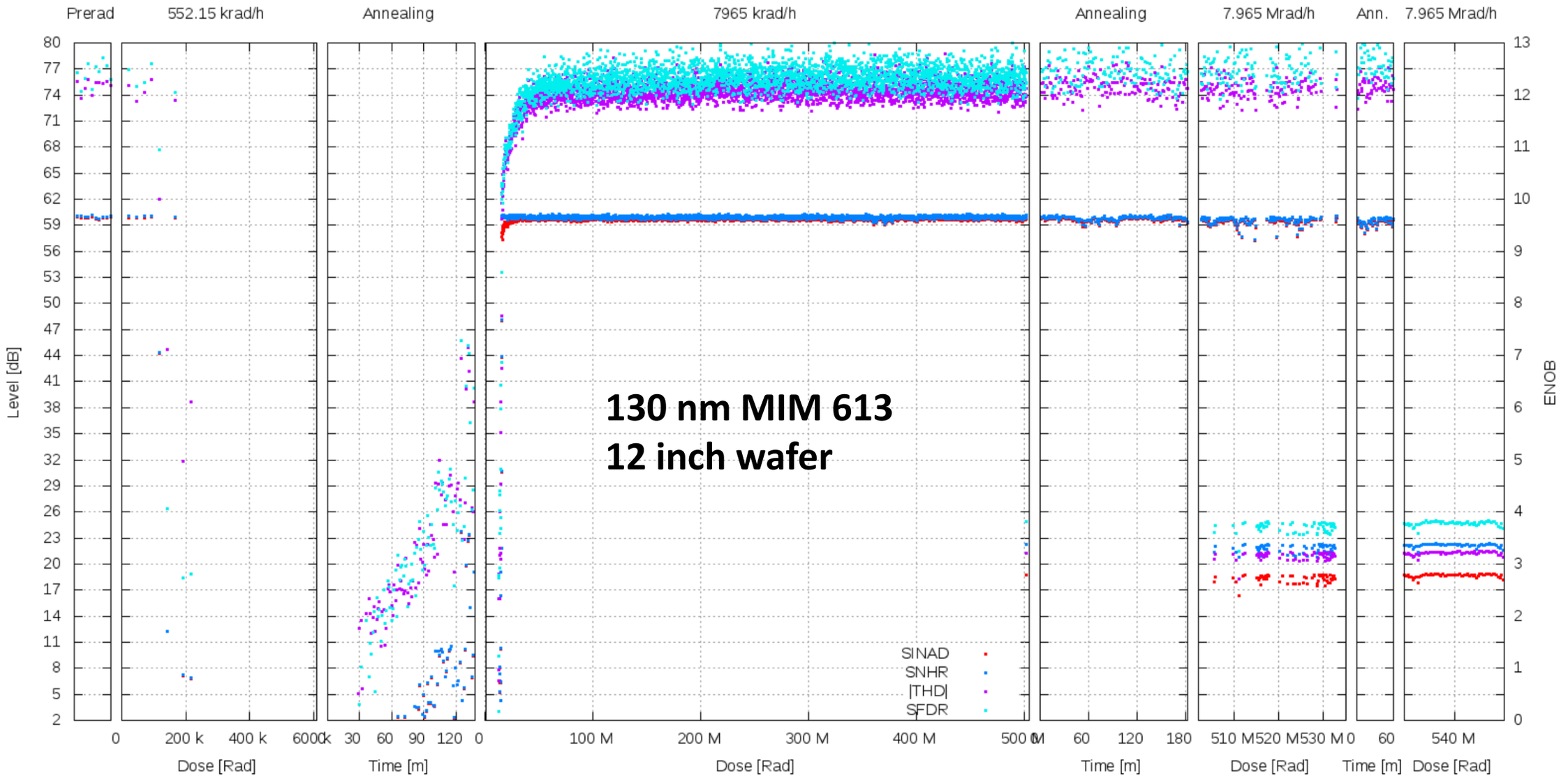
$FoM_{lf} \leq$ **27** fJ/conv up to 45 MSps

Measurements: ADC FoM – – 65nm and 130nm comparison



- 65nm – FoM$_{lf}$ ≤ **23** for sampling rates <60 MSps (MOM) and <80 MSps (MIM)
  For lower sampling rates, FOM$_{lf}$ increases due to decoupling leakage current
- 130nm achieves similar FoM (even at Nyqist) – larger power but better ENOB

Radiation hardness of ADC in 130nm CMOS technology



Resolution drops after few hundred krad but recovers in few hours and stays good up to 500 Mrad

TDC

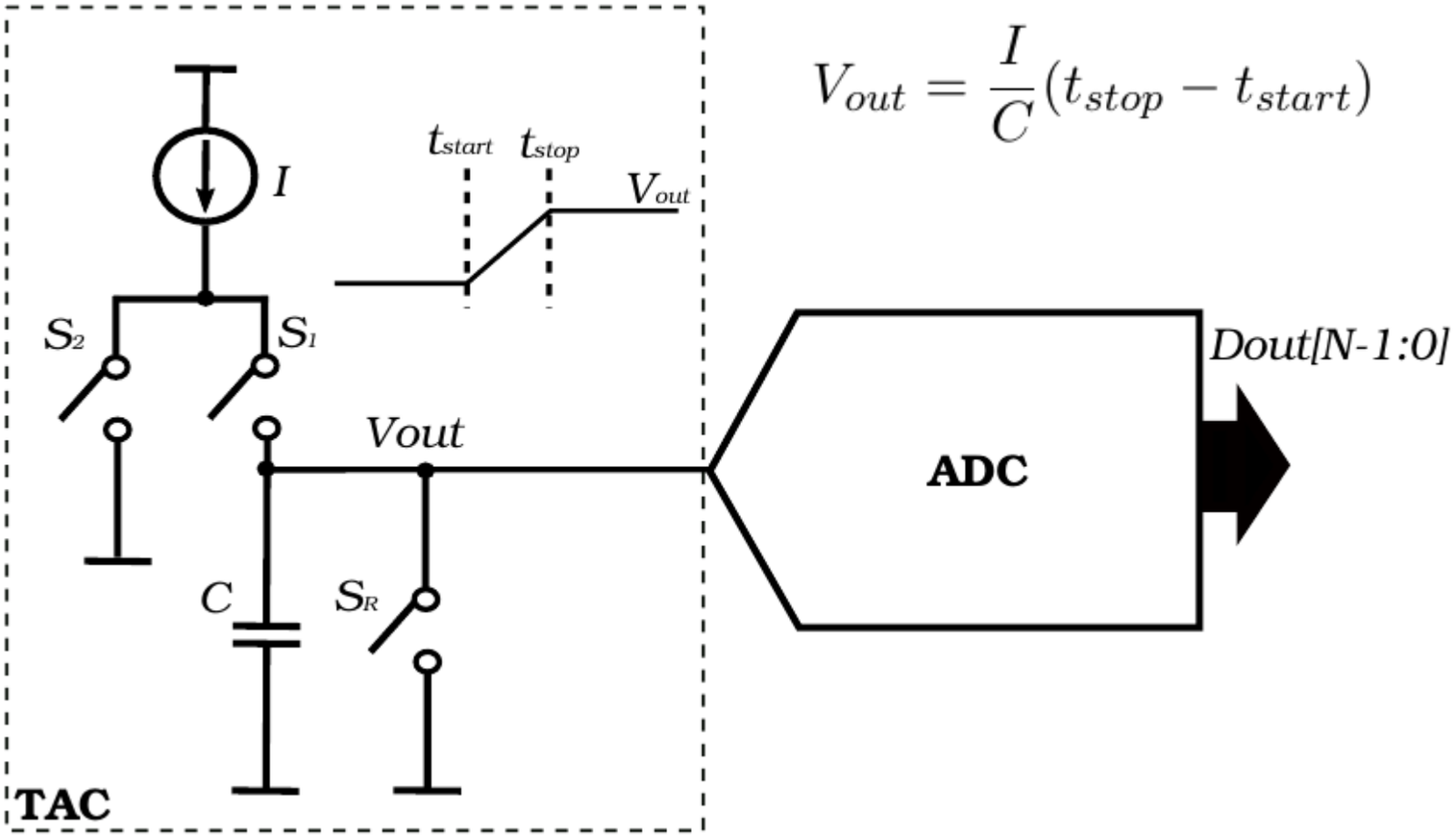
TDC design – general idea

General idea: take advantage of the excellent ADC we have (130nm 613) and build analogue interpolation TDC around it.

- Time-to-Analog Converter (TAC) – converts time into voltage (proportional to time)
- ADC converts TAC output voltage to binary number

TAC operation:

1. Reset sampling capacitor to constant, known voltage
2. Charge it with constant current between “Start” and “Stop” signals

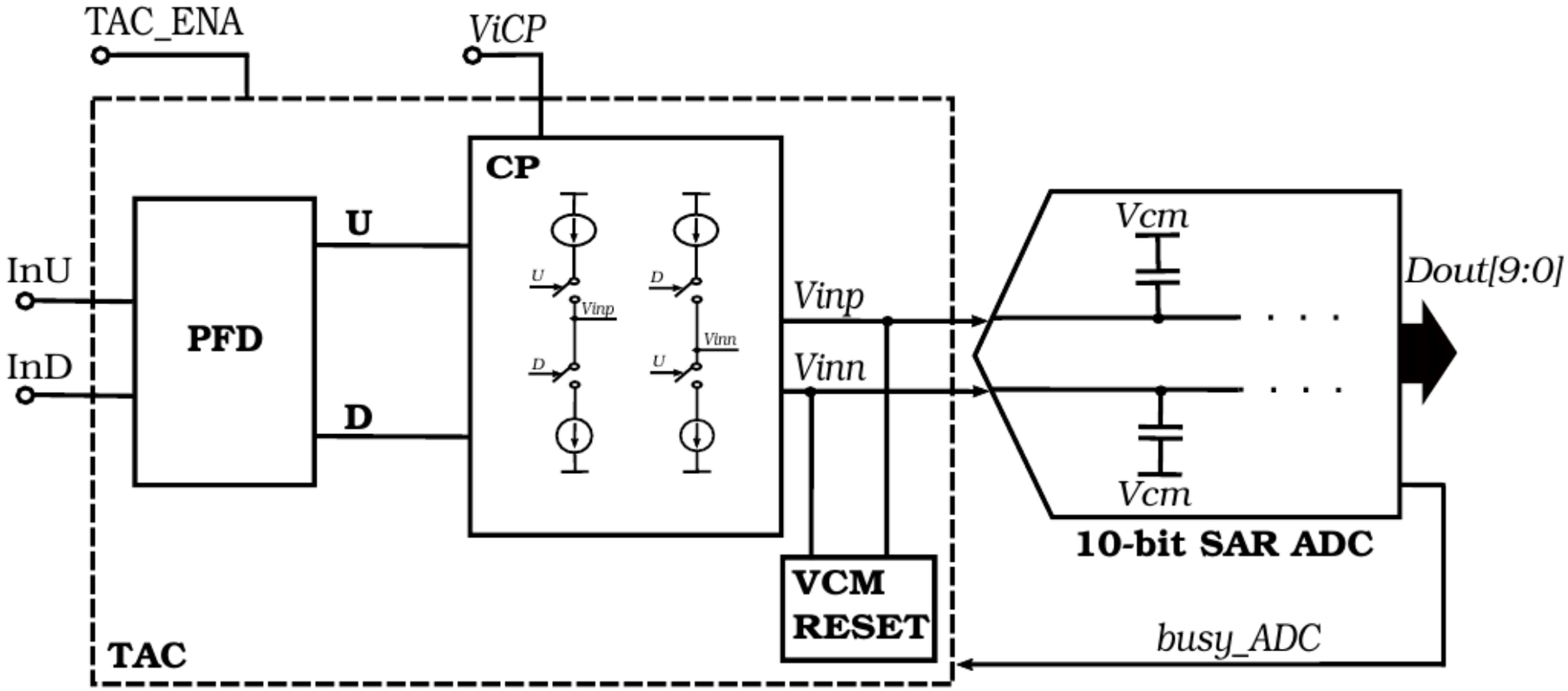


$$V_{out} = \frac{I}{C}(t_{stop} - t_{start})$$

TDC architecture

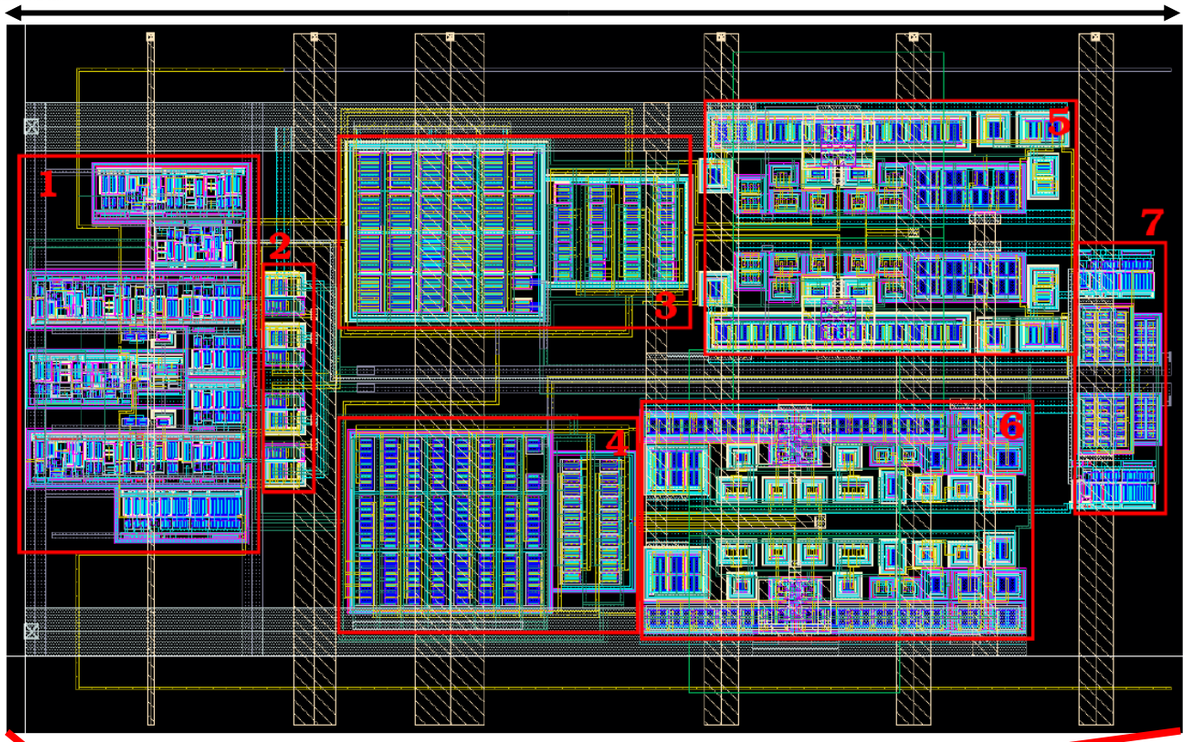
Since ADC comprises capacitive DAC, an additional sampling capacitor in TAC is not really needed, and constant current can directly charge capacitive DAC in the ADC

- Phase Frequency Detector (PFD) – converts time difference between rising edge on InU and InD inputs into current source control signals U, D
- Charge Pump (CP) – charges (U) or discharges (D) capacitive DAC in the ADC. Charging current is determined by the bias voltage ViCP

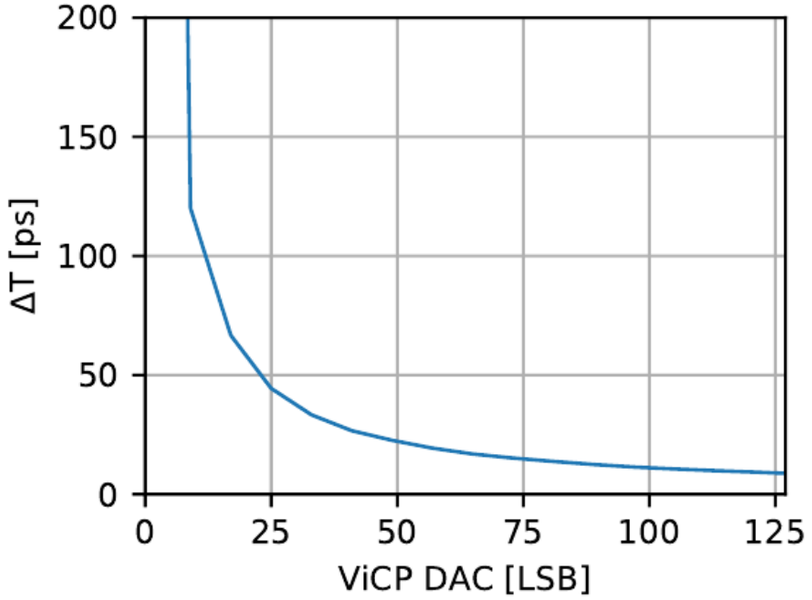


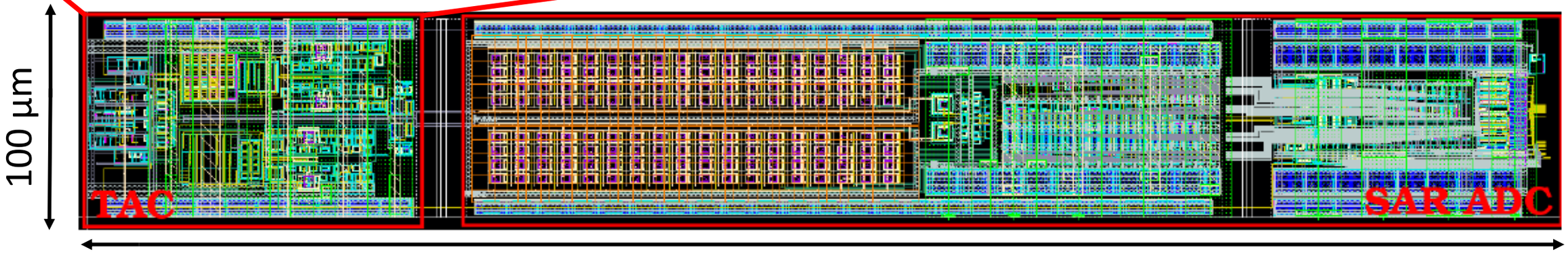
TDC layout

TAC layout

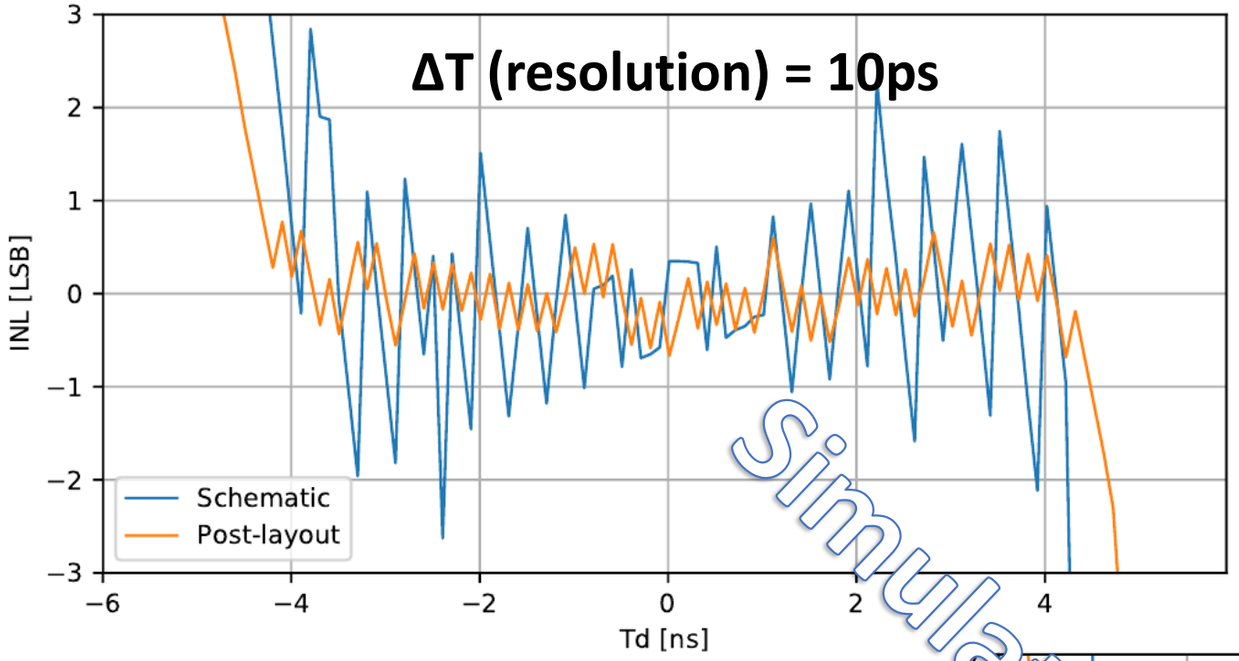


Time resolution in function of ViCP bias voltage DAC (7-bit) setting





TDC simulations – linearity



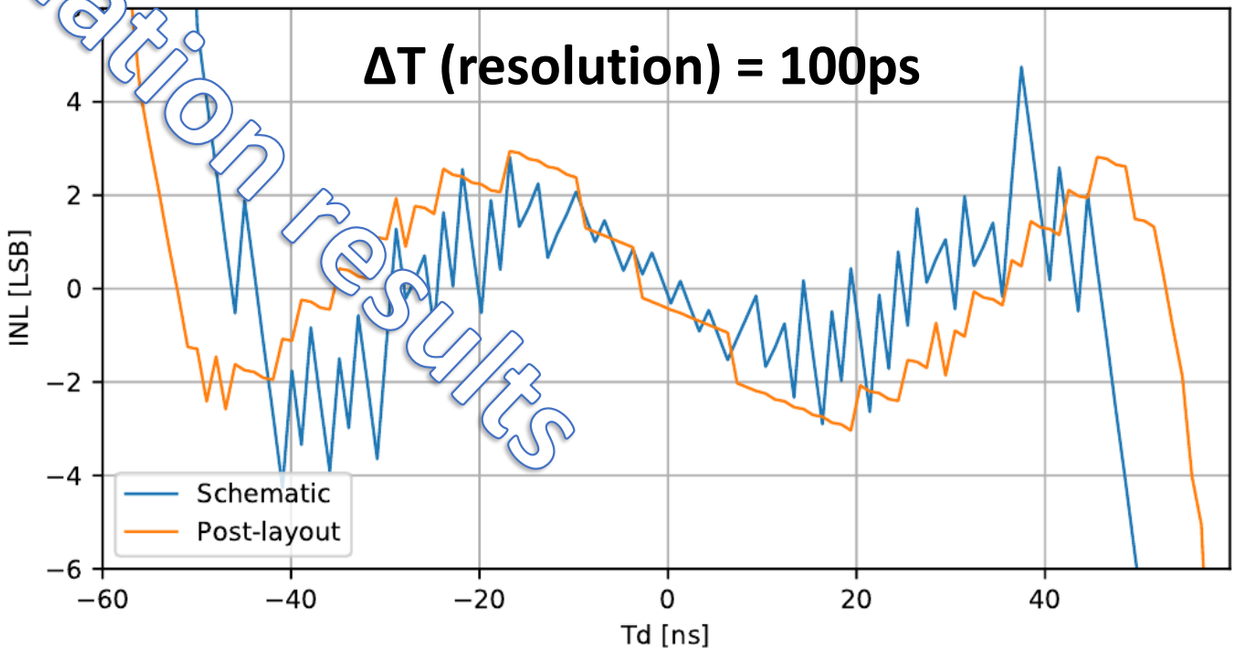
Post-layout, 10ps resolution:
INL within ±0.5 LSB in range:

- -4.29ns (-365 LSB)
- +4.42ns (+375 LSB)

Simulation results

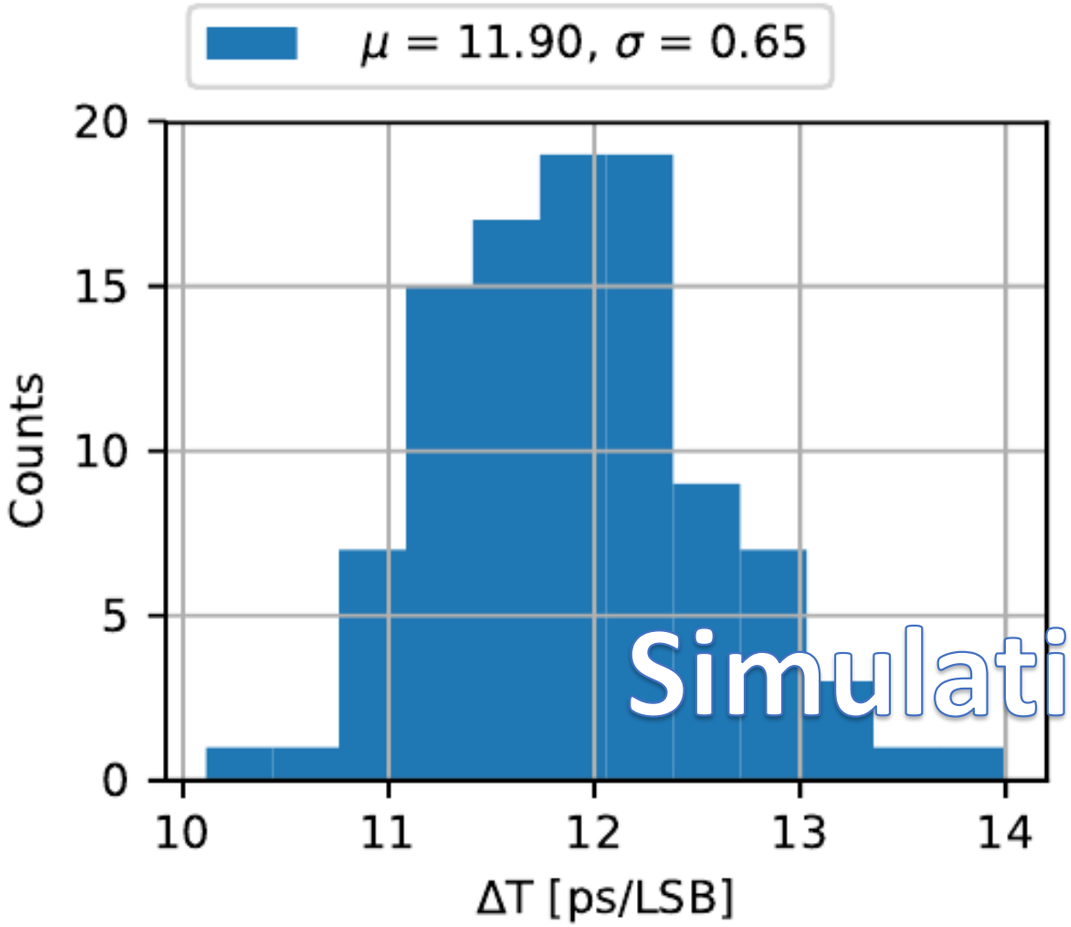
Post-layout, 100ps resolution:
INL within ±3 LSB in range of
± 53ns (± 480 LSB)

TDC was optimized for 10ps resolution, so 100ps performance is much worse

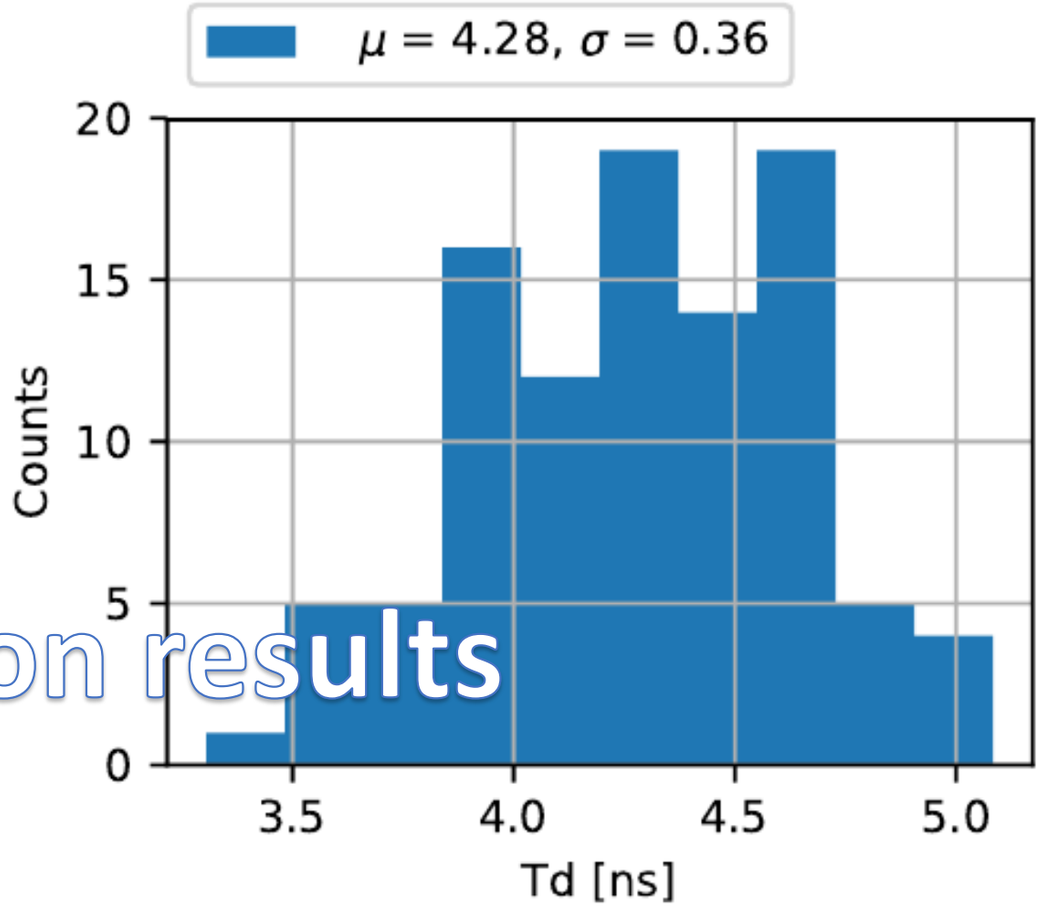


TDC simulations – Monte Carlo

Time resolution dispersion
for 100 MC simulations



Linear range dispersion for
100 MC simulations



Simulation results

ΔT (resolution) = 10ps

Summary

Summary

- Two ADC prototypes in 130nm CMOS technology designed and tested:
  - 613 split DAC:
    - Excellent resolution (**$ENOB_{lf}$ > 9.65, $ENOB_{Nyq}$ ≈ 9.5** up to **50 MSps**)
    - **680 µW** at 40 MSps with excellent **FoM_{lf} = 21** and **FoM = 24 fJ/conv**.
    - One of the best State of the Art ADC till now
    - Multichannel ready – in fact already used in:
      - HGCROC (*see D. Thienpont talk, Thursday 9:30*)
      - FLAME and FLAXE (*see M. Idzik talk, Thursday 10:30*)
    - Radiation hardness (with annealing) up to 500 Mrad
  - 514 split DAC:
    - Slightly lower power consumption, but also lower resolution than 613

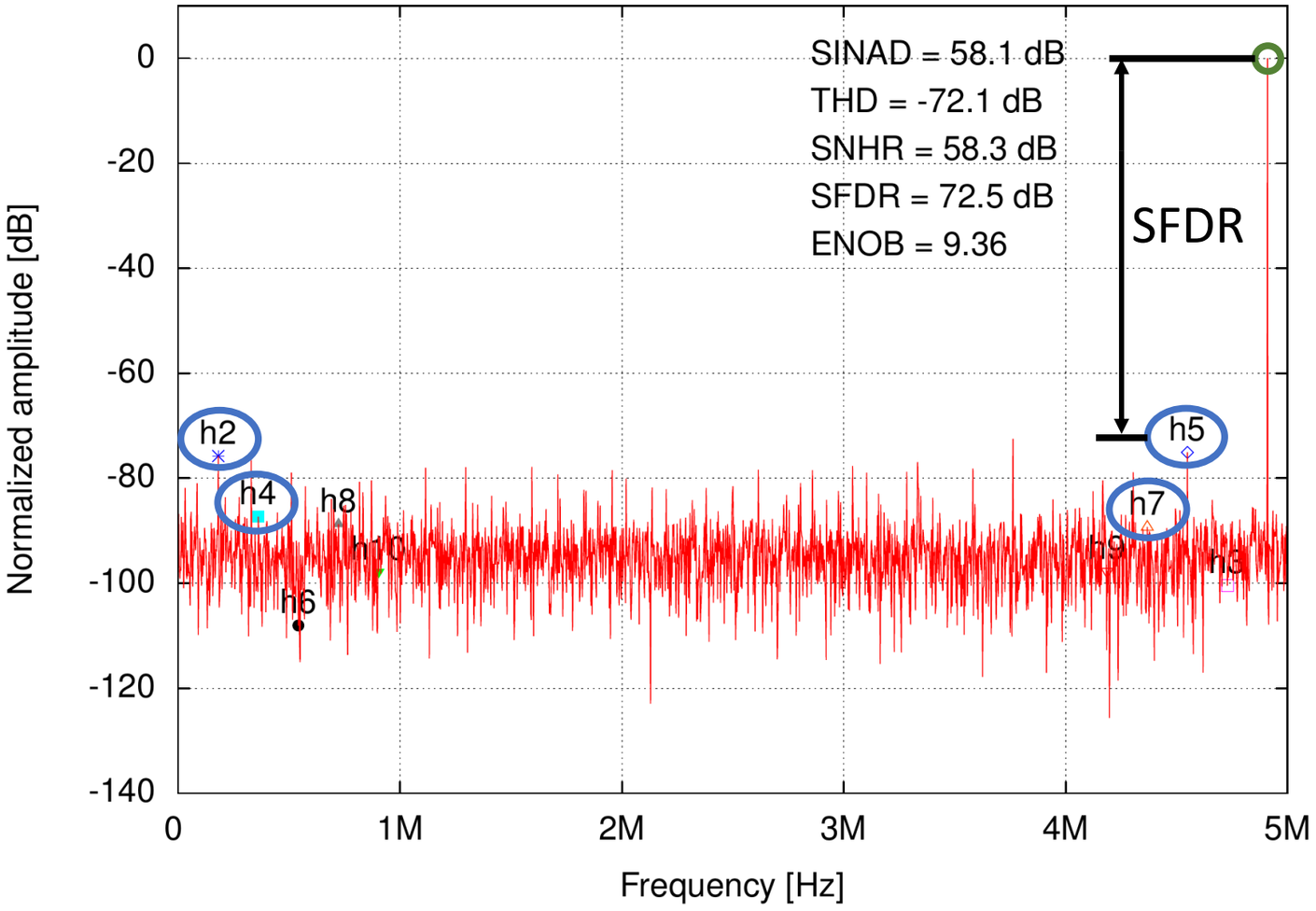
Summary

- Two ADC prototypes in 65nm CMOS technology designed and tested:
  - MIM-based, 613 split DAC:
    - Good resolution (ENOBlf **≈ 9.3** up to **60 MSps**, ENOBlf ≈ 8.9 at 90 MSps)
    - Power consumption around 80% of 130nm technology
    - Modified version (not shown here) used in lpGBT in monitoring circuitry
  - MOM-based, 712 split DAC:
    - Smaller than MIM-based (70% area), similar resolution but slower
- ADC-based TDC designed, simulated and fabricated.
  Post-layout simulation results shows resolution < 12ps in range up to 4ns with good linearity
  Due to unexpected delays in test setup preparation measurement results not ready yet

Thank you for the attention

Backup slides

ADC dynamic metrics basics



$$SNR = SNHR = \frac{P_{Sig}}{\sum P_{Noise}}$$

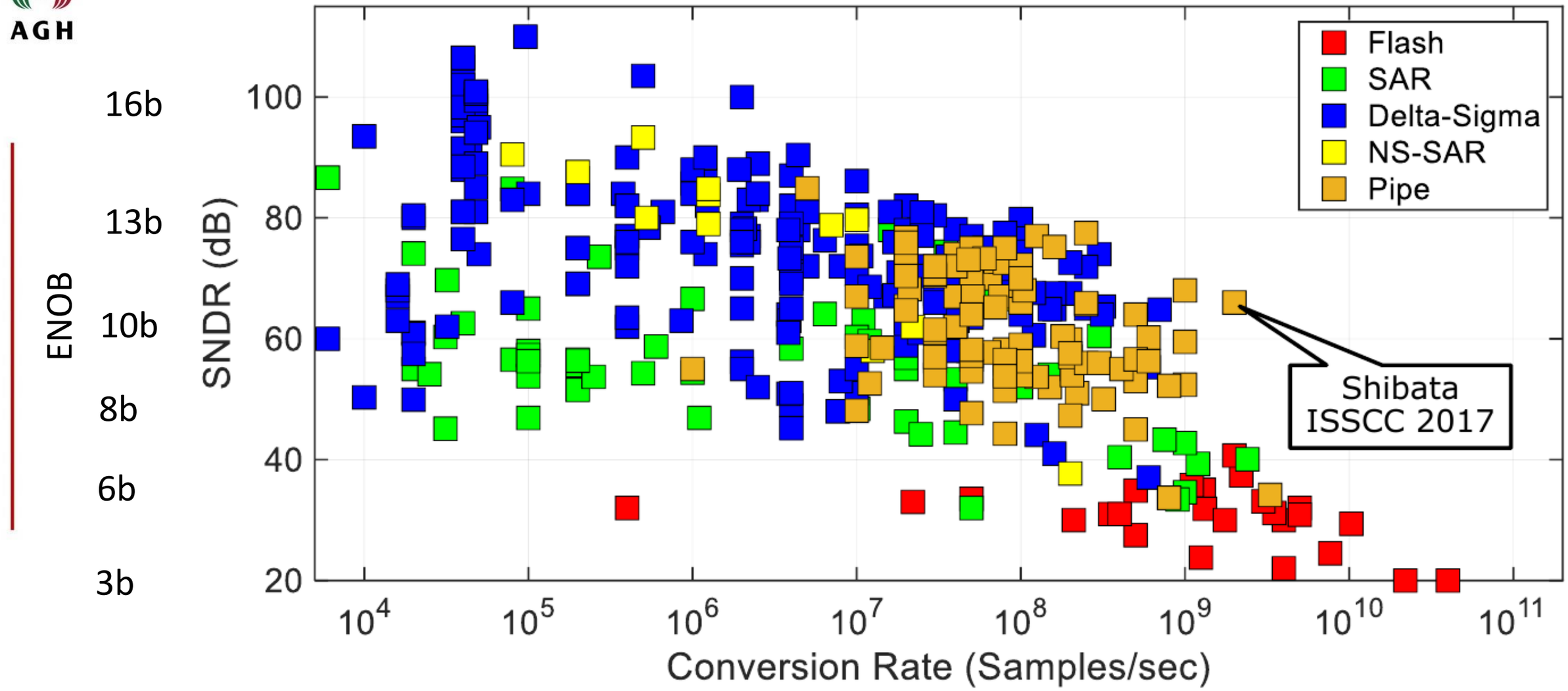
$$SNDR = SINAD = \frac{P_{Sig}}{\sum P_{Noise} + P_{HD}}$$

$$THD = \frac{P_{Sig}}{P_{HD}}$$

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

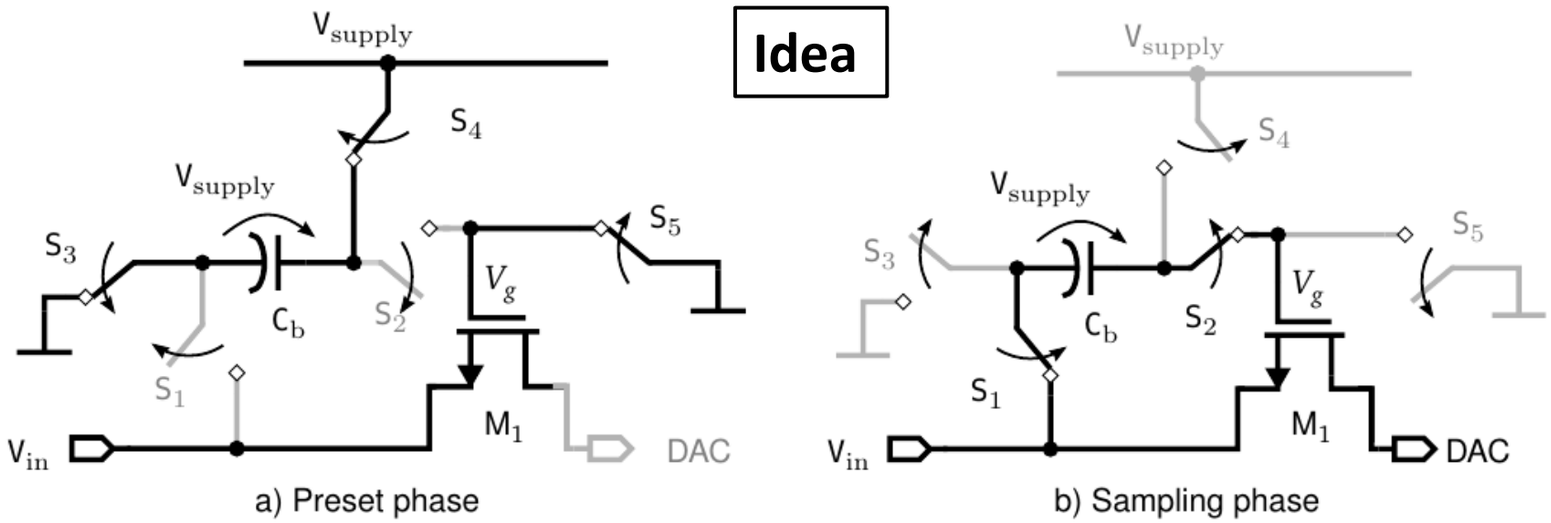
ADC dynamic metrics: DFT of the samples of the pure sine input signal

ADC architectures State of the Art – resolution vs speed



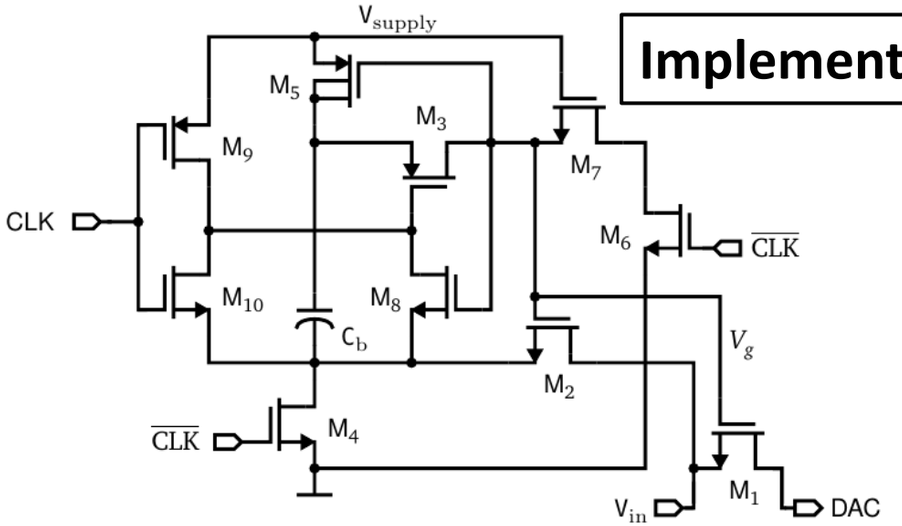
Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications, Boris Murmann
https://github.com/bmurmann/ADC-survey/blob/main/pdf/ISSCC2022-Short%20Course-Murmann.pdf

SAR ADC – bootstrapped switch



To minimize distortions during sampling, a bootstrap switches implemented.

General idea: keep V_{gs} equal to power supply voltage, regardless the V_s (input) voltage.



M. Dessouky and A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits," Electronics Letters, vol. 35, no. 1, pp. 8–10, 1999

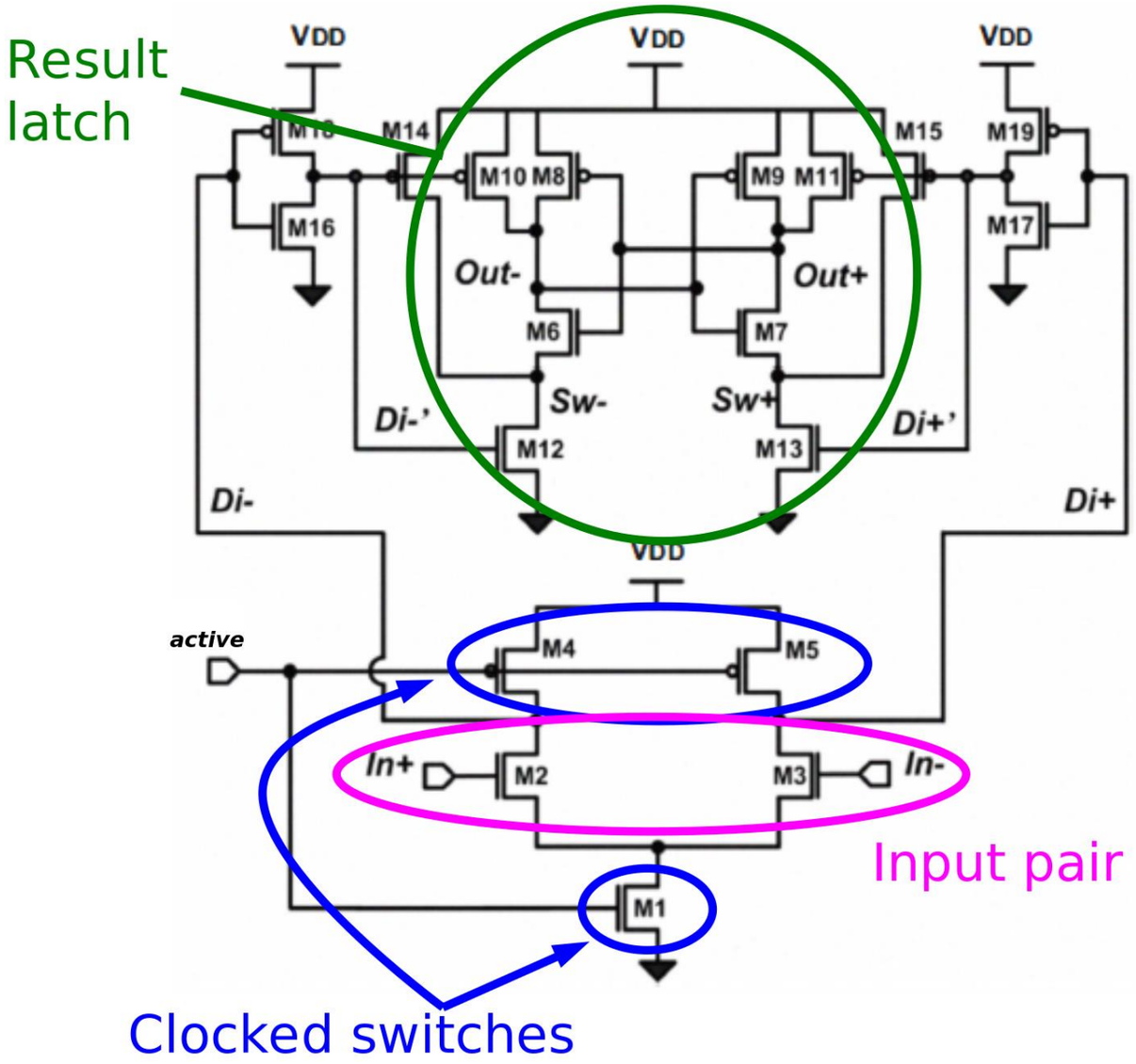
SAR ADC – dynamic comparator

Dynamic comparator

- Comparison performed on rising edge of “active” signal
- Reset (“active” low level) needed before next comparison

Pros and cons:

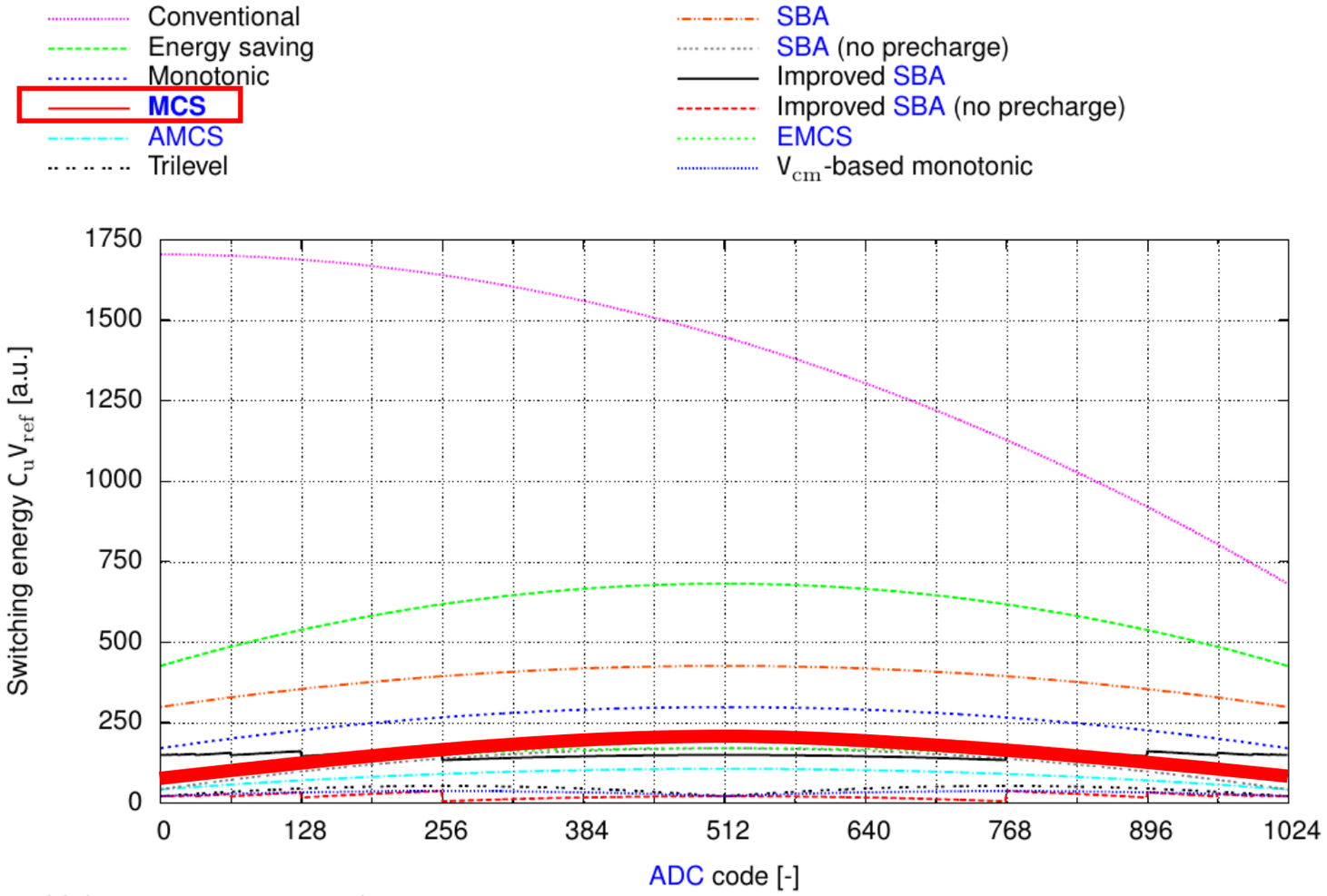
+ No direct path current
+ Low power consumption
- Dead time needed for reset
- Response time depends on input voltage difference



H.J. Jeon, Y-B. Kim, M. Choi “Offset voltage analysis of dynamic latched comparator”, IEEE 54th Int. Midwest Symp. On Circuits and Systems, 2011

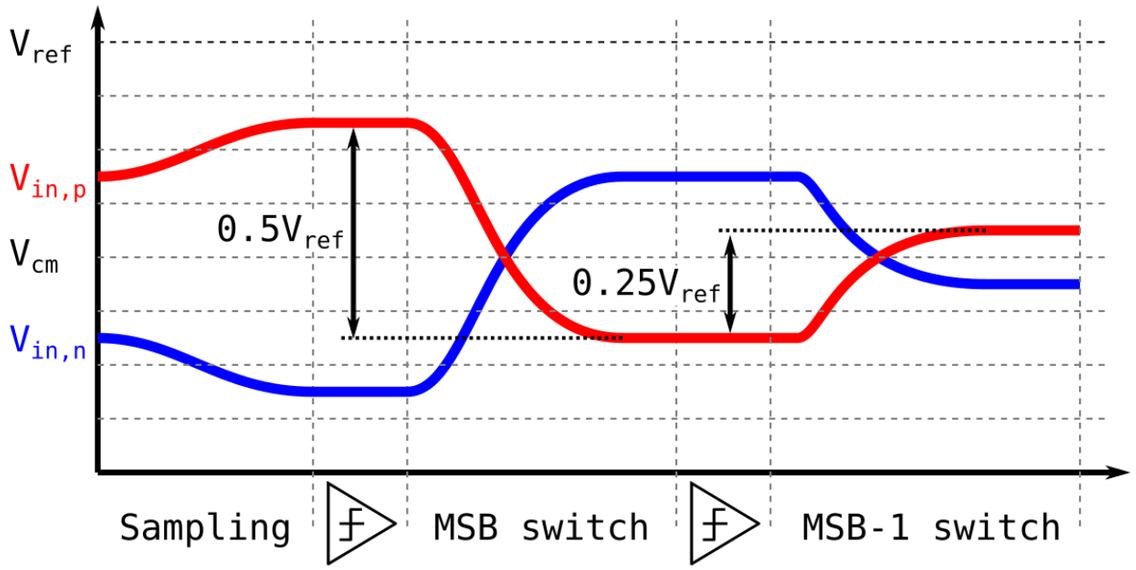
SAR ADC switching schemes

With CMOS technology scaling digital power consumption is decreasing rapidly, so minimizing analog power (DAC, comparator) is of main interest.
Huge progress has been obtained in the last ~10 years in optimizing capacitive DAC configurations and their switching schemes

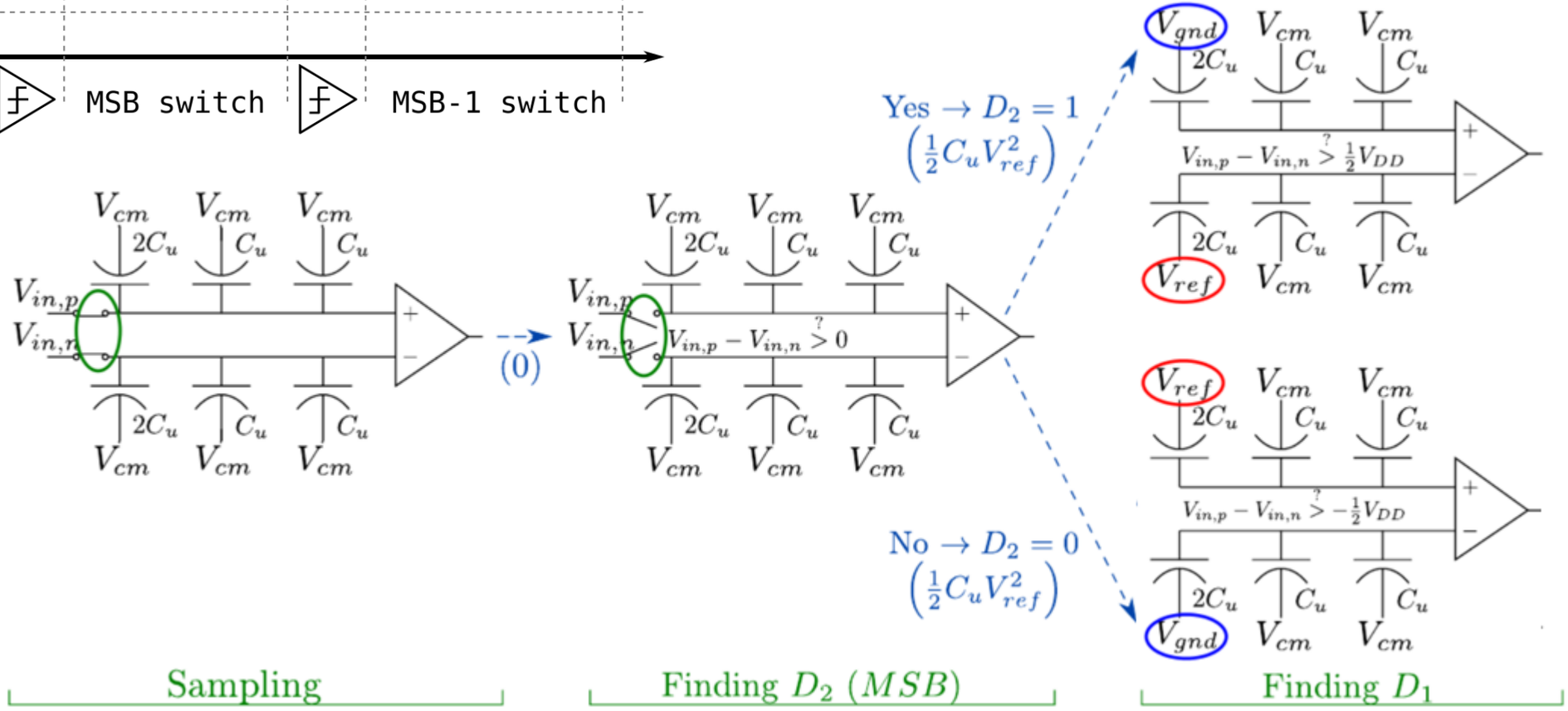


- Conventional – 100%
- Energy saving – 44%
- Switchback (SBA) – 18%
- Monotonic – 18%
- Improved SBA – 13%
- **Merge Capacitor Switching (MCS) – 7%**
- (…)
- Tri-level switching – 3.1%
- Vcm-based – 2.3%

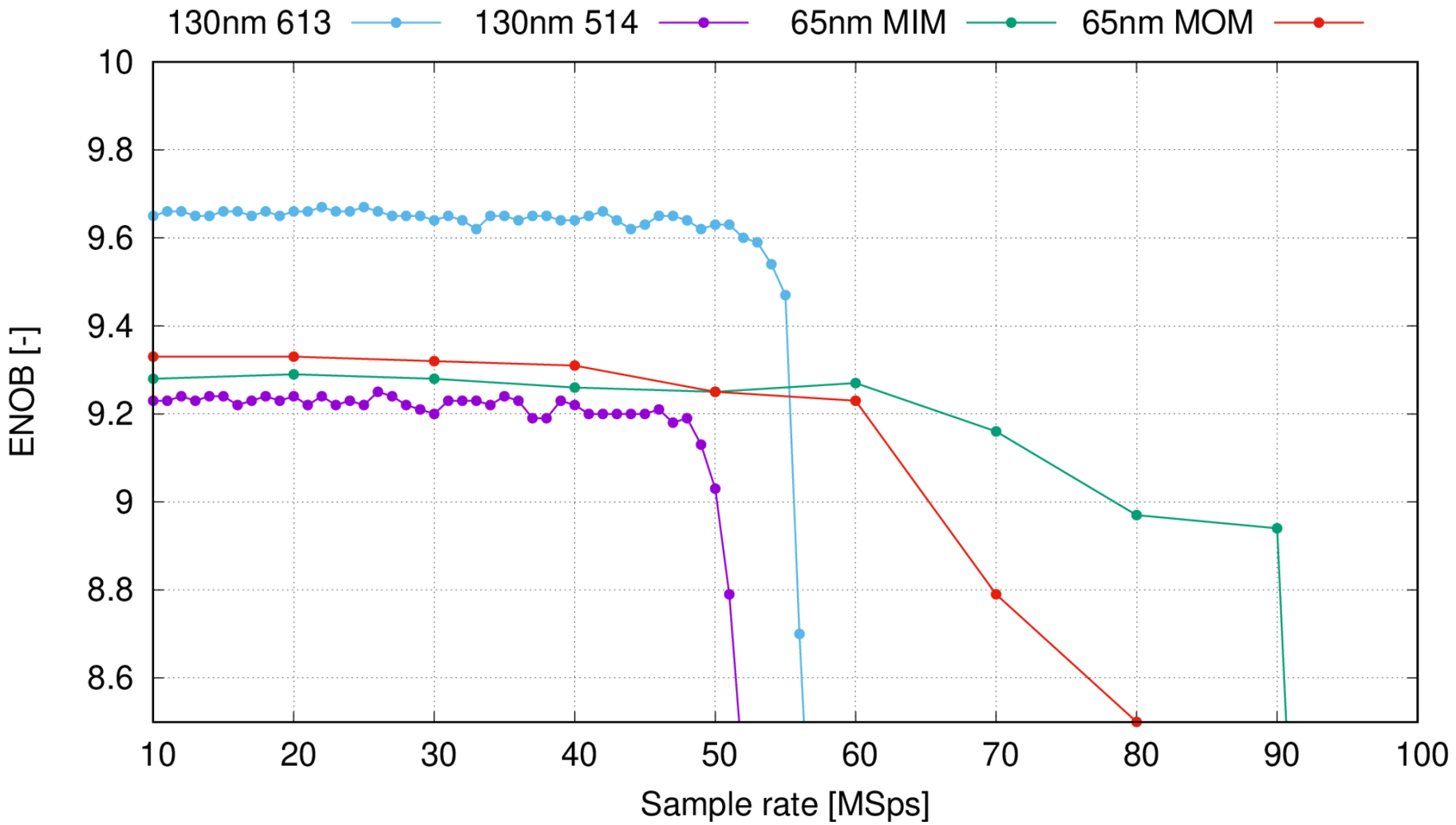
MCS (Merge Capacitor Switching) scheme



First comparison done before any switching – (N-1) capacitors needed

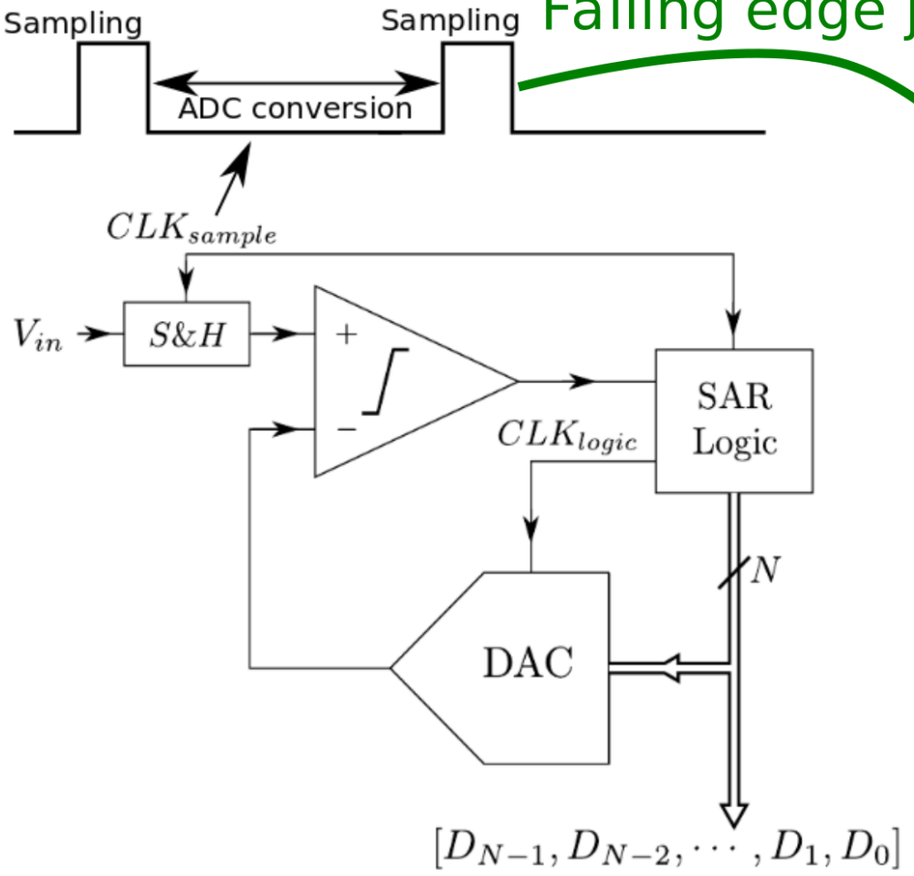


Measurements: ADC dynamic metrics – 65nm and 130nm comparison

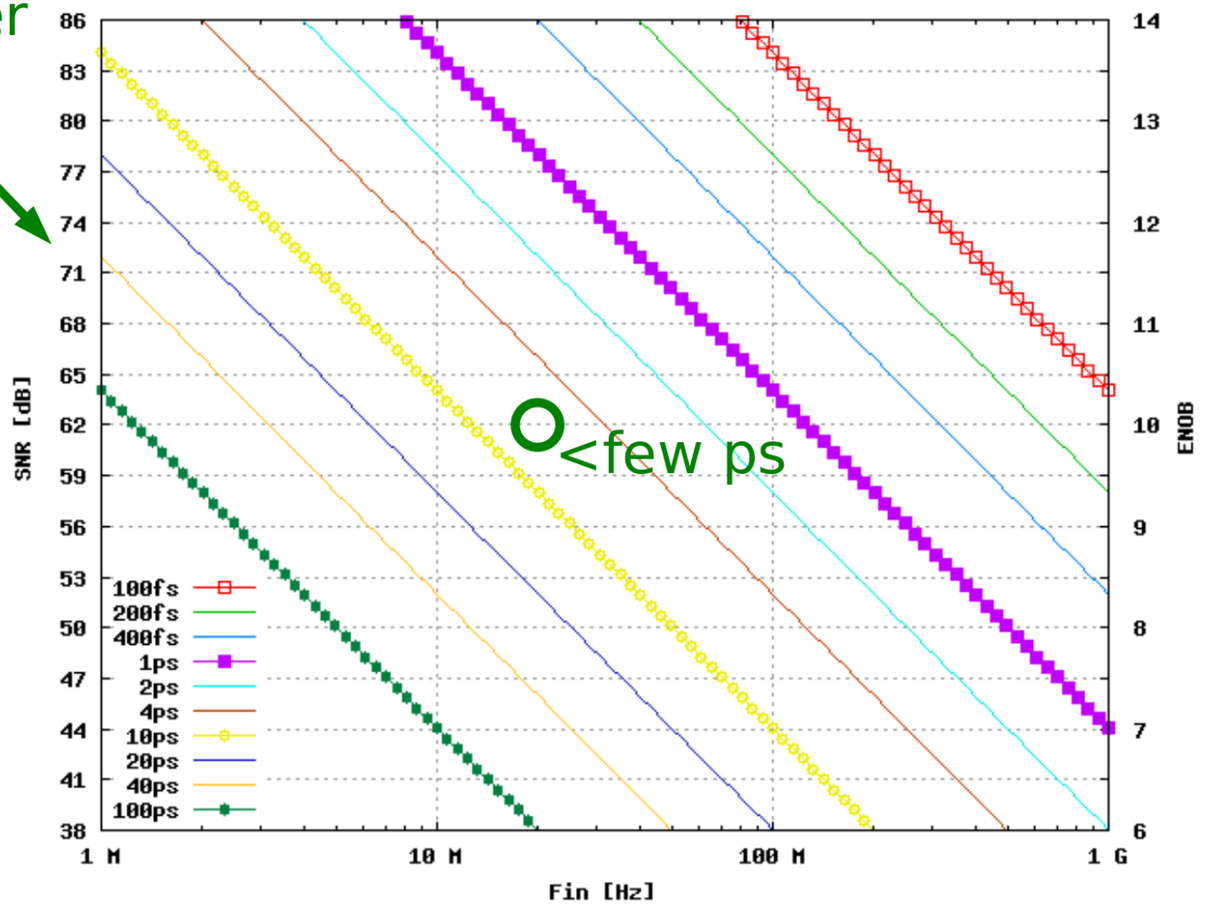


- 130nm 613 – excellent performance up to 55 MSps
- 130nm 514 and 65nm – similar, with 65nm being faster (MIM version up to 90 MSps)

SAR ADC – sampling clock jitter



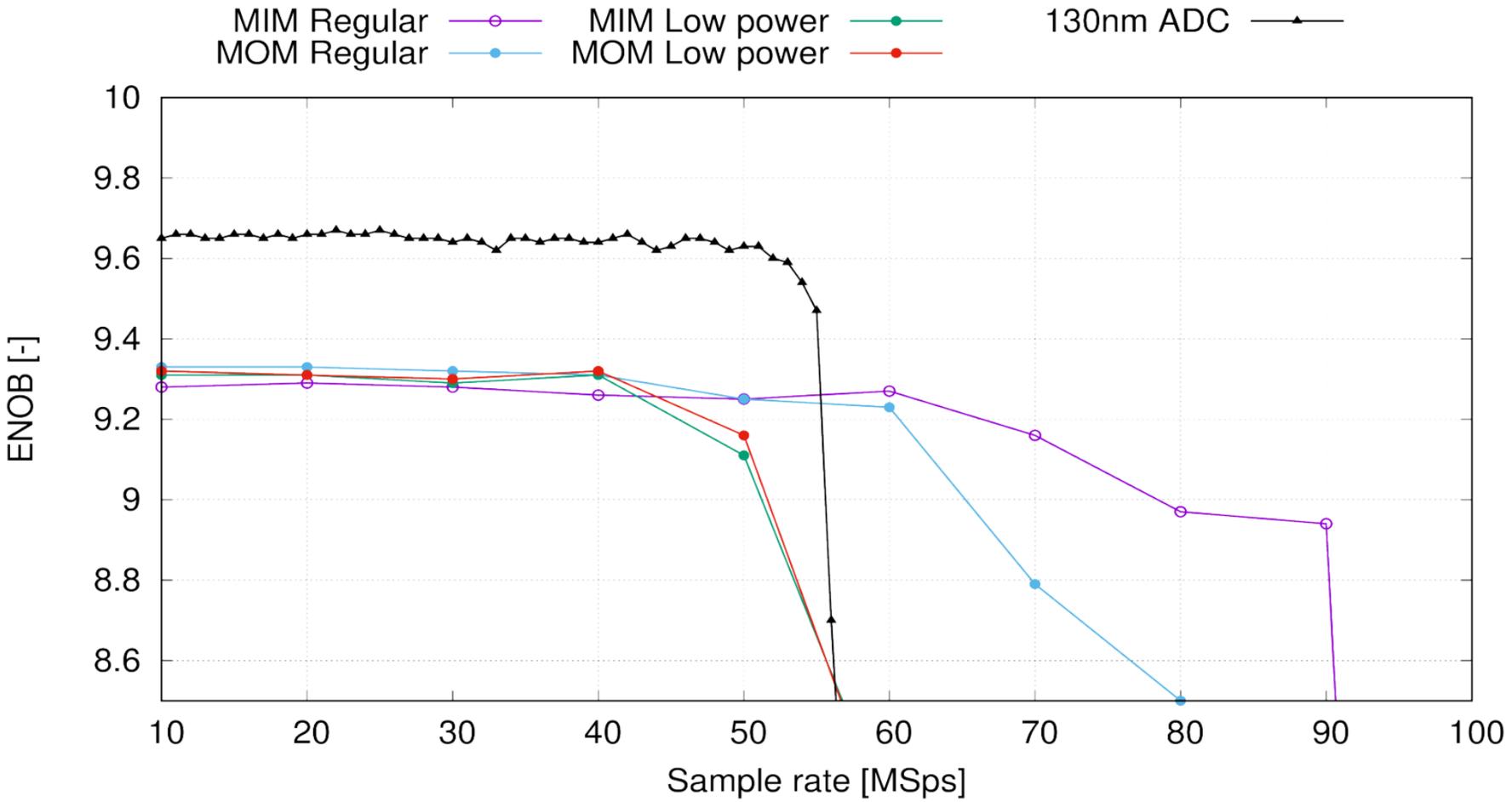
Falling edge jitter



O<few ps

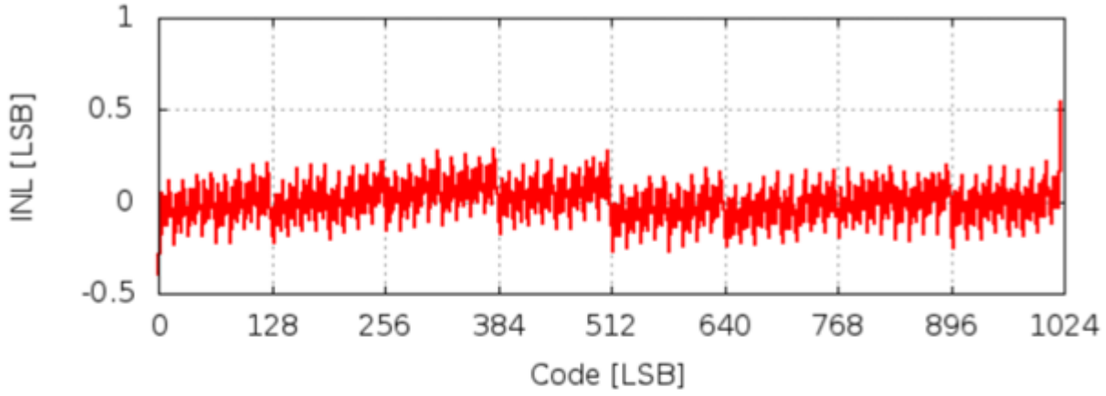
- To achieve 10b resolution (SNR = 61.96 dB), jitter of the end of the sampling phase, for 20 MHz input frequency, have to be lower than few ps.
- If the sampling clock provided to the ADC (in reference to the input sine wave) has already higher jitter, it will artificially degrade ADC performance…

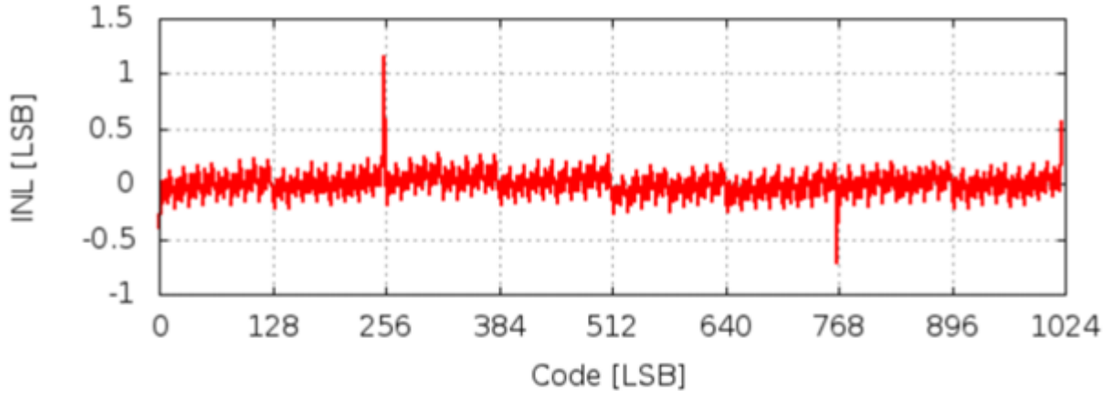
SAR ADC – 65nm “low power” control logic

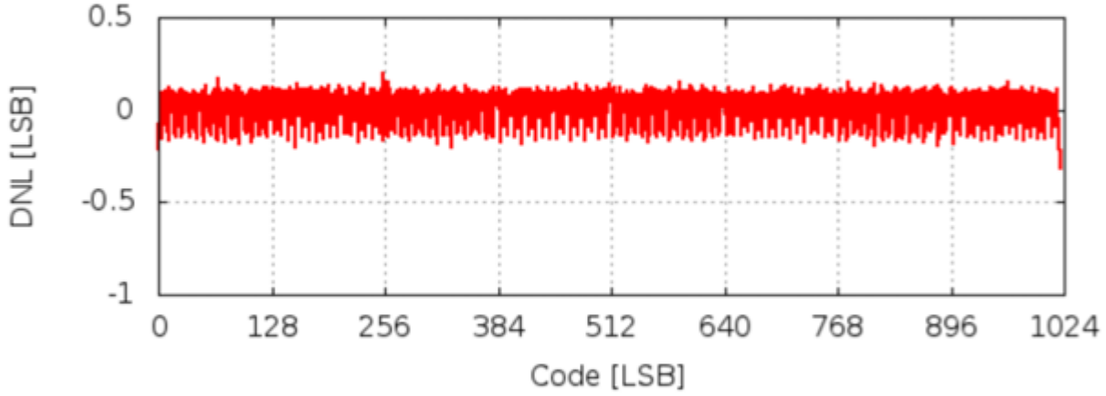


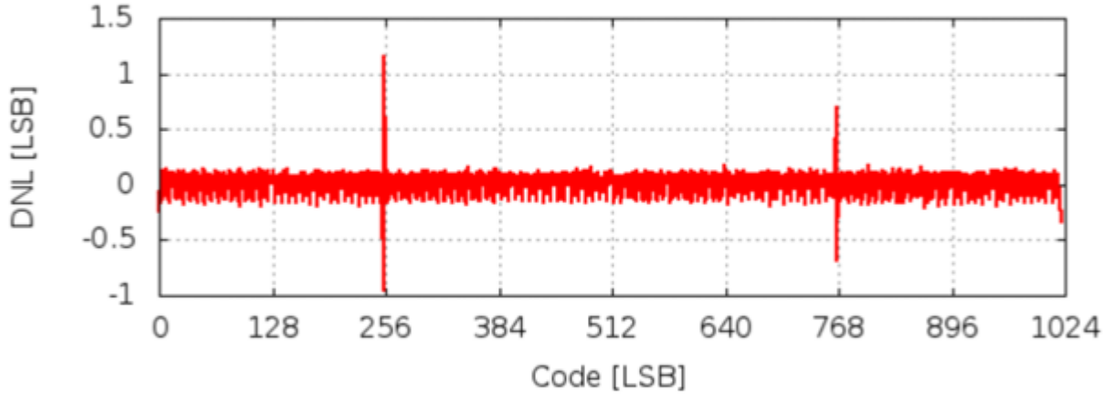
We have also made “low power” version of control logic in 65nm, but the performance is not the best – ENOB similar to the “regular” version, but sampling rate limit as in 130nm

SAR ADC – settling delay tuning





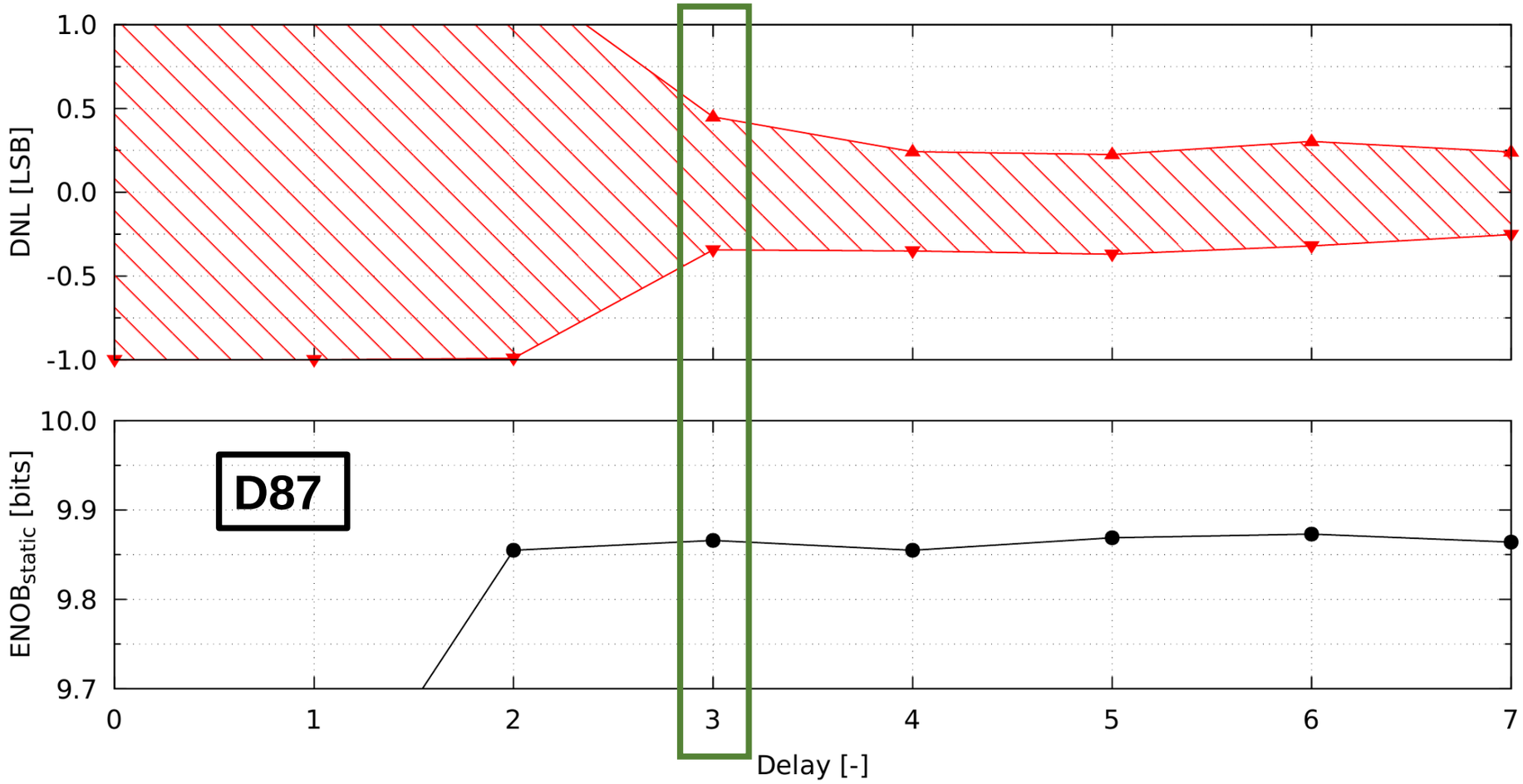




- **DAC 613 – maximal delay**
- -0.32 < **DNL** < 0.20
- -0.40 < **INL** < 0.54
- Static **ENOB** = 9.92
- Max sampling rate ~ **30 MSps**

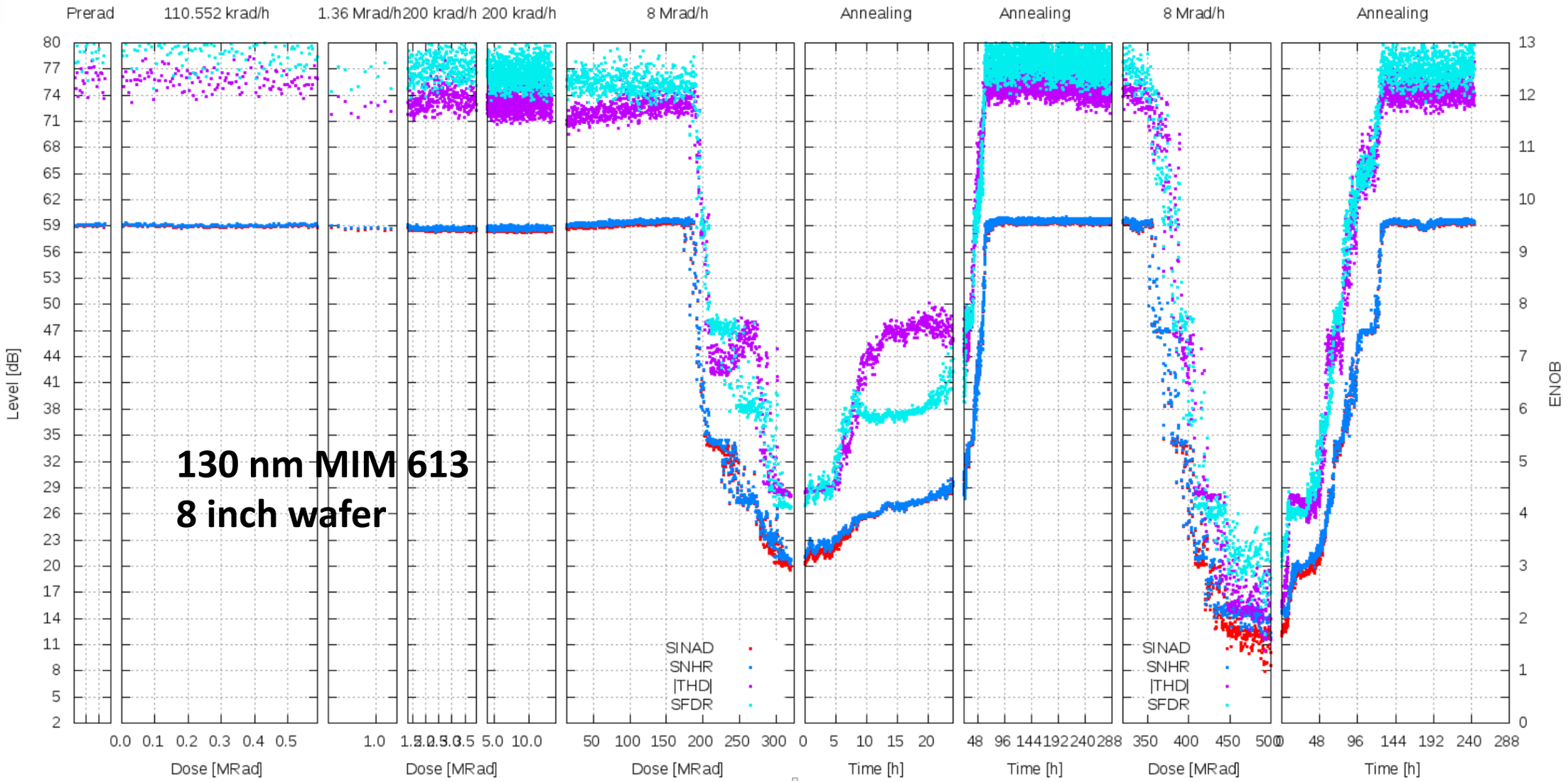
- **DAC 613 – shorter delay**
- -0.96 *(-0.35)* < **DNL** < *(0.20)* 1.15
- -0.70 *(-0.40)* < **INL** < *(0.55)* 1.15
- Static **ENOB** = 9.9
- Max sampling rate ≥ **40 MSps**

SAR ADC – settling delay tuning



1. Measure static metrics, scanning delay for each group (4 groups x 8 settings = 32 meas.)
2. Get minimal and maximal value of the DNL and calculate static ENOB
3. Choose smallest delay providing similar performance to the longest one

Radiation hardness of ADC in 130nm CMOS technology



No effect up to 200 Mrad. Resolution degradation above (high dose intensity), recovered after annealing even above 500 Mrad