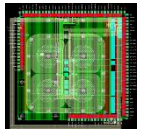
Fast Timing with ALTIROC and LIROC

Front End Electronics 2023
Torino

Christophe de LA TAILLE (OMEGA)

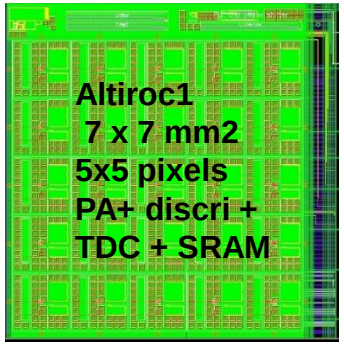
ATLAS LGAD readout : ALTIROC (TSMC 130n)

2016

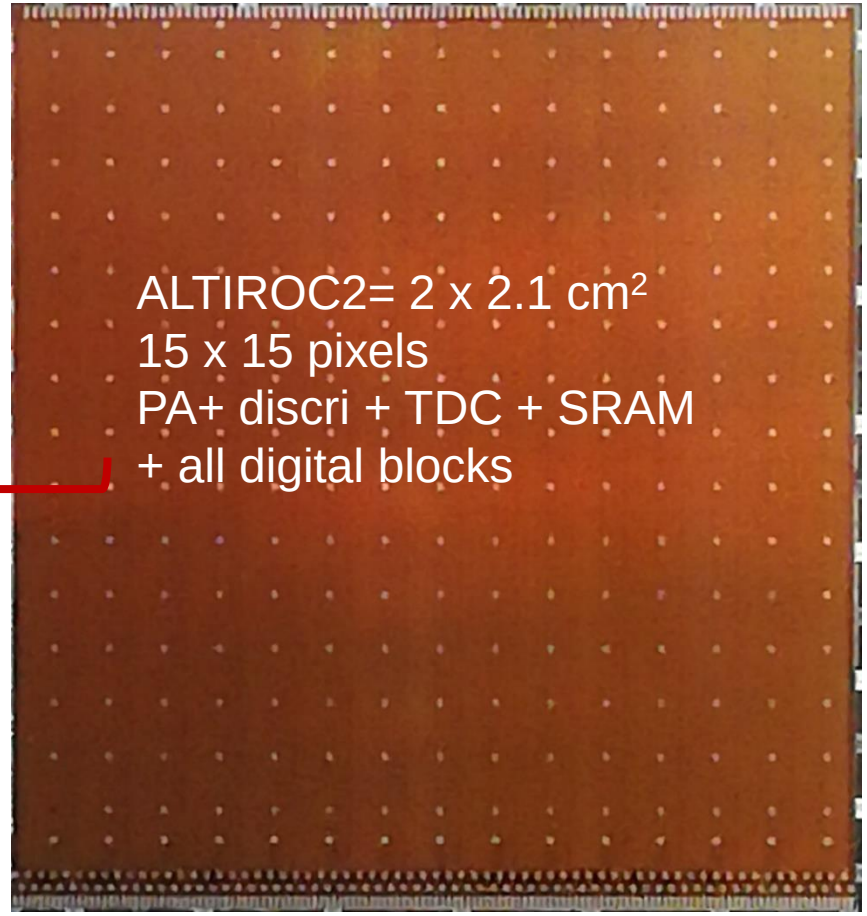


Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

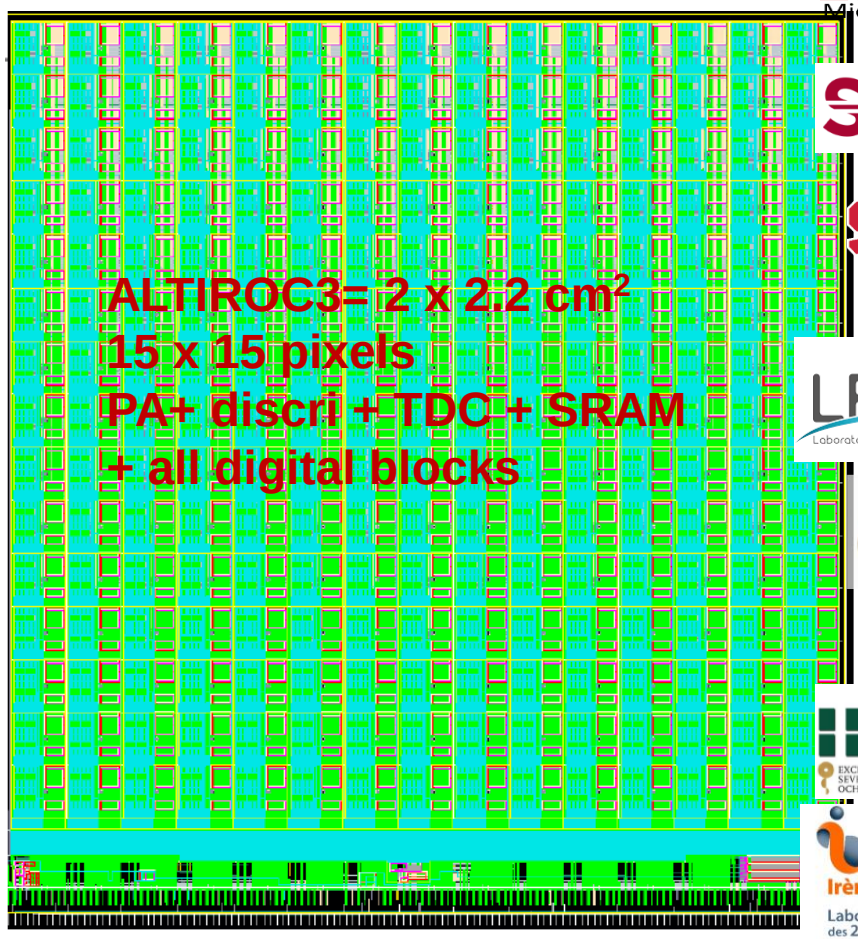
2017



2019



2022

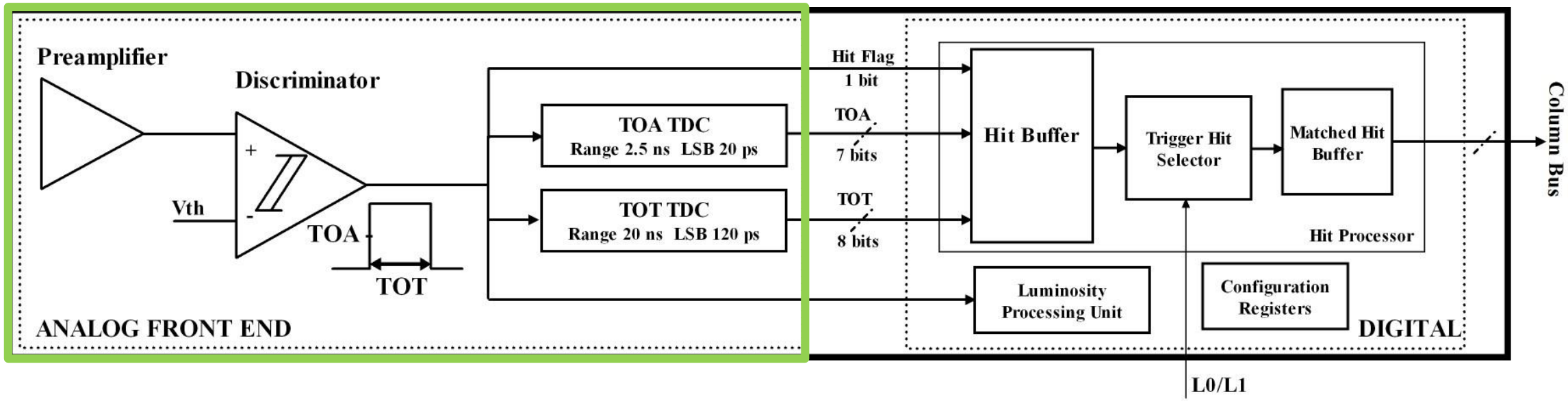


Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

ALTIROC2 : pixel analog front-end



ALTIROC2's pixel integrates :

- A voltage (VPA) or trans-impedance (TZ) **1 GHz preamplifier** followed by a high-speed **discriminator**:
  - Time walk correction made with a Time over Threshold (TOT) architecture
  - Main challenge = small jitter (low noise/capacitance) down to 4 fC

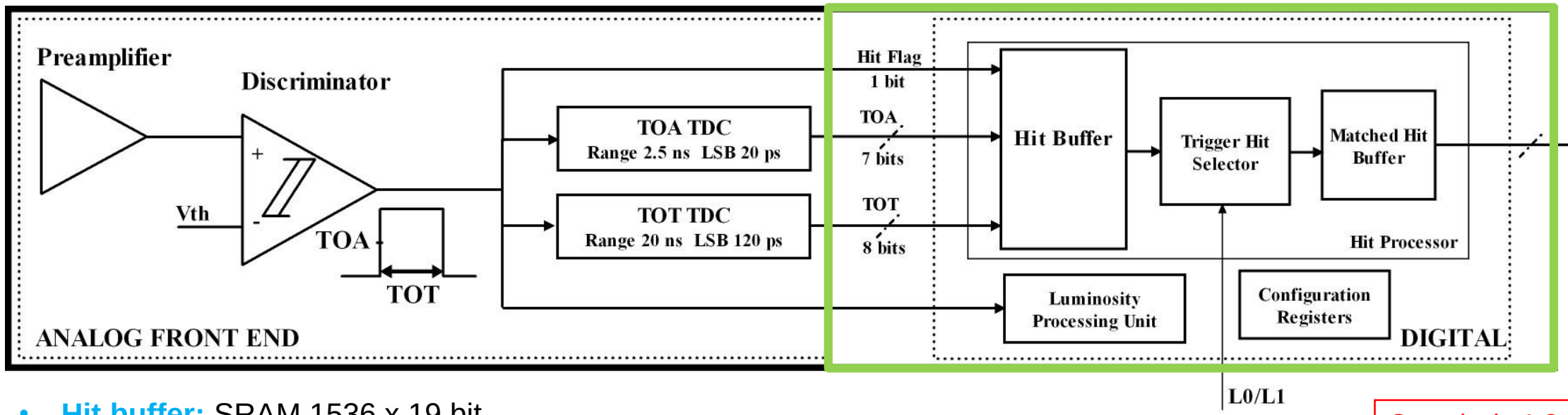
  ⇒ **Analog FE performance crucial**

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

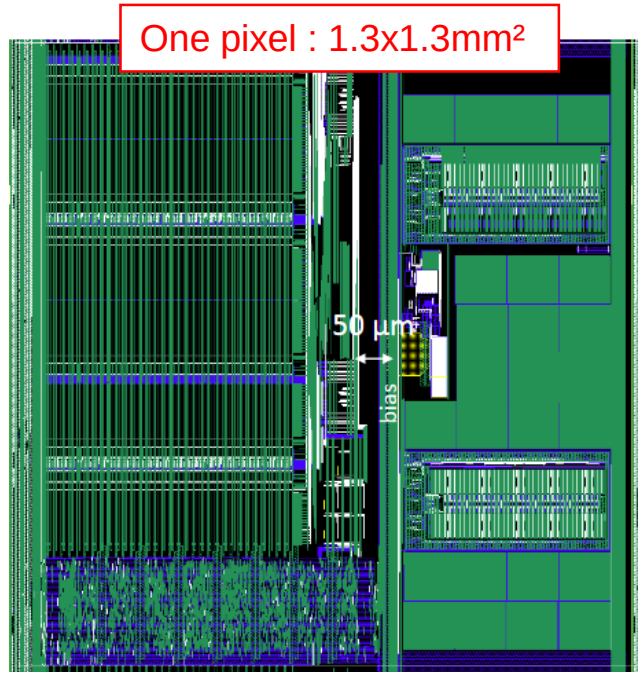
C_d: sensor cap (~4 pF)
t_d: LGAD drift time, 600 ps
Q_{in}: MIP charge (10 fC at start, 4 fC at end)
e_n: noise spectral density of input trans.

- **Two TDC** (Time to Digital Converter) to provide Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
  - TOT TDC: bin of 120 ps (8 bits), range of 20 ns

ALTIROC2 : pixel digital back-end

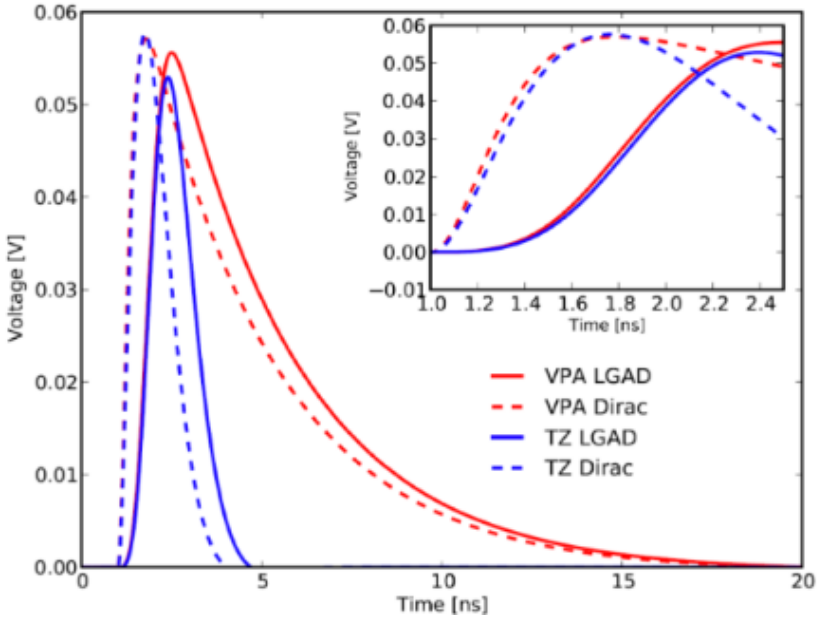


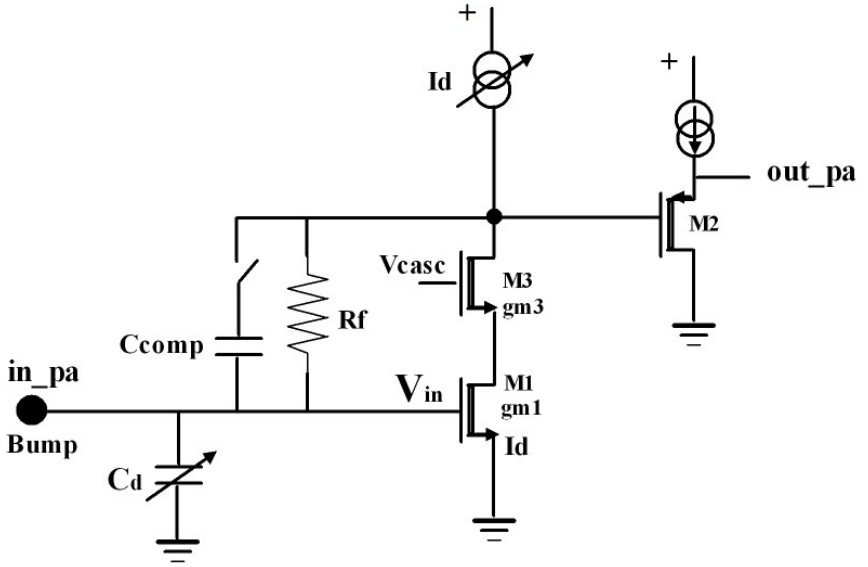
- **Hit buffer:** SRAM 1536 x 19 bit
  - Circular buffer to store timing data for each bunch-crossing, until a L1 trigger arrives
  - Data = TOT and TOA bits, only in case of hit to save power ; with zero suppress.
  - Depth of about 38 µs
- **Trigger Hit Selector:**
  - Each received trigger associated to a trigger tag
  - If data stored in Hit buffer related to received trigger, TOA/TOT data + trig tag stored into Matched Hit Buffer
- **Matched Hit Buffer:** 32 positions FIFO
  - Control Unit: looks for data related to a trigger event when requested by the End Of Column
  - Matched flag handled through a priority OR chain. Pixel at the top of the column with highest priority
  - Synchronous readout at 40 MHz
- **Luminosity process unit**
  - checks if hits are within 2 programmable windows
- **I2C configuration registers**

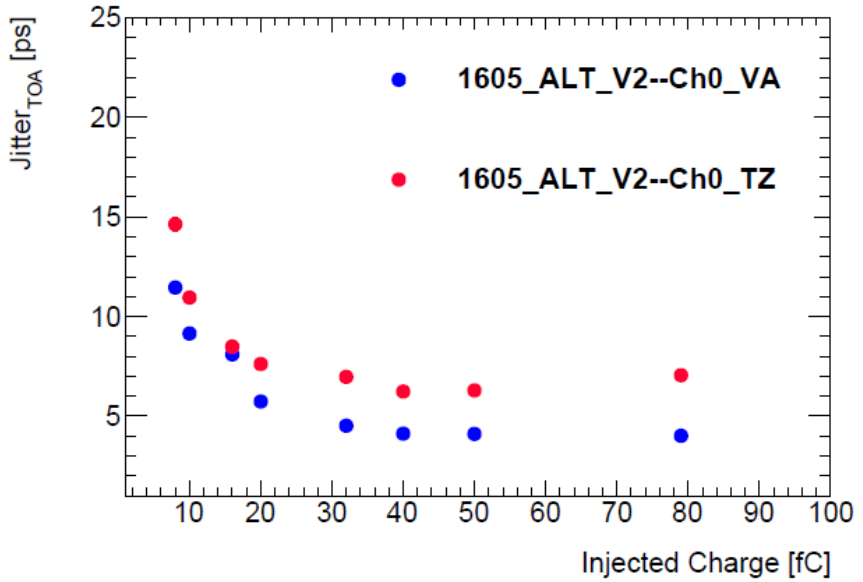


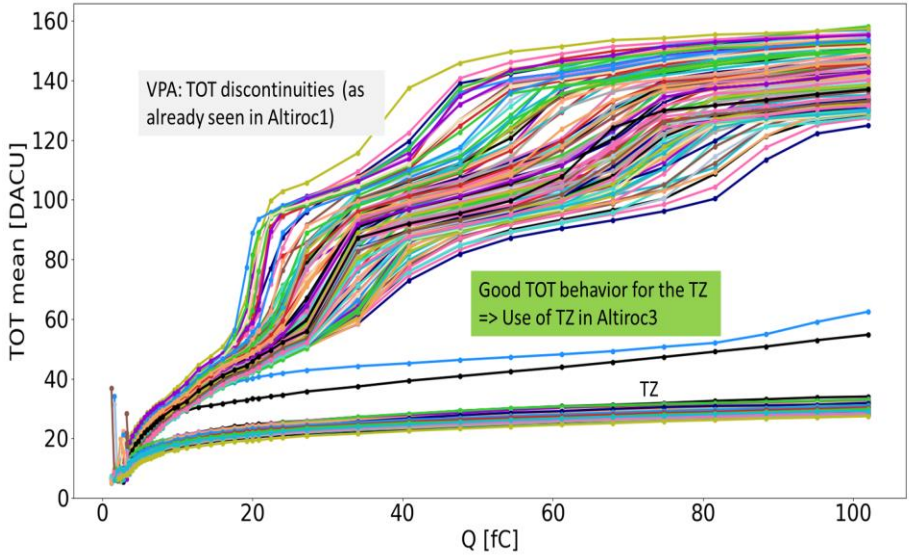
ALTIROC1 : voltage and TZ preamps, test pulse

- « voltage » PA (VPA)
  - Rf = 12k/25k
  - G0 ~ 26 dB
  - Less parallel noise
- Transimpedance PA (TZ)
  - Rf = 4k (+opt Cf)
  - G0 ~ 50 dB
  - Shorter occupancy
  - Better ToT
- Test-pulse
  - « delta » via Ctest : optimistic
  - Rtest added in series
  - Slower rise-time (matche to LGAD pulse)









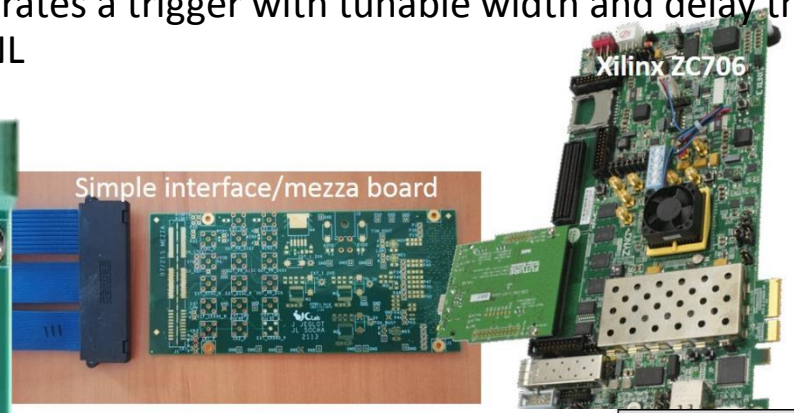
Testbench for ALTIROC2

- Setup = ASIC board (ASIC alone or bump bonded onto sensor) + interface board + FPGA board

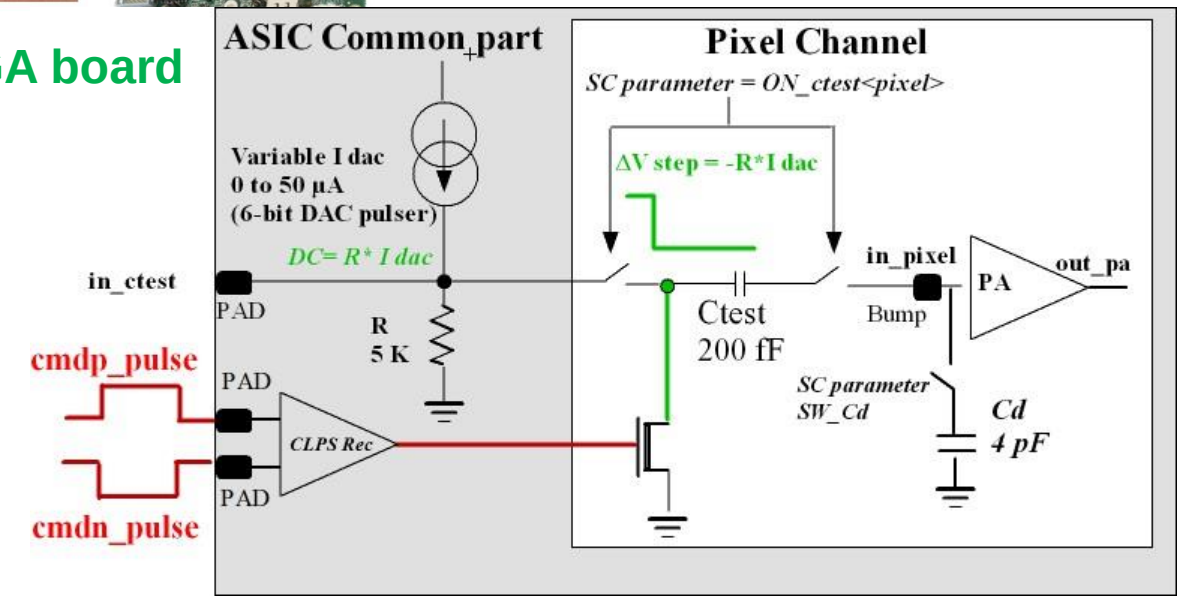
- **Front-end calibration :** charge injection (0 up to 50 fC) using **ASIC internal calibration pulser**, controlled by the FPGA, synchronous to 40 MHz clock, ASIC alone: Cd=3,5 pF can be set by SC to mimic sensor capacitor

- **TOA/TOT TDC calibration :** ASIC periphery generates a trigger with tunable width and delay thanks to the phase shifted 640 MHz clock from the PLL + Random Phase Generator for DNL

ASIC board

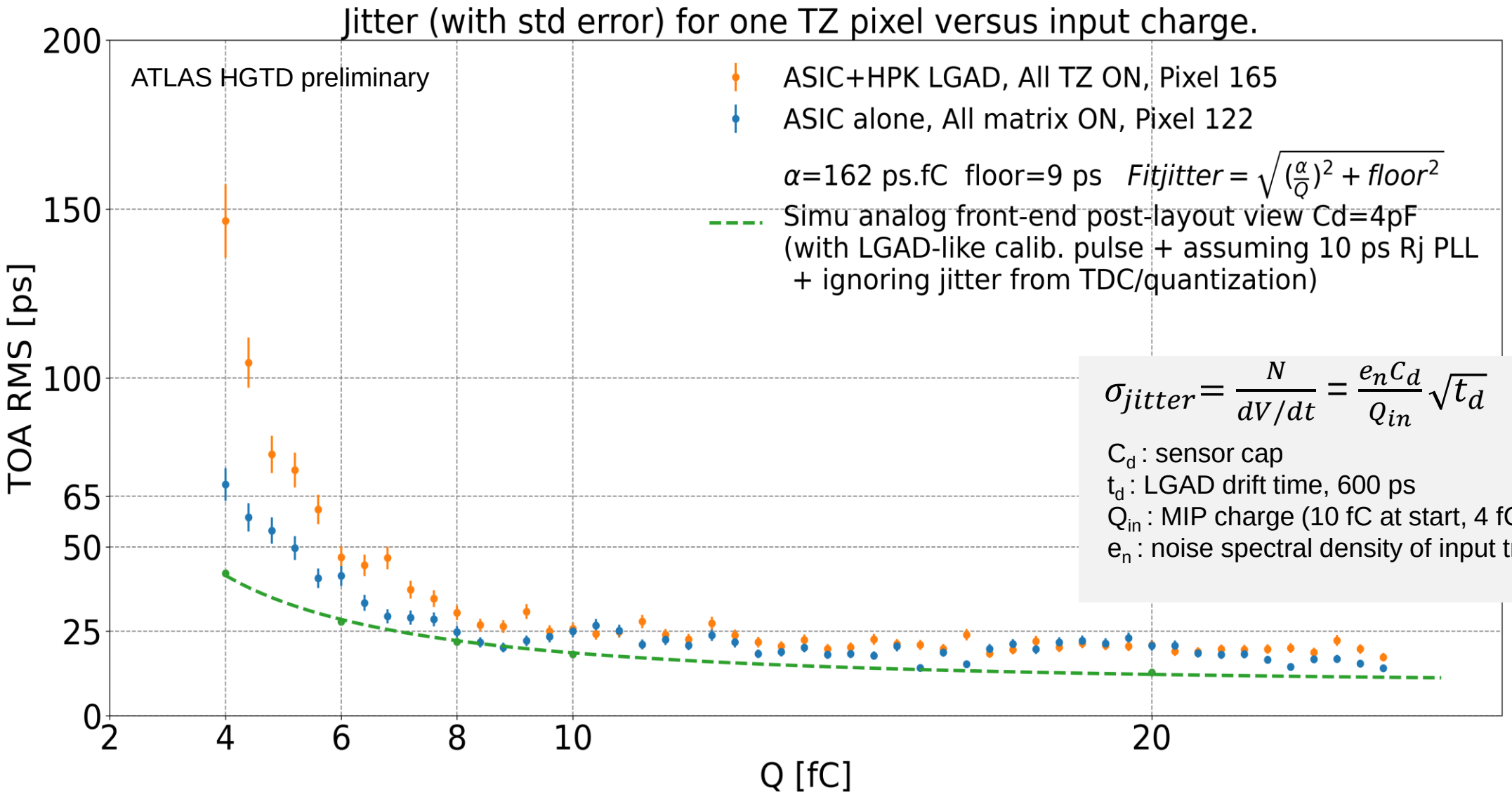


Interface + FPGA board



Designed by Pierrick Dinaucourt (OMEGA)

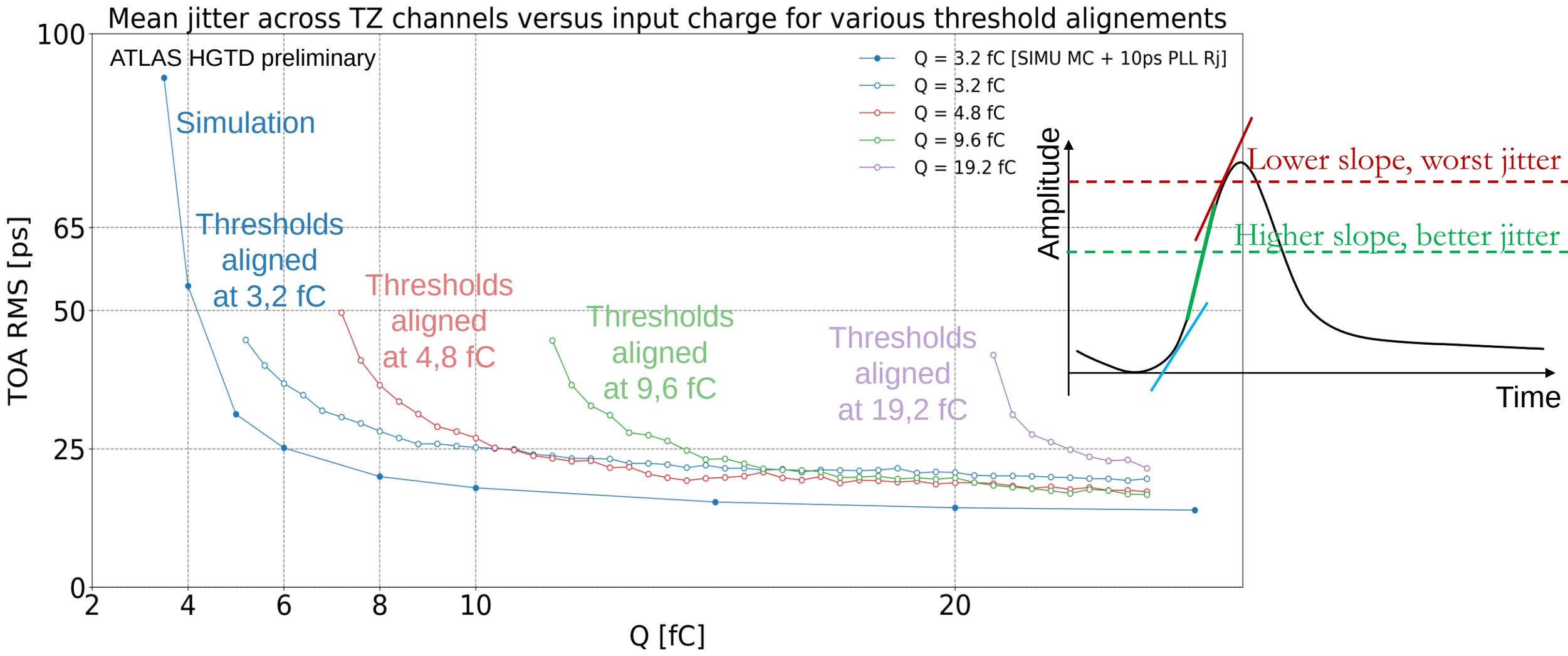
Comparing measured time-of-arrival jitter with simulation



$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

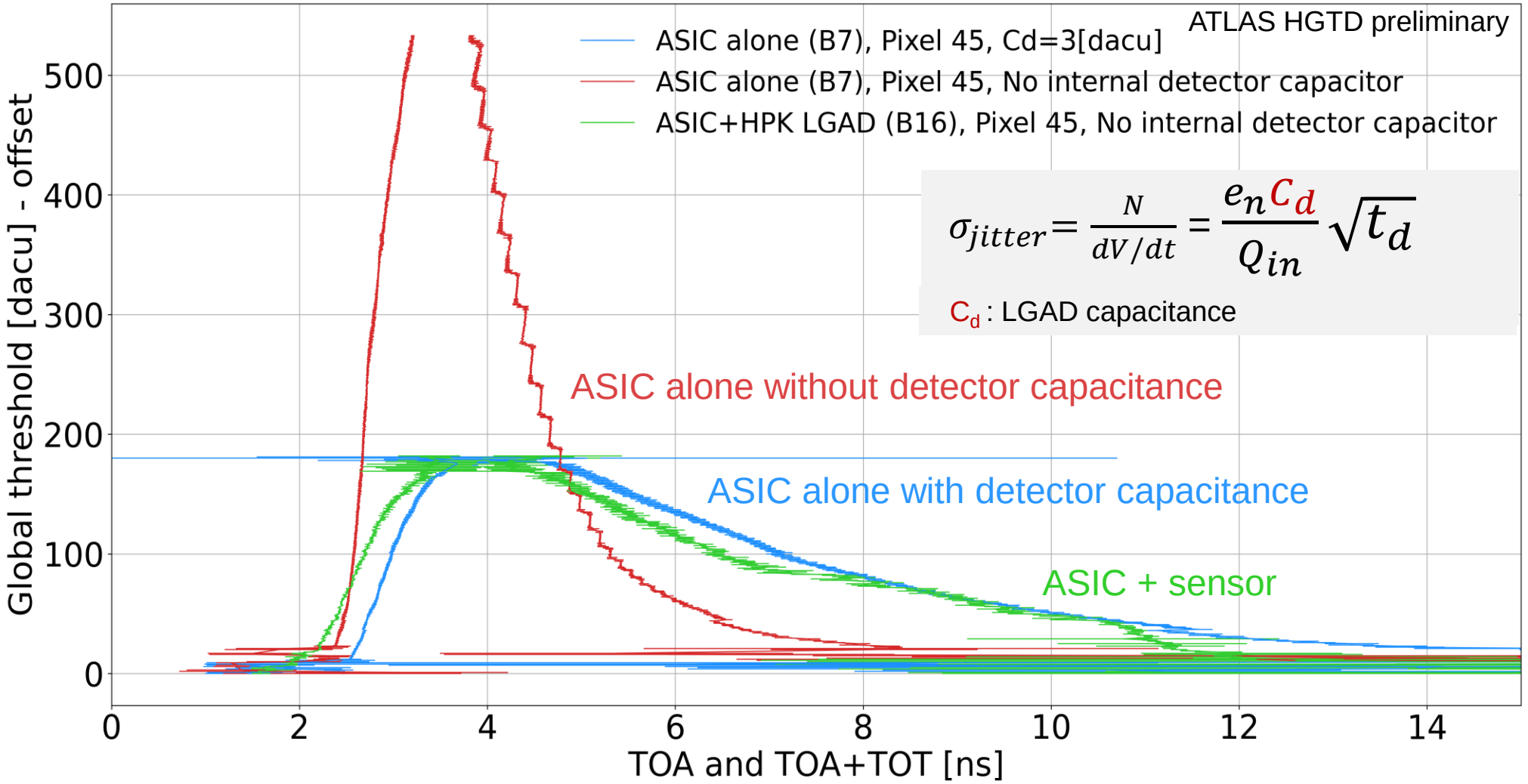
C_d : sensor cap
t_d : LGAD drift time, 600 ps
Q_{in} : MIP charge (10 fC at start, 4 fC at end)
e_n : noise spectral density of input trans.

Jitter depends on the charge, but also on the discriminator thres.



Threshold trade-off to maximise pulse slope (dV/dt), thus minimize jitter.

Is the internal detector capacitance equivalent to an LGAD's ?

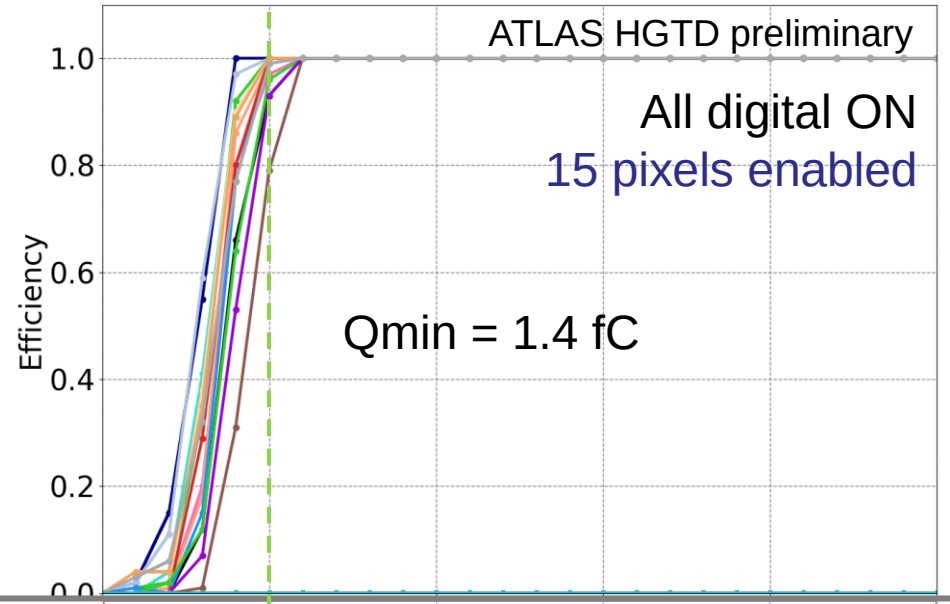


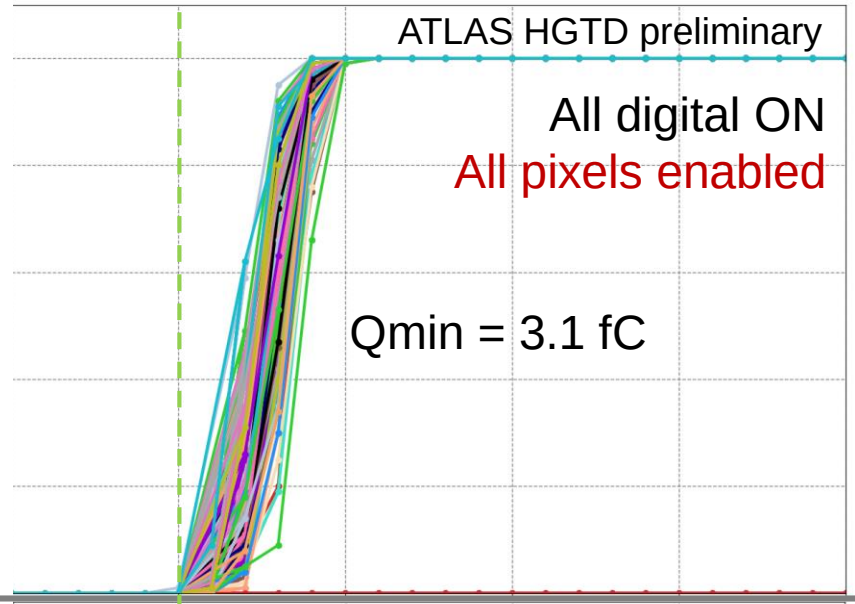
with calibration pulse

Pulse reconstruction of a voltage preamplifier, between ASIC alone and ASIC + sensor :
Showing same amplitude & falling edge decay time → the internal LGAD-like capacitance corresponds to 3.5 pF.
Showing slightly slowly rising time → partially explains worst jitter with sensor.

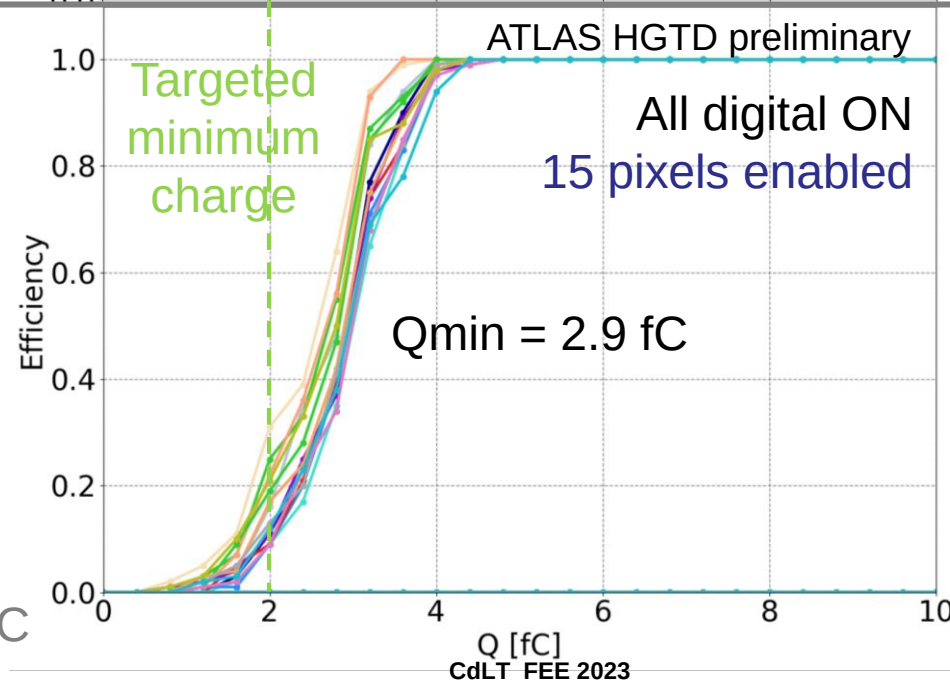
What is the minimum detectable charge ? (Median at 50%)

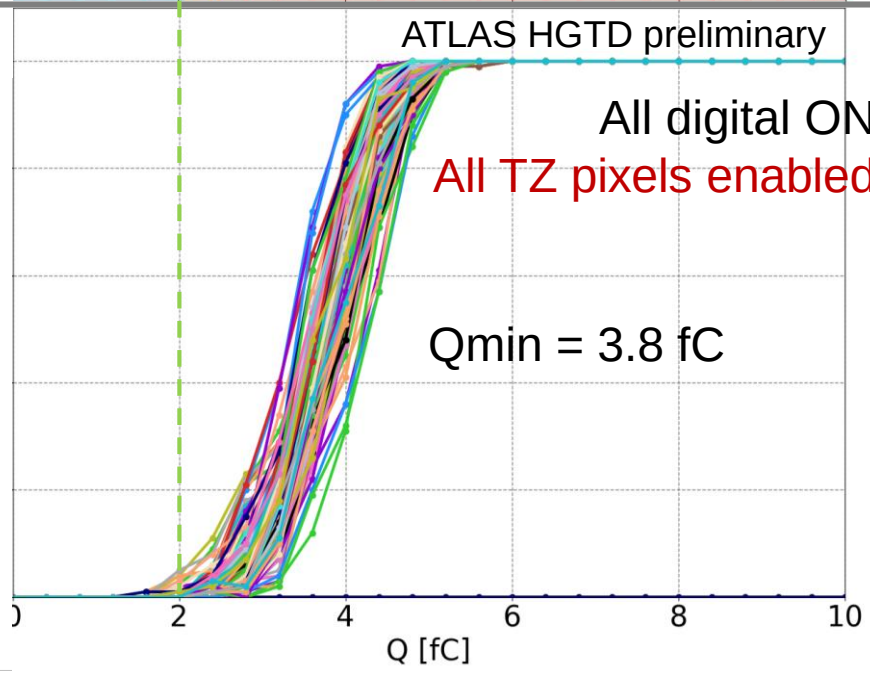
ASIC alone
irradiated up to 200 Mrad





ASIC + LGAD
(unirradiated)





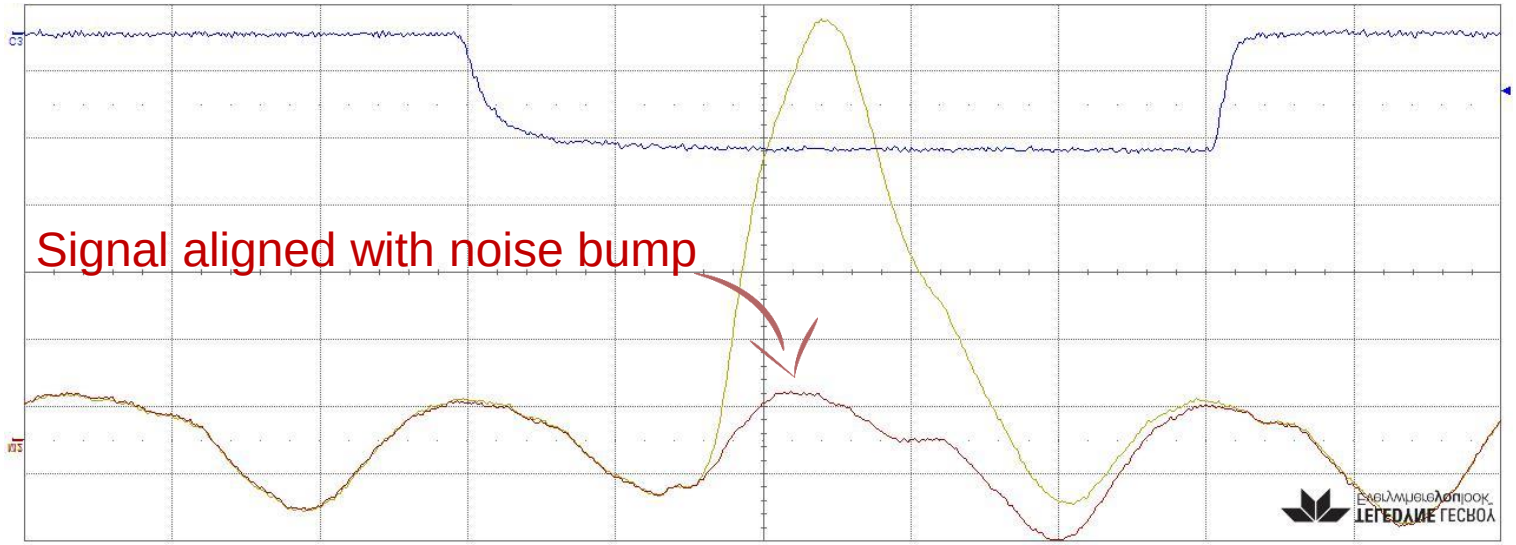
Transimpedance preamplifier results
Thresholds aligned at 3.2 fC

Fighting against digital activity

Probing one transimpedance preamplifier :

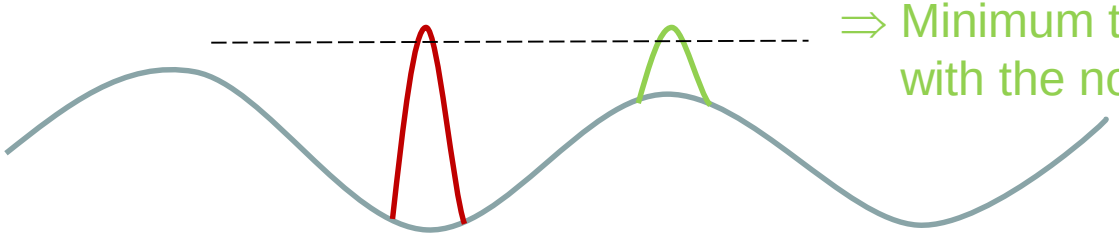
20 fC injected
Signal = 30 mV

ASIC+HPK LGAD biased at -80V (B16)



Digital clock couples on preamplifier gnd input : induces a noise ripple ~ 3 fC = our limit !

Preamplifier output baseline : (exaggerated)

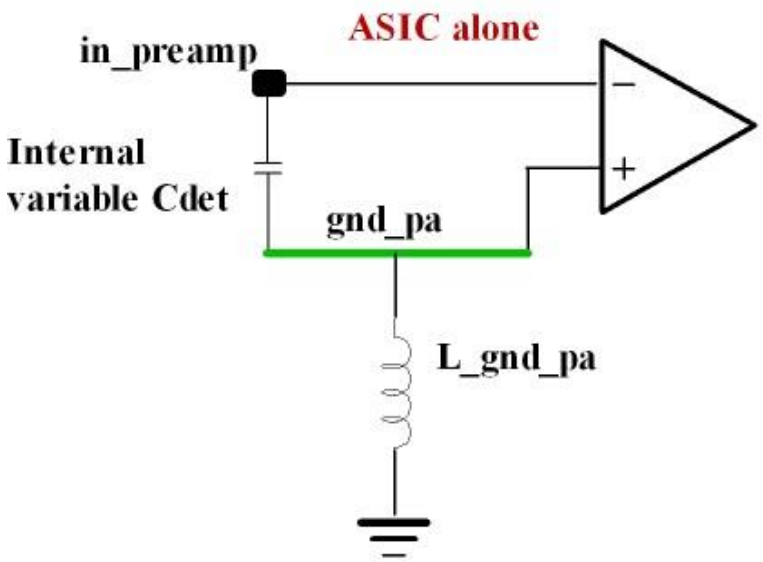


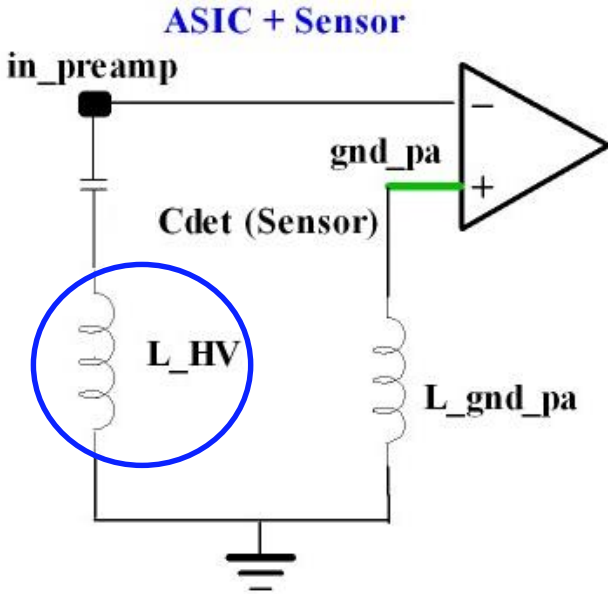
⇒ Minimum threshold obtained aligning the signal with the noise bump.

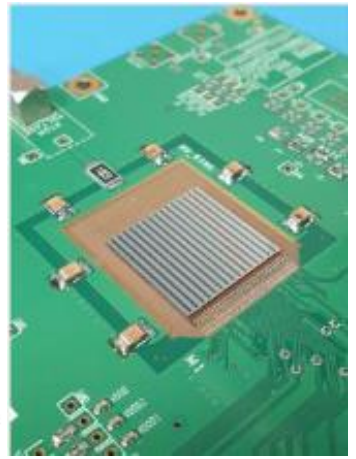
⇒ Signal amplitude seen by the discriminator reduces : “hidden” inside the noise ripple !

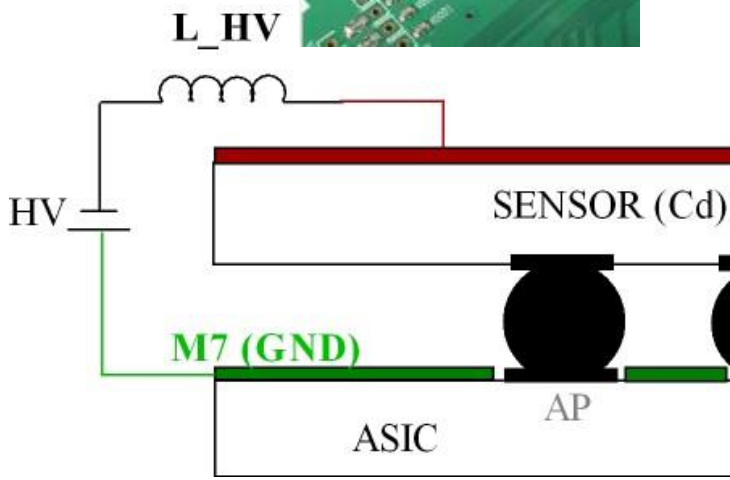
Sensor effect on noise

One channel









Noise on analog gnd amplified x1
"common mode"

ASIC alone = favourable situation

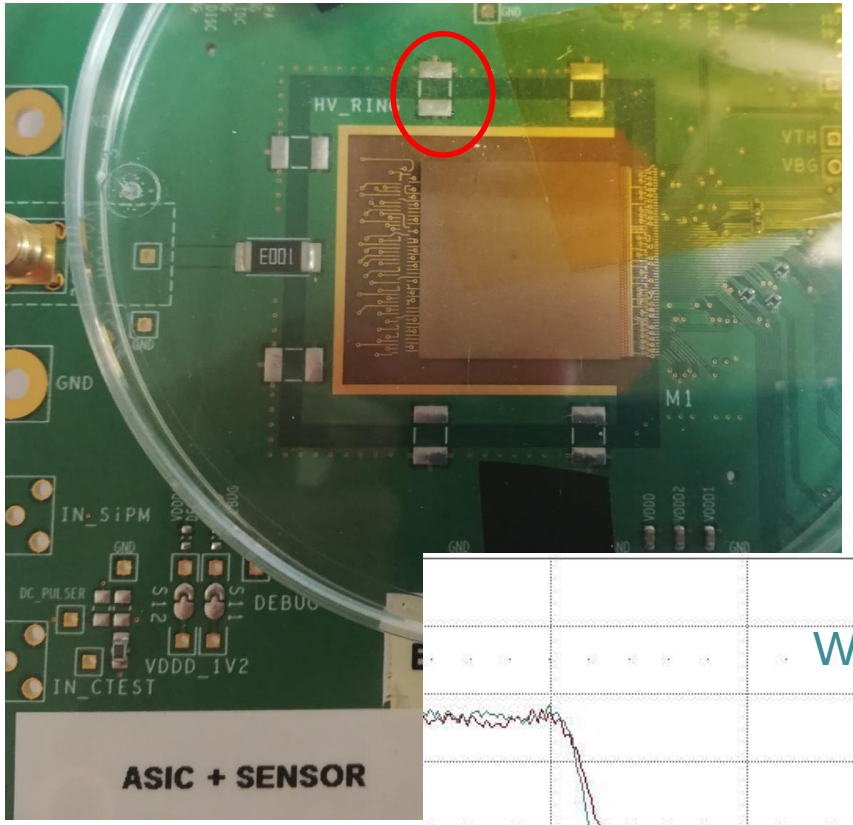
Can this parasitic inductance be hidden from the preamplifier ?

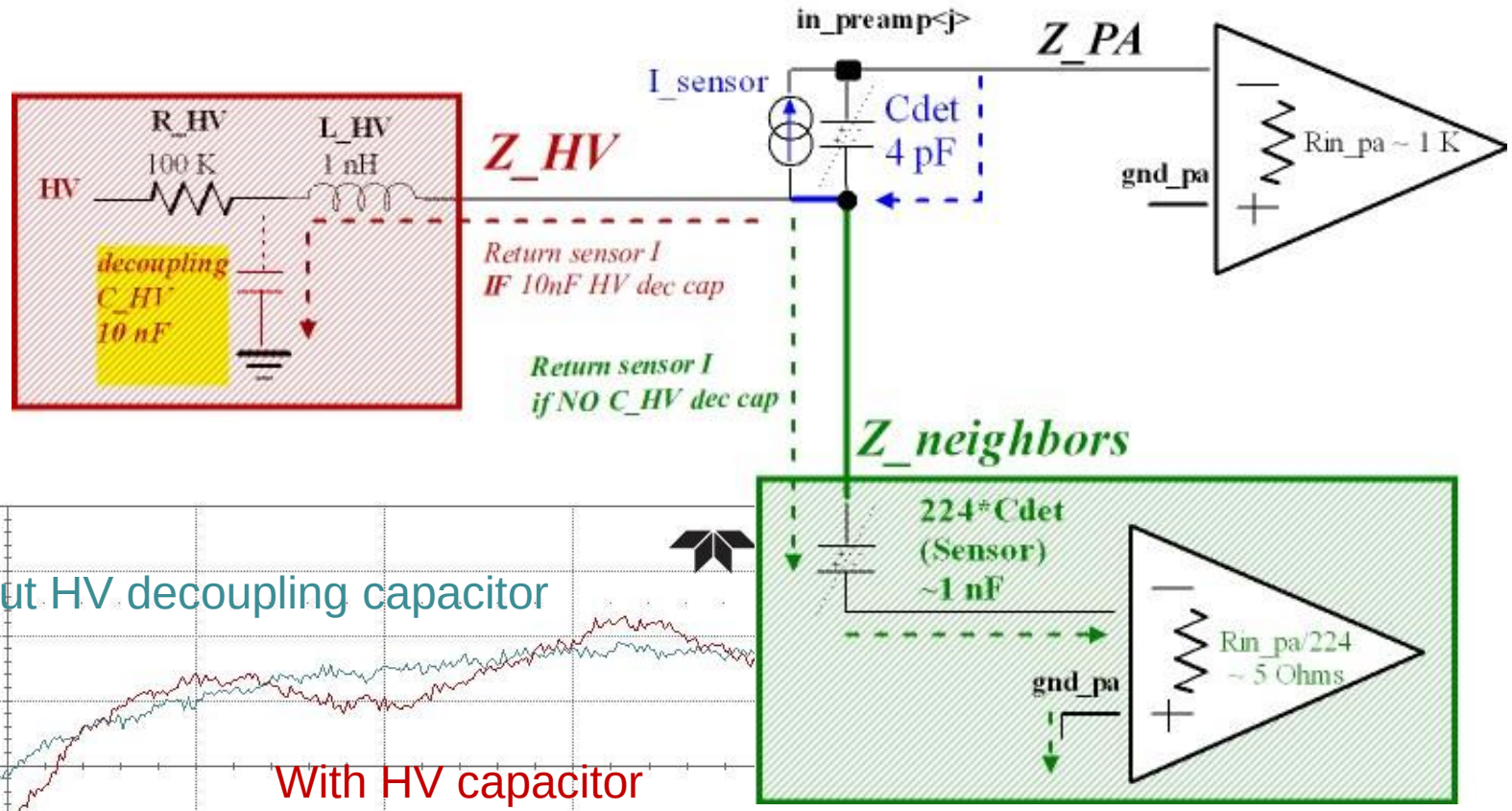
Noise on gnd_pa amplified x20
"differential mode"

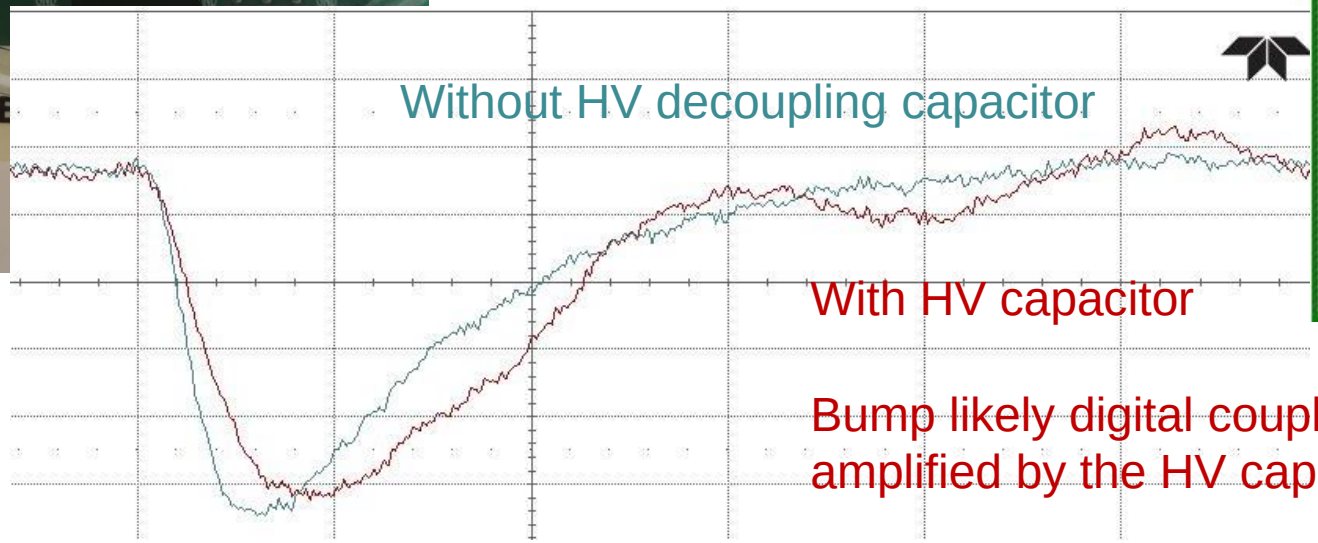
Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero : when the sensor is connected !

Effect of HV decoupling : where is the AC current flowing back to ground ?

10 nF HV decoupling capacitor adds 50% more noise on a TZ output.







Bump likely digital coupling inside the asic amplified by the HV capacitor

Optimal HV impedance is very different for 5x5 and 15x15 sensor

- **HV resistance :**
  - varied from 0 to 1kOhm
  - Effect on gnd_pa noise amplification
    - Goes from 20 to 1
    - ~1 for R>100 Ohm
  - Current return ensured by the 224 spectator channels
    - Was not the case with smaller sensor

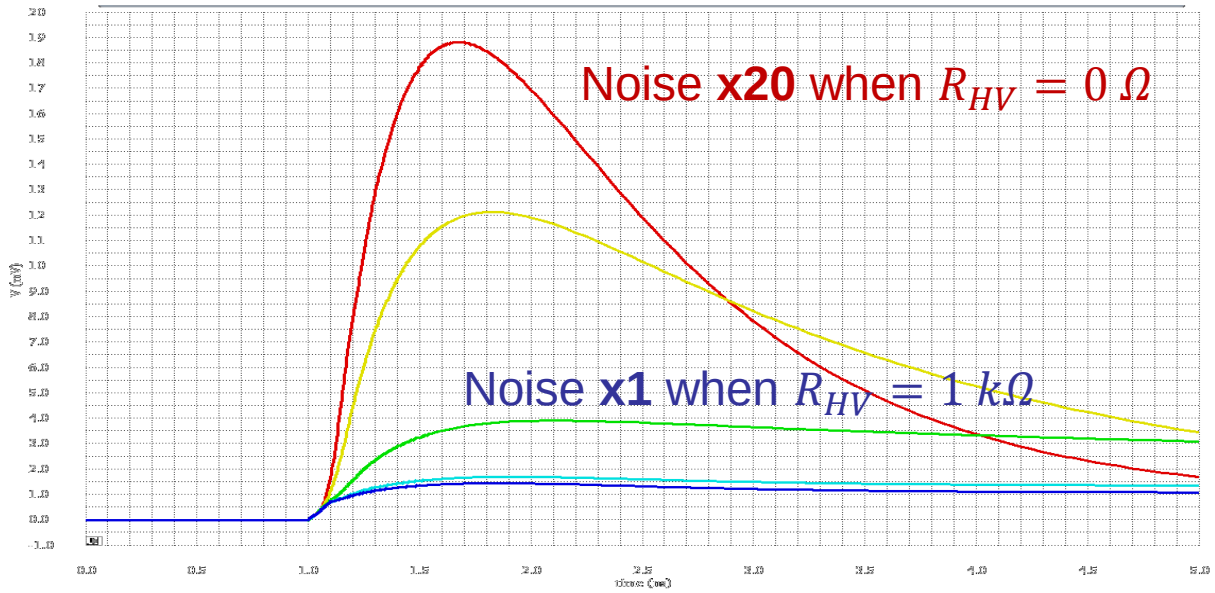
- **HV parasitic inductance :**
  - Effect of 10 nH in HV

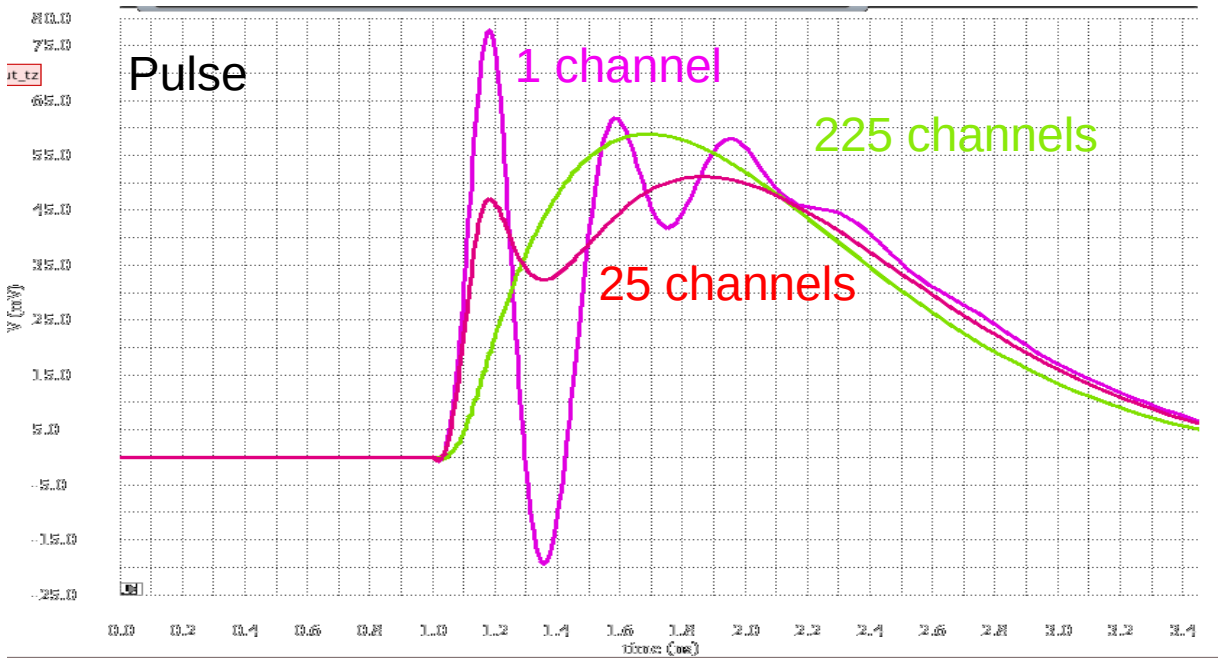
  1 channel, 25 channels, 225 channels

  = Altiroc0/Altiroc1/Altiroc2

Altiroc2 doesn't suffer from HV parasitic inductance !

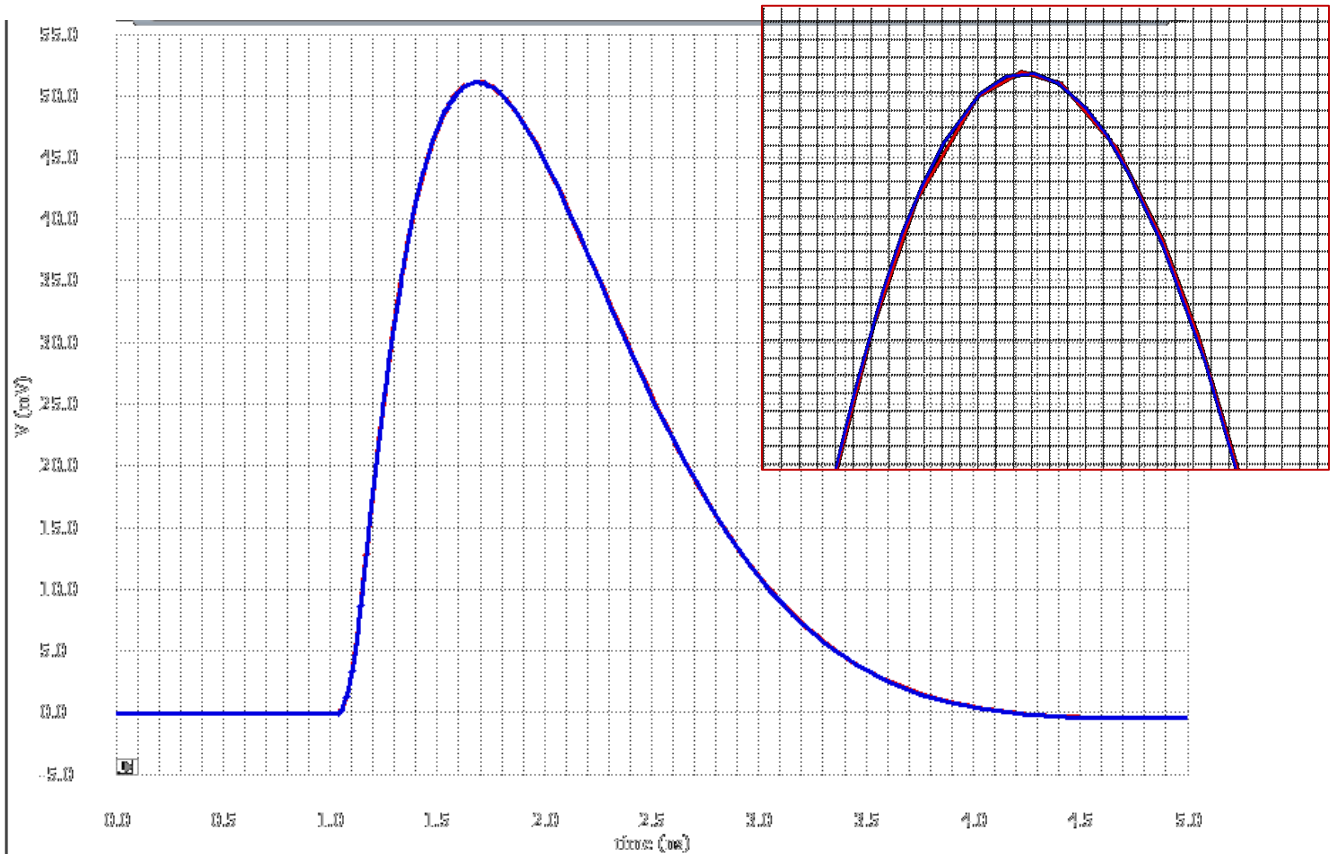
Noise amplified by PA as signal



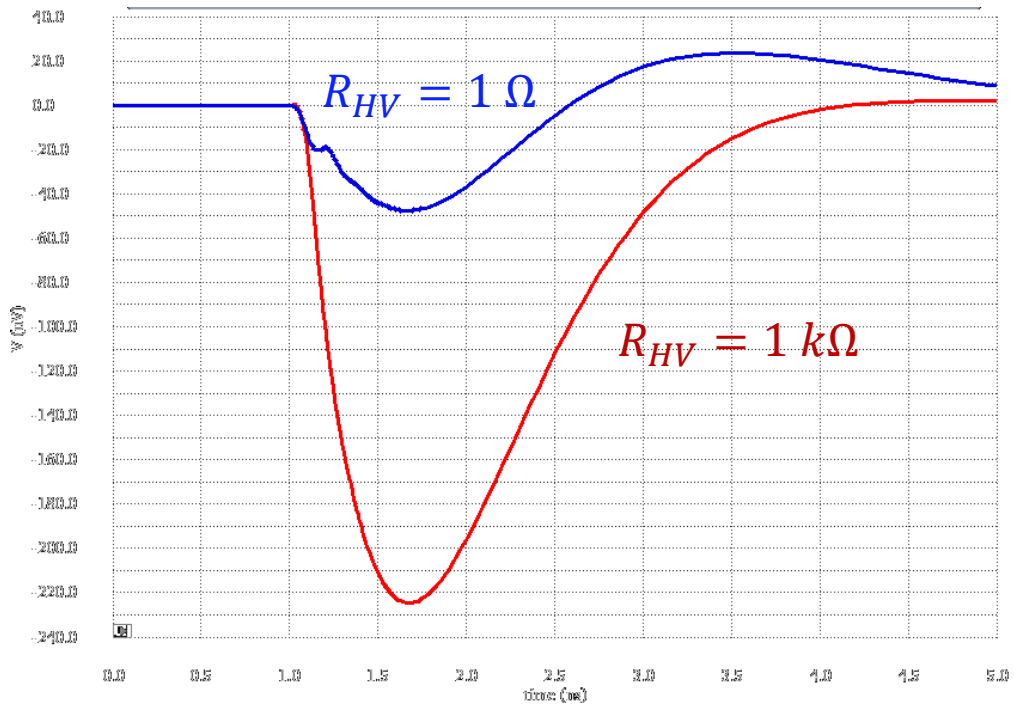


HV impedance effect on signal & crosstalk ?

Signal injected still intact :



Negligible crosstalk on neighbour preamplifier :

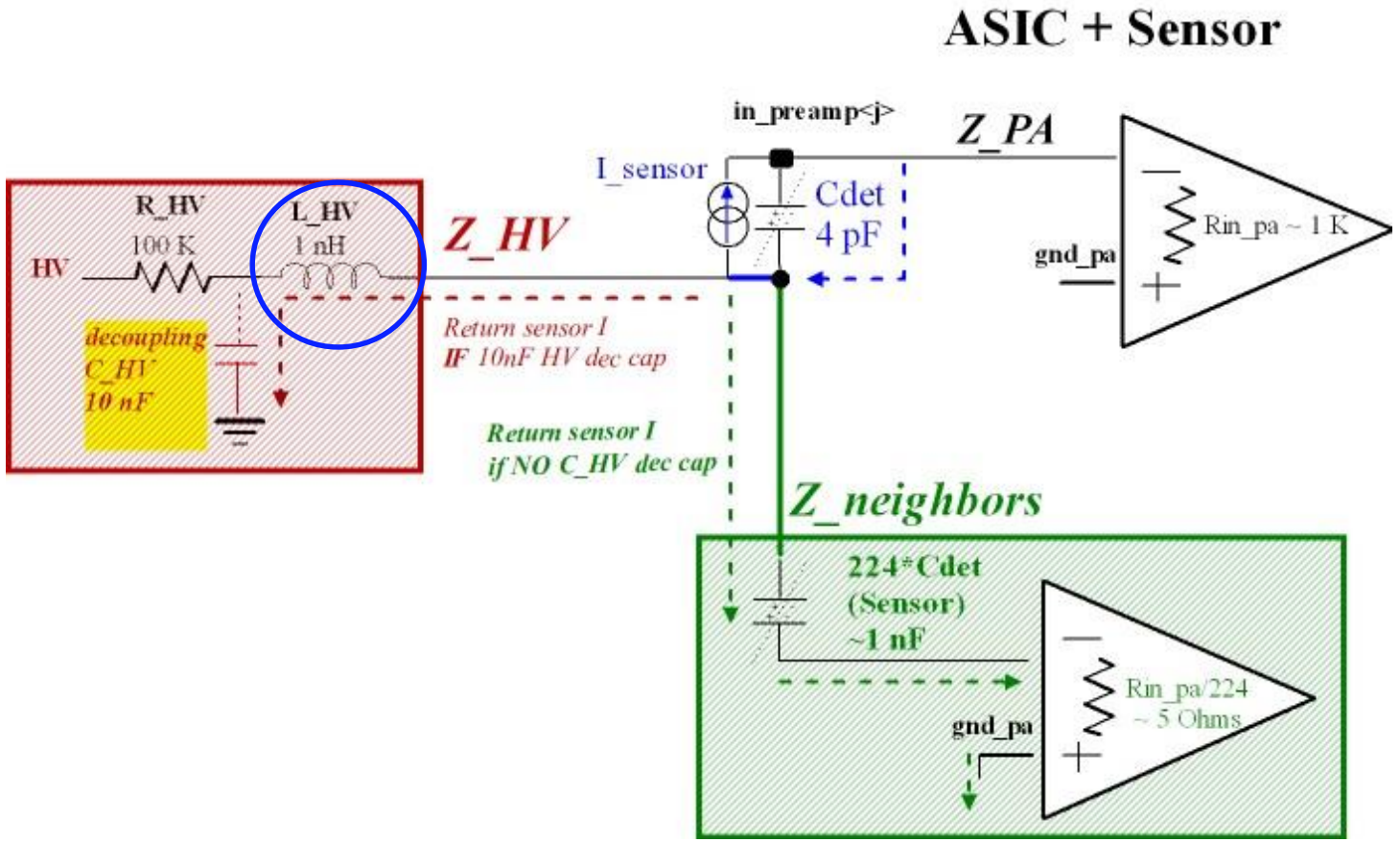


No difference on signal shape
with $R_{HV} = 1\ \Omega$ and $R_{HV} = 1\ k\Omega$

Current return induces -1/225 crosstalk
in all neighbours

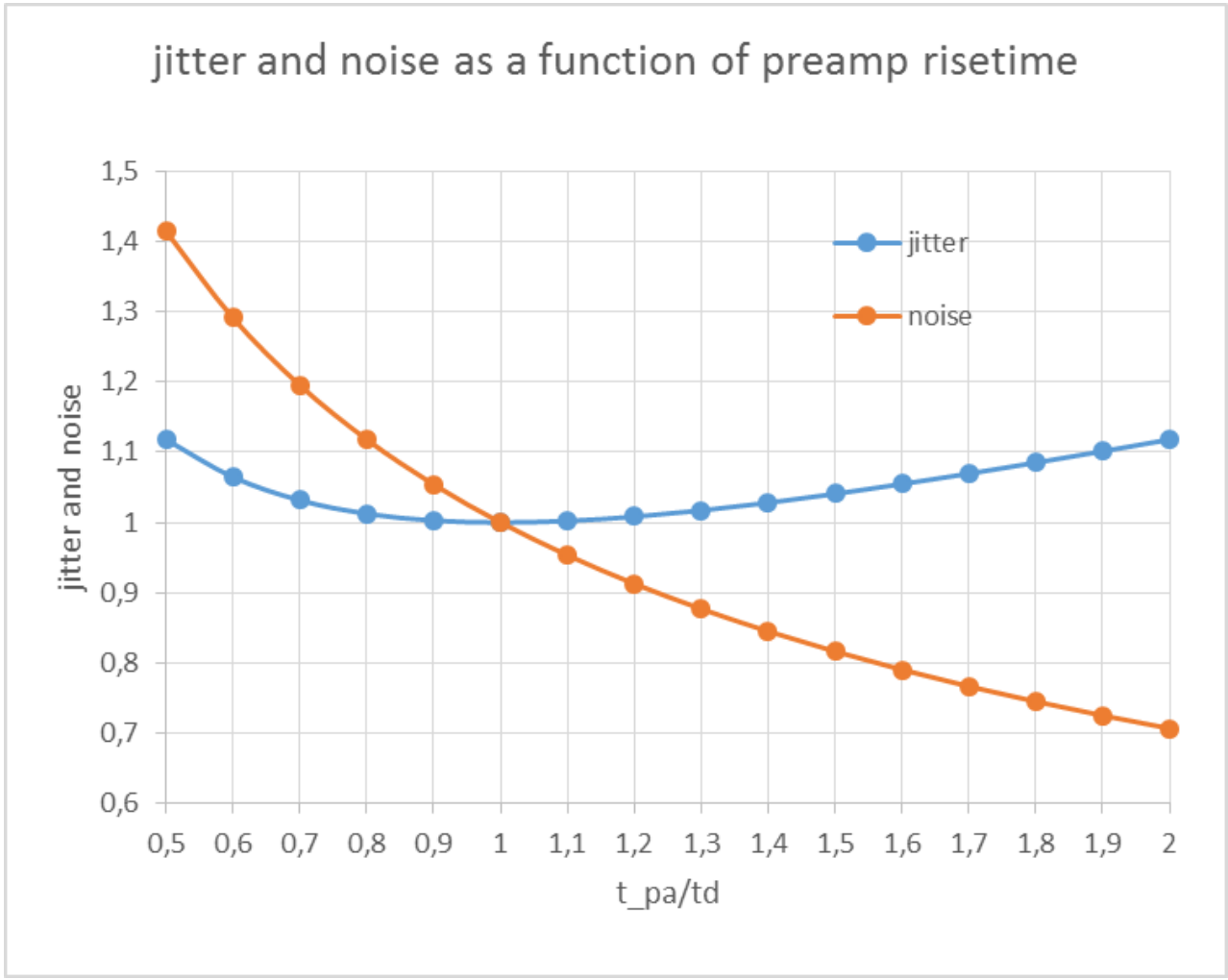
HV impedance (resistance/inductance) is very different for 5x5 and 15x15 sensor

- For small sensor, high impedance leads to deformed signals => the smallest L, the better !
- For large sensor, the low impedance is no longer required as « spectator channels » ensure a low impedance current return
- Higher HV impedance (>100 Ohm) minimizes the gain on gnd_pa => better digital noise



Jitter and minimum threshold

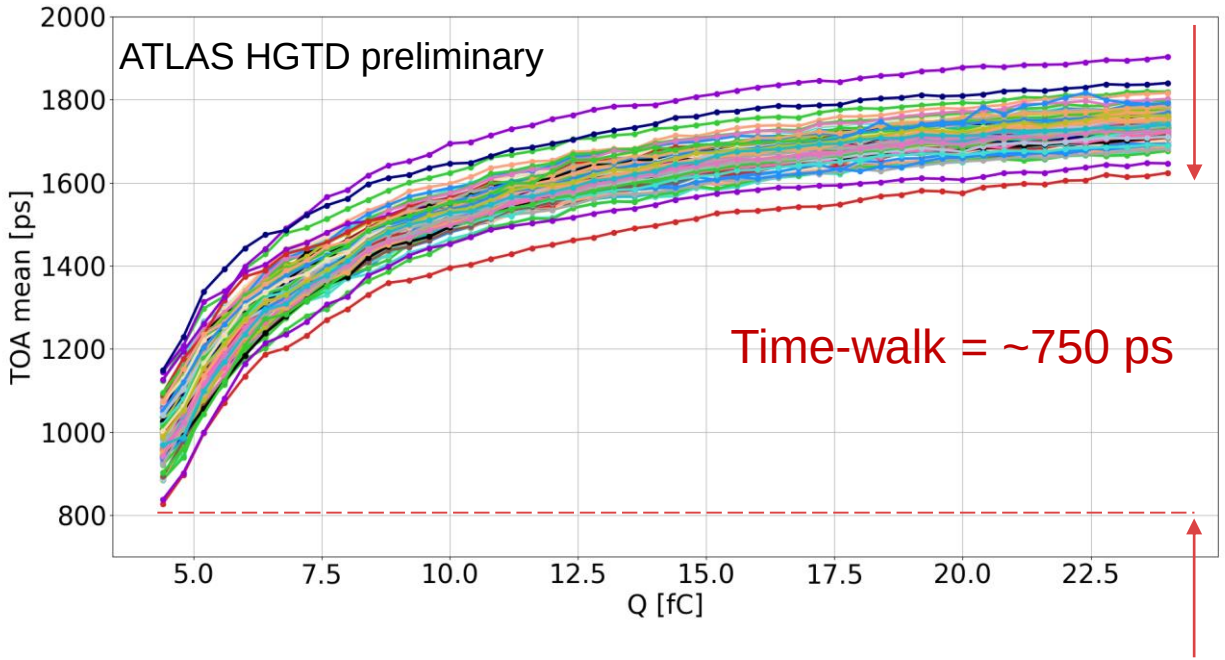
- Jitter optimum is rather shallow with preamp risetime
- But noise and minimum threshold goes up quickly with speed (as sqrt)



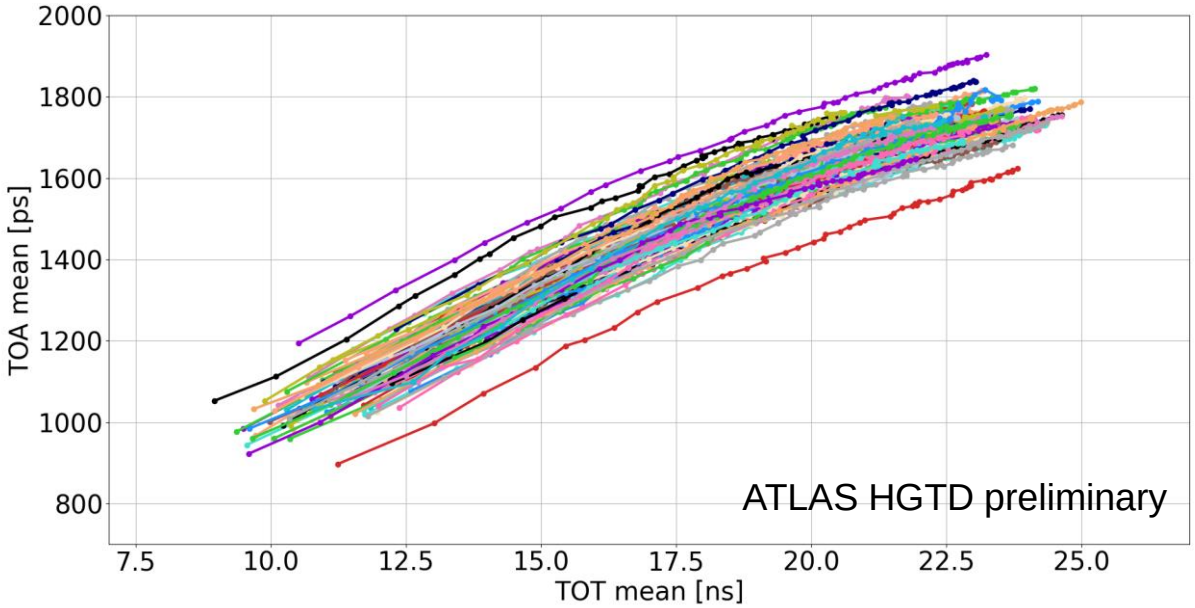
Correcting time-of-arrival timewalk with time-over-threshold

ASIC+HPK LGAD biased at -80V (B16) All TZ ON

TOA versus charge



TOA versus TOT



- Time-walk = convolution of the preamplifier rise time (300 ps) with LGAD rise time (600 ps)
- Skew between bottom and top of the column pixel : due to clock tree distribution

- Offline time-walk correction using TOT

Main challenges: organizational difficulties

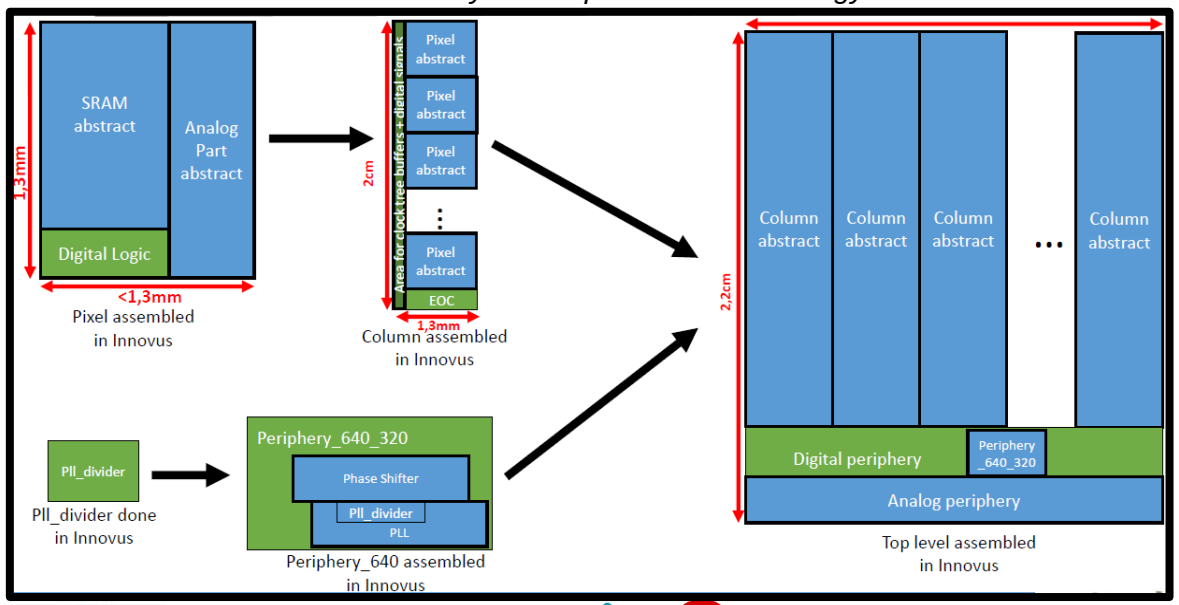
- Organization: Design done by engineers spread in 6 labs – ~ 7.5 FTE
  - SOS, Trello and Mattermost: to ensure quick/"easy" communication but some drawbacks too

- **Analog 30 %** of the chip
  - Analog performance and **Floorplan crucial** to guarantee analog performance at system level
  - 2.5 FTE: Omega (1.8 FTE) , Clermont (0.7 FTE) , SLAC (< 0.1 FTE for TDC) , SMU (< 0.1 FTE for Phase shifter)

- **Digital 70 %** of the chip
  - **Clock Domain Crossing, timings, SEE robustness**
  - 5 FTE: Clermont (2.2 FTE) , Chips (2 FTE) , IFAE (0.8 FTE)

- Assembly done **Full Digital on Top** + UVM verification
  - Top level assembled with INNOVUS
  - Verilog models and lib files to be done for all analog/mixed blocks
  - Analog periphery treated as a macro block

Altiroc3: Physical Implementation strategy



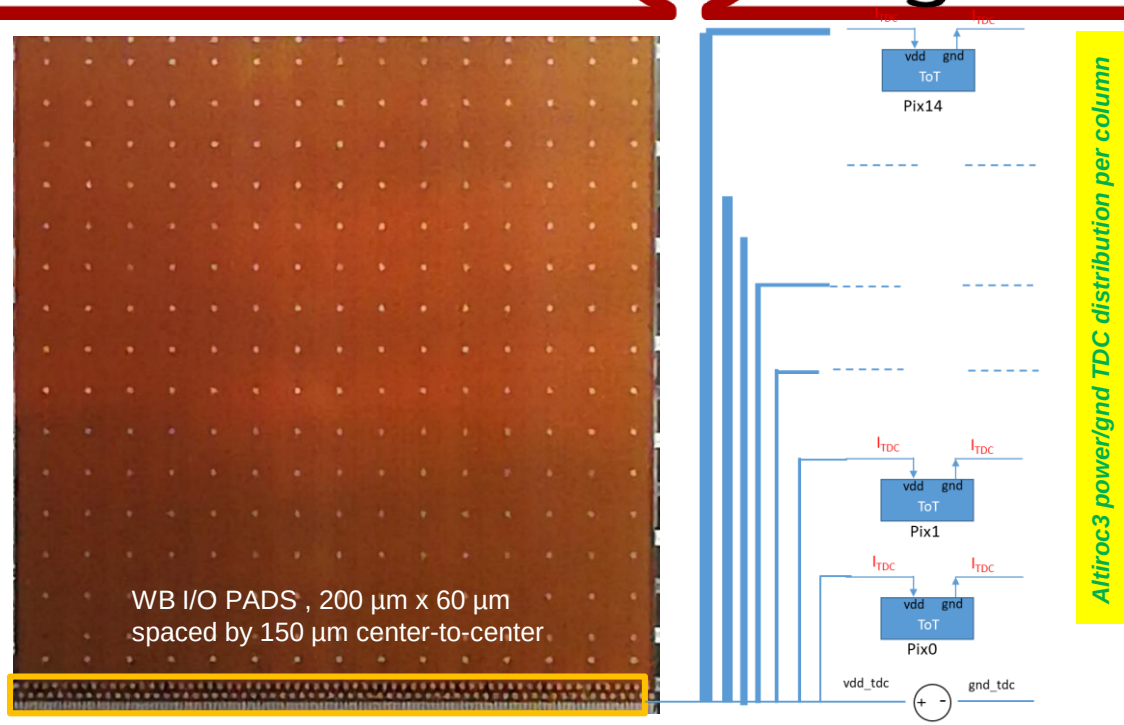
⇒ **Difficulties:**

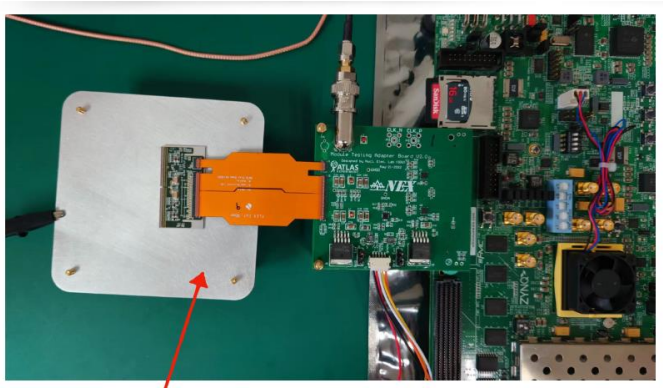
- Design driven by digital while analog floor plan crucial for the performance
- UVM manpower: mainly at CERN, difficult to recruit UVM engineers at IN2P3
- Any modification, even very minor ones, in the analog or digital part implies that the implementation (layout) of the full chip must be redone + verifications to be redone from the beginning (regressions)

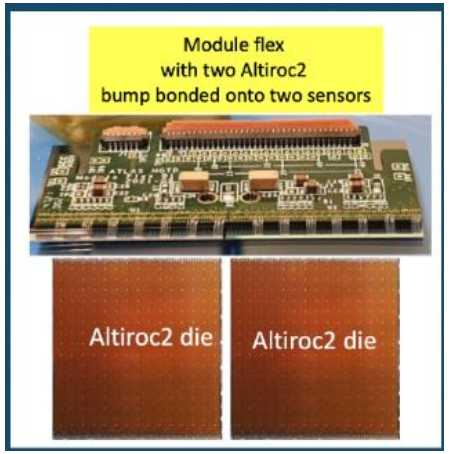
Main challenges: technical difficulties

- Large chip (2 x 2 cm2) powered on one side only => sensitivity to IR drops

- Very delicate floorplan to be done to guarantee the analog performance
  - Ultra Low impedance for the ground of the preamp crucial
  - **Several power domains**:
    - Specific power lines for each analog/mixed block: vdd_pa/gnd_pa, vdd_disc/gnd_disc, vdd_toa/gnd_toa, vdd_tot/gnd_tot
    - For Altiroc3: Vdd_toa, vdd_tot, gnd_toa, gnd_tot per column and then distribution of powers/grounds to each pixel with same R to avoid LSB dependency with activity
    - Specific power lines for digital blocks: vddd/gndd, vddd1/gndd1, vddd2/gndd2







An ATTRACT project which aims at demonstrating :

+ Single Photon Time Resolution better than 20 ps RMS with 100 pF detector capacitance
+ 3 ns double pulse separation
+ Photon counting up to 300 MHz

Key functionalities

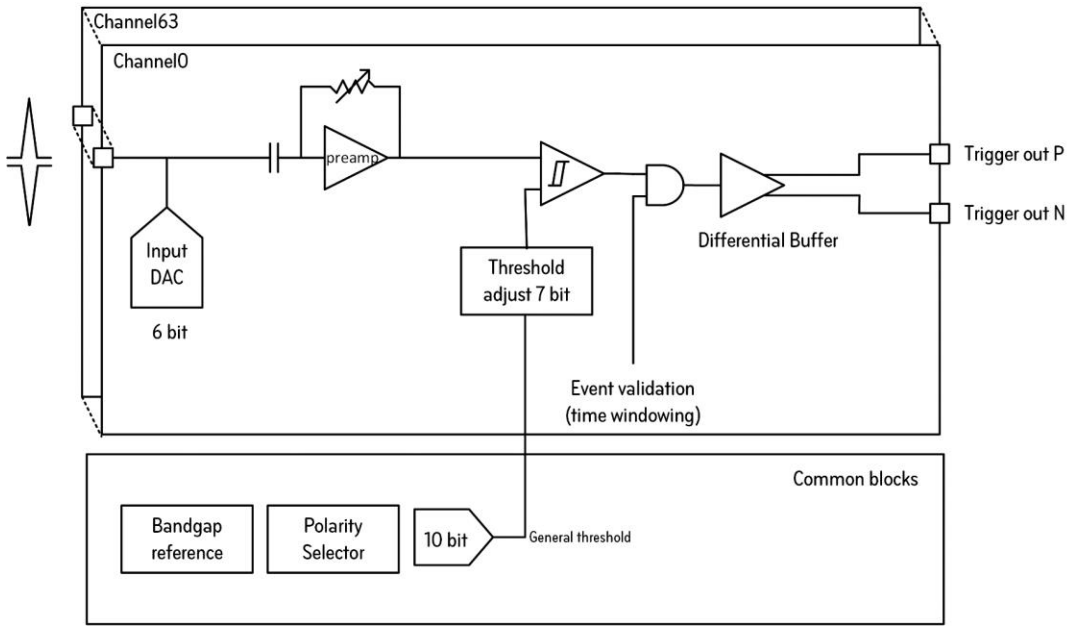
Pole-zero cancellation

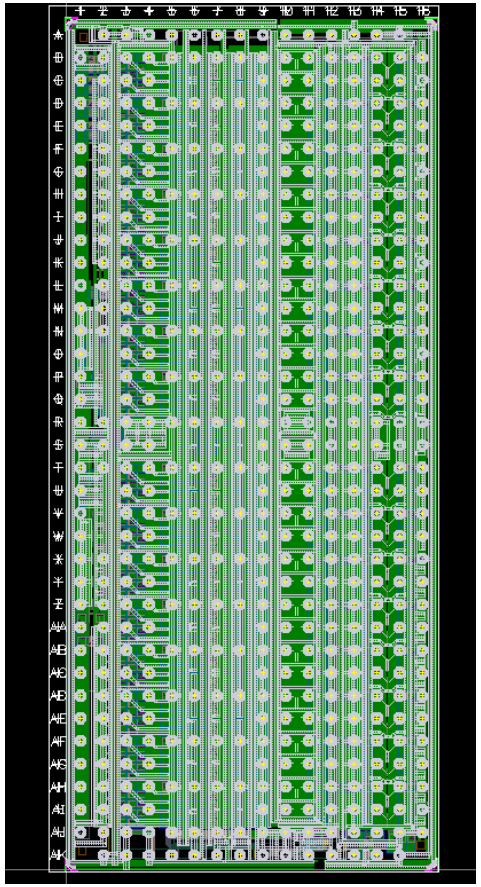
Channel-wise Input DAC

1 GHz bandwidth preamplifier

High-speed discriminator

Native interface to picoTDC



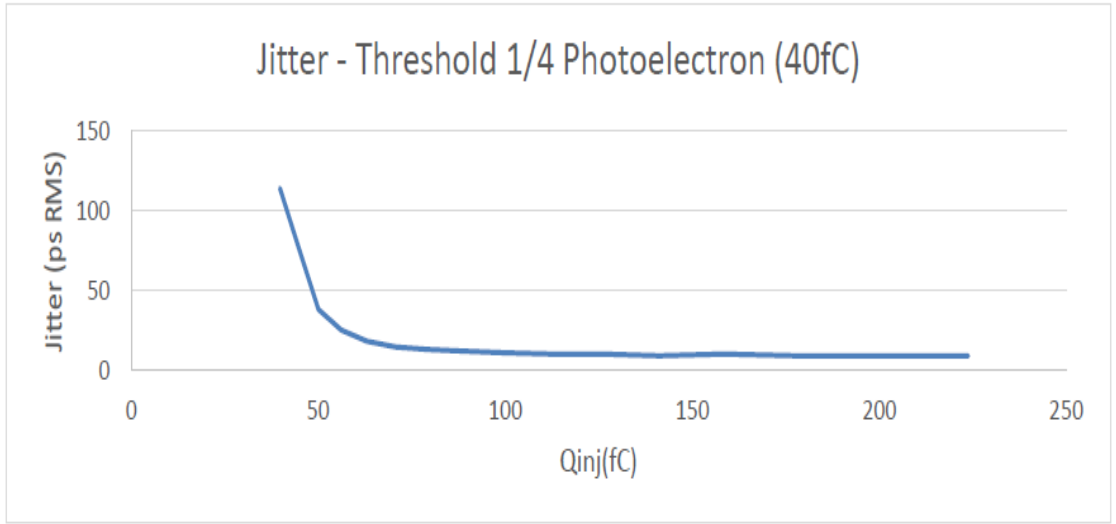


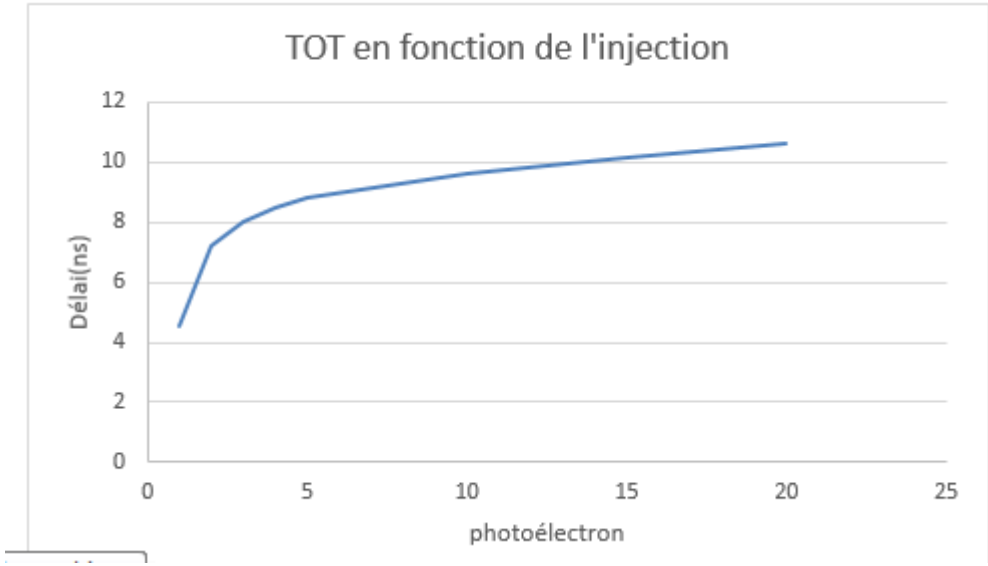
Parameters & Performances

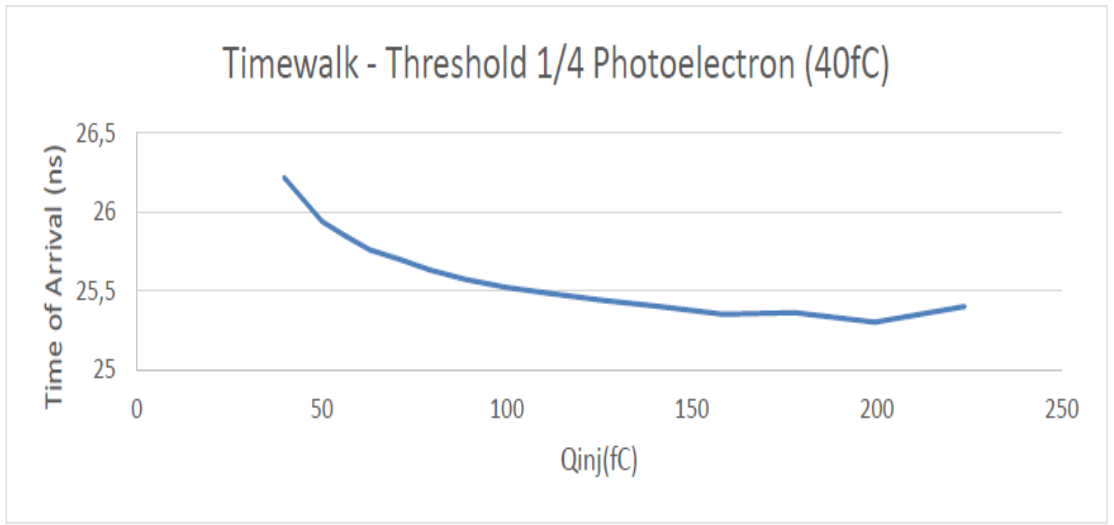
Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps RMS on single photo-electron Better than 3 ns double-peak separation on single photo-electron
Dynamic Range	Over 300 MHz photon counting rate
Packaging & Dimension	BGA 20x20 mm^2 Flip-Chip low inductance packaging technology
Power Consumption	180 mW (2,9 mW per channel) – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 low-common-mode LVDS triggers (CLPS) – compatible with CERN picoTDC and all LVDS FPGA I/Os
Internal Programmable Features (I^2C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7 bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp pole-zero cancellation adjustment, individual trigger masking and cell powering.
Radiation Hardness	Rely on TSMC 130nm MS-RF technology, « CERN qualified » for irradiation, as ASIC design blocs are used for LHC and have been tested up to 300 Mrad

RMS jitter performance with input charge (test pulse)

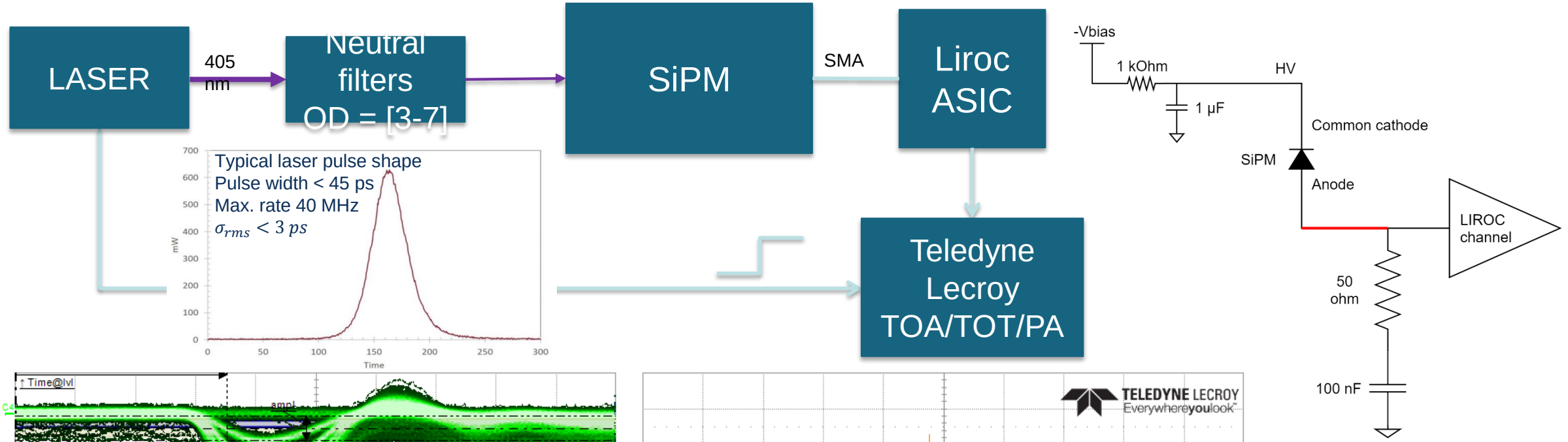
A fast-rising edge pulser is used to inject voltage steps into a capacitor to mimic charge deposited inside an SiPM.

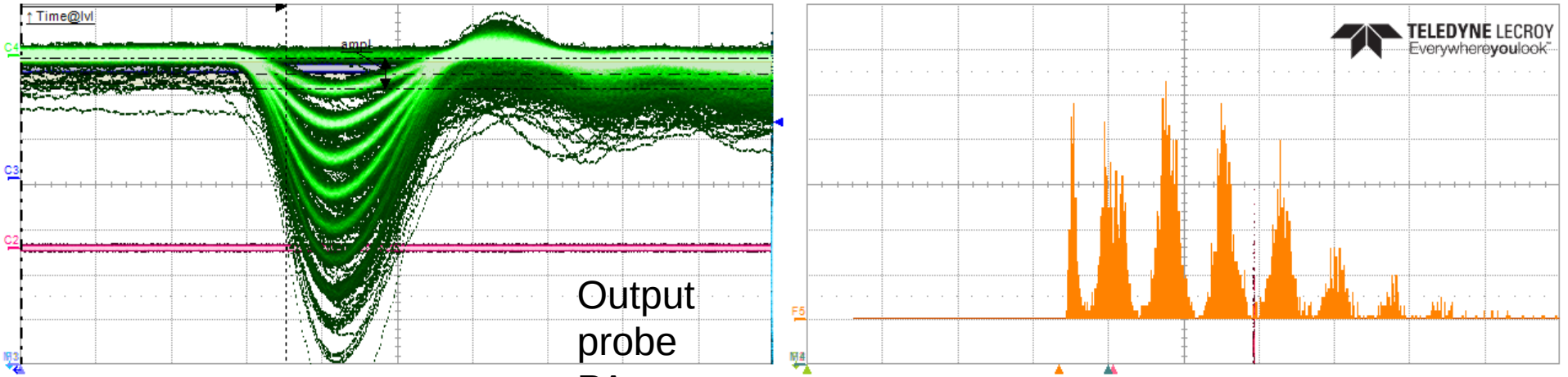






Laser testbench setup





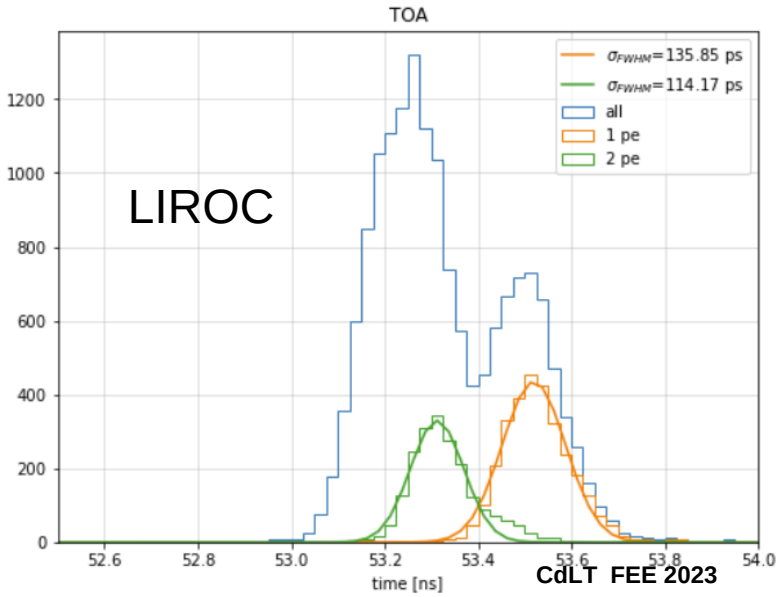
Output probe PA

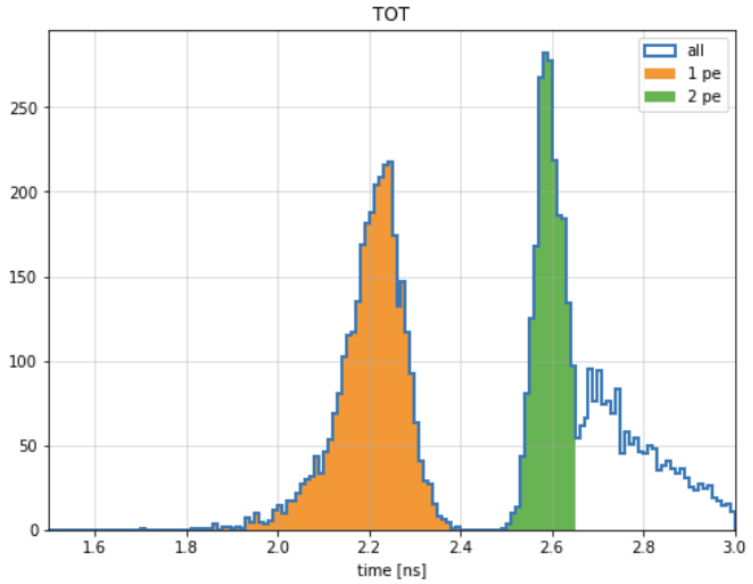
Measure	P1:time@lv(C4)	P2:ampl(C4)	P3:fall(C4)	P4:sdev(C2)	P5:time@lv(C3)	P6:max(C2)	P7:min(C2)	P8:edge@lv(C2)
value	44.224 ns	6.94 mV	4.810 ns	21 mV	---	75 mV	-51 mV	0
mean	42.9060 ns	> 19.29 mV	3.6175 ns	19.7571 mV	---	52.753 mV	-50.727 mV	0
min	41.518 ns	> 1.14 mV	374 ps	17 mV	---	28 mV	-93 mV	0
max	45.360 ns	> 71.52 mV	9.057 ns	22 mV	---	106 mV	-31 mV	0
sdev	762.5 ps	> 12.16 mV	717.4 ps	738.3 µV	---	9.778 mV	6.969 mV	0
num	2.584e+3	2.868e+3	2.779e+3	2.868e+3	0	2.868e+3	2.868e+3	2.868e+3
status	✔	✔	⚠	✔	⚠	✔	✔	✔

Laser testbench results

Compilation results from Roberta Pillera (INFN

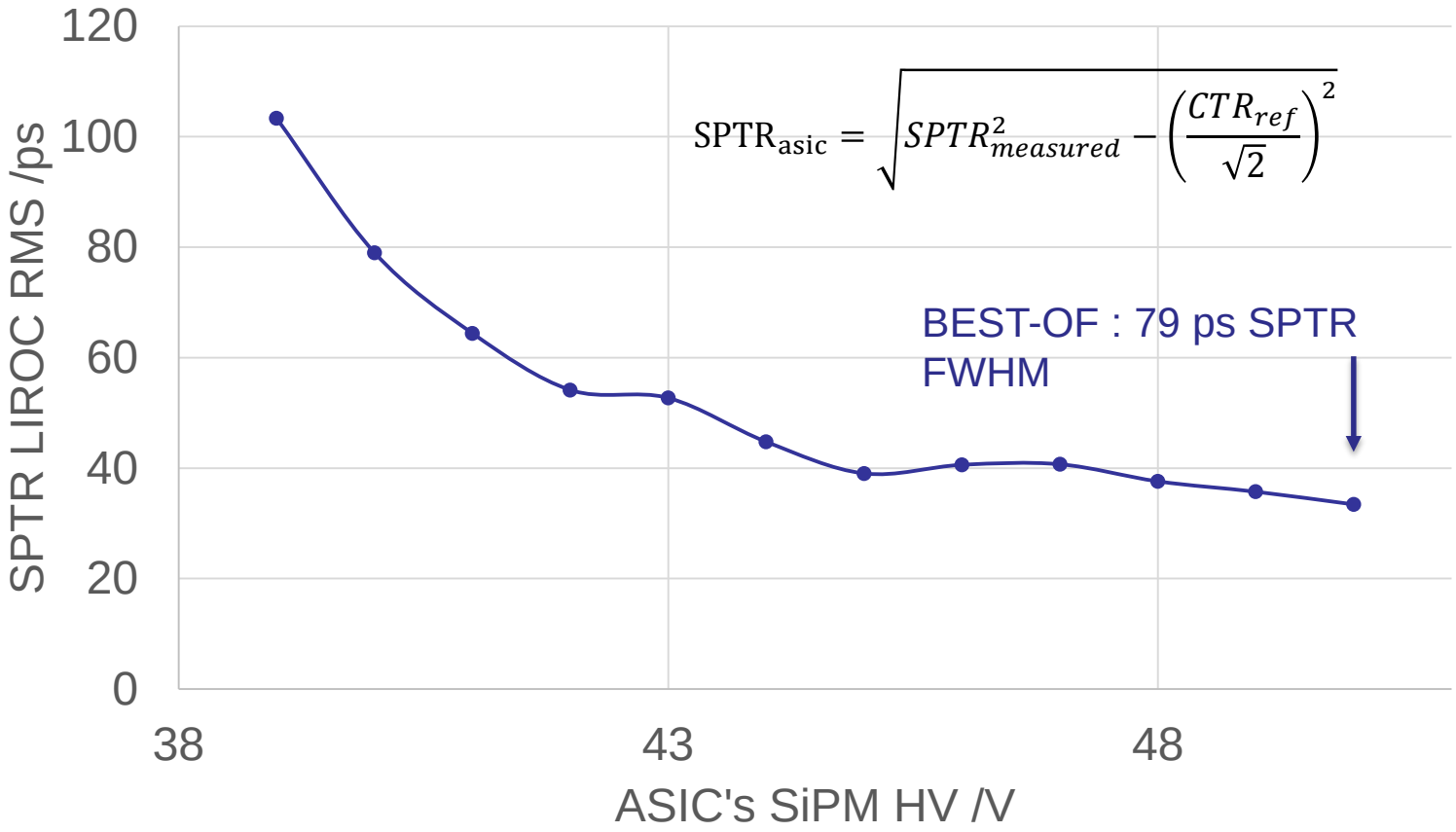
Device	HV - OV	Oscilloscope SPTR FWHM (ps) (measured)	Liroc SPTR FWHM (ps) (measured)	SiPM characteristics
Hamamatsu S13360-1350CS	58.6V - 6 ov	150.22	162.02	1,3 x 1,3 mm - 50 µm
Hamamatsu S14160-1315PS	46V - 8 ov	372.77	354.44	1,3 x 1,3 mm - 15 µm
Broadcom AFBR-S4N33C013	34.9V - 8 ov	304.41	300.02	3,14 x 3,14 mm - 30 µm
AdvanSiD ASD-NUV1S-P	32V - 6 ov	109.29	135.85	1 x 1 mm - 40 µm

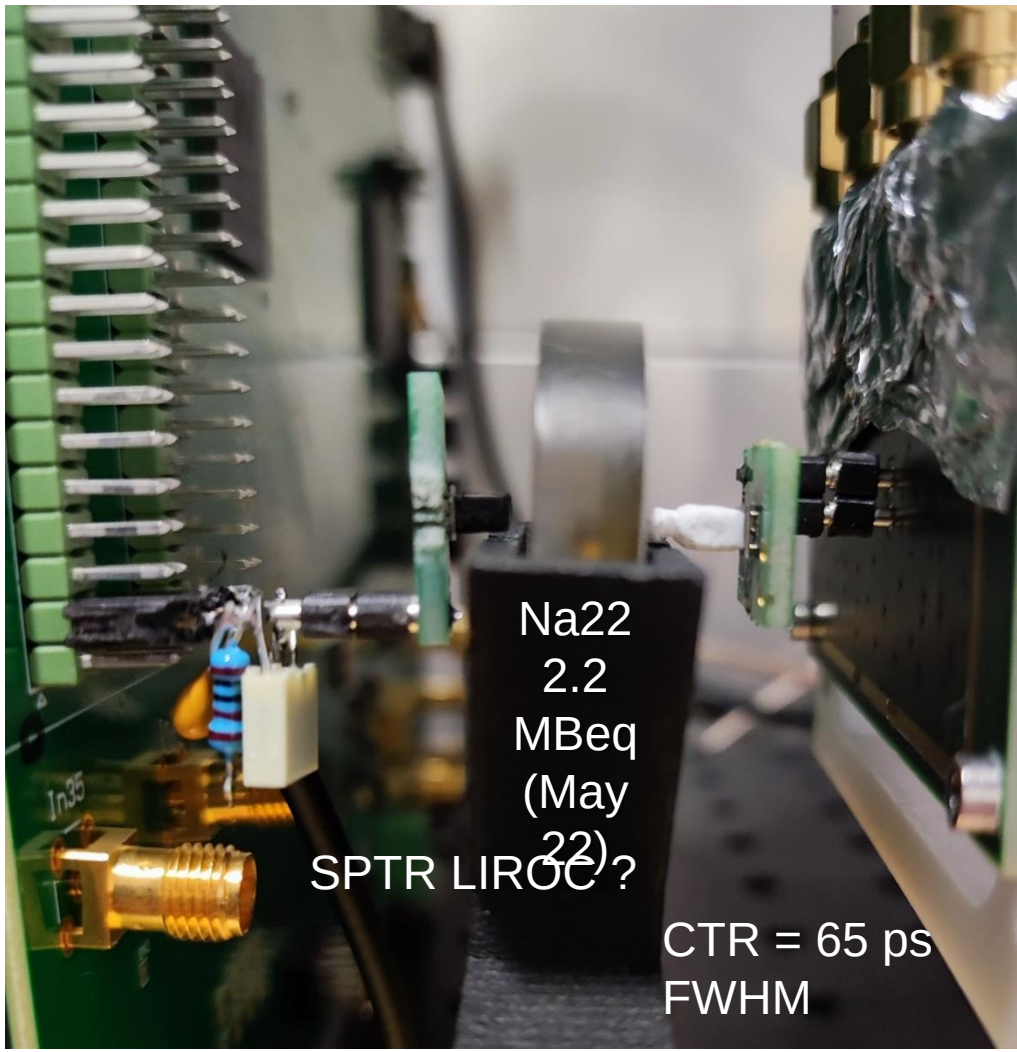




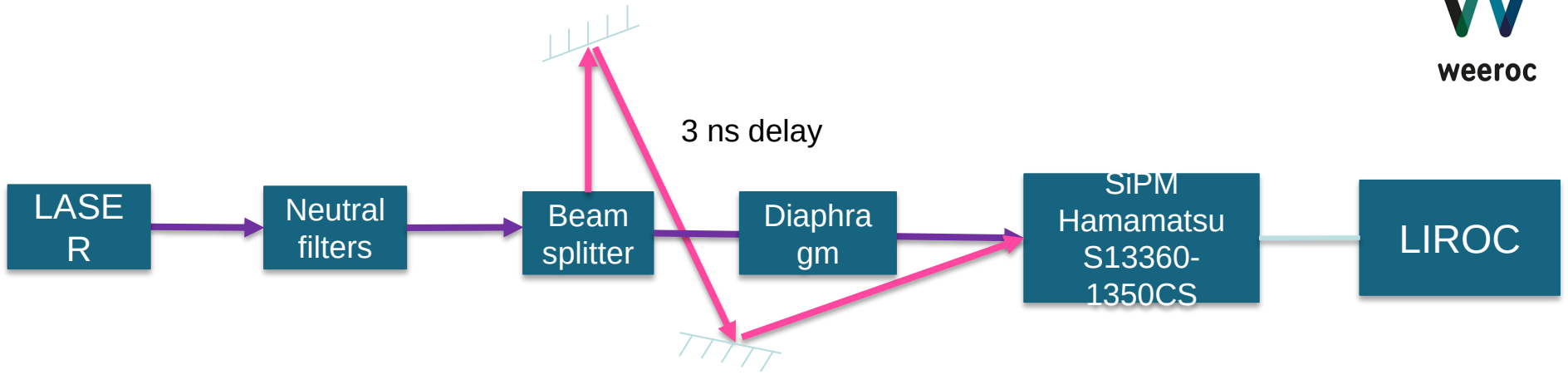
LIROC + FBK NUV UHD DA SiPM

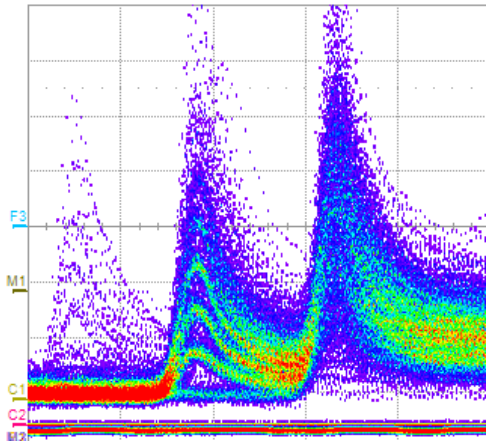
Crystal PbF2 black painted 2x2x3 mm



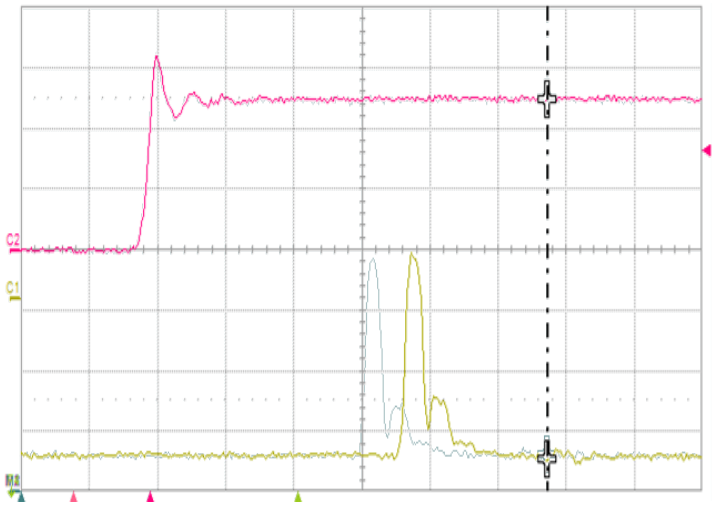


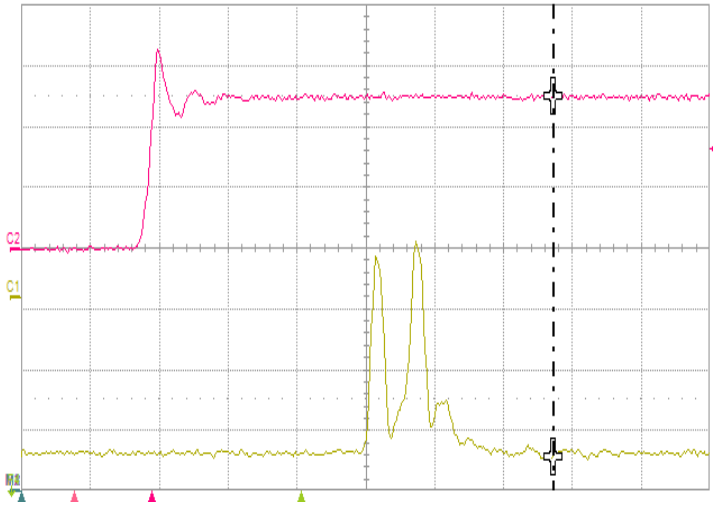
Double pulse separation measured



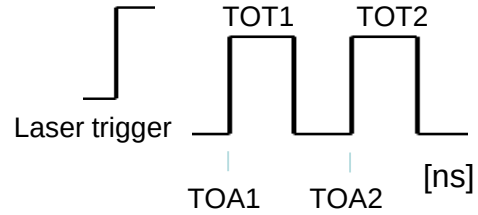


Direct to oscilloscope, 3 ns interval





50 mV/div
5 ns /div



Conclusion : 3 ns double pulse well separated

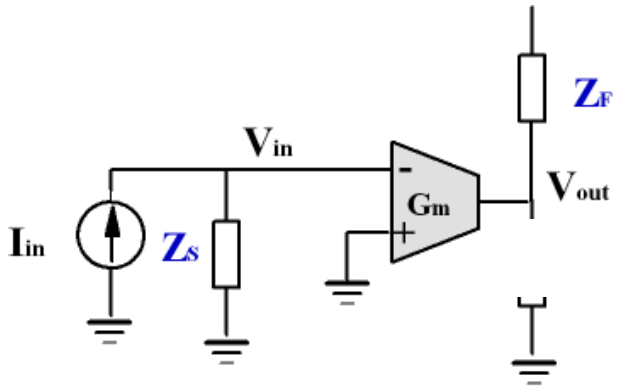
Summary

- ALTIROC2 (ATLAS HGTD LGADs) extensively measured
  - Good performance : 30 ps at 10 fC
  - Digital noise increases with sensor
- ALTIROC3 just received
  - Already indications of improved performance : better uniformity, digital noise…
  - Tests with sensor delayed by TSMC/IMEC bug on polymide openings
- LIROC : SiPM high speed preamp and discriminator
  - 64 ch, native interface to picoTDC
  - 34 ps rms SPTR

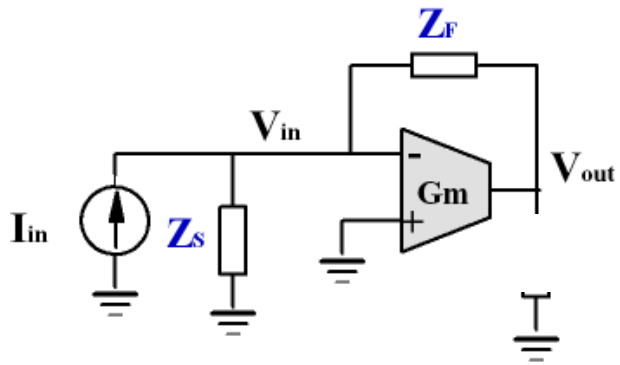
backup

- Response to very short pulse

- Broadband
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $\mathbf{V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}}$



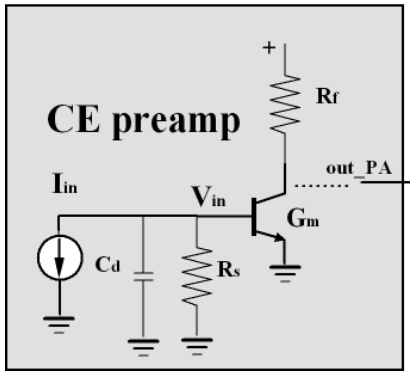
- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $\mathbf{V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega\frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}}$



- Same response at High Frequency
- For highest speed : go to broadband. Faster, less stability issues

- Jitter is given by [details in backup] :

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$



- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

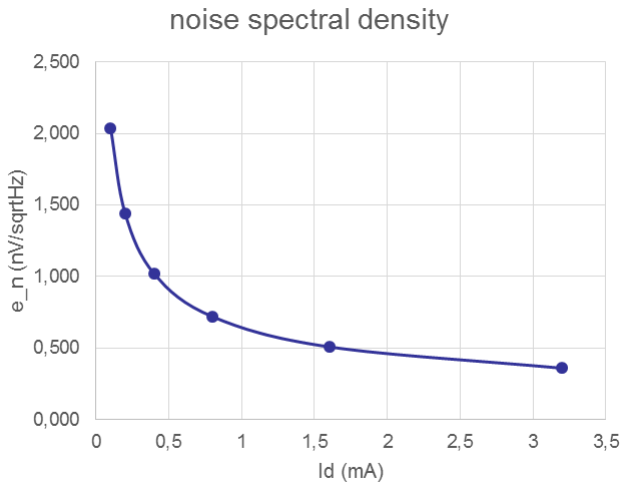
Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

Dominated by sensor
Electronics only gives the spectral density of the input transistor e_n

- Gives ps/fC as scales with 1/Qin

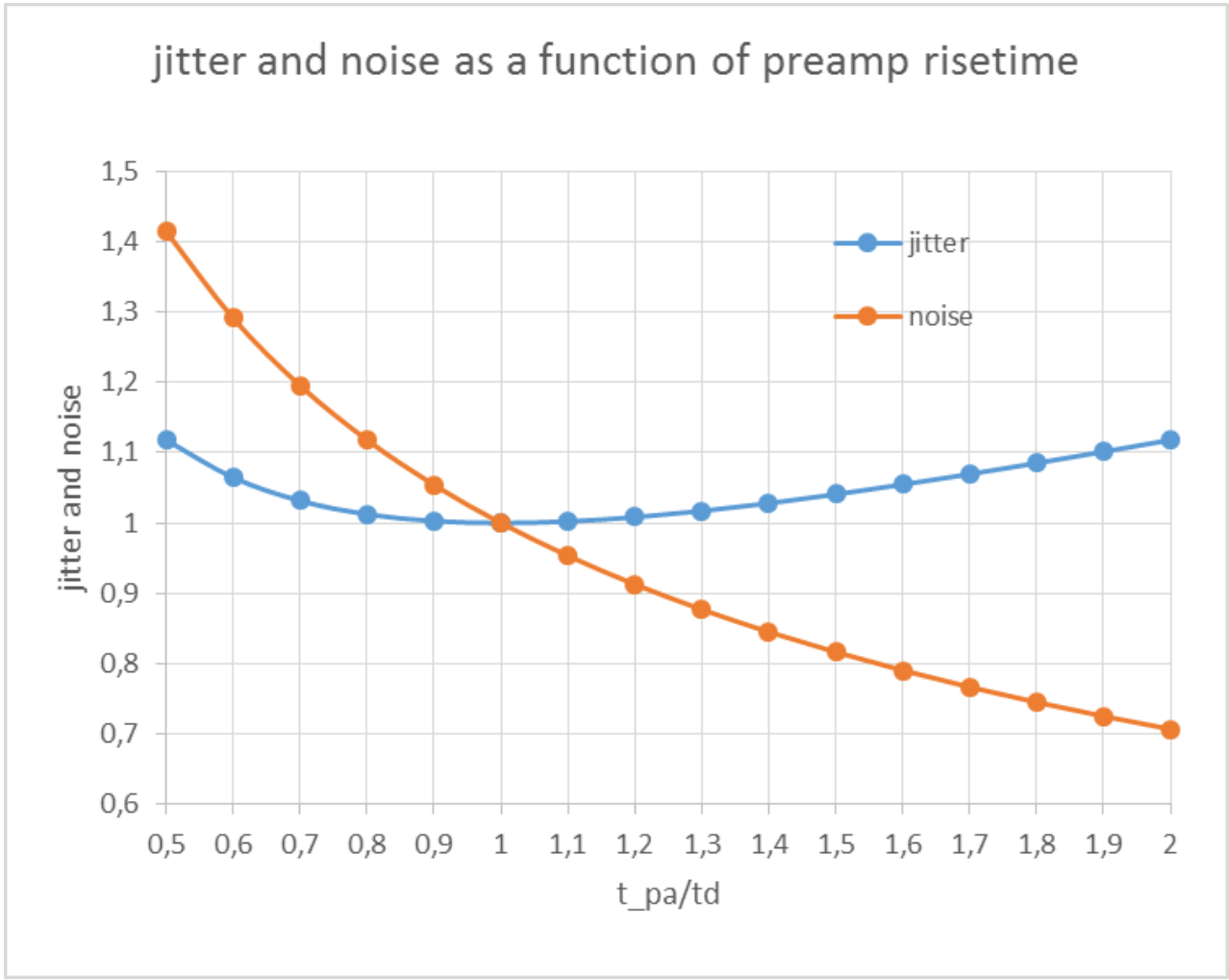
- Electronics noise e_n given by the input transistor transconductance g_m:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



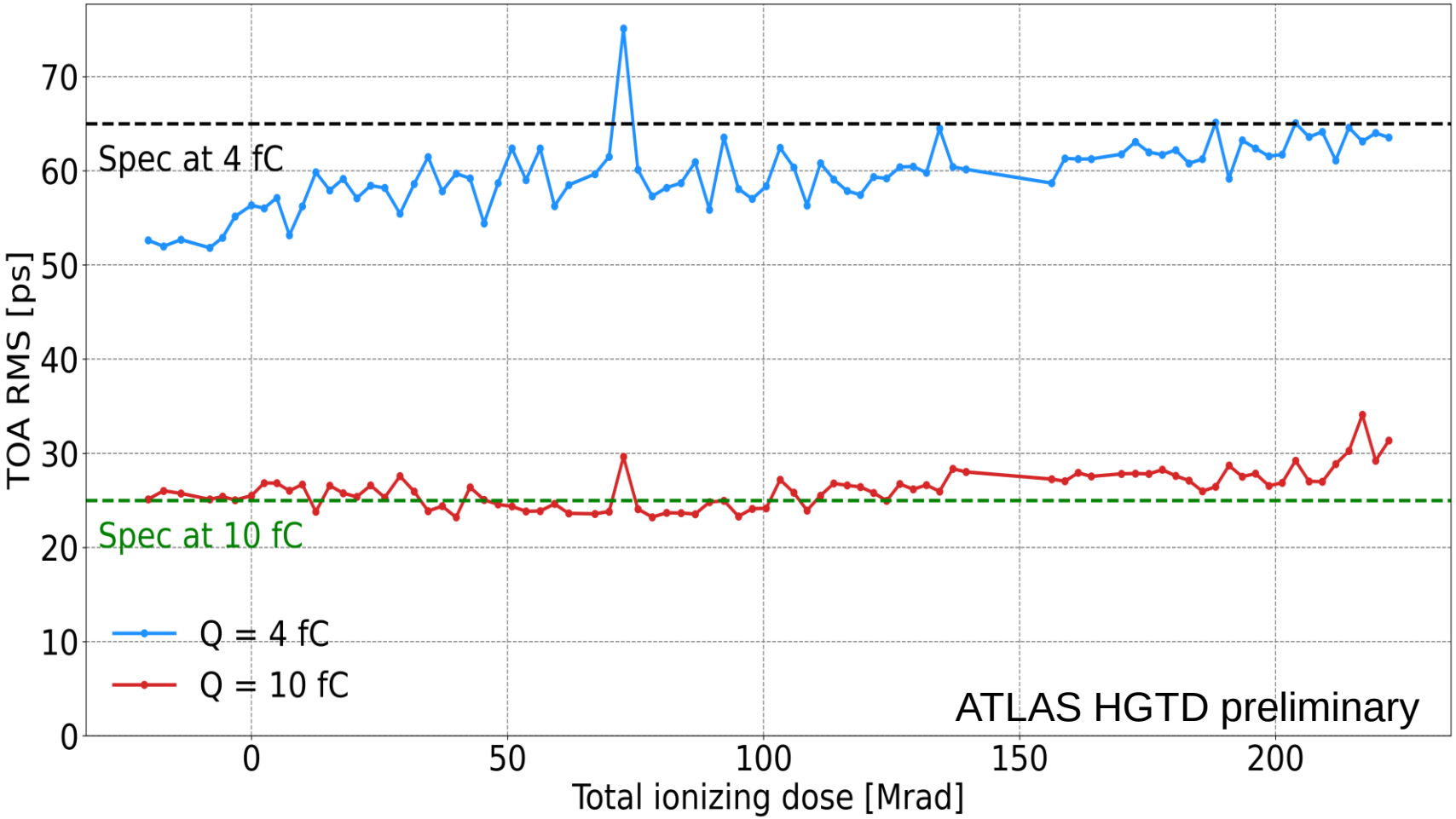
Jitter and minimum threshold

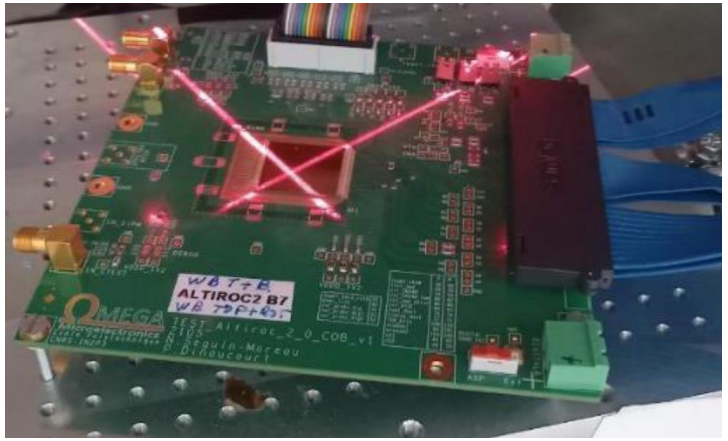
- Jitter optimum is rather shallow with preamp risetime
- But noise and minimum threshold goes up quickly with speed (as sqrt)



Jitter stability under TID irradiation

ASIC alone (B7) Pixels ON : Col 7 (VPA) or 8 (TZ)





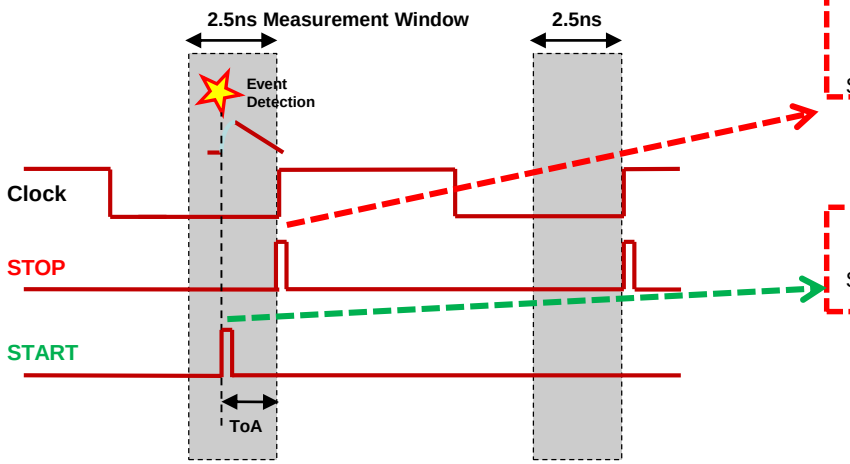
TID : 220 Mrad
Dose rate : 3 Mrad/h
Temperature : 22°C

All DC values and TDC bin remain constant along irradiation.

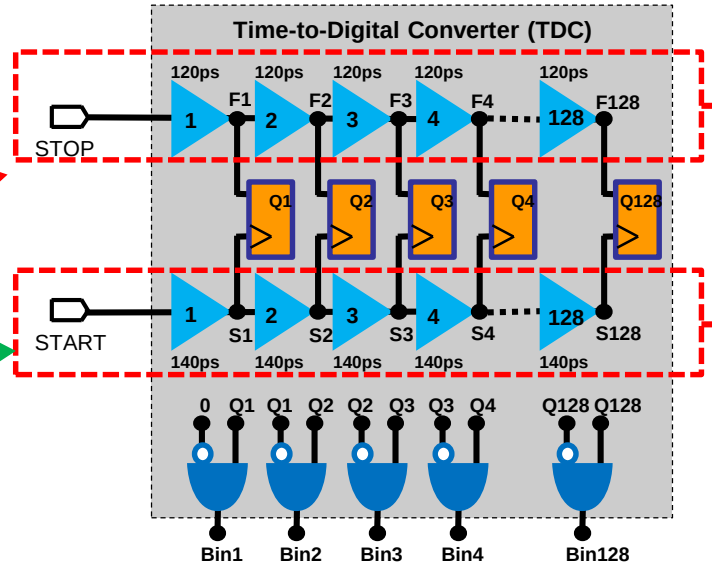
TOA TDC Architecture : Vernier Delay Line

TOA TDC
- Resolution: 20 ps
- Range: 2.5 ns
- 7 bits

TDC Power consumption 0.4 mA *1.2 V = 0,5 mW @ 10%



Simplified Block Diagram



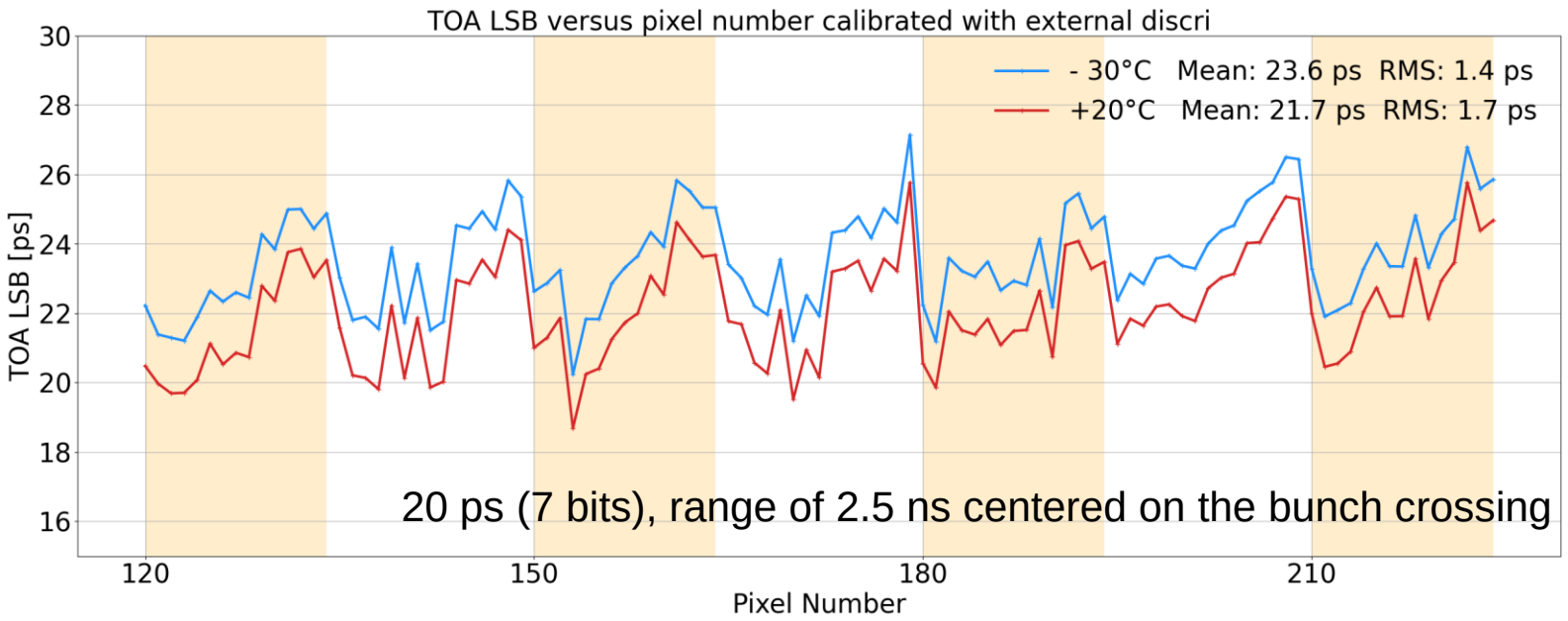
STOP (rsing edge of signal of 40 MHz) propagates in the **Fast Delay Line**
Delay of one cell = **120 ps**

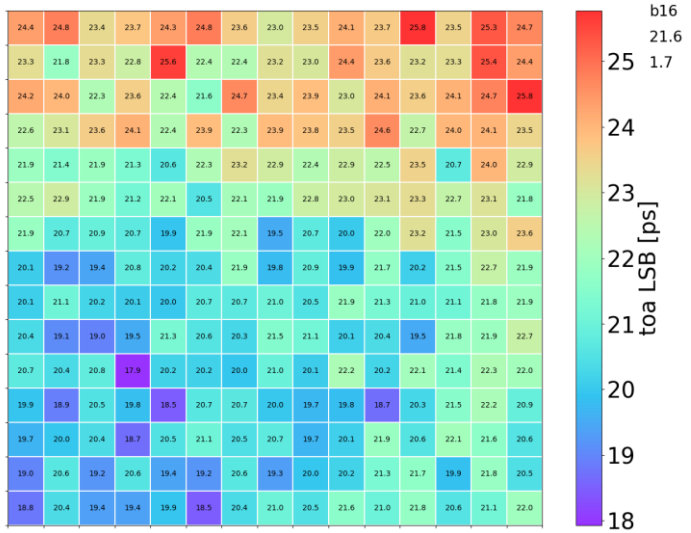
START (rising edge of the discriminator) signal propagates in the **Slow Delay Line**
Delay of one cell = **140 ps**

Differential shunt capacitor voltage-controlled delay cells

- **START** pulse comes first and initializes the TDC operation. **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line, **STOP** signal catches up to the **START** signal by the difference of the propagation delays of cells in Slow and Fast branches: i.e. **140ps – 120ps = 20ps** (**LSB**).
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion
- Cycling configuration used in order to reduce the total number of Delay Cells.
- TDC range is equal to **128 * 20 ps = 2.56 ns**

Natural TDC LSB fluctuation of TZ with temperature





Maps at 20°C