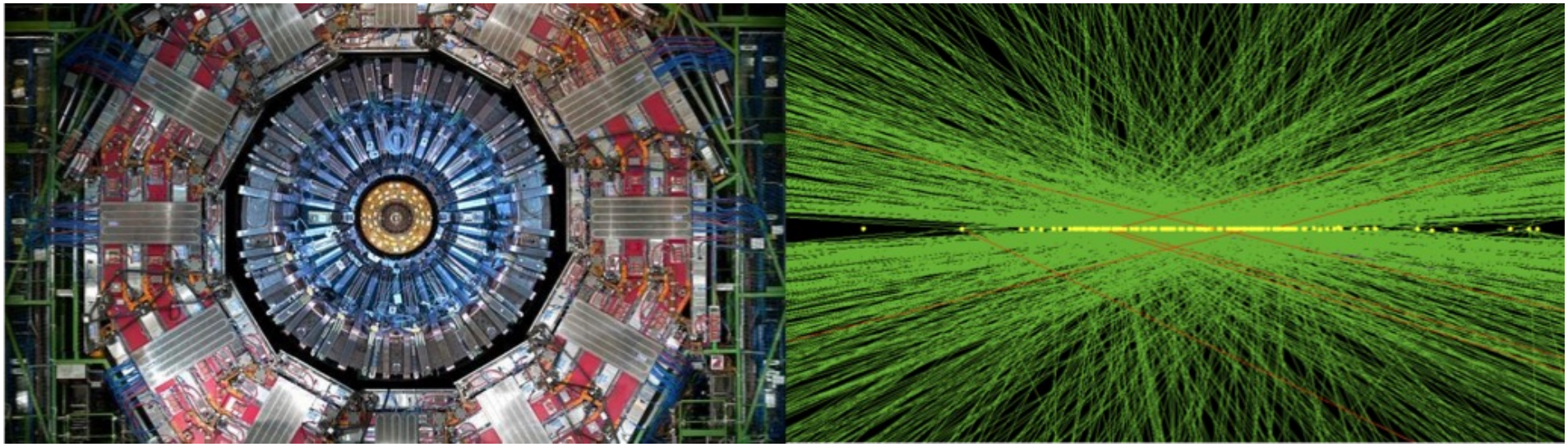
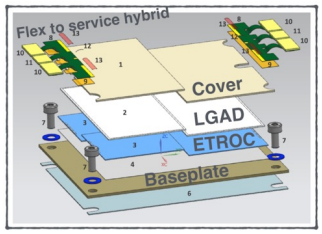
Precision timing ASIC (ETROC) development for CMS Endcap Timing Layer

Ted Liu (Fermilab)

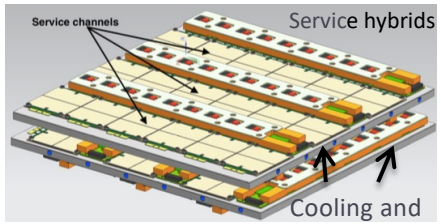
June 12, 2023, FEE-2023 (Torino, Italy)

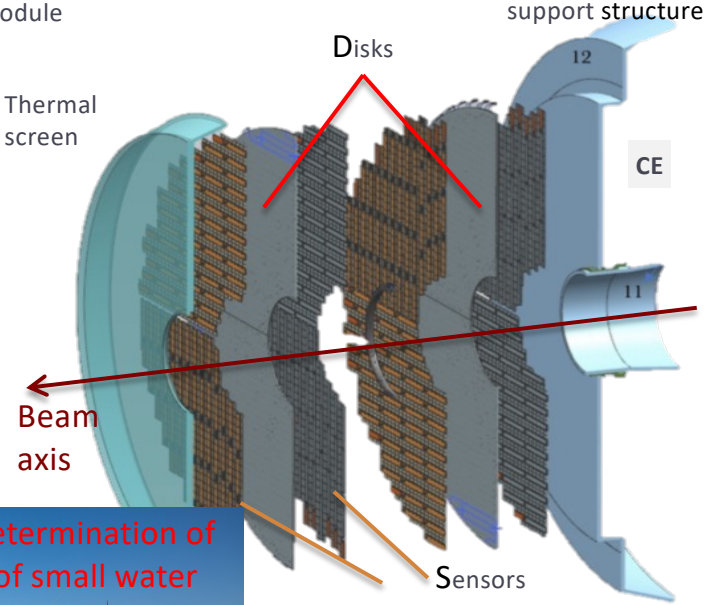


ETL precision timing *challenges*



Module





- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm^2 LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
  - Two layers/disks per endcap (~2 hits per track)
  - $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~9 M channels
  - Nominal fluence: ***1.7x10^{15} n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - LGAD Landau contribution: ~ 30ps
  - Front-end contribution should be kept < 40ps
  - < 50ps per hit, or 35ps per track (with 2 hits)
- ***Extract precision timing from***

  Small LGAD signal (typical 10-20 fC)
  - ***With low power: < 4mW/channel on average***

Challenges:

Low power and fast/precision timing,
Precision clock distribution,
Minimizing readout digital activities

Design considerations for precision timing detector

- System power and cooling constraint and how it influences ASIC design
- Design methodology to optimize front-end from system point of view
- Single layer detector vs multi-layer (ETL design: 1 layer →2 layer)
- TDC design choice: very low power required → new design
- Precision clock distribution considerations: from system to detector, to chip, to pixel and to each TDC delay unit (using H-tree approach)
- Design to enhance physics reach:
  - such as detection/trigger for long live particles, with wide TDC window
- Design for testability, monitoring and calibration considerations:
  - Internal pattern generator within each pixel
  - Internal automatic threshold calibration within each pixel
  - waveform sampler
  - FPGA emulator
- **…**

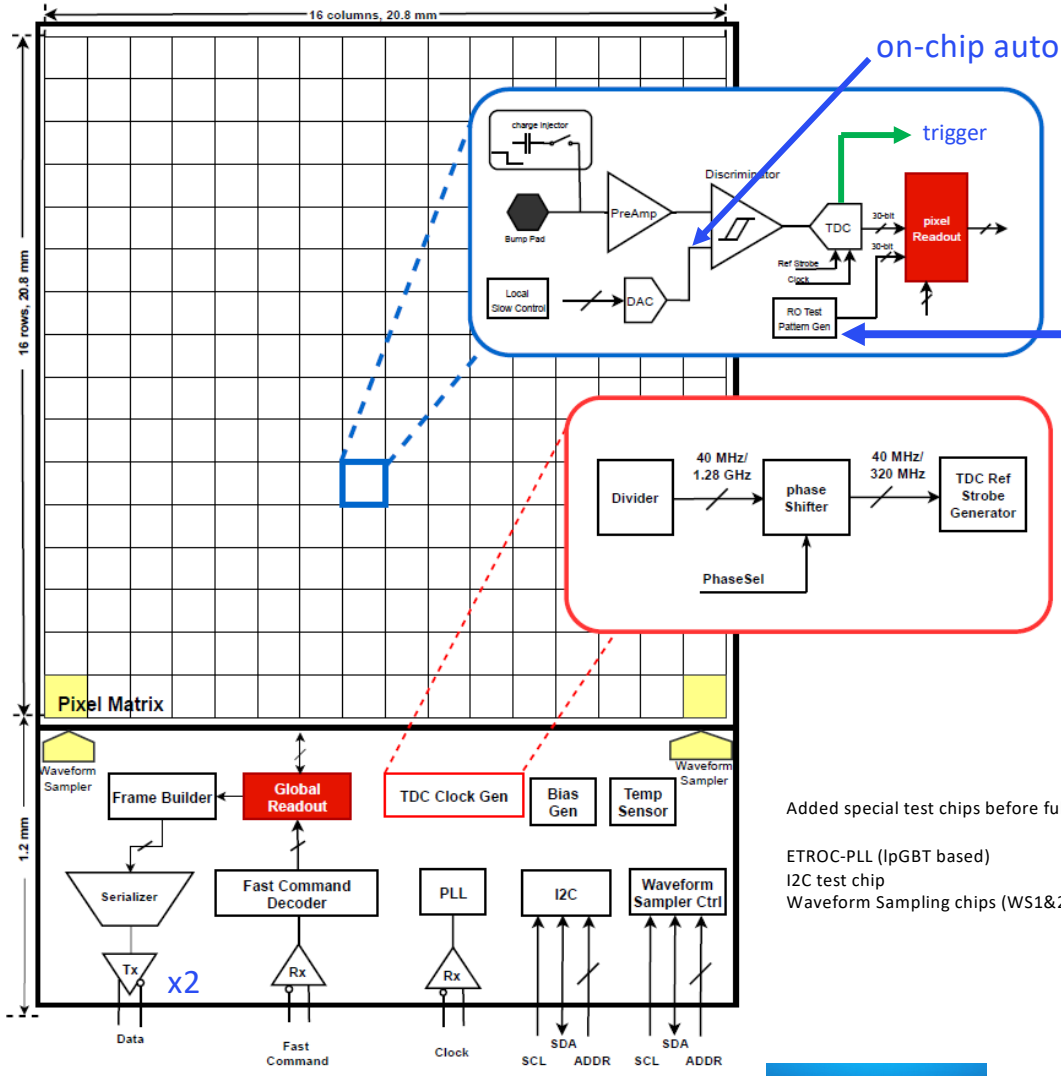
Proper System Design is the Key to the success of any challenging ASIC project

A good design is a compromise between system design and ASIC design

Our approach: "ASIC == A System design Including a Chip"

ETROC Design: from TDR to now

Blue: not described in MTD TDR



on-chip auto threshold calibration

Self-test capability (for ***design verification*** & chip and system level testing with backend)

- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
  - L1 latency circular buffer
  - L1A-driven readout with zero suppression
  - A coarse map of ***delayed*** hits for L1 trigger
- Interface of ETROC
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Serial data link 320/640/1280 Mbps
- Waveform Sampling of preamp output (only 1 pixel)
  - For test & monitoring purpose

Added special test chips before full-size ETROC2:

ETROC-PLL (lpGBT based)
I2C test chip
Waveform Sampling chips (WS1&2)

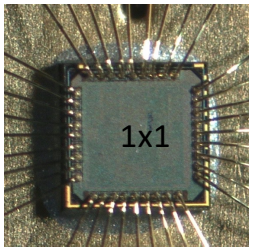
ETROC: Precision determination of the arrival time of small water drop ripples

ETROC prototyping history (R&D phase before ETROC2)

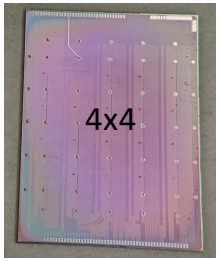
Sept 2018 — Dec 2018 — May 2019 — Aug 2019 — March 2020 — May 2020 — July 2021 — Sept 2021 …

Project started

ETROC0 submitted



ETROC1 submitted

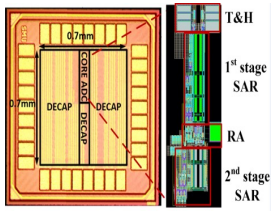


Covid

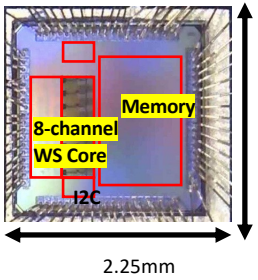
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2,
Delay submission and add few test chips …

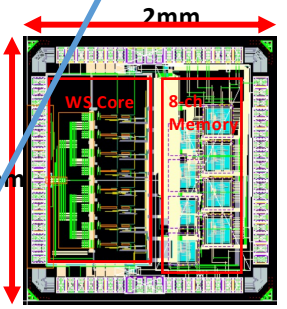
Single channel
ADC submitted



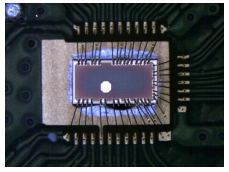
8-channel ADC
Waveform Sampler (WS1)
submitted



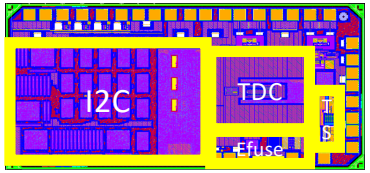
Rad-hard version of
Waveform Sampler (WS2)
submitted



ETROC-PLL mini ASIC
submitted



I2C Test chip submitted



Total of 7 testing chips so far, all successful

All analog blocks have been silicon proven in test chips
ETROC2 FPGA emulator: has verified digital readout and system interfaces

ETROC2 was submitted on Oct 21, 2022
Testing on going since end of April 2023 …

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFCA with students from KSU/KU/CNU

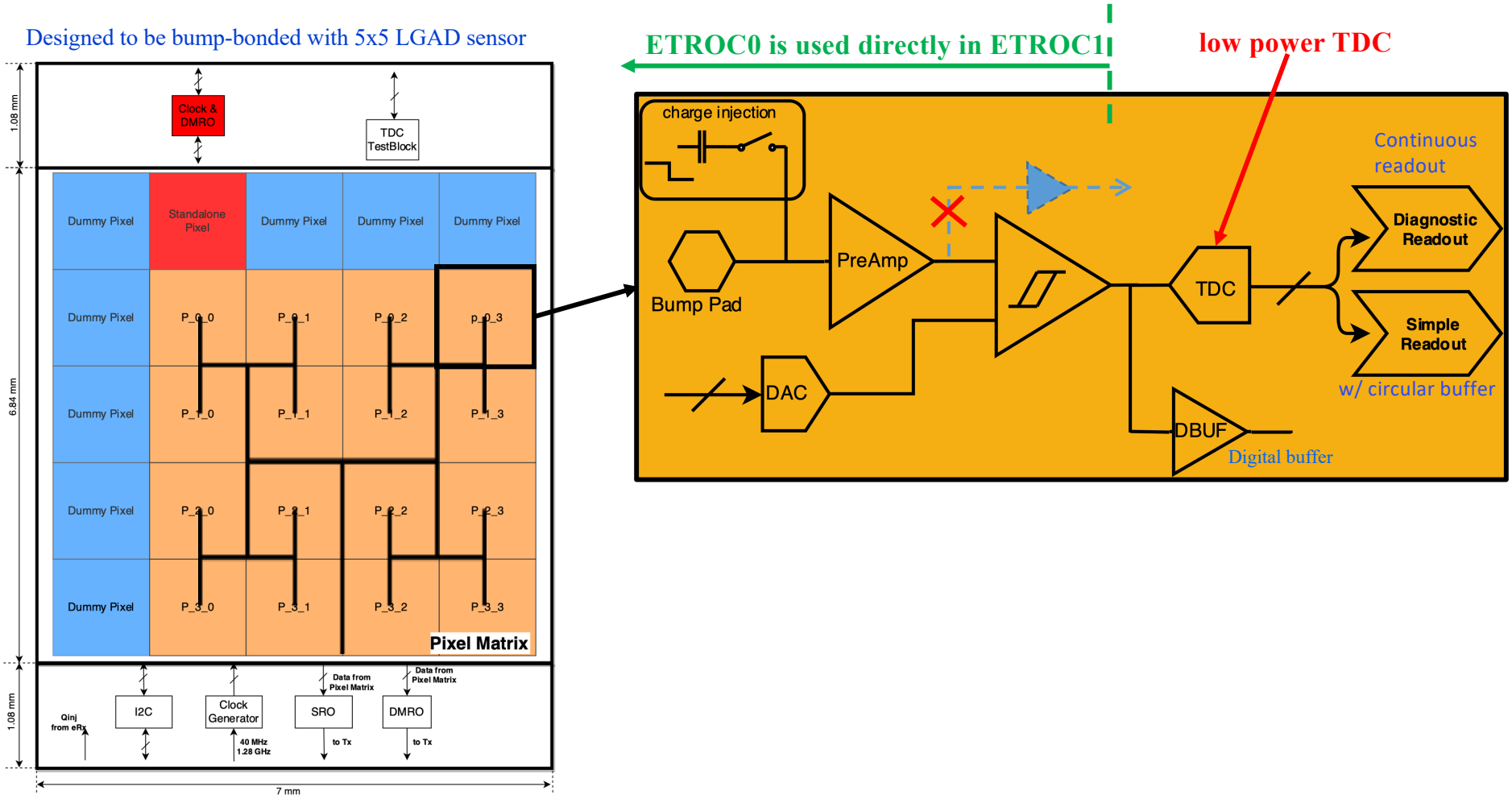
in collaboration with lpGBT team for PLL,
With help from ETROC God Parent Committee, ***CERN ASIC Support & CHIPS for ETROC2***,
Torino/UCSC groups (sensor), and Barcelona group (bump bonding)

ETROC Overall Status

- ETROC0 (single channel, preamp + discriminator)
  - Charge injection/Cosmic/Laser done
  - TID test to 100Mrads done
  - Beam testing: ~30ps achieved in beam.
- ETROC1 (4x4), preamp + discriminator + new TDC
  - New TDC extensively tested: excellent performance and low power (<~6ps resolution)
  - Bare ETROC1 charge injection testing: excellent performance (~10ps resolution with charge injection)
  - ETROC1 and 5x5 LGAD sensor bump-bonded
    - ***Encountered noise related to 40MHz memory activity after bump bonding with sensor***
      - ***Noise source identified and understood, addressed in ETROC2 design***
    - ***Beam testing: results from beam telescope with LGAD at higher gain***
      - ***Obtained down to ~ 40ps per hit at system level in beam in 2021***
      - ***Second round of beam testing in 2022, results consistent***
  - *ETROC1 TID testing (not done, delayed due to COVID)*
- Towards ETROC2 (16x16): full size and full functionalities
  - ETROC PLL mini-ASIC (with lpGBT PLL core)***: test results very good, including SEU***
  - Waveform Sampler prototypes and I2C test chip work well.
  - ETROC2 emulator (for pixel and global readout) works well
- ***ETROC2 design submitted in Oct 2022, testing started April 2023***
- ETROC3: intended as final version, submission in 2024

Due to limited time, this talk will only have few highlights

ETROC1: 4x4 pixel array under H-tree clock distribution



The 4x4 H-tree is designed in such a way to be able to scale up to 16x16 (for ETROC2)

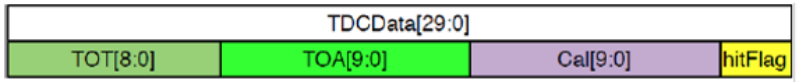
ETROC1 TDC Design

For TDC details: see TDC paper
https://ieeexplore.ieee.org/document/9446843

- TDC requirements
  - TOA bin < ~30ps, TOT bin < ~100ps ***(achieved: 18 ps TOA bin, 36ps TOT bin)***
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel (achieved 0.1mW)***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
    - TOA bin size = 3.125ns / CAL_code
    - CAL_code is the difference between the two time stamps
  - Important to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

For calibration details, see talk by Jinyuan Wu at TWEPP 2022:
"TDC with Uncontrolled Delay Lines: Calibration Approaches and Precision Improvement Methods",
https://indico.cern.ch/event/1127562/contributions/4904530/

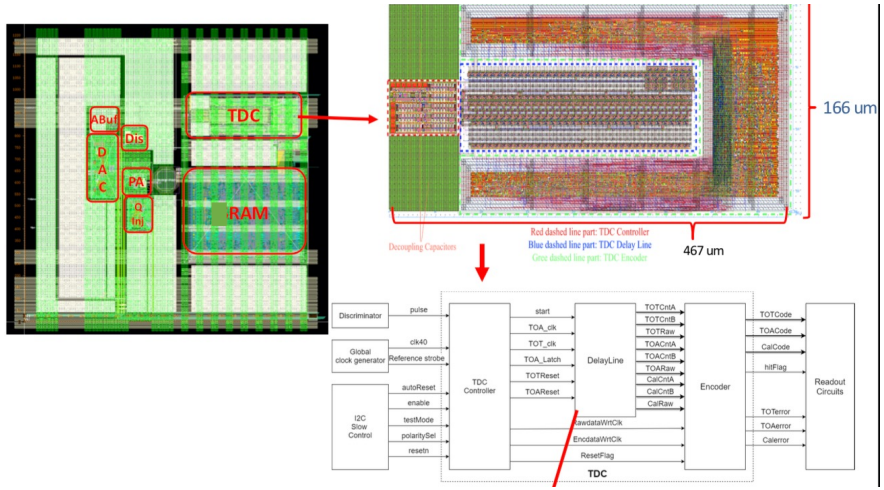
ETROC TDC

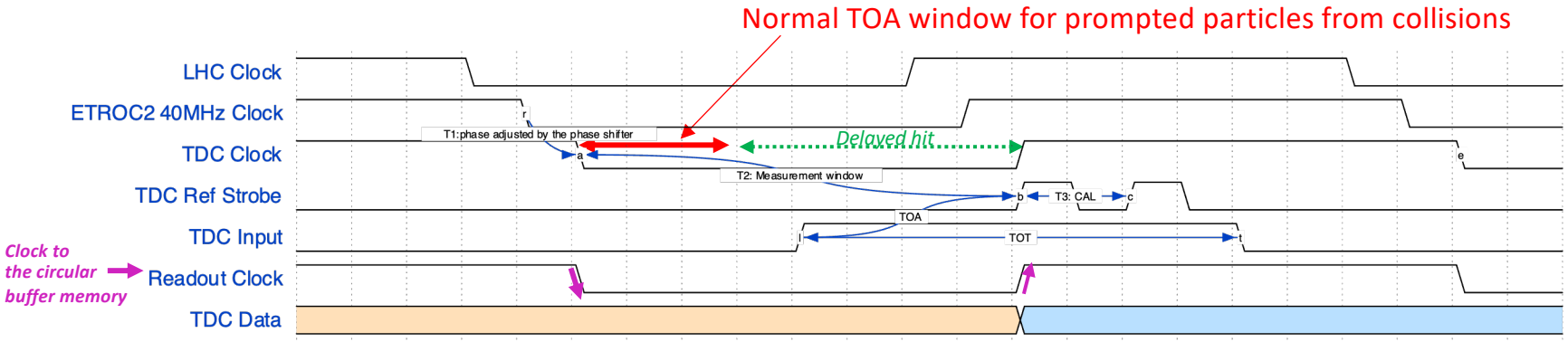


hitFlag: discriminator is fired or not

- bin= T3/Cal_code
- TOA=12.5 - bin*TOA_code

T3 is programable with, 3.125 ns by default.



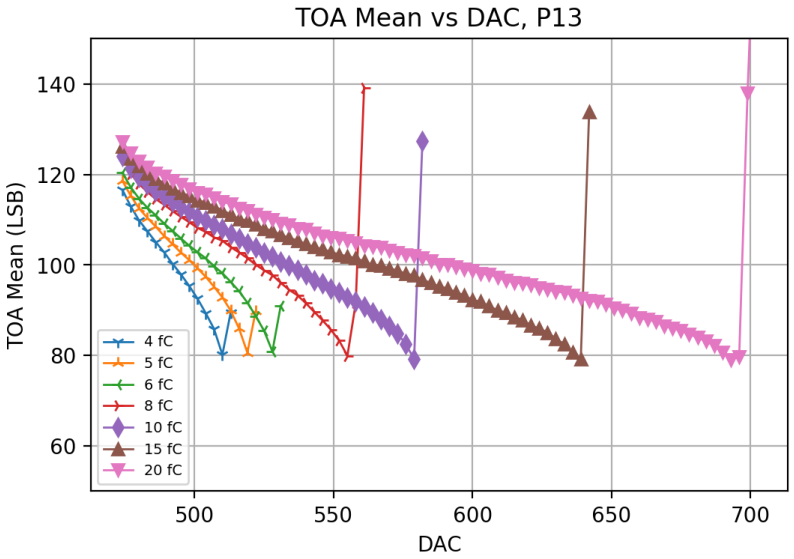


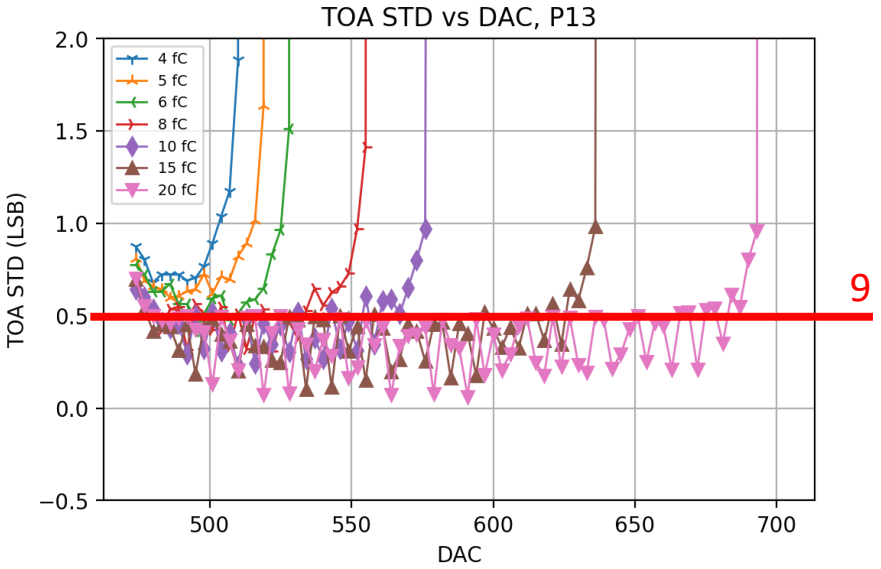
1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

https://ieeexplore.ieee.org/document/9446843

Bare ETROC1 performance

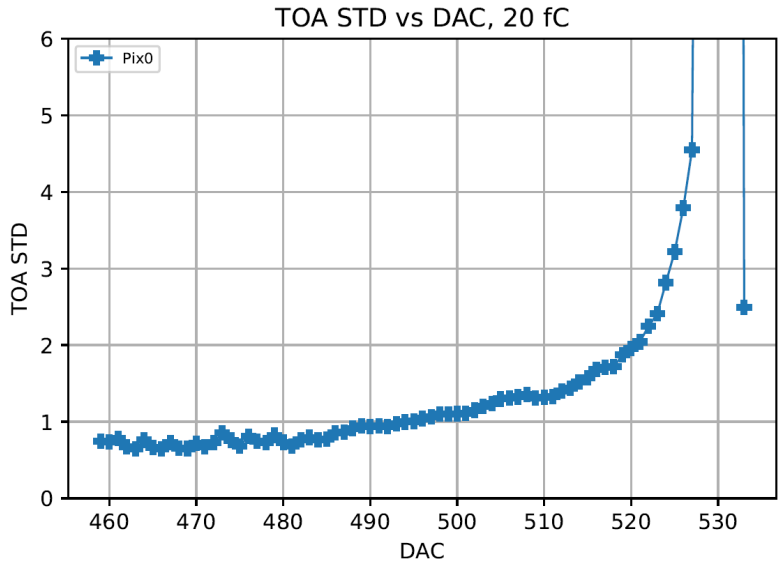




9 ps line

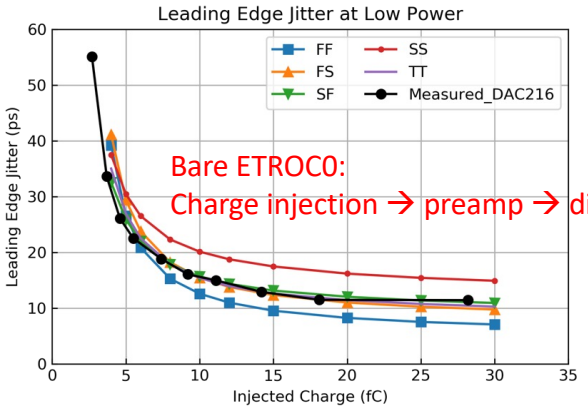
With sensor bump-bonded: with sensor capacitance loaded

18ps line

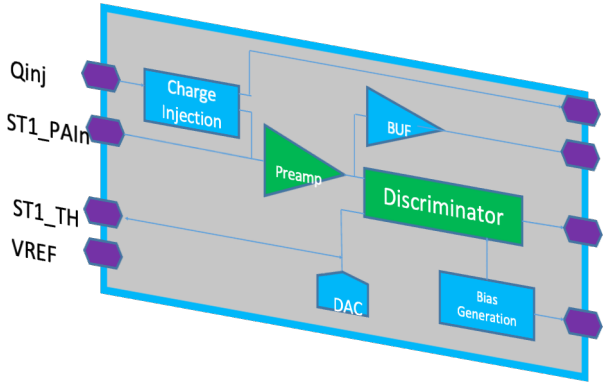


Bare ETROC1 works very well, matches with simulation and ETROC0

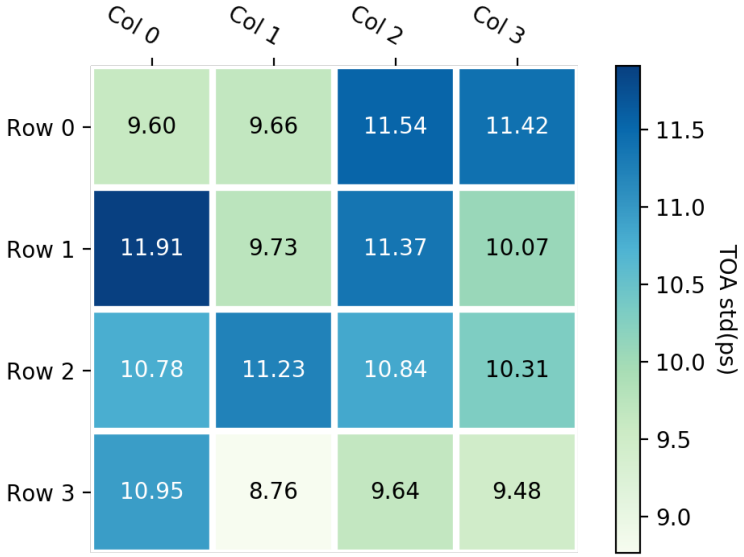
ETROC0 jitter (ps)



Bare ETROC0:
Charge injection → preamp → discriminator → scope



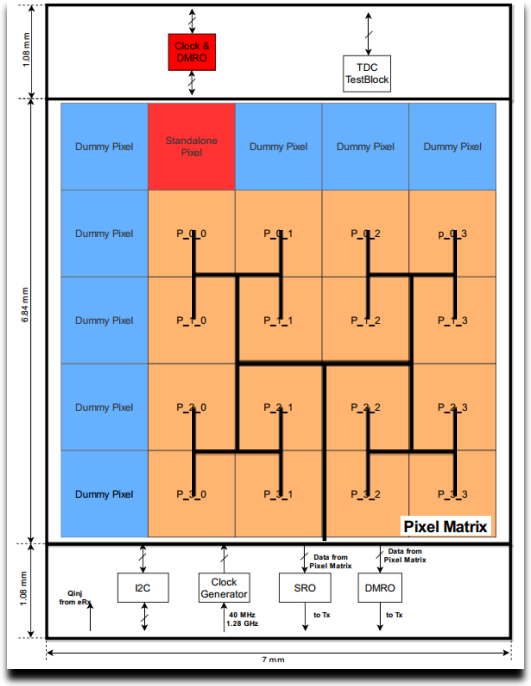
ETROC1 jitter (ps)



No cross talk observed

Charge injection test with bare ETROC1 at 20fC

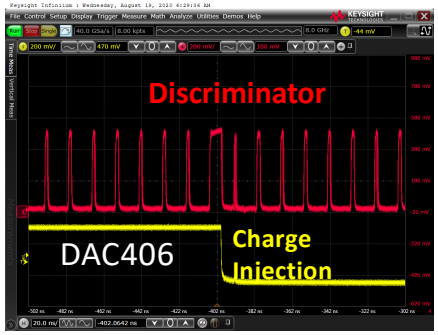
The TDC contribution to jitter is negligible

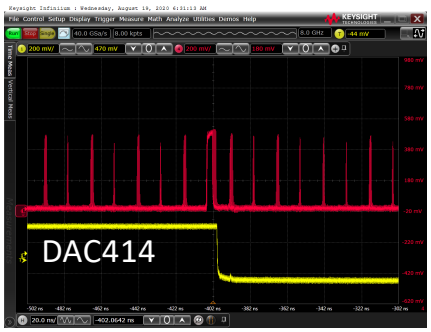


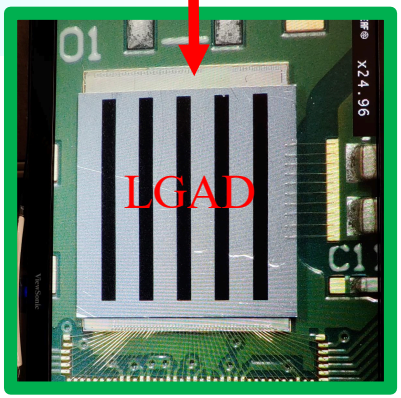
Charge injection → preamp→ discriminator→ TDC → readout

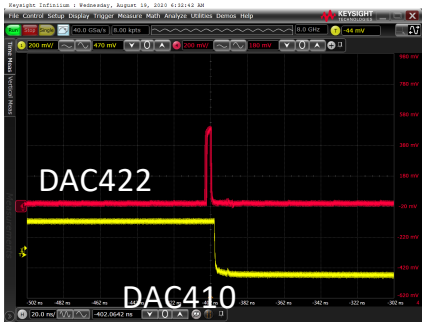
After ETROC1 is bump bonded with LGAD sensor:

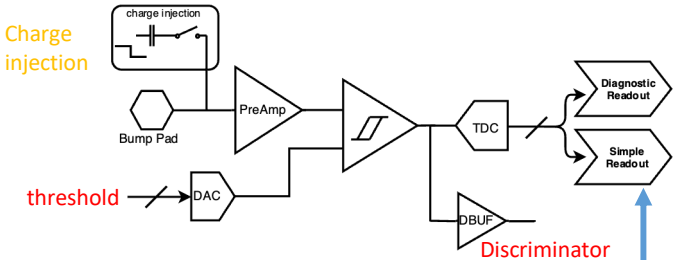
40MHz noise observed at discriminator output (with low threshold)











40MHz noise gone at discriminator output with high enough threshold

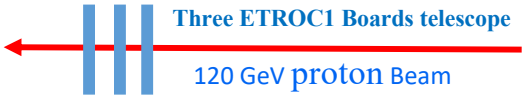
Sensor board, clock enabled

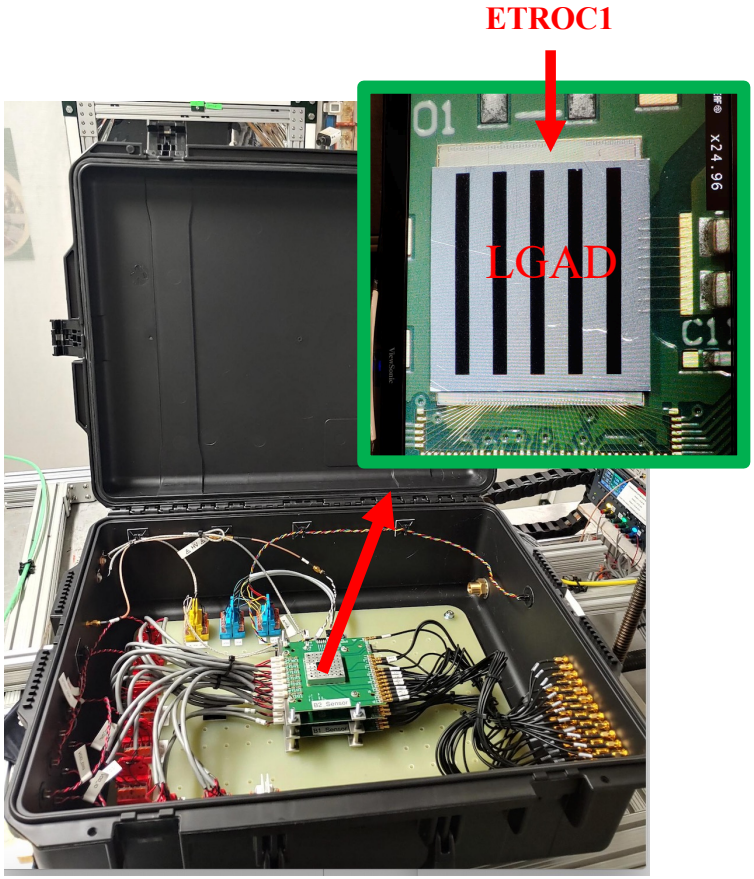
- Q=20 fC
- HV=-170 V

The 40MHz noise source was identified: the clocking activity in the circular buffer memory operation. The circular buffer memory in ETROC1 was for testing purpose only, not optimized for low power (ETROC2 circular buffer is x10 lower power, with clock gating, more on this later)

For ETROC1 Beam test, used high enough threshold (~8fC) to avoid this noise

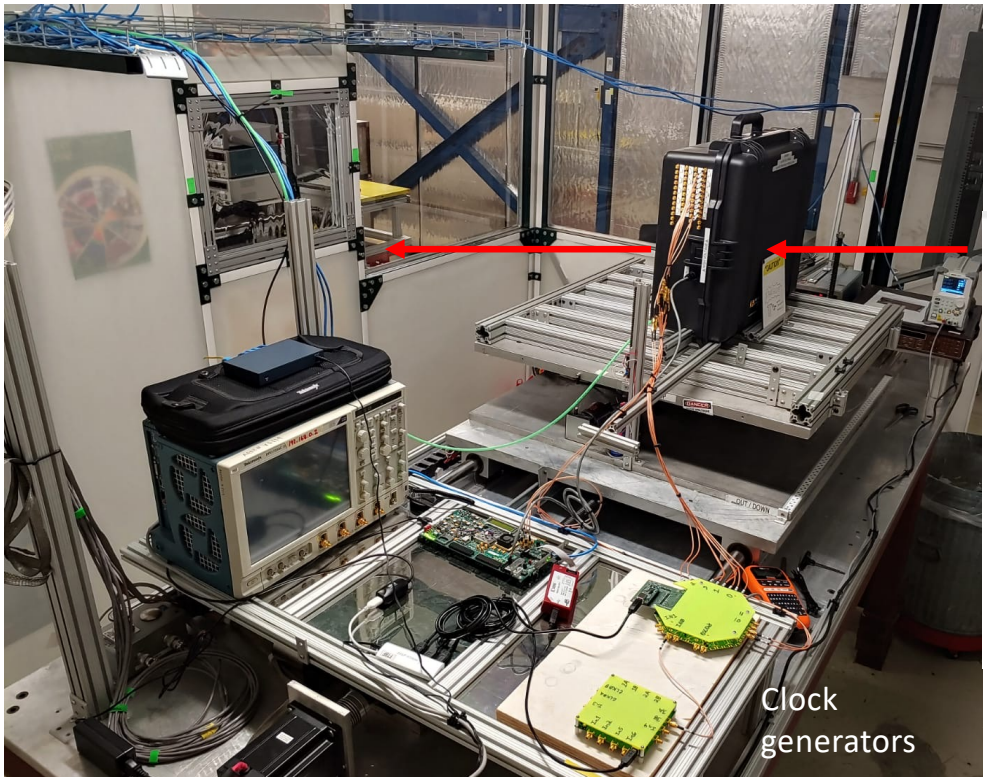
ETROC1 Beam Telescope @ FTBF

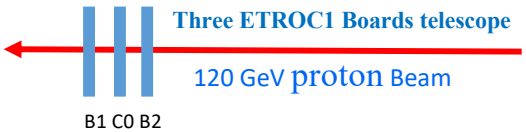




Precision timing full chain signal processing: preamp → discriminator → TDC (TOA/TOT)→ output with external and internal precision clock distributions

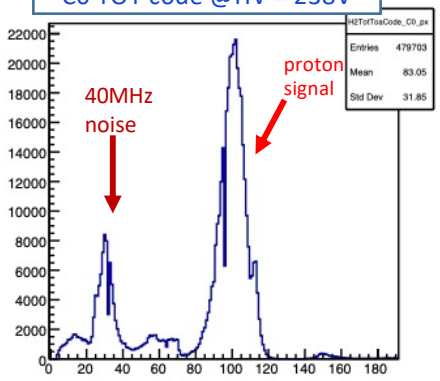
ETROC1 Beam Telescope @ FTBF (Fermilab)



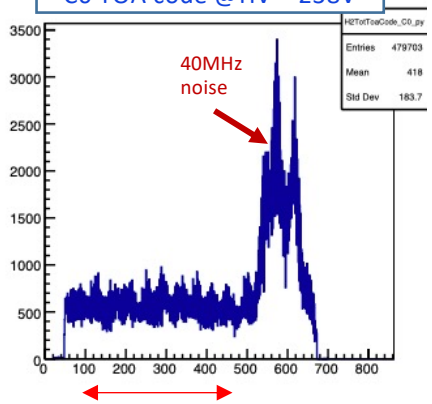


Telescope DAQ:
Triggered on B1
offline confirmed with B2
C0 is Device Under Test

C0 TOT code @HV = 238V



C0 TOA code @HV = 238V

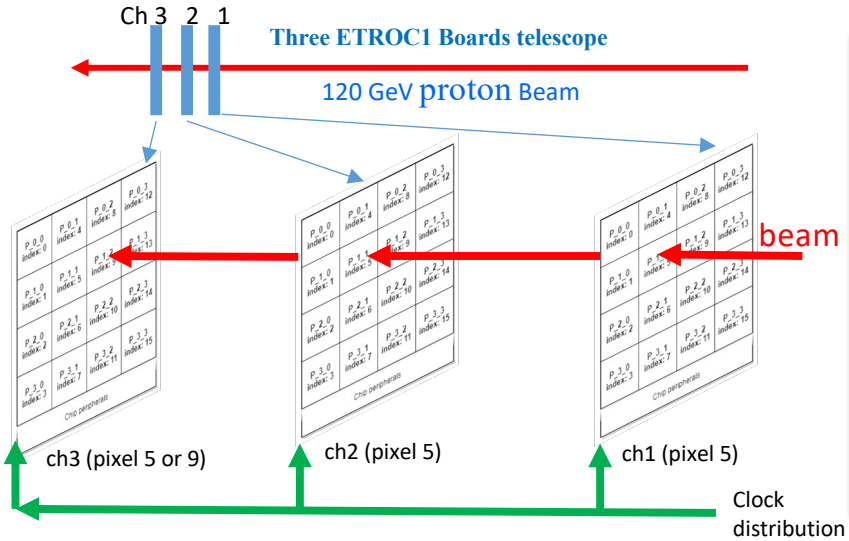


Tevatron machine clock 53MHz
ETROC clock 40MHz

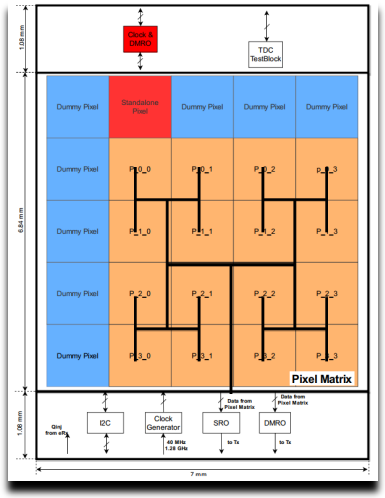
Beam TOA (time of arrival) is flat, and 40MHz noise is not.
Can stay away from the noise this way

2021 vs 2022 Test Beam test results

- Testing team (UIC/SMU/FNAL + students from KSU/KNU/CNU)



ETROC1 4x4 H-tree clock distribution within chip

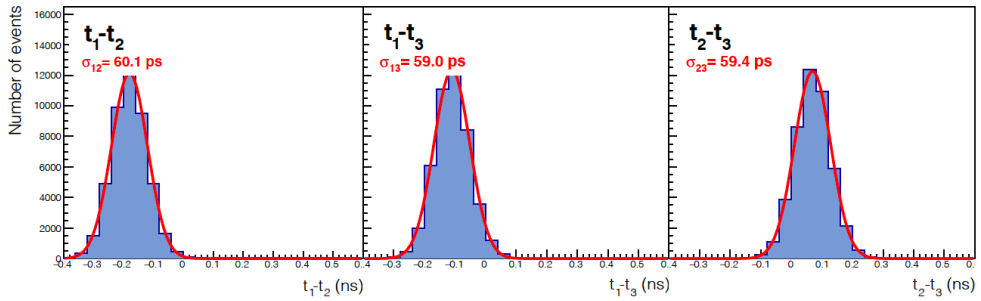


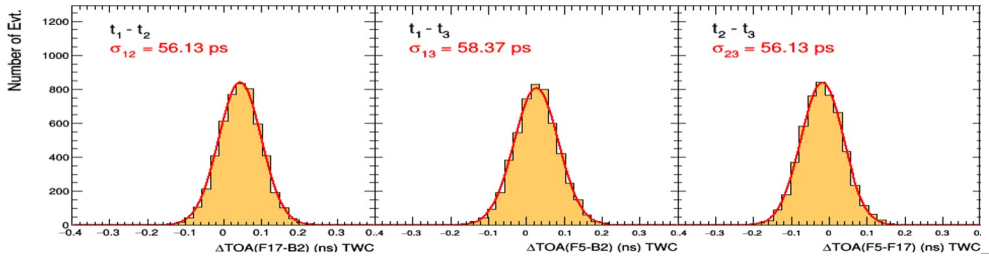
ETL Time resolution

Simulation /expectation vs spec

LGAD+ preamp/discriminator + TDC bin	35 ps	
Time-walk correction residual	< 10 ps	
Internal clock distribution	< 10 ps	
System clock distribution	< 15 ps	
Per hit total time resolution	41 ps	50 ps
Per track (2 hits) total time resolution	29 ps	35 ps

(with LGAD HV=230V for all three channels)





The measured time resolution includes all four contributions in the table

Single-hit timing resolution (ps) with TWC:

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

~ 42.0/42.7/41.3 ps (2021 beam test)

~ 41.3/38.0/41.3 ps (2022 beam test)

reproduced 2021 beam test results, with new ETROC1 boards and independent analysis

(2022 beam test mostly done by 4 graduate students)

Main lesson learned from ETROC1 for ETROC2

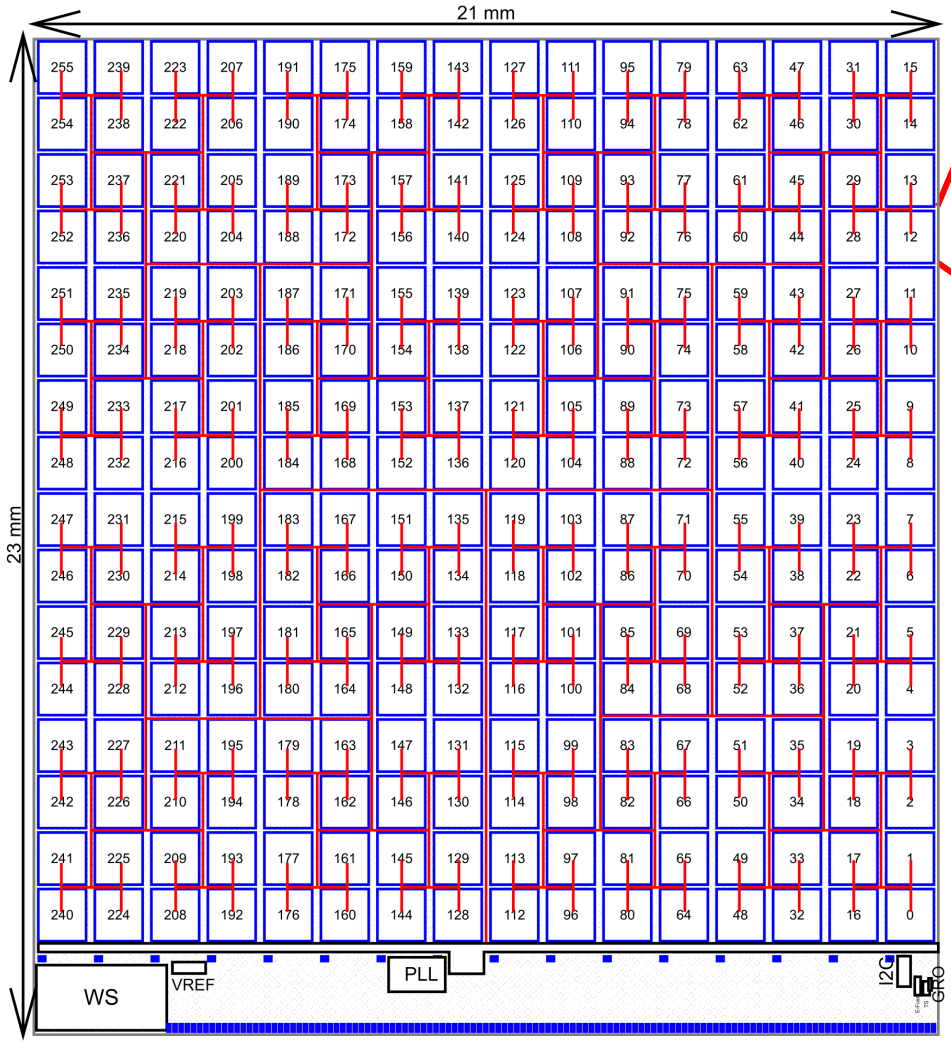
- Main lesson learned from ETROC1
  - ***40MHz clocking activity of memory causes noise*** through coupling with sensor
    - Bare ETROC1 (without senor) does not have this issue
    - With higher threshold (to avoid the noise), and proper TOA/TOT windows, good time resolution has been obtained from test beam data for the 4x4 array pixels (~40 ps per hit).

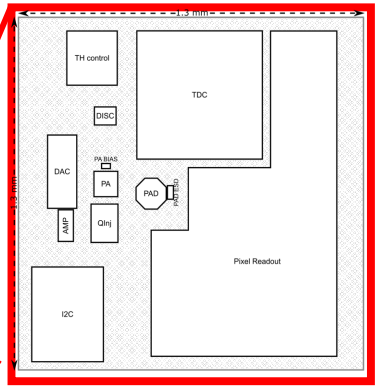
- ETROC2 design to address the noise issue: ***minimize it at its source (circular buffer memory operation)***
  - *Memory clock (and address line) gated based on hit*, only on for valid TDC hit
    - ***ETROC2 pixel readout is optimized to be x10 lower than that of ETROC1 power consumption***
  - Some clocks are offset to avoid "marching in sync"
  - *Shielding layer at the top* of ETROC2 (from sensor)
  - *Separated 40MHz clock for readout* (vs TDC clock) with adjustable phase
  - …

Bottom line:
ETROC2 front-end and TDC are the same as in ETROC1
ETROC2 16x16 clock H-tree is scaled up from ETROC1 4x4 H-tree
ETROC2 has brand new readout design optimized to minimize the 40MHz noise

→ ETROC2 pixel digital power is 10 times lower than that of ETROC1

ETROC2 design: most building blocks have been silicon proven

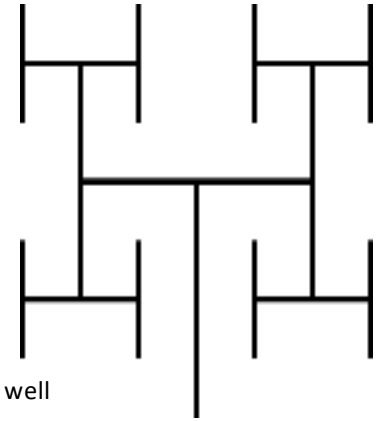




Front-end:
Charge injection/DAC
Preamp,
Discriminator
TDC

All tested in ETROC0/1,
and reused in ETROC2

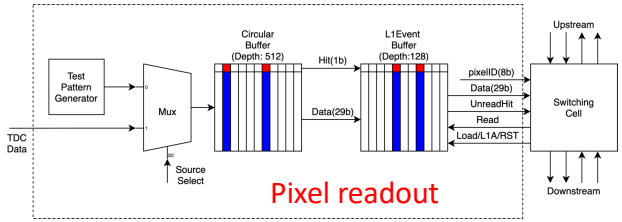
- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- I2C
  - I2C design validated with I2C test chip, including SEU
  - In-pixel I2C register expanded and verified
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - reusing Tx in ETROC1
  - Reusing Rx in ETROC1(from lpGBT)
- WS (Waveform Sampler)
  - Rad-hard version tested and works well
- In-pixel threshold calibration
  - tested with ETROC0 via FPGA emulator



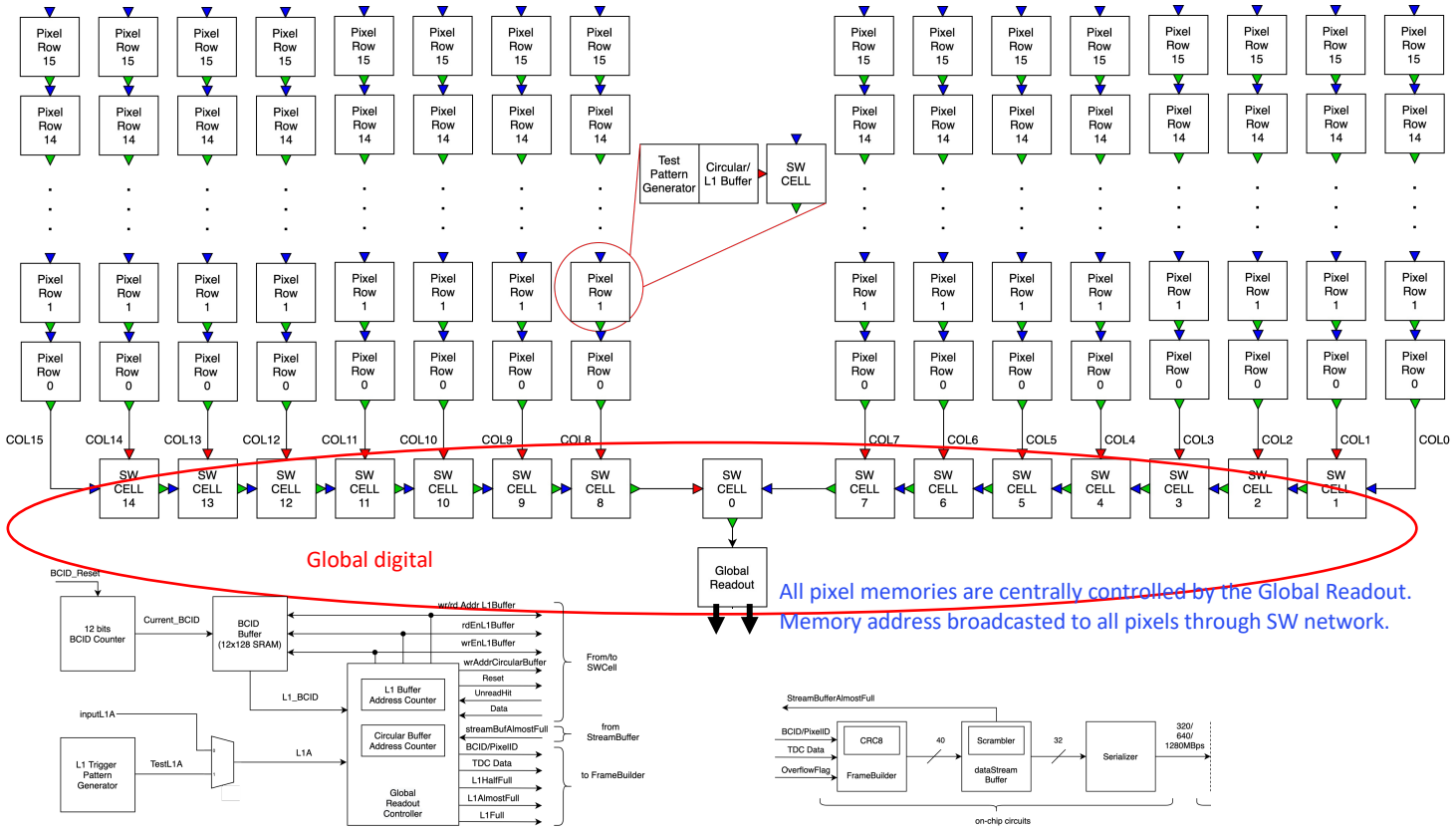
All critical analog building blocks have been silicon proven in testing chips,
and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend.

The overall ETROC readout

Datao Gong

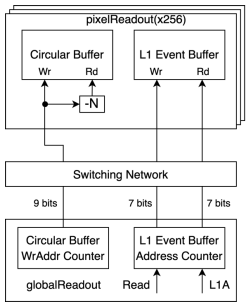


Pixel readout



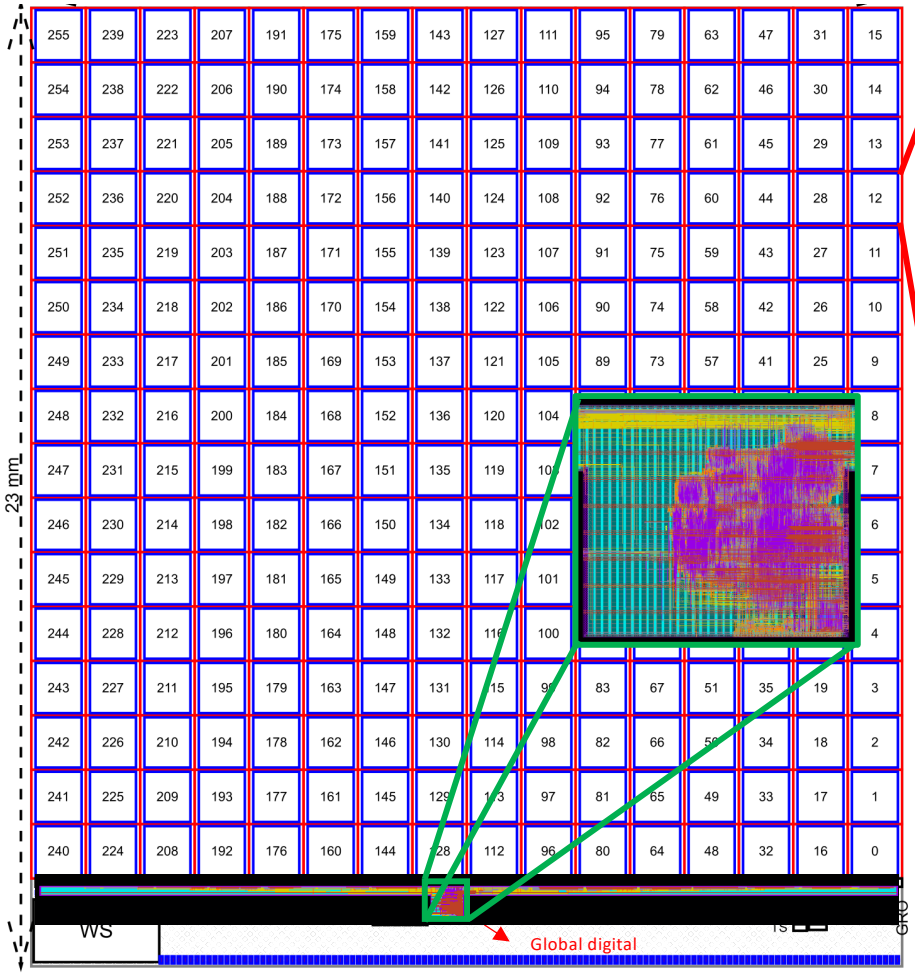
Global digital

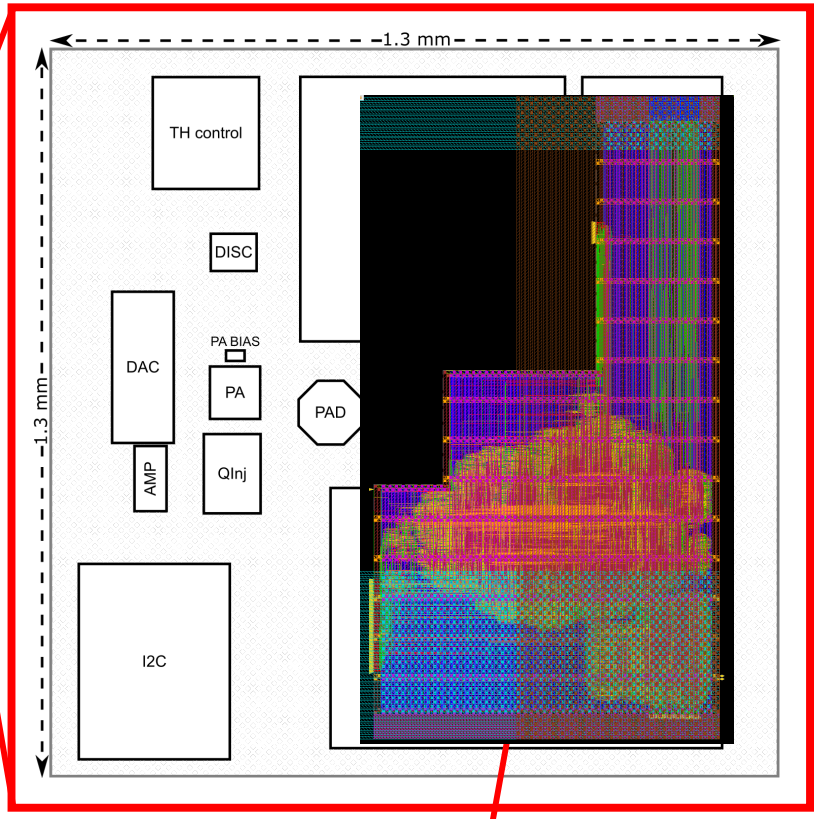
All pixel memories are centrally controlled by the Global Readout.
Memory address broadcasted to all pixels through SW network.



The ETROC2 emulator will emulate the entire ETROC2 digital processing chain. Details see talk at TWEPP 2022,
"An FPGA-based readout chip emulator for the CMS ETL detector upgrade" by Tiankuan Liu/Jinyuan Wu.
https://indico.cern.ch/event/1127562/contributions/4904781/

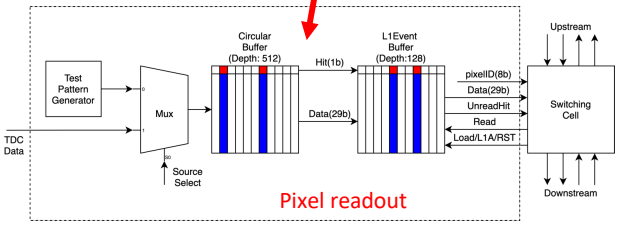
ETROC2 digital readout: pixel and global





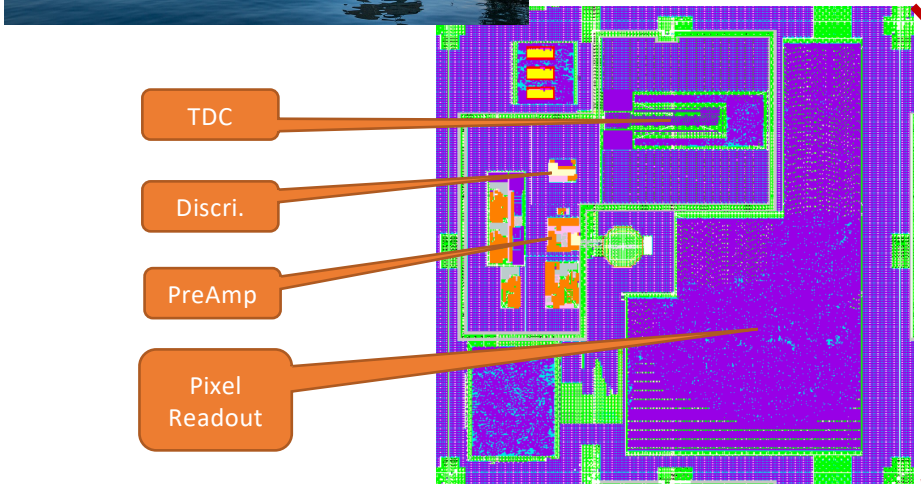
What's new & time consuming:

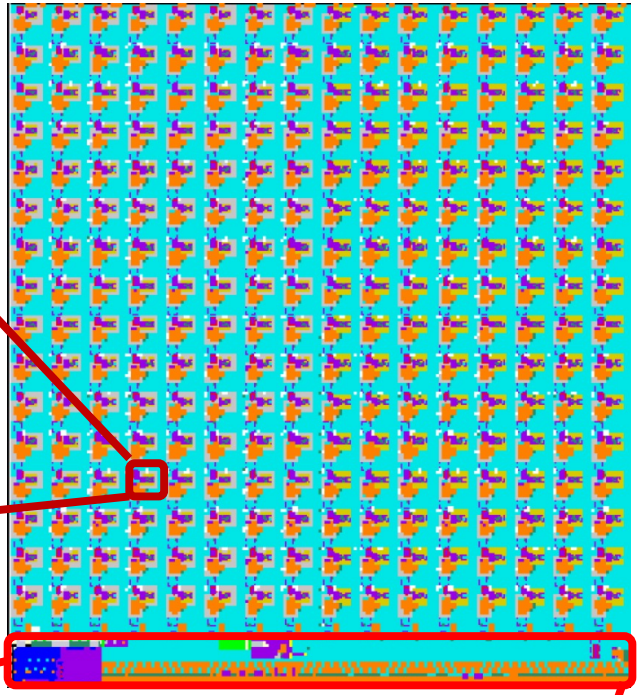
Pixel readout & Global digital

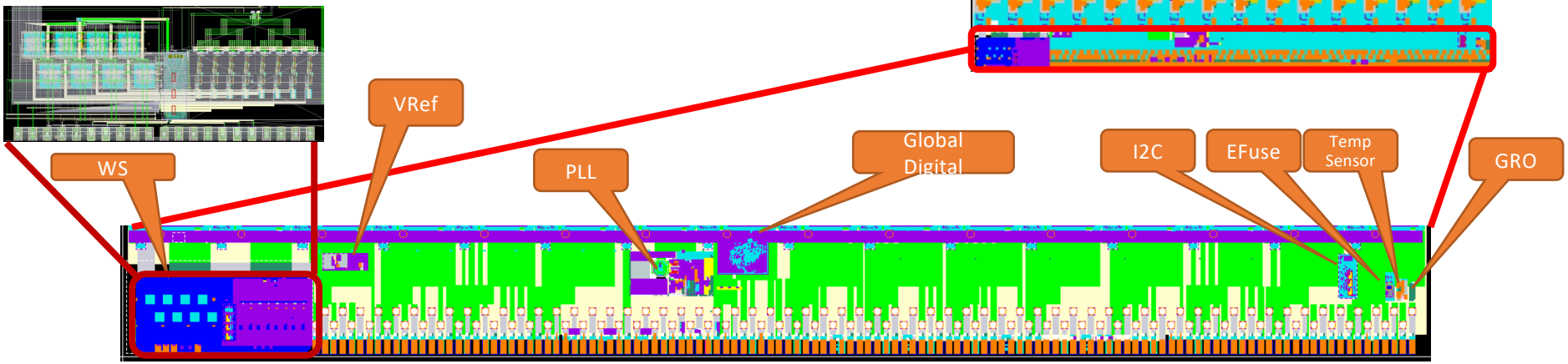


ETROC2 layout (submitted on Oct 21, 2022)

From Quan Sun





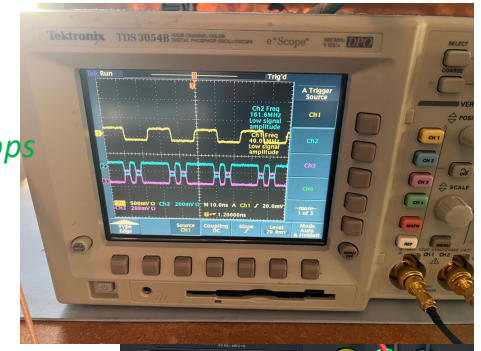


ETROC2 testing started on April 21, 2023

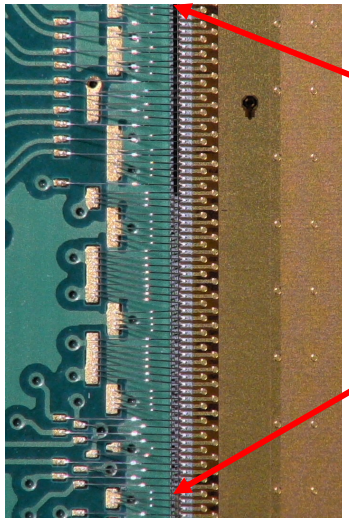
ETROC2 powered up for the first time:

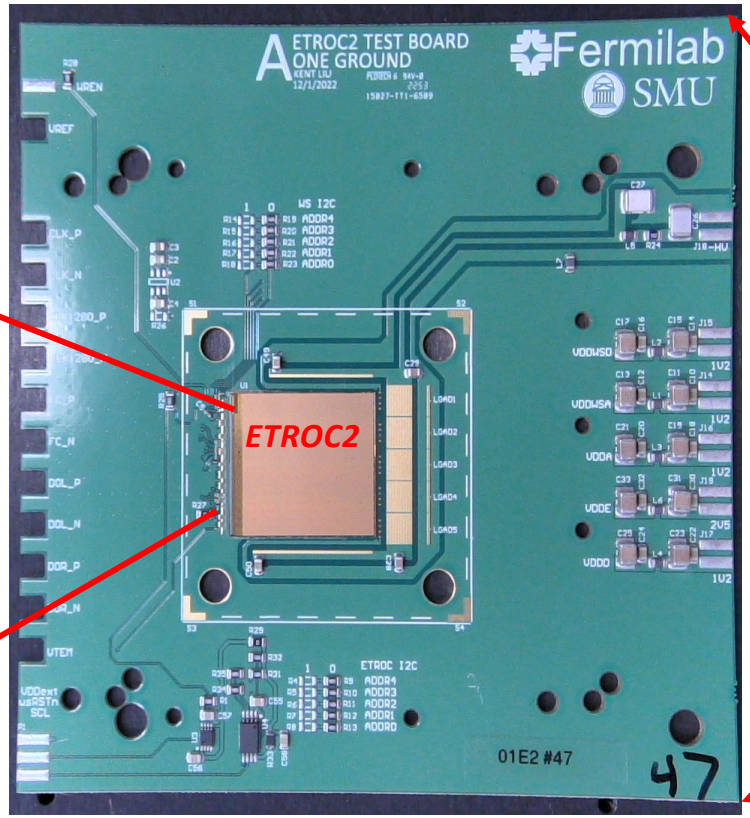
- Chips arrived Fermilab on April 20th Thursday afternoon
- Test board fully assembled April 21 Friday afternoon
- *Initial smoke test successfully performed on April 21 evening*
  - *test stand already tested with ETROC2 emulator*

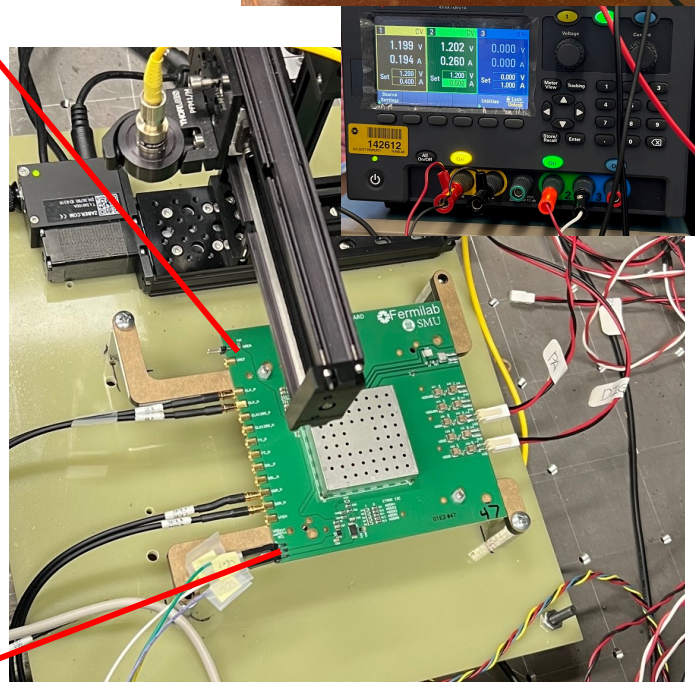
Essentially Plug & Play:
I2C works, PLL locks
Output can be switched between 320/640/1280Mbps
…



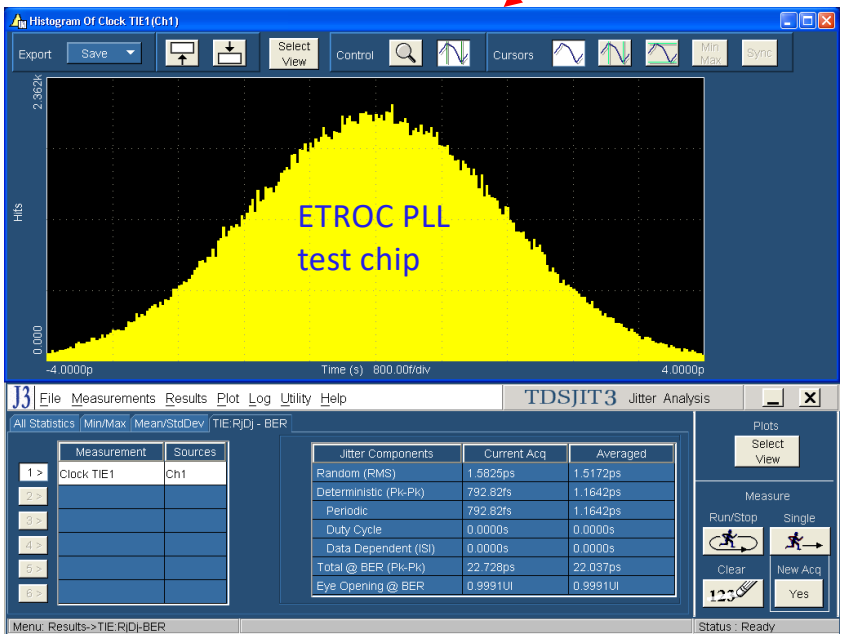
Wire bonds

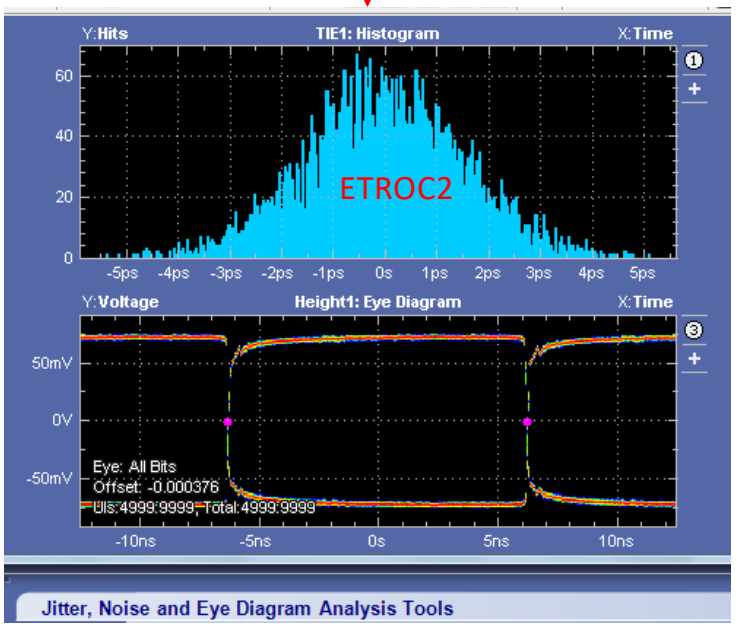






Jitter: ETROC PLL test chip vs ETROC2 PLL





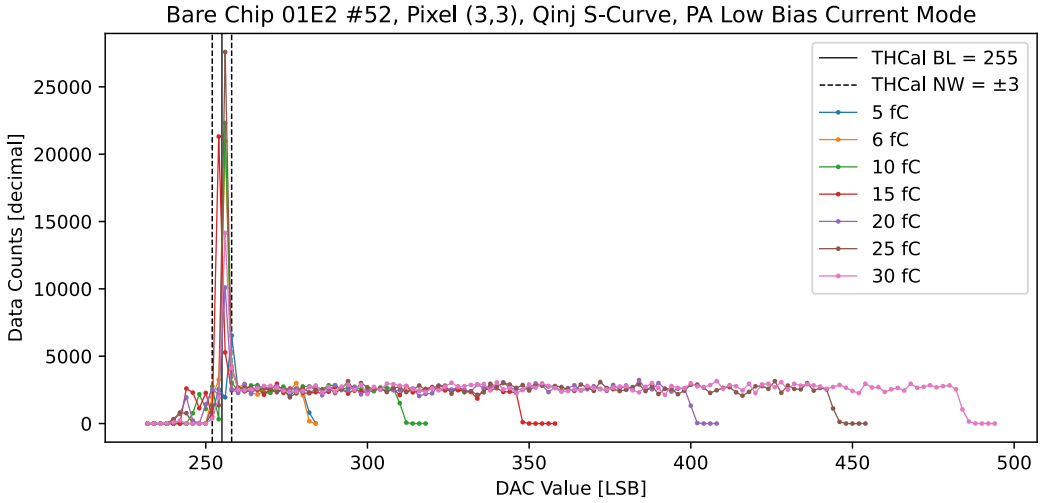
The random (rms) jitter < 2 ps

The random (rms) jitter < 2 ps

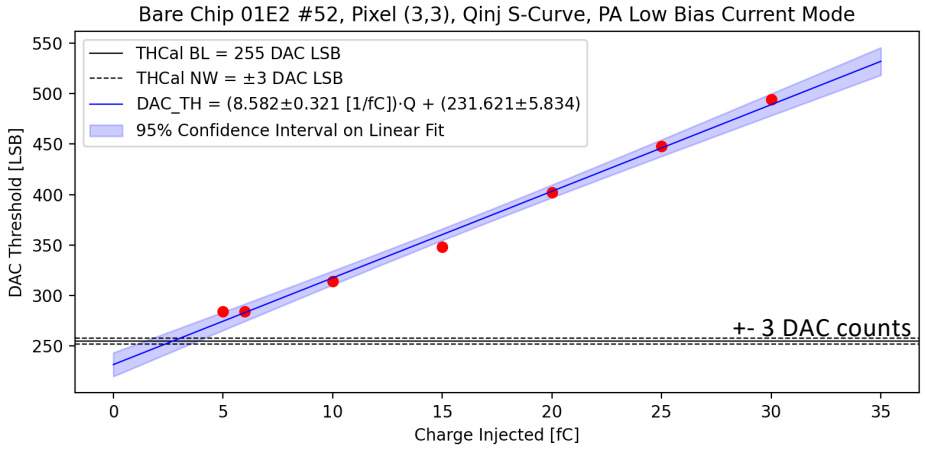
ETROC2 output Tx: 320Mbps and 640Mbps modes all looking good, eyes wide open

- Jitter of 40 MHz TDC clock from PLL

Preliminary ETROC2 Pixel S-curve scan study



The manual S-curve scan results agree with internal pixel automatic threshold calibration, as shown by the agreement of the automatically Determined Baseline (BL) and Noise Width (NW) with the S-Curve data

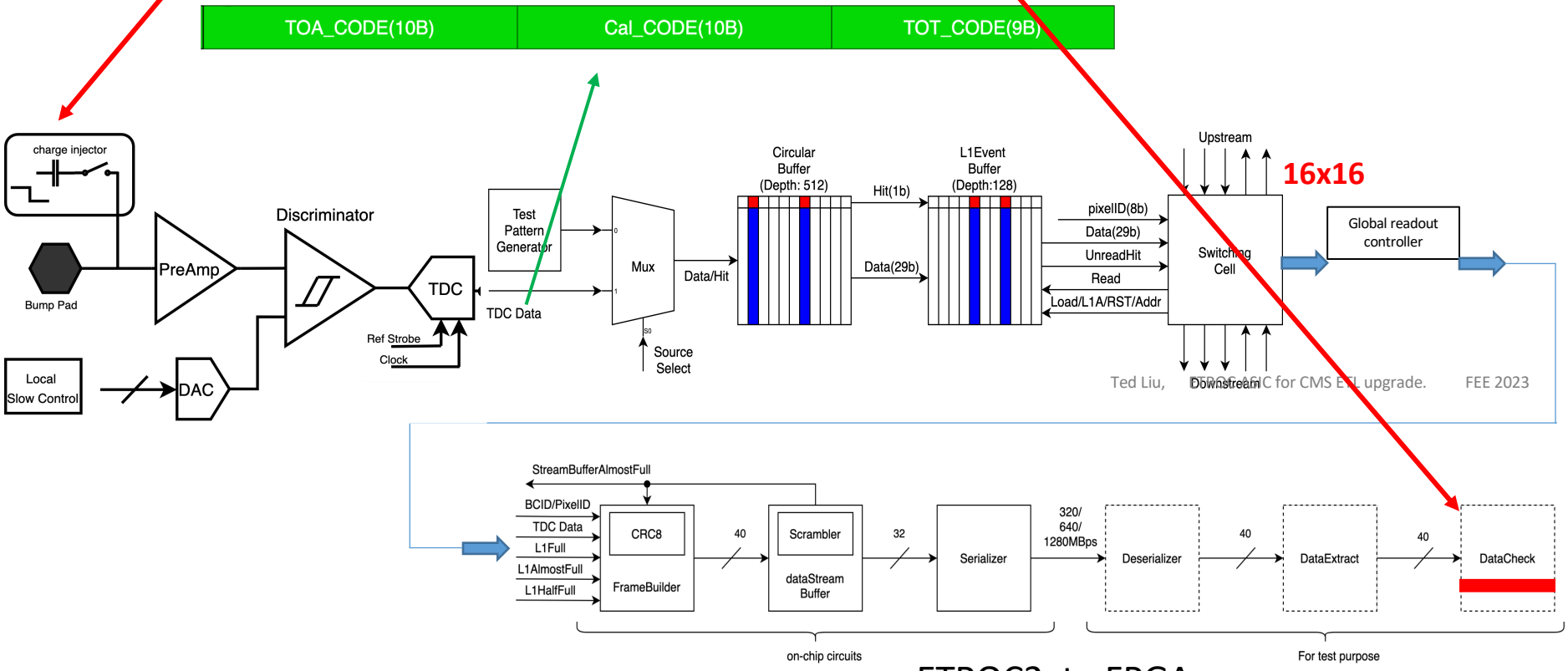


In pixel automatic threshold calibration:

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

Charge injection full chain testing: what's involved?

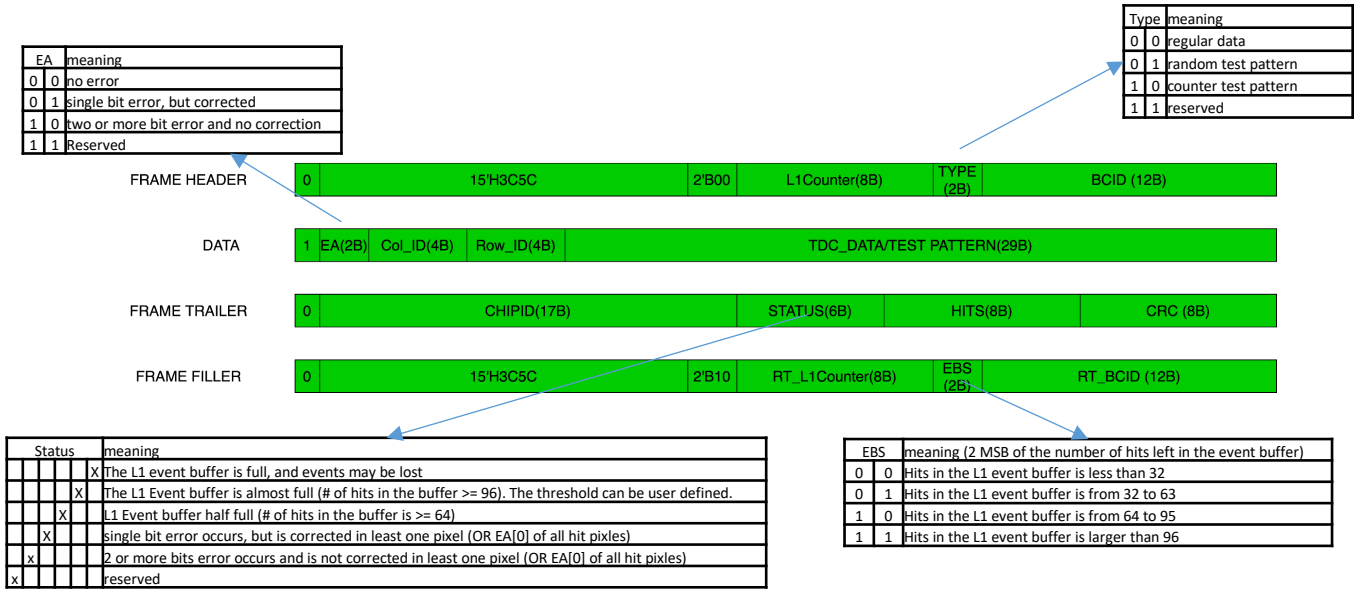
almost the entire chip …



ETROC2 to FPGA

ETROC2 data output frame

- Composes of a header, variable hit words, and a trailer.
- When there is no L1A, a filler is sent.
- Each header, data words, trailer, or filler has 40 bits.



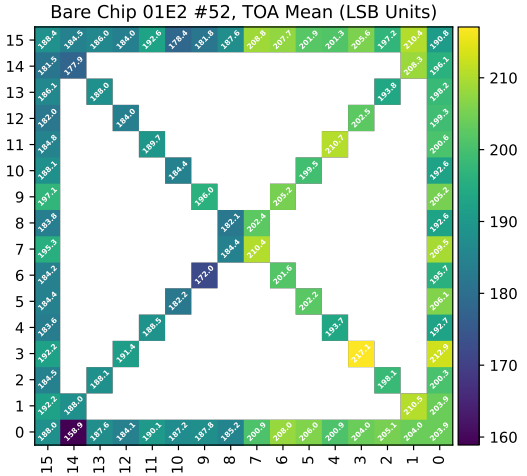
EA		meaning
0	0	no error
0	1	single bit error, but corrected
1	0	two or more bit error and no correction
1	1	Reserved

Type		meaning
0	0	regular data
0	1	random test pattern
1	0	counter test pattern
1	1	reserved

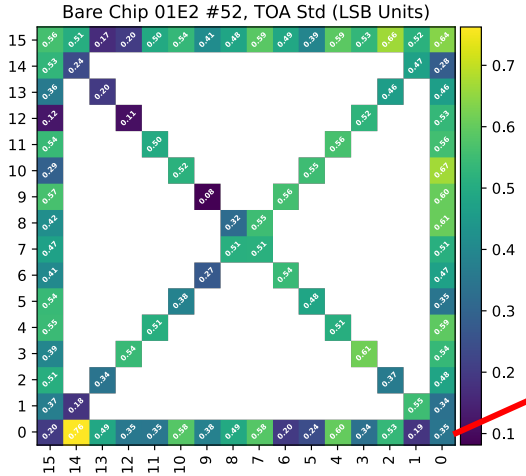
Status						meaning
					X	The L1 event buffer is full, and events may be lost
				X		The L1 Event buffer is almost full (# of hits in the buffer >= 96). The threshold can be user defined.
			X			L1 Event buffer half full (# of hits in the buffer is >= 64)
		X				single bit error occurs, but is corrected in least one pixel (OR EA[0] of all hit pixles)
	x					2 or more bits error occurs and is not corrected in least one pixel (OR EA[0] of all hit pixles)
x						reserved

EBS		meaning (2 MSB of the number of hits left in the event buffer)
0	0	Hits in the L1 event buffer is less than 32
0	1	Hits in the L1 event buffer is from 32 to 63
1	0	Hits in the L1 event buffer is from 64 to 95
1	1	Hits in the L1 event buffer is larger than 96

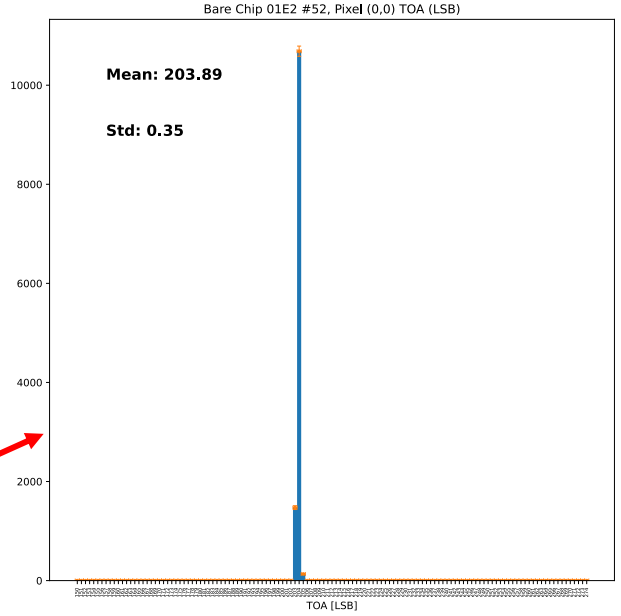
Preliminary ETROC2 single pixel charge injection, with TOA mean and Std



TDC with Analog Power supply



TDC with Digital Power supply

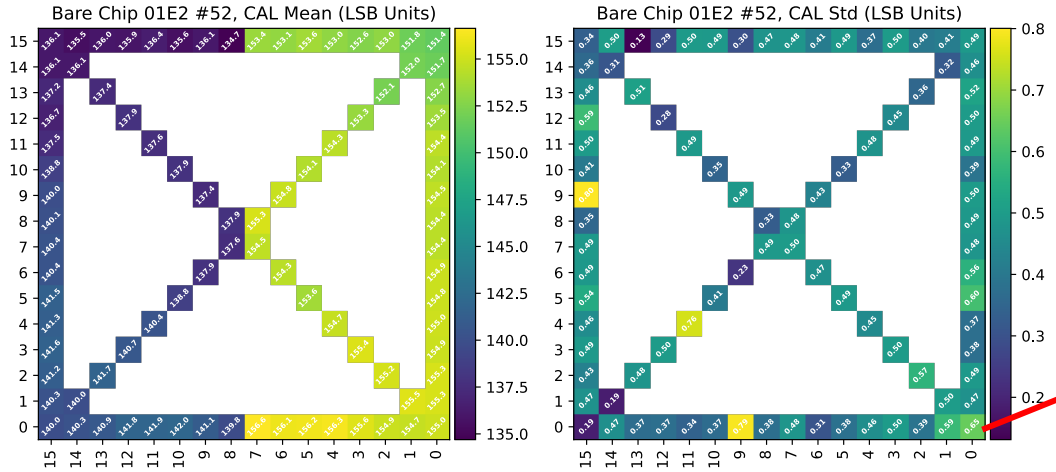


TDC bin ~ 20ps

Similar to ETROC1

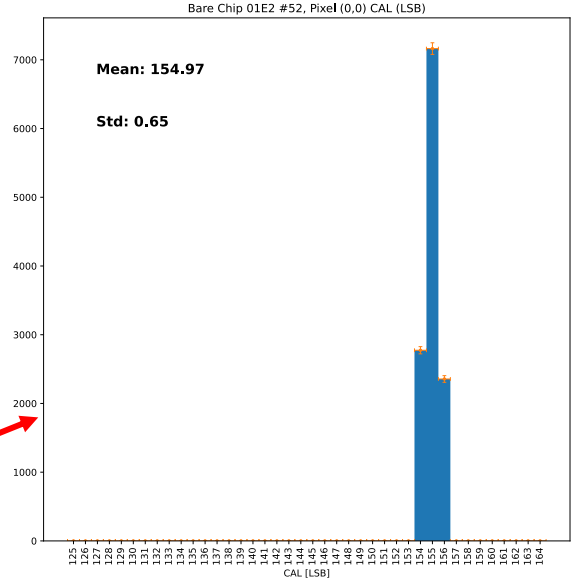
Preliminary ETROC2 single pixel charge injection, with CAL mean and Std

CAL is the difference in TDC code
between two consecutive clock ticks (3.125ns)



TDC with
Analog
Power supply

TDC with
Digital
Power supply



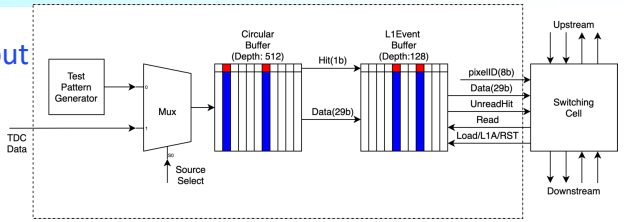
TDC bin ~ 20ps

Similar to ETROC1

Just started last week: Torture testing with charge injection for cluster of pixels

ETROC2 key features: from testing point of view

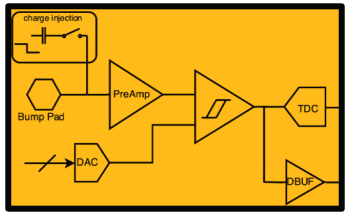
ETROC2 pixel readout



Initial testing done, chip is functional well, torture testing next

To be tested soon

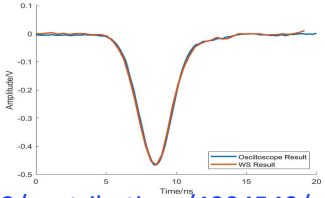
- Self-test pattern generator
  - Can be used to test the digital data flow and link interfaces. Users can dial the occupancy of pixels and change patterns
    - This feature has been used extensively to simulate and verify the readout design of ETROC2, at RTL level and post layout stage
    - First thing user can test with ETROC2 emulator, the same test can then be done for bare ETROC2 and bump bonded ETROC2
    - At chip level (as *build in self-testing capability*), board level, and system level (with DAQ backend)
- Testing with charge injection
  - *Test the full path from charge injection to preamp to discriminator to TDC to circular buffer to event buffer to global digital readout*
  - Discriminator threshold scan and jitter measurements (bare ETROC2 first, then bump bonded ETROC2)
  - User can define the window for TOA, TOT and CAL to filter/suppress hits before readout
  - User adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - Each pixel can be enabled or disabled for DAQ readout
  - The relative phases adjustable between the TDC clock, pixel readout clock and global readout clock



- ETROC2 testing with LGAD sensor, laser, source and then beam
  - Full path timing performance study including LGAD
- Auto-threshold scan within pixel
  - This new feature will be studied first by dedicated ETROC2 chip level testing

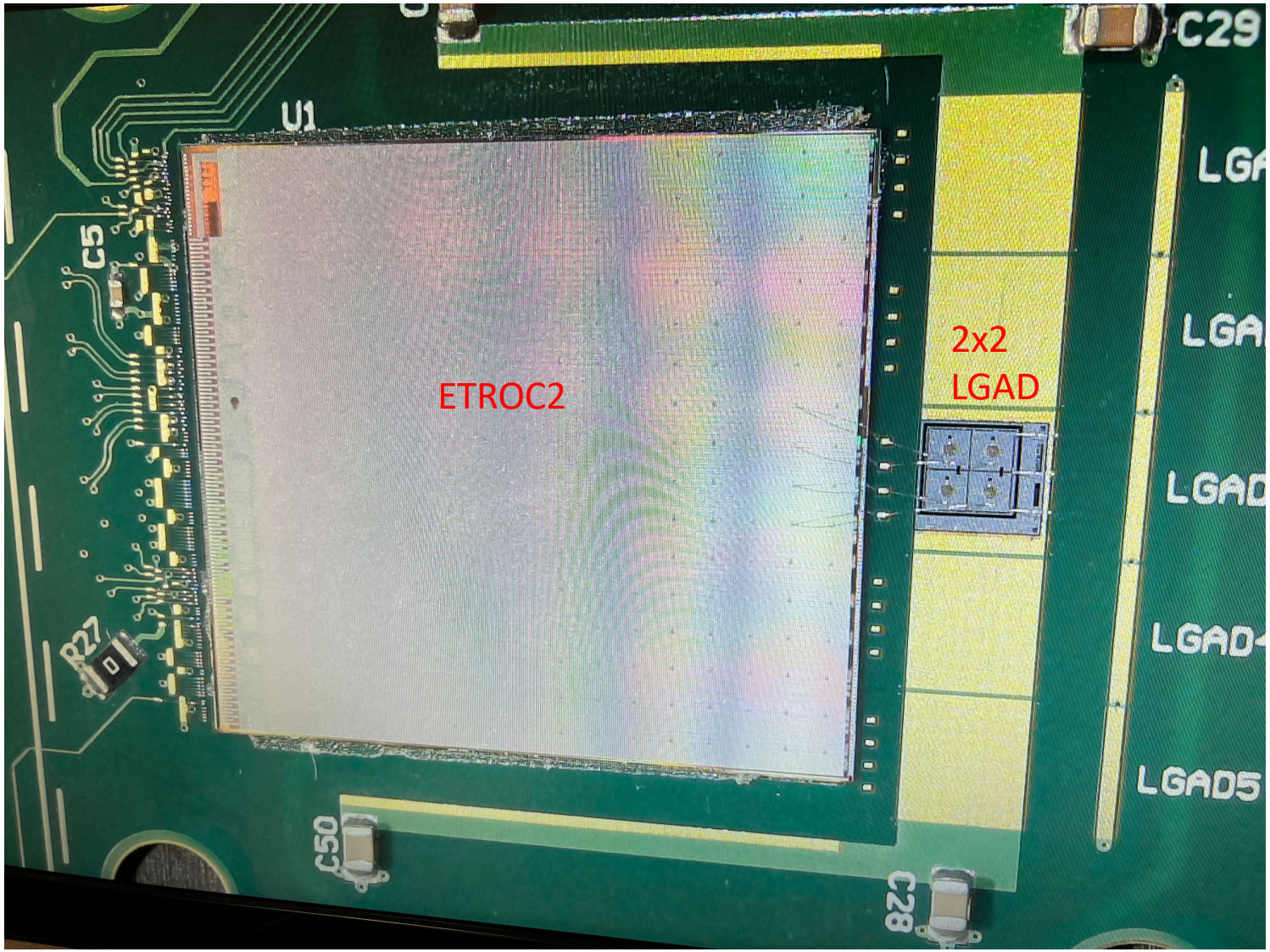
https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

- Trigger path
  - Can be used for monitoring purpose initially, a coarse map of user defined hits continuously sent out every BC
  - Can be used for self triggering for beam test if so desired, user can define the window for TOA, TOT and CAL for triggered hit
  - Use flashing bits in empty BCID (beam gap), defined via I2C. Can be used as cross check and monitoring purpose.
- Waveform Sampler
  - Able to record waveform of one pixel up to 16 bunch crossing (400 ns), start and stop controlled via fast command, readout via I2C
  - power-down when not used, intend to use for monitoring purpose during detector operation
- Power consumption estimate is ~1W per chip, being confirmed with ETROC2 chips



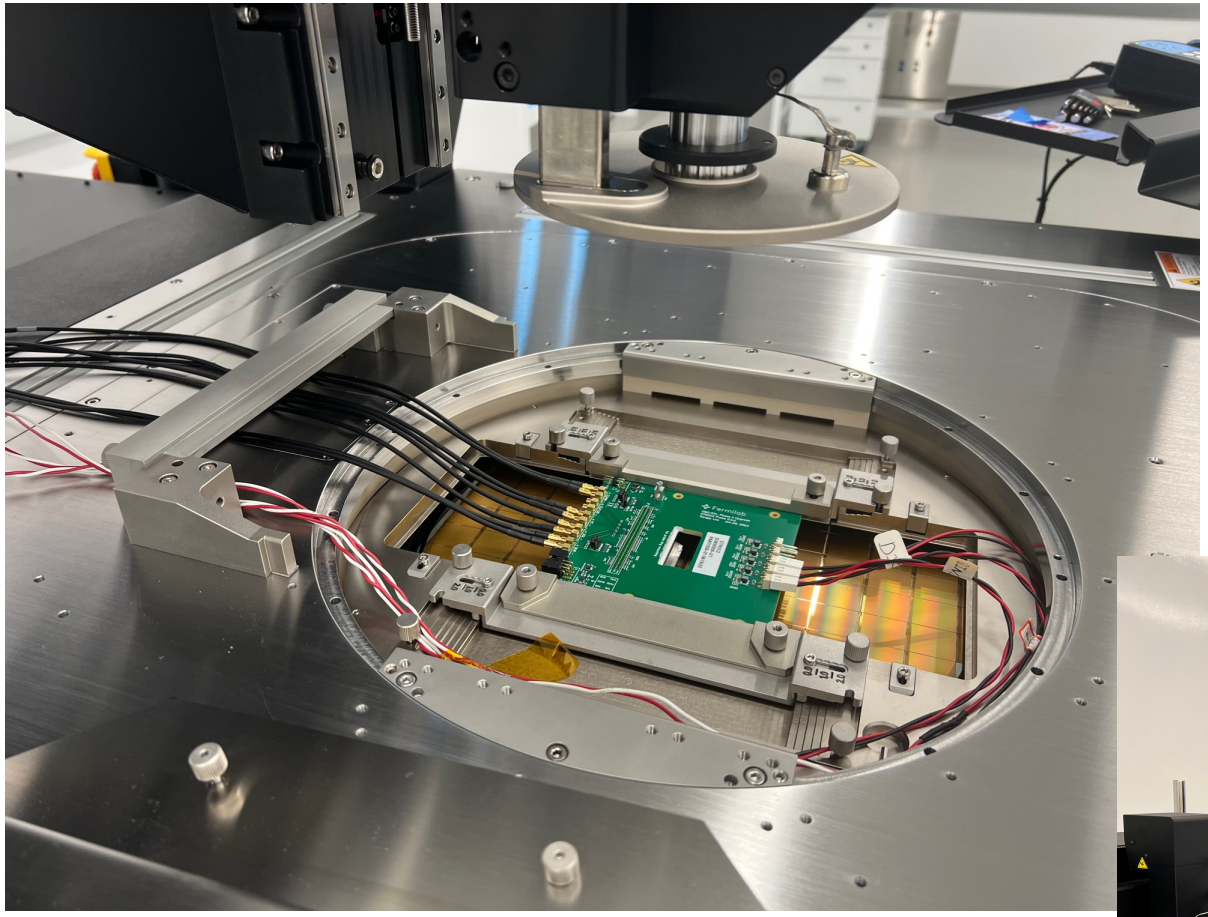
https://indico.cern.ch/event/1127562/contributions/4904540/

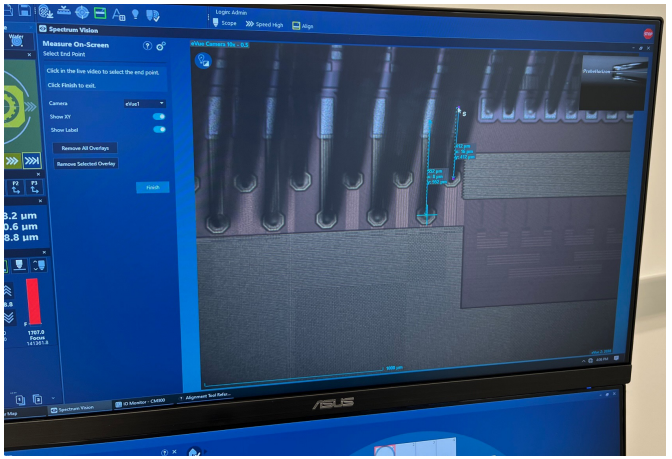
Getting ready to test with 2x2 sensor

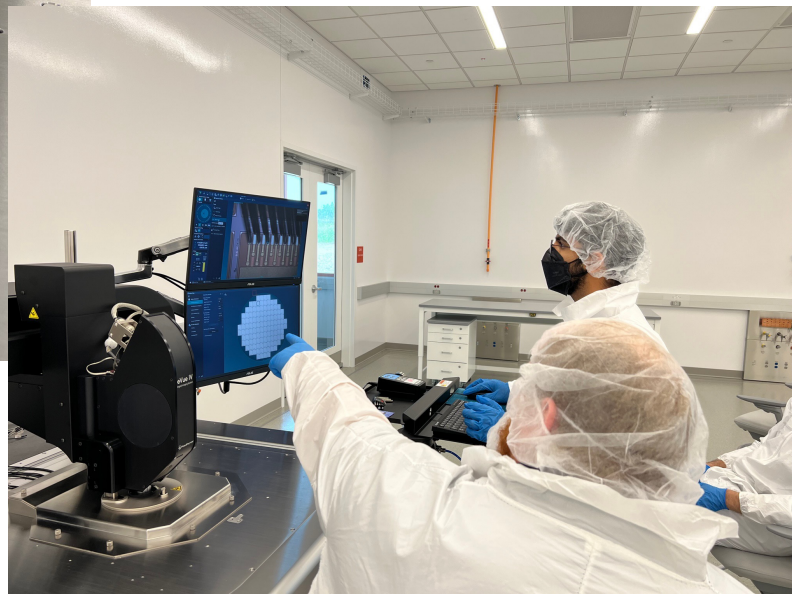


2x2 LGAD wire bonded to ETROC2 last week

Preparation for ETROC2 wafer probe testing



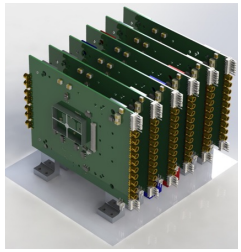




New 12” wafer probe station installed and calibrated on May 9th, ETROC2 probe card and wafer installed on May 11, initial testing works

Fermilab IERC clean room

From ETROC1 Beam Telescope to ETROC2 Beam Telescope

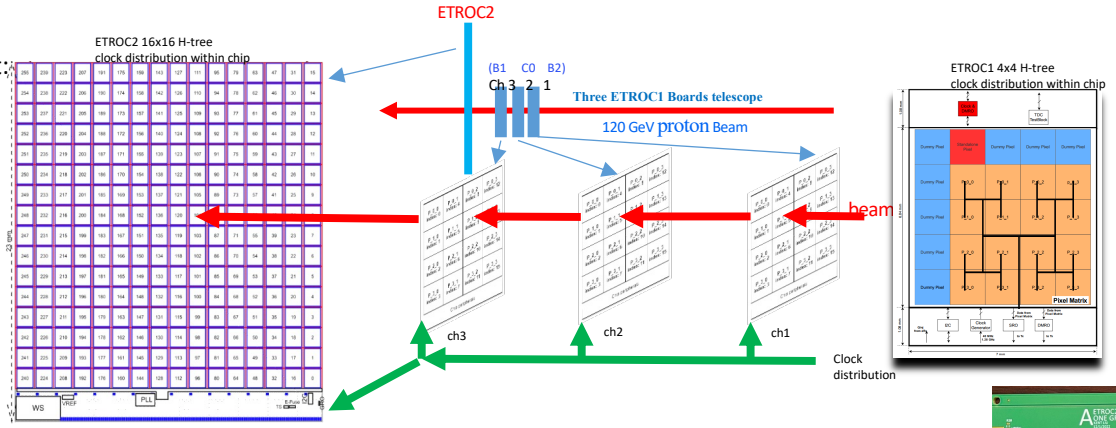


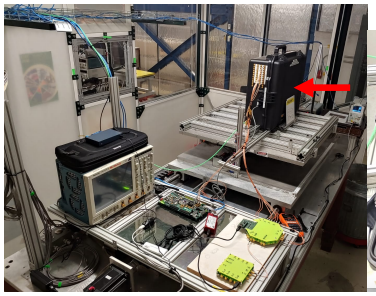
The telescope is being commissioned with FNAL beam

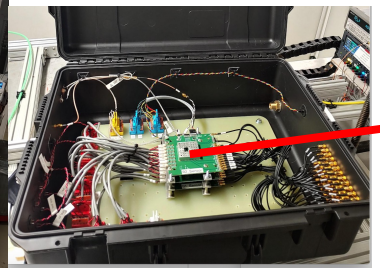
Initial ETROC2 beam test:

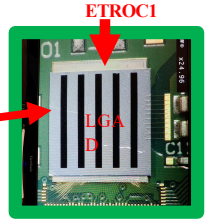
Simply add one ETROC2 test board into ETROC1 Telescope

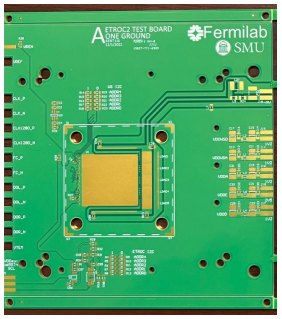
Three ETROC1 boards will be used as trigger and reference boards











ETROC2 test board is designed to be fully compatible with the ETROC1 beam telescope

ETROC status summary

- ETROC2 is the first full size full functionality prototype design
  - Designed as if it were the final version, from functionality point of view
  - Steady progress in testing bare ETROC2 chips
    - charge injection for the full chain is working
      - ***Initial results looking good, similar as ETROC1***
      - ***Extensive study of the performance on going (with torture tests)***
      - ***Prepare for TID and SEU testing***
      - *Wafer probe testing*
  - Testing ETROC2 with sensor
    - Preparation for ETROC2 bump bonding with 16x16 sensor
    - ETROC2 has been wire bonded with 2x2 sensor, ***initial testing starts this week***
    - ETROC2 board being integrated in ETROC1 beam telescope
    - Beam testing
  - *A busy year ahead … tons of work yet to be done. So far, no show stopper encountered.*
- ETROC3
  - The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
  - Submission scheduled for 2024

For technical details, please see ETROC papers and recent talks.

Characterization of the CMS Endcap Timing Layer readout chip prototype with charge injection

https://iopscience.iop.org/article/10.1088/1748-0221/16/06/P06038

The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL

https://arxiv.org/abs/2012.14526

In-pixel automatic threshold calibration for the CMS Endcap Timing Layer readout chip

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

FERMILAB-CONF-20-549-E

A New Scheme of Redundant Timing Crosschecking for Frontend Systems

https://ieeexplore.ieee.org/document/9447027

A 2.56 GS/s 12-bit 8x-Interleaved ADC with 156.6 dB FoM_S in 65 nm CMOS

IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

https://ieeexplore.ieee.org/document/9446843

2022 TWEPP talks related to ETROC:

From ETROC1 to ETROC2:

https://indico.cern.ch/event/1127562/contributions/4904521/ (***TWEPP 2022***, Tuesday)

ETROC Emulator:

https://indico.cern.ch/event/1127562/contributions/4904781/ (***TWEPP 2022***, Wed)

ETROC Waveform Sampler:

https://indico.cern.ch/event/1127562/contributions/4904540/ (***TWEPP 2022***, Thursday)

TDC with Uncontrolled Delay lines: calibration approach and method

https://indico.cern.ch/event/1127562/contributions/4904530/ (***TWEPP 2022***, Thursday)

ETROC power consumption estimate with measurements

ETROC0/ETROC1 testing results

Final ETROC0/1 design simulation results

Table from TDR

Circuit component	Power per channel [mW]		Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	0.76 0.74	171.5	189.4 (preamp low power)
Preamplifier (high-setting)	1.25	1.31 1.27	320	325.1 (389.1, the highest power)
Discriminator	0.71	0.87 0.84	181.8	215.0
TDC	0.2	0.07 0.1	51.2	25.6
SRAM (→ memory)	0.35	0.25 (sim)	89.6	64.0
Supporting circuitry	0.2	0.2 (reserve)	51.2	51.2
Global circuitry			200 →	234.5

Sum: ~780/915/980 mW (low/high/highest power)

- Measurements agree with simulation of ETROC0 and 1 design
  - TT corner numbers shown, mostly agree reasonably well
  - ***But should assume up to 20% variation with real production***
  - Note: preamp highest setting (4th gear) power is 1.52mW (measured), the high-setting above is the 3rd gear.
- The new 0.25mW SRAM is based on estimate by expert (ETROC2 will not use SRAM, power is expected to be lower)
- The "supporting circuitry": reserved for circuitry hard to be separated clearly
- The "global circuitry" (a guess back then for TDR, with large uncertainty)
  - ***A lot is known now about global circuitry blocks (simulation and test chips)***
    - ***PLL: 60mW; Phase shifter: 2 mW; Clock distribution: 25mW;***
    - ***Tx: 16mW; Rx 1mW. Fast command decoder: 2mW***
    - ***Voltage reference generator: 0.5mW.***
    - ***Readout: 100mW ; other misc: 20mW***

106.5
+
120
+ 8
= 234.5 mW

- ***Waveform sampler: when disabled, ~8mW (negligible)***
  - ***When fully enabled (for a short period, sub ms or micro-second): 141mW***
  - ***This means momentarily, the ETROC power could reach 1100mW when WS is enabled.***

Use 980mW & add 20% for worst case.
(***to be confirmed by ETROC2 measurements***)

To be compared with ETROC2 measurements soon