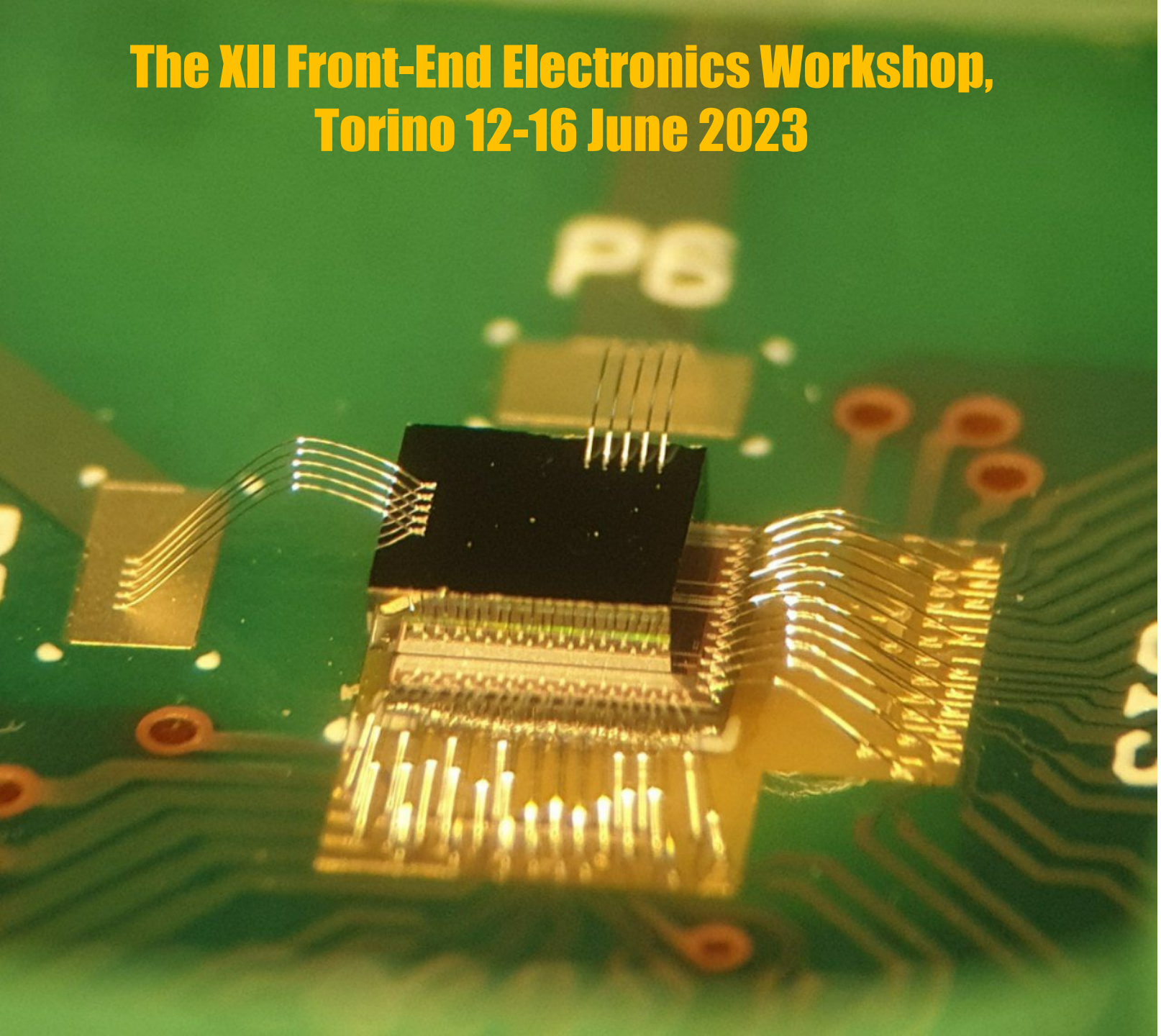


The XII Front-End Electronics Workshop,
Torino 12-16 June 2023

The TimeSPOT pixel front-end IC in 28-nm CMOS

Adriano Lai
INFN Cagliari

INFN
Istituto Nazionale di Fisica Nucleare

TimeSPOT
TIME and SPace real-time Operating Tracker

IGNITEd
INFN Ground-up iNITiative for µElectronics Developments

Requirements (and challenges) for 4D-Tracking

1. Space Resolution $\sigma_s \approx 10$ µm (→ pixel pitch ≈ 40–60 µm)
2. Time Resolution $\sigma_t \leq 50$ ps on the full chain ($\sigma_t = \sigma_{sensor} \oplus \sigma_{FE} \oplus \sigma_{TDC}$). Safety margin: ≈ 30-40 ps before irradiation (?)
3. Radiation hardness to high fluences (for sensors) and high doses (for electronics). Fluences $\Phi = 10^{16} \div 10^{17}$ 1 MeV n_{eq}/cm^2 and Doses > 1 ÷ 2 Grad
4. The material budget per layer must be kept below 1 ÷ 0.5 % radiation length
5. A detection efficiency of ε > 99% per layer is tipically required (high fill factor)
6. Huge data bandwidth > 100 Gbps per ASIC

Design in CMOS 28nm appears as a mandatory path, due to its superior integration capabilities and radiation resistance (≥ 1 Grad). ***BUT we have serious technology/operational limitations, especially against timing performance:***

a. High time resolution @ limited power budget ≈ 10 µW/pixel
b. Limited headroom for supply (0.9 V)
c. Limited intrinsic MOST g_m (with respect to SiGe Bipolar, for example)
d. Significative IR drop (issues in global design aspects)

source:
Considerations for the VELO detector at the LHCb upgrade II – CERN-LHCb-2022-001

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Lifetime fluence [1×10^{16} 1 MeV n_{eq}/cm^2]	> 6	> 1
TID lifetime [MGy]	> 28	> 5
Sensor Timestamp per hit [ps]	≤ 35 *	≤ 35
ASIC Timestamp per hit [ps]	≤ 35 *	≤ 35
Hit Efficiency [%]	≥ 99	≥ 99
Power per pixel [µW]	≤ 23	≤ 14
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94
Material budget	≤ 0.8% X_0 per station (all included)	

*Corresponds to < 50 ps on sensor+electronics

TimeSPOT ASIC developments

*Purpose and scope: the **high-intensity-4D** challenge*

TimeSPOT
TIME and SPace real-time Operating Tracker

1. Explore the capabilities and technical pitfalls of CMOS 28-nm, which has been chosen as the successor of 65 nm for future HEP developments
2. **Concentrate first on pixel performance** by addressing the questions:
   - What can be integrated in a pixel ≈ 50x50 μm^2 ?
   - Refererred to a target $\sigma_t \approx 30$ ps ($\sigma_{FE} \oplus \sigma_{TDC}$), what is the minimum power required ?
   - What is the maximum sustainable rate/pixel – or – is it possible to integrate 1 TDC per pixel?
   - What would be the best TDC resolution and its power consumption?
3. **Design and produce the largest possible chip, compatibly with time and money budget (32x32 pixels was the choice)**
4. Drop for now the requirement about high data bandwidth, which will surely need specific additional developments (as Silicon Photonics)

2 submissions made: Timespot0 (single test-cells)
Timespot1 (complete matrix)

Timespot1 ASIC

28-nm CMOS

- **Reduced size (1024 pixels, 6 mm²)**
- **HPC flavour**
- **Complete set of functionalities for pixel readout**
- **Slow read-out (demo-test purpose)**
- **No SEE protection**

640 MHz master clock

Digital row: 16x2 TDC
+ Controls, Conf. registers, I²C I/F

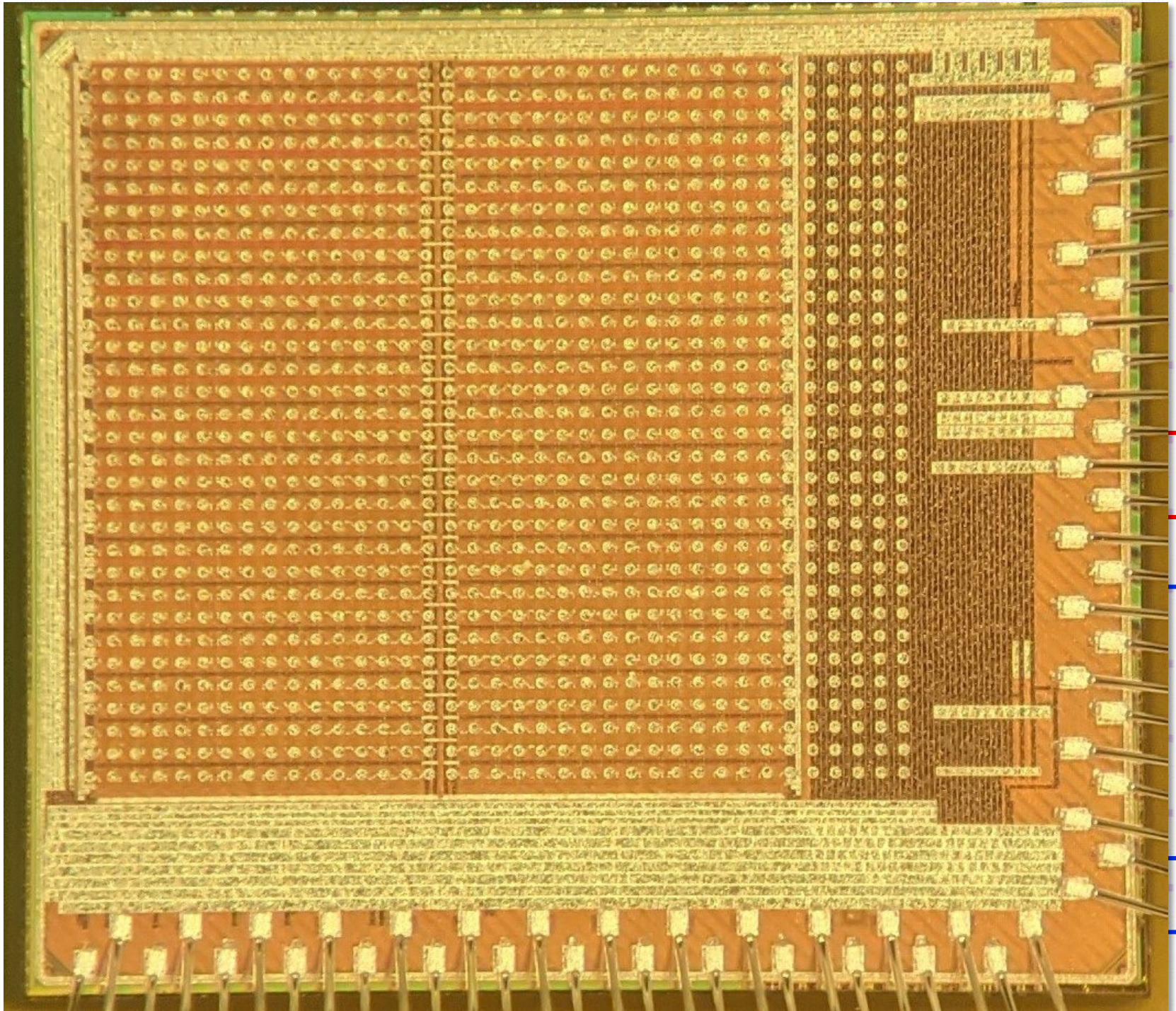
Analog row (16x2 AFE)

Analog (service) column.
Each contains:

- 1 Band-Gap circuit
- 5x Σ–Δ DACs (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

4x Read Out Trees

8x LVDS driver
(each @1.28 Gbps)



Timespot1 ASIC

28-nm CMOS

- **Reduced size (1024 pixels, 6 mm²)**
- **HPC flavour**
- **Complete set of functionalities for pixel readout**
- **Slow read-out (demo-test purpose)**
- **No SEE protection**

640 MHz master clock

Digital row: 16x2 TDC
+ Controls, Conf. registers, I²C I/F

Analog row (16x2 AFE)

Analog (service) column.
Each contains:

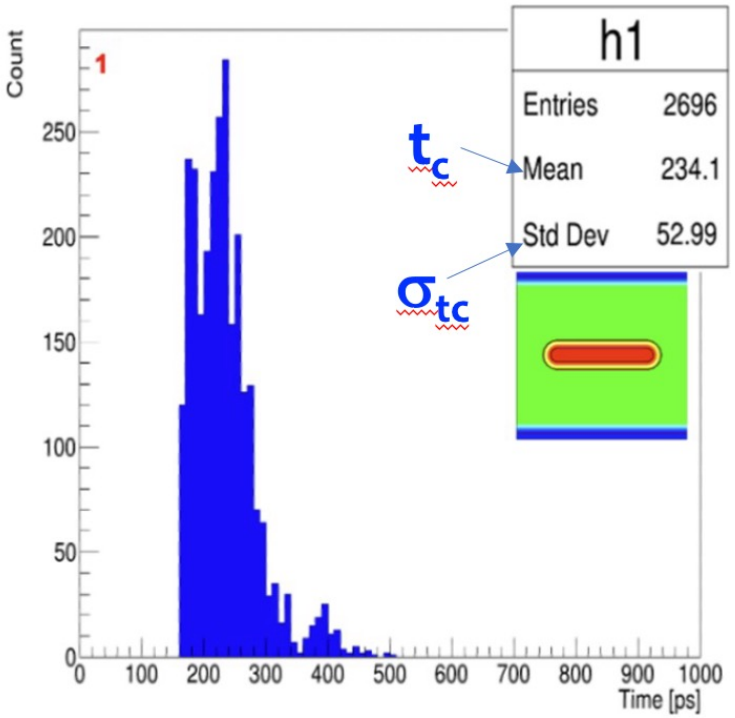
- 1 Band-Gap circuit
- 5x Σ–Δ DACs (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

4x Read Out Trees

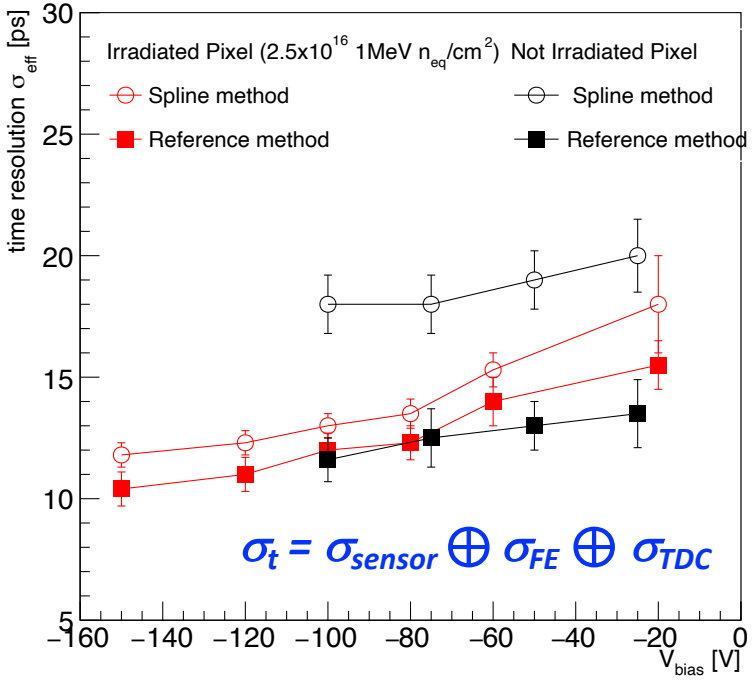
8x LVDS driver
(each @1.28 Gbps)

4D-pixel performance
and related electronics

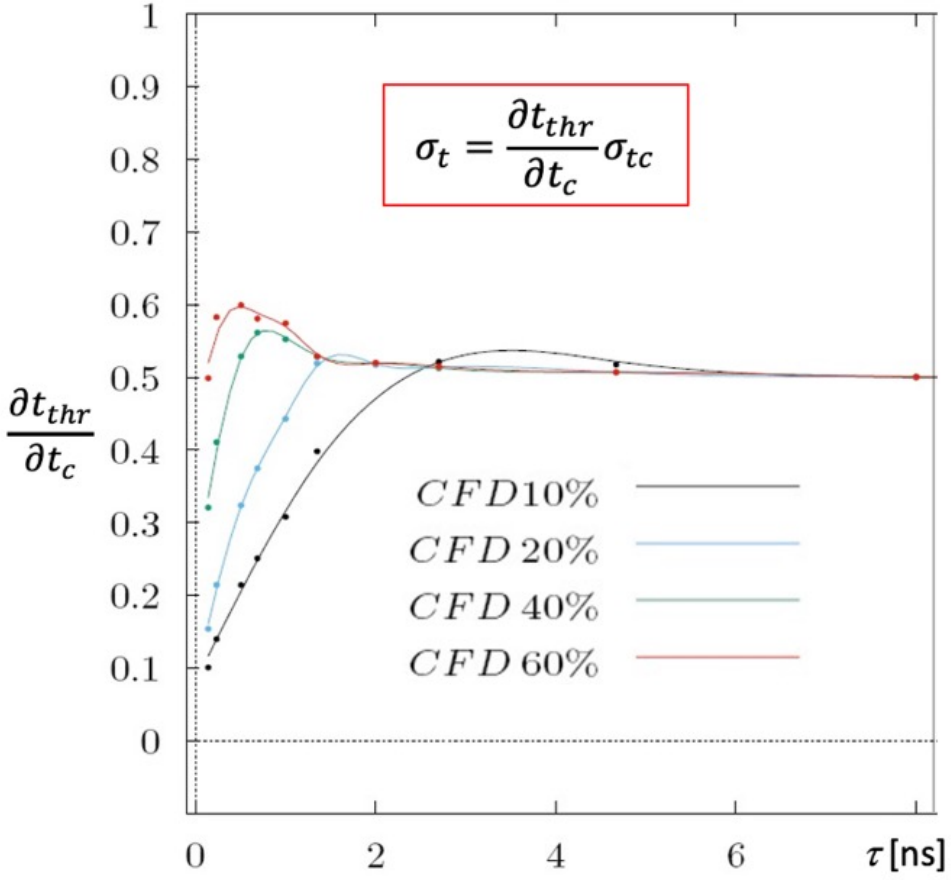
G. M. Cossu and A. Lai, " *Front-end Electronics for Timing with pico-seconds precision using Solid State Sensors*", JINST,vol. 18, 2023
A.Lai and G. M. Cossu, "*High-resolution timing electronics for fast pixel sensors*", arXiv2008.09867, 2020
W. Riegler and G. A. Rinella, "Time resolution of silicon pixel sensors," JINST,vol. 12, 2017



Charge Collection Time of 3D-trench pixel



Timing performance with HBT (Si-Ge) and trans-impedance amplifier stages (high BW, high power)



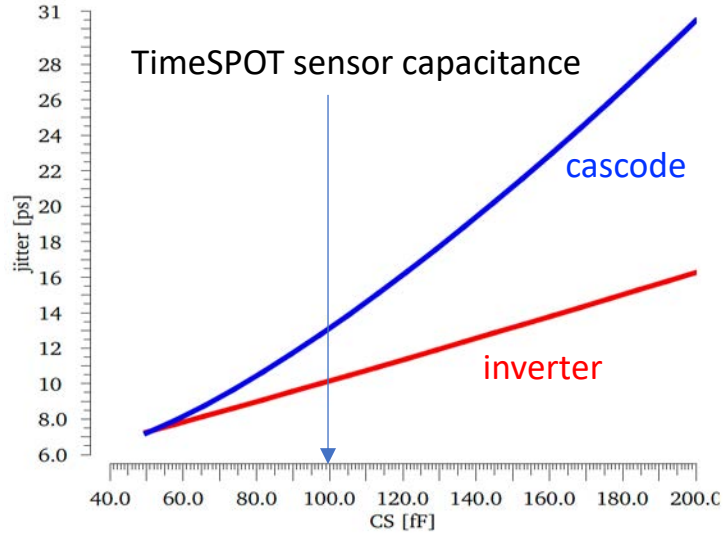
Time resolution vs std. dev. of CCT distribution
Fraction of rms is ½ for "slow" electronics (CSA)

With TimeSPOT sensors, 20-25 ps of resolution are theoretically feasible also with the CSA approach

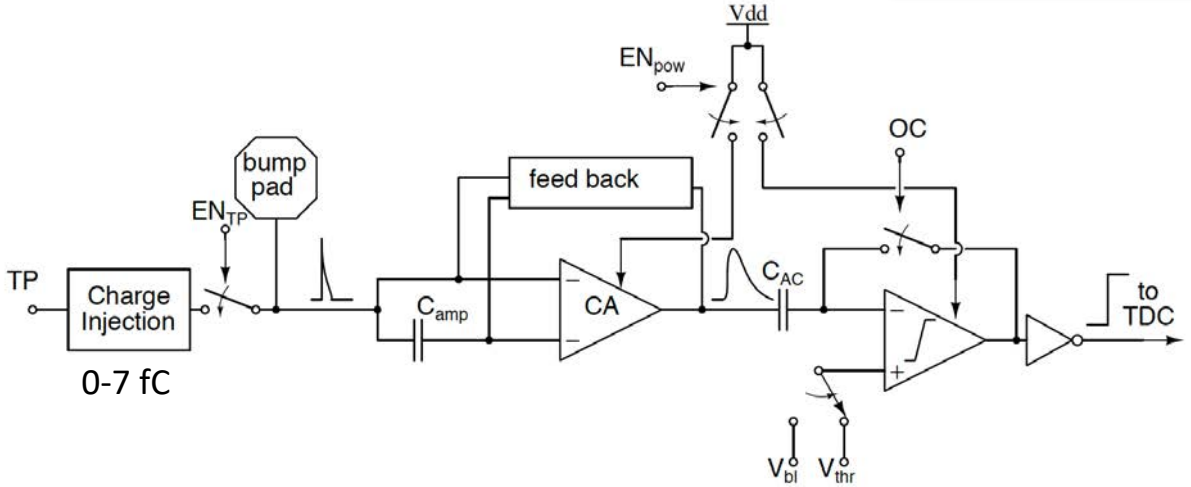
Timespot1: Analog Front End

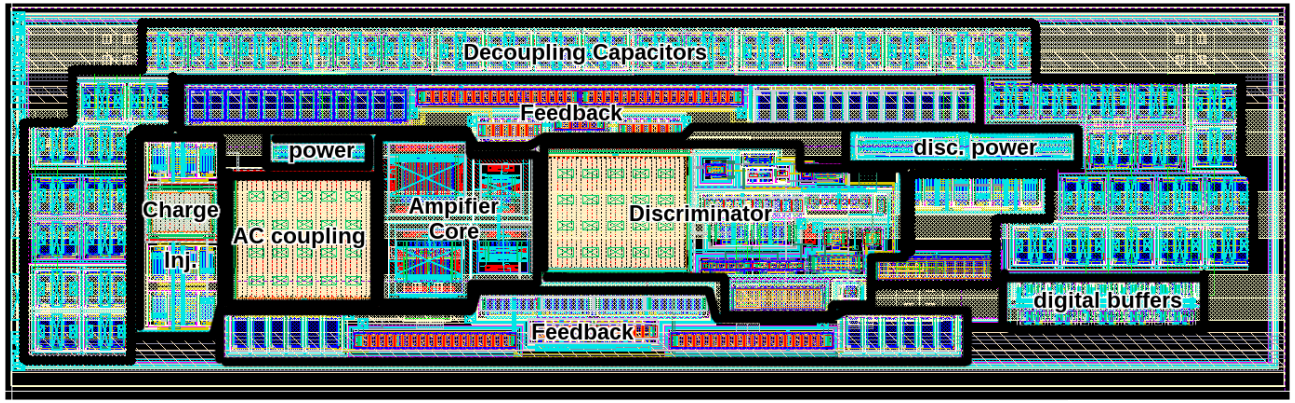
Inverter core amplifier with double Krummenacher FB

- **Charge Sensitive Amplifier (CSA) with DC current compensation (2 Krummenacher filter paths N,P) and constant current discharge**
- **Leading Edge Discriminator (LED) with Discrete-time Offset-Compensation (OC) for threshold uniformity. OC procedure: 250 ns every ≤800 µs**
- **Cascoded inverter used as core amplifier instead of classical telescopic cascode: almost doubles g_m and OLG**
- **Higher g_m: higher slew rate, less capacitance sensitivity of time jitter**



Post-layout simulations





50x15 µm²

Expected from post-layout simulations:

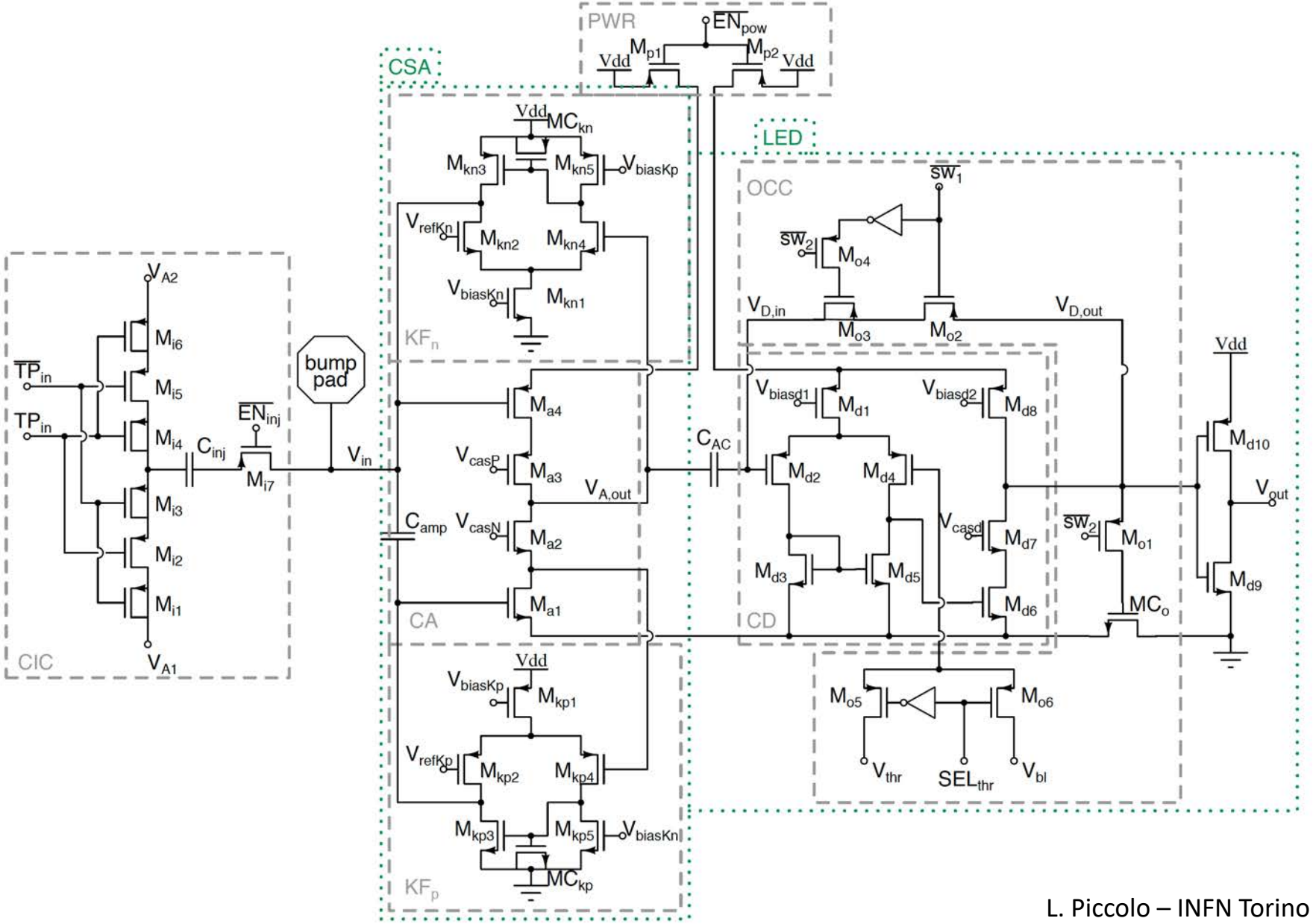
15-20 ps jitter (CSA + LED)

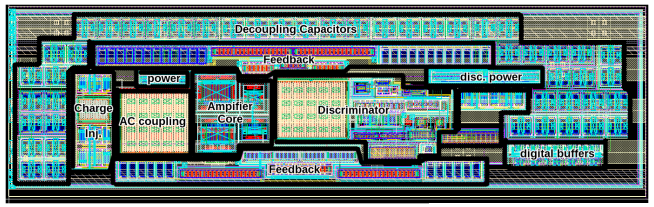
12 µW – programmable from 2.3 µW to 32 µW

(Individual channels can be powered off)

L. Piccolo – INFN Torino

Timespot1 ASIC: transistor level Analog Front End





50x15 µm²

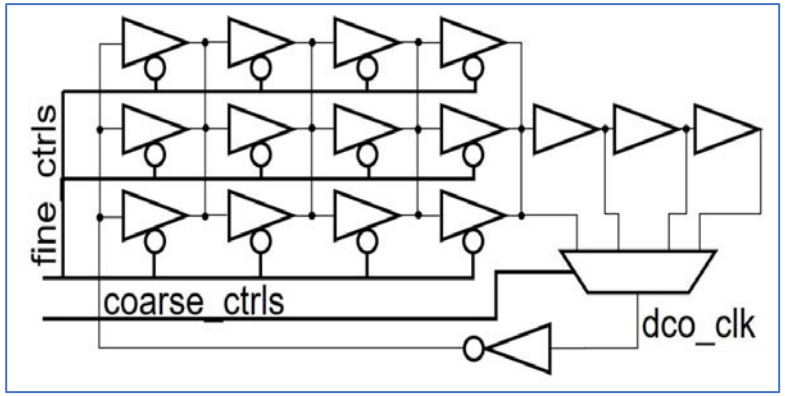
L. Piccolo – INFN Torino

Timespot1: TDC

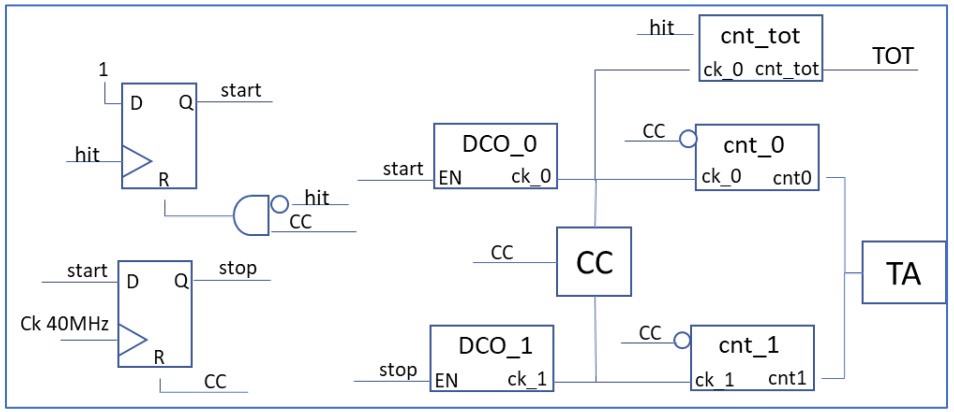
Fully digital design, standard-cell based, Vernier scheme

To maximize sustainable rate, **1 TDC per pixel channel** has been integrated

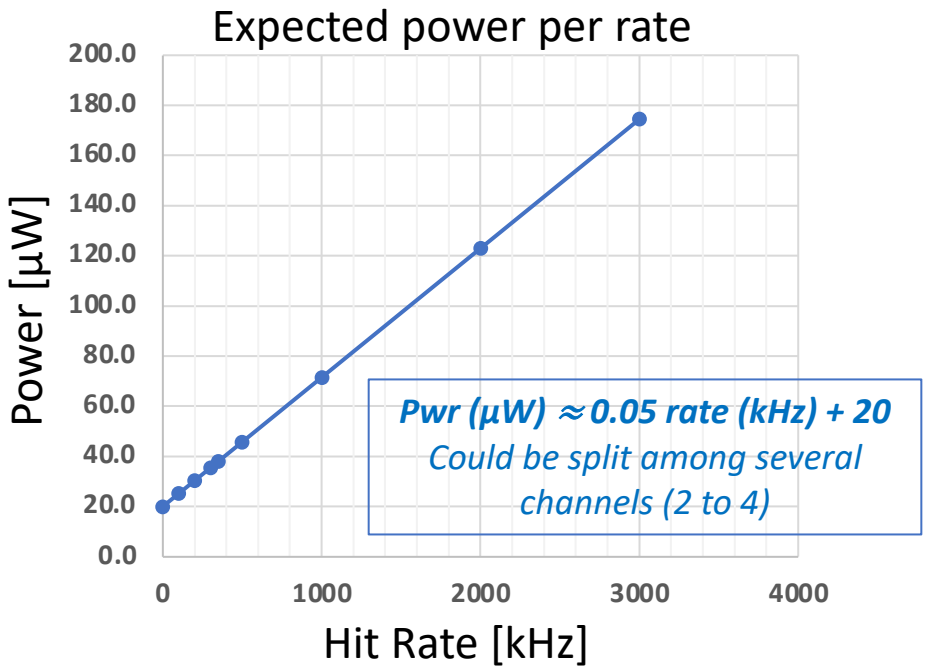
Max input rate = 3 MHz
23 bits output word
(ToA + ToT)
ToT resolution ≈ 1 ns

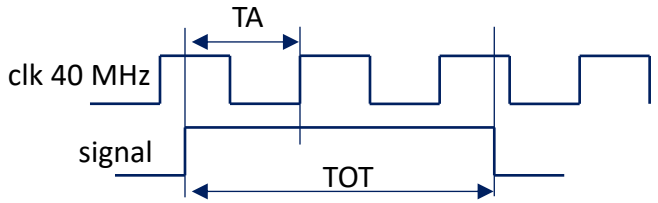


DCO scheme

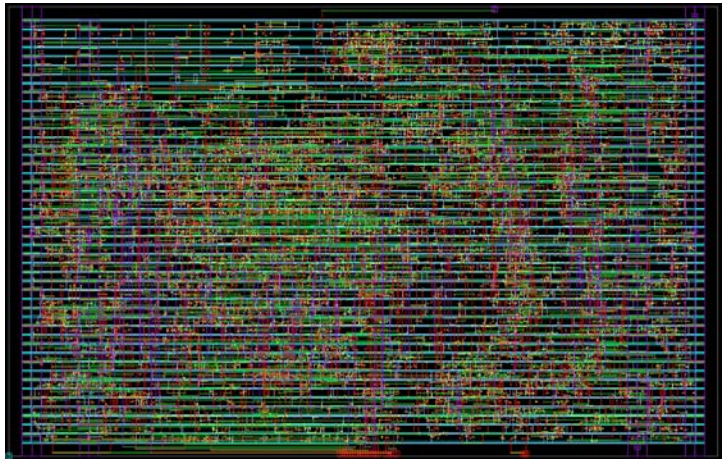


High resolution, "low" consumption TDC based on 2 DCOs and a Vernier architecture





The TDC gives the phase of the signal wrt the 40MHz BX clock
4 levels of Vernier precision (Δf in DCOs) can be programmed.
Typical LSB from simulations = 12 ps

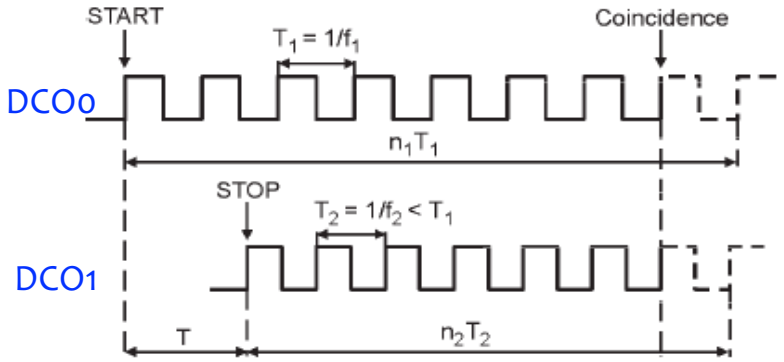


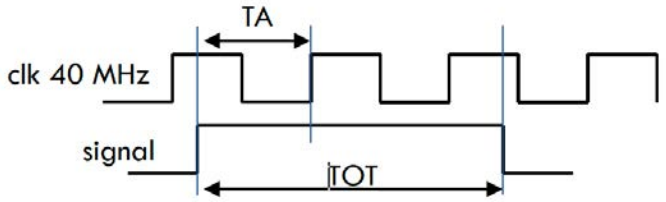
50x32 µm²

S. Cadeddu – INFN Cagliari

Timespot1: TDC (2)

Circuit operations and criticalities





$$TA = (cnt_1 - 1)T_1 - (cnt_2 - 1)T_2$$

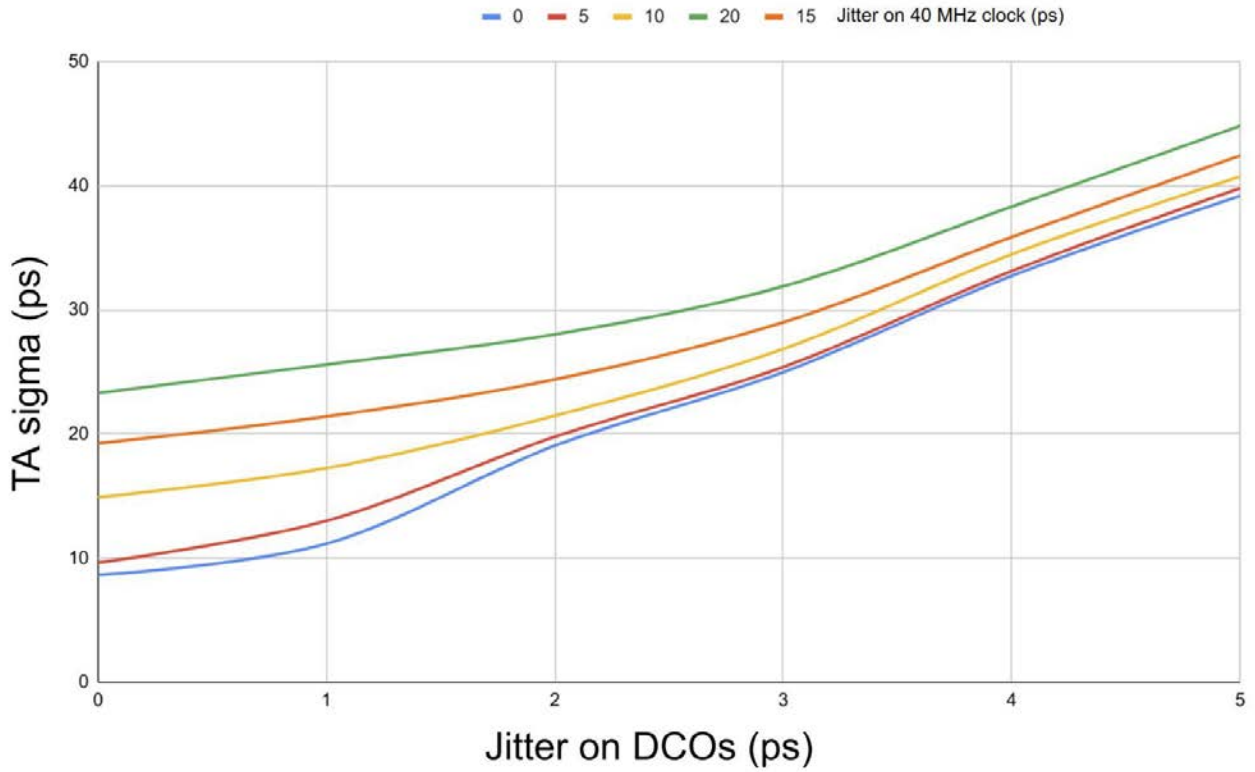
$$T_{conv\_max} = \frac{T_1 \cdot T_2}{r(10ps)} \approx 100\ ns$$

Set LSB

$$T_{conv\_max} = \frac{T_1 \cdot T_2}{r(30ps)} \approx 35\ ns$$

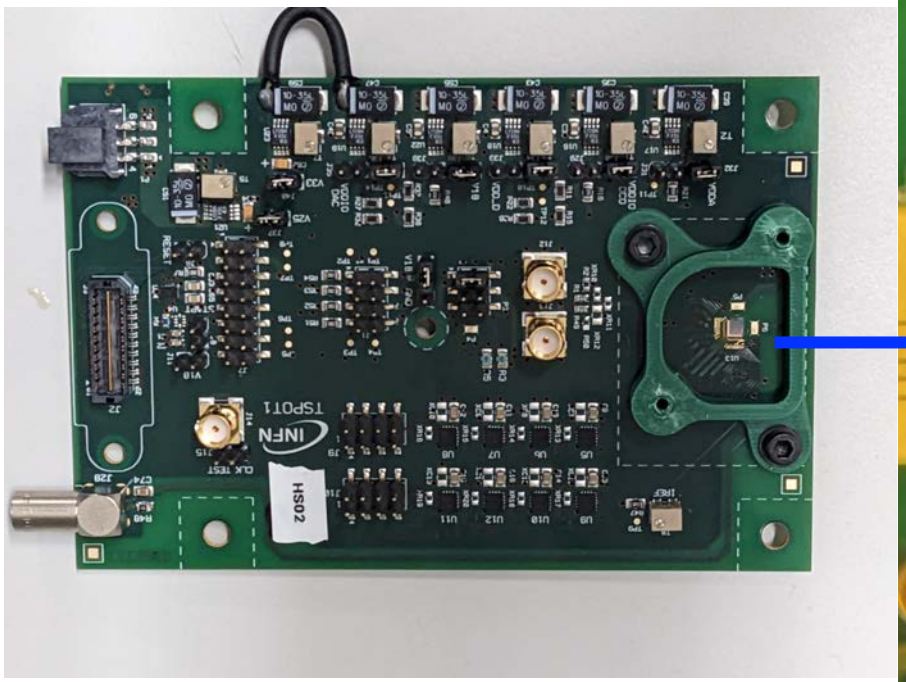
- TDC requirements:
  - Time of Arrival (TA): 30ps rms overall
  - Less than 15ps each controbution (Det. – AFE –TDC)
  - TDC LSB < 50ps
  - Time Over Threshold: LSB around 1ns or less
  - Max TOT < 200ns
- Vernier Architecture DCOs Frequency: ~ 1GHz
- DCO's is switched off after measurements
- The resolution does not depend on the periods but on their difference Δf
- Max conversion time depends on DCO Periods: Larger periods mean larger conversion time

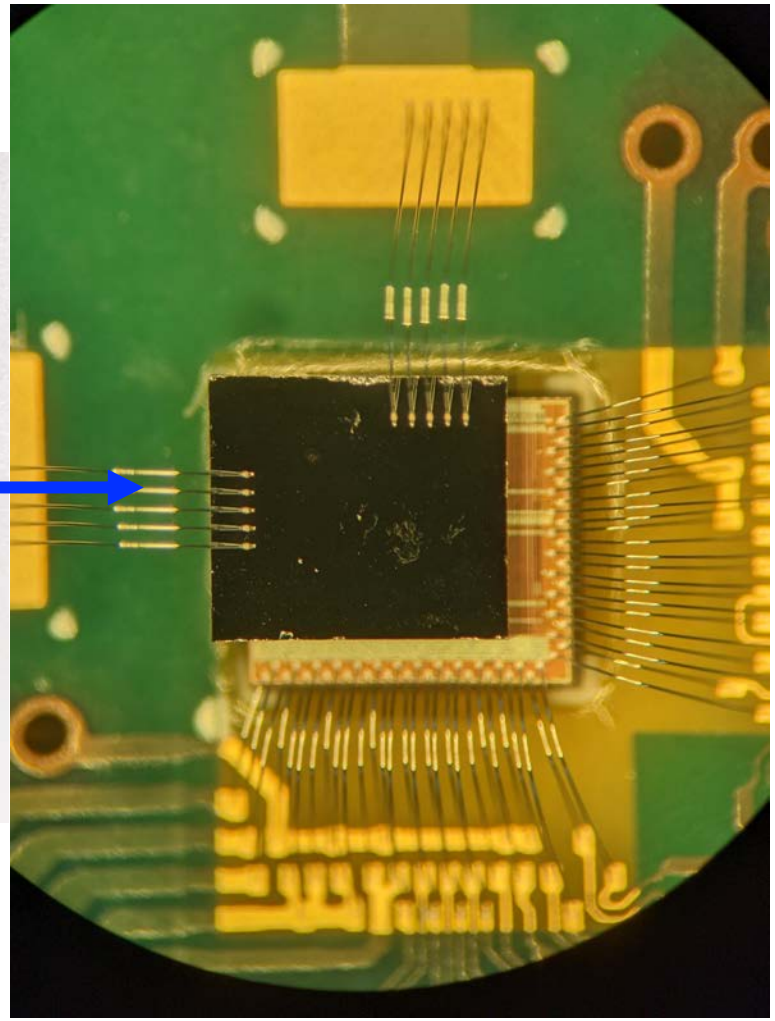
The final TDC resolution depends on the jitters of the 40 MHz clock and of the DCO



(not)hybridized devices

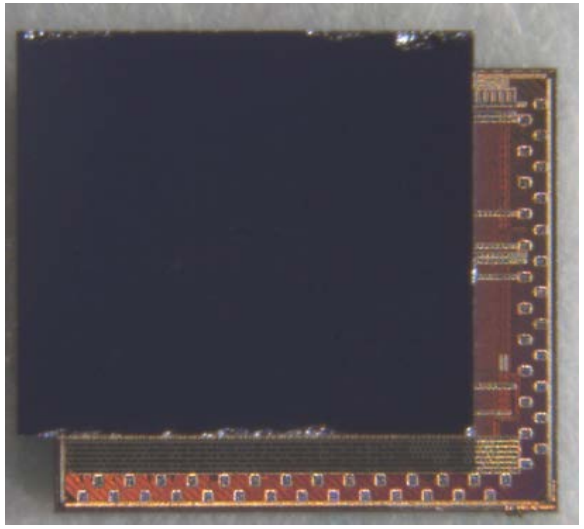
same test PCB



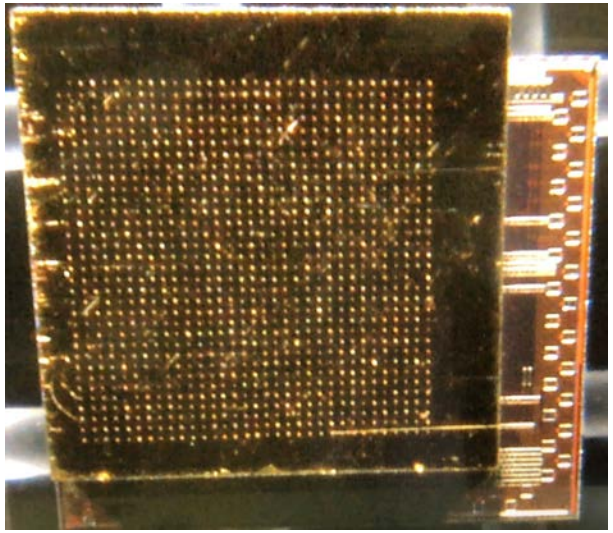


The test-bench PCB
(named TSPOT1)
operates also as a tracking station in the
demonstrator (test beam at SPS)

Timespot1 on 3D-trench silicon matrix



Timespot1 on 3D-column diamond matrix

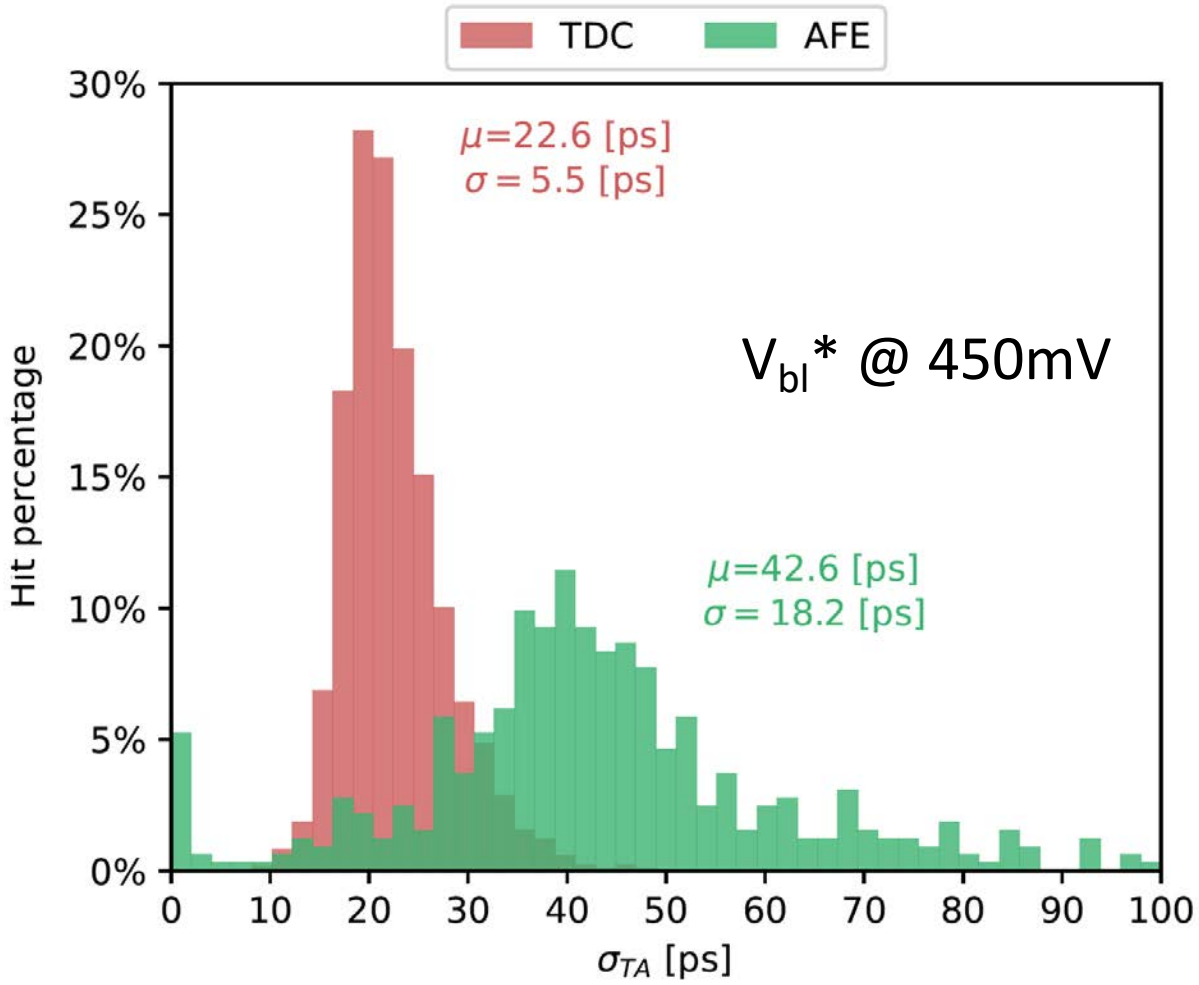


Fraunhofer IZM

Pixel characterization

Time resolution (no sensor)

- The **TDC** has a typical $\sigma_t \approx$ **20 ps**, with a dispersion around 5 ps. No improvements are visible when increasing the Vernier precision (DCO jitter limit?)
- The AFE σ_t **is intrinsically better than 20 ps** but an identified **bug** in the Offset Compensation of the LED spoils σ_t in most of the channels (see next slide).
- In general, issues which are extrinsic to circuit design limit the very good resolution at the pixel level (clock distribution, OC bug). The pixel circuit **design appears adequate** to system requirements.
- **Keeping uniformity under control across the ASIC area is particularly critical for timing performance in this technology**

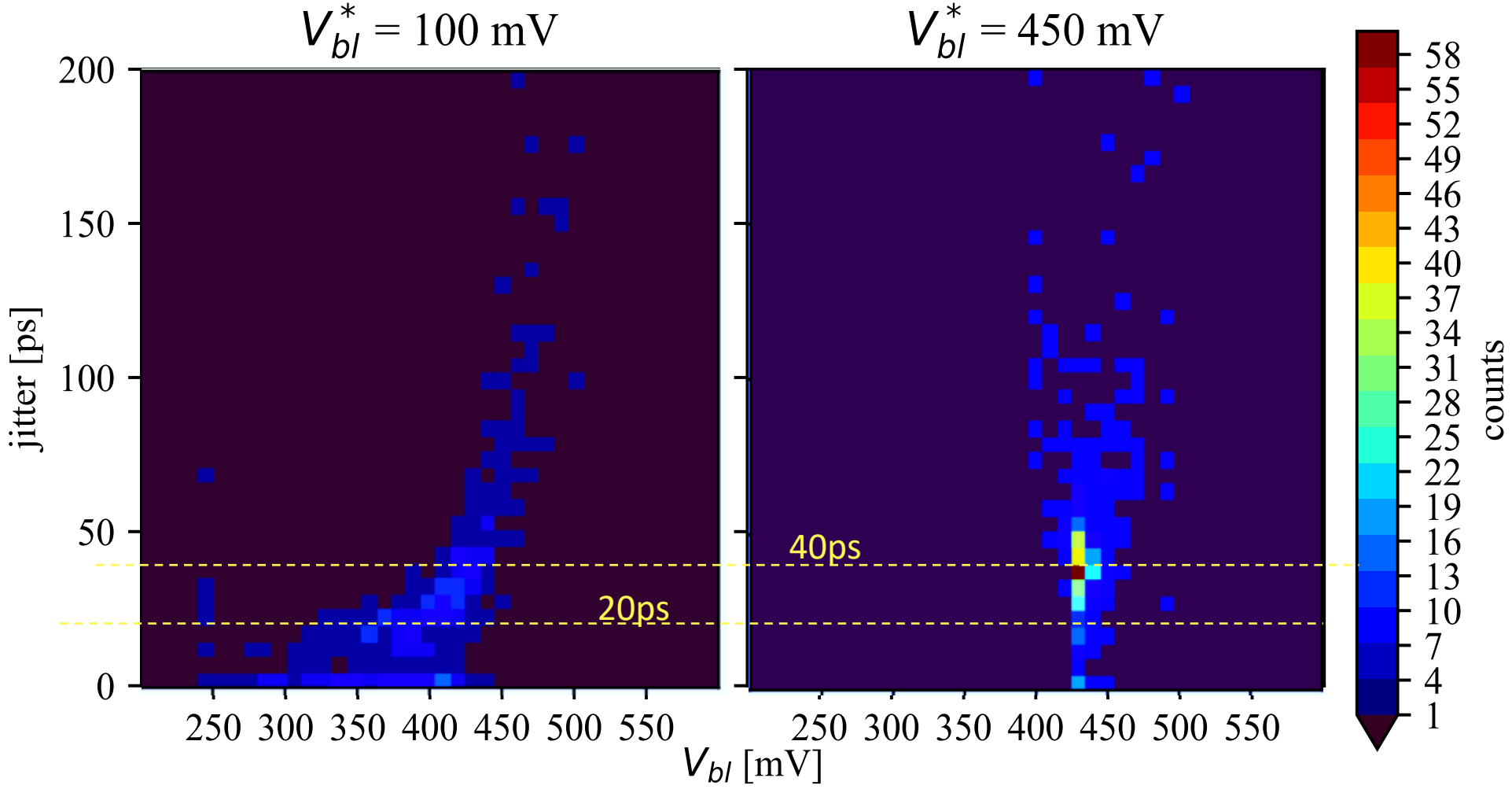


V_{bl}* @ 450mV

@ 12 µW on AFE

Pixel: the Analog Front End

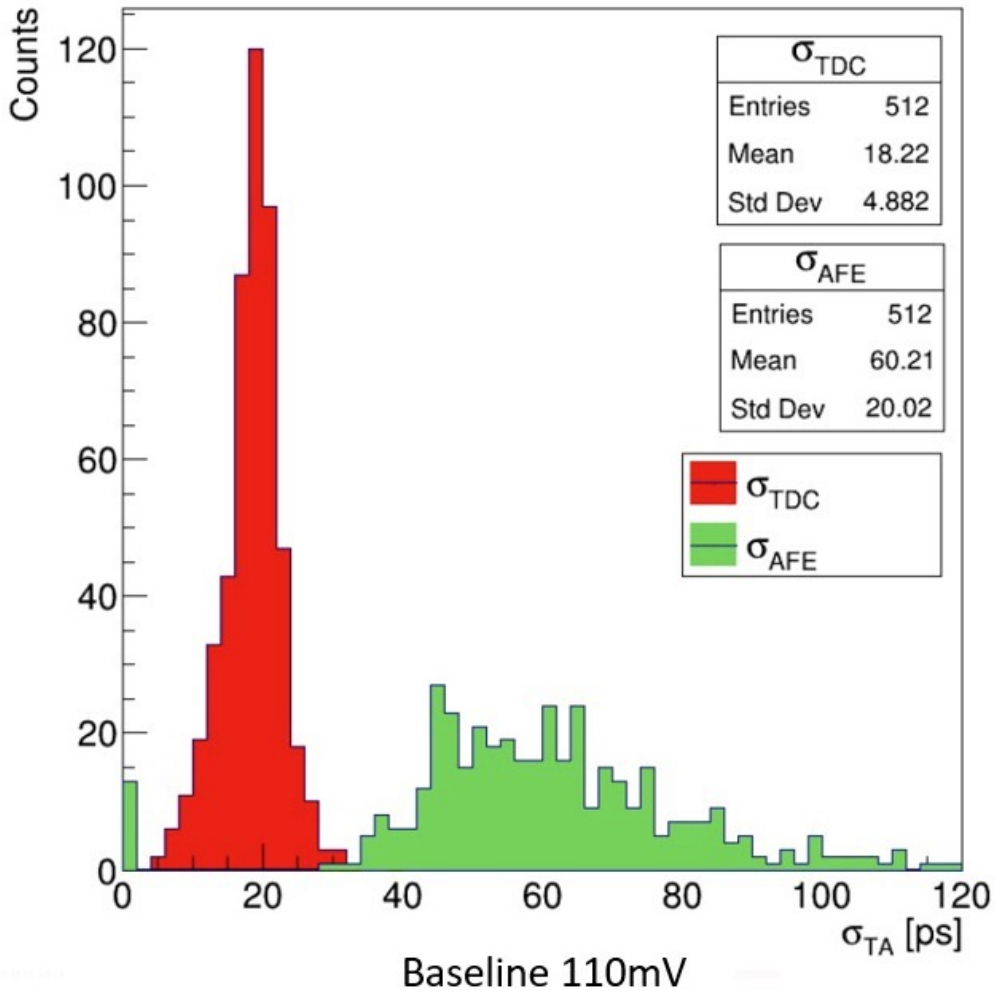
inadequate Offset Compensation

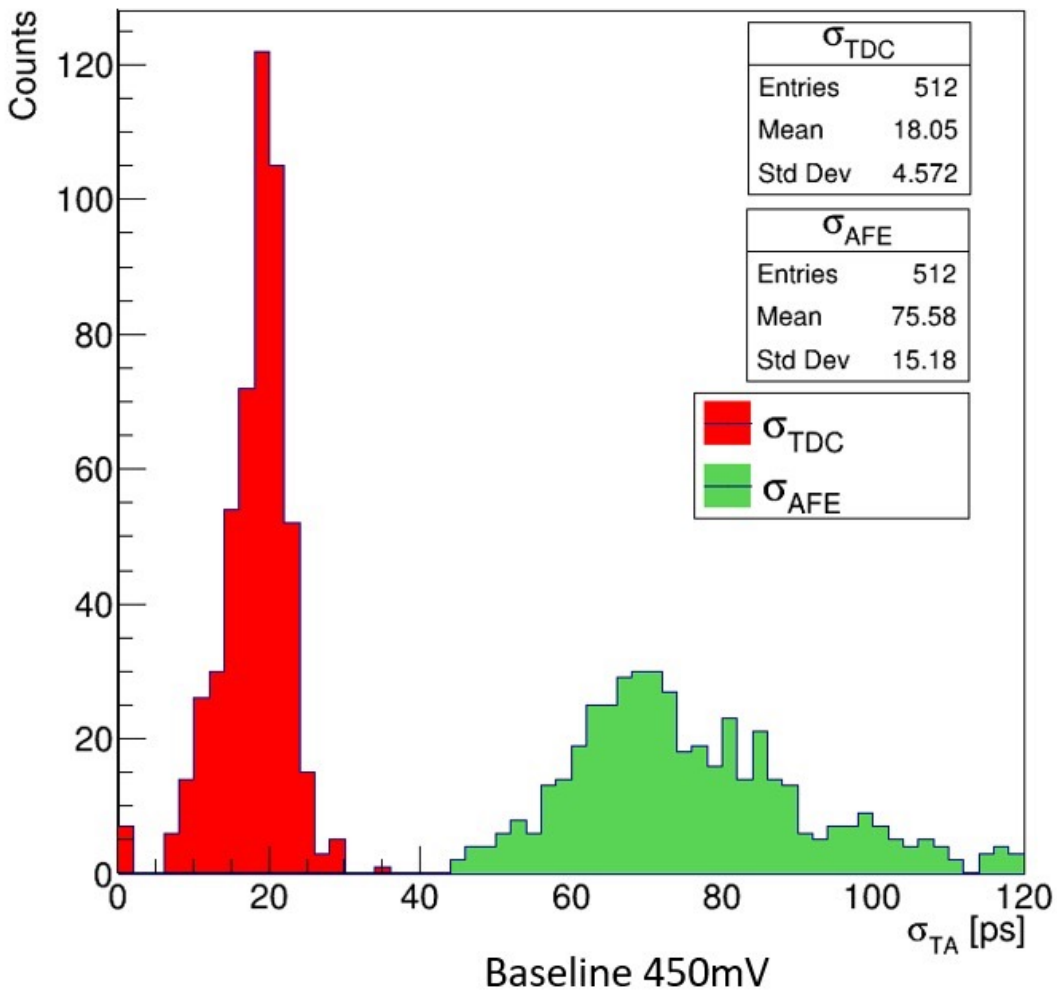


- When V_{bl} is set at low values, in most of the channels, the OC circuit fails to charge the memory capacitance C_{OC} .
- The discriminator is forced to work at high voltages, where it is band-limited
- The timing performance is heavily degraded

Hybridized devices

time resolution (2 fC pulses) – 2

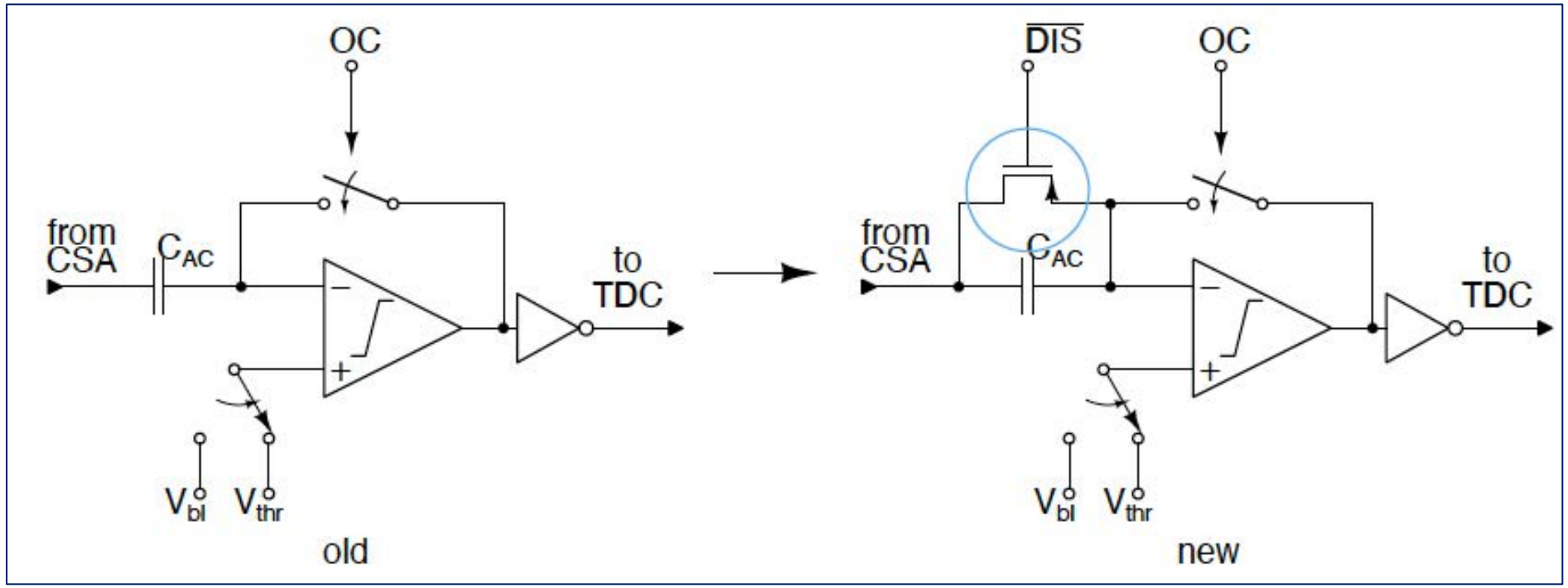




Consistent behaviour with worsening of timing performance (C_{in})

A remedy

to the inadequate Offset Compensation

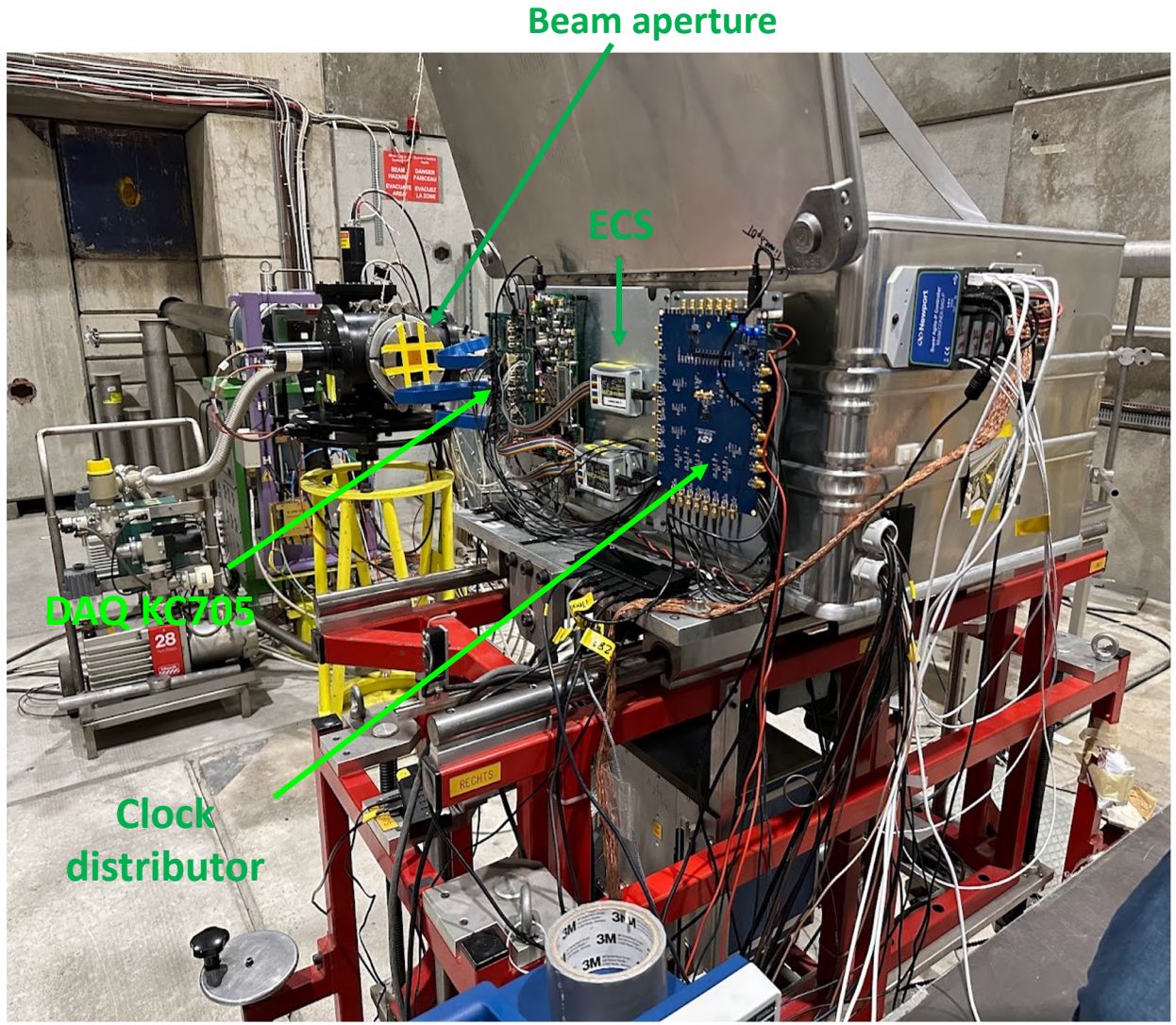


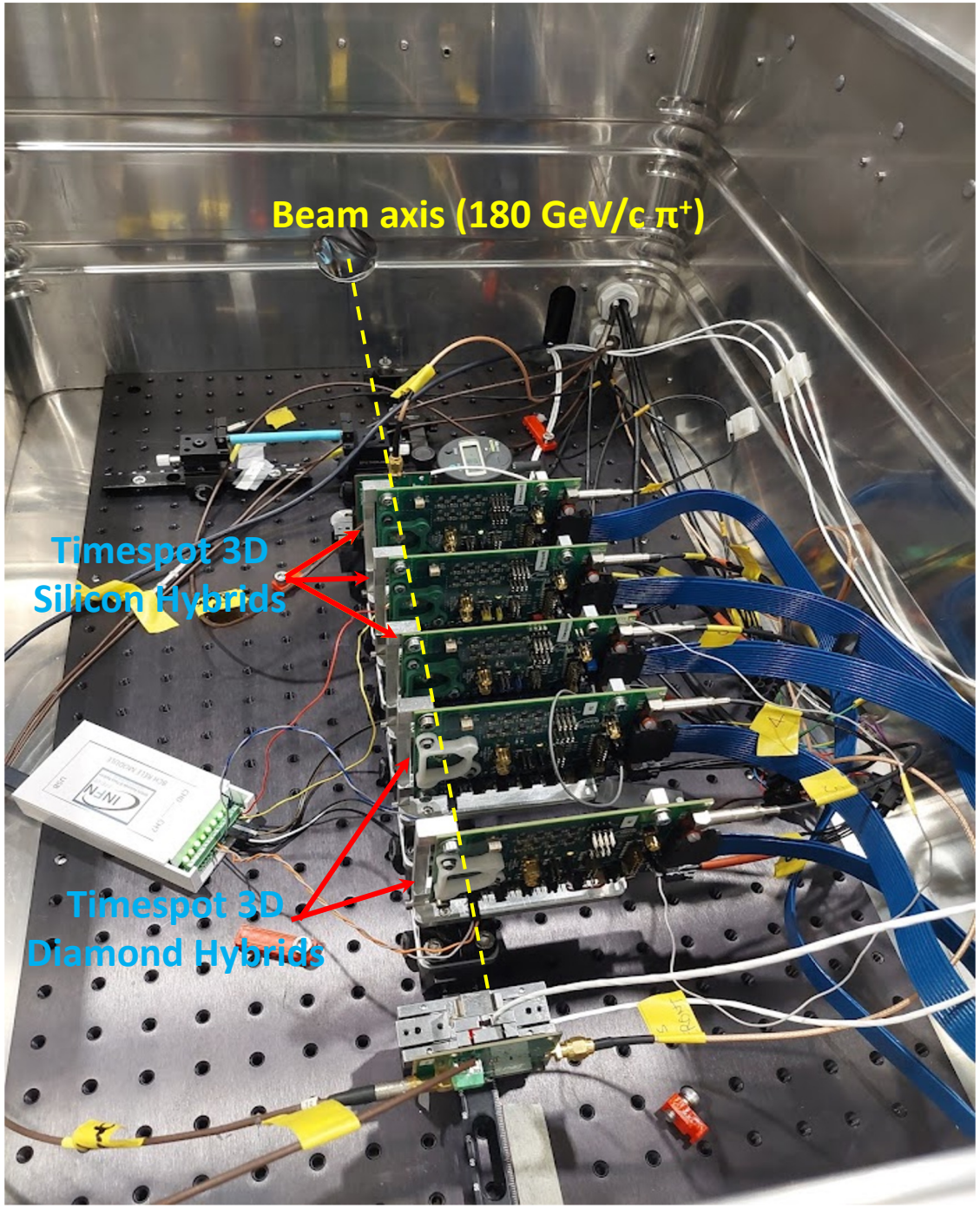
- Add a reset to force C_{AC} discharge
- Make the threshold setting switches CMOS (they were changed to PMOS for increasing ad-hardness)
- Use larger transistors to limit the post irradiation off-current.
- **More radically: switch to settable individual thresholds (DACs)**

L. Piccolo INFN Torino

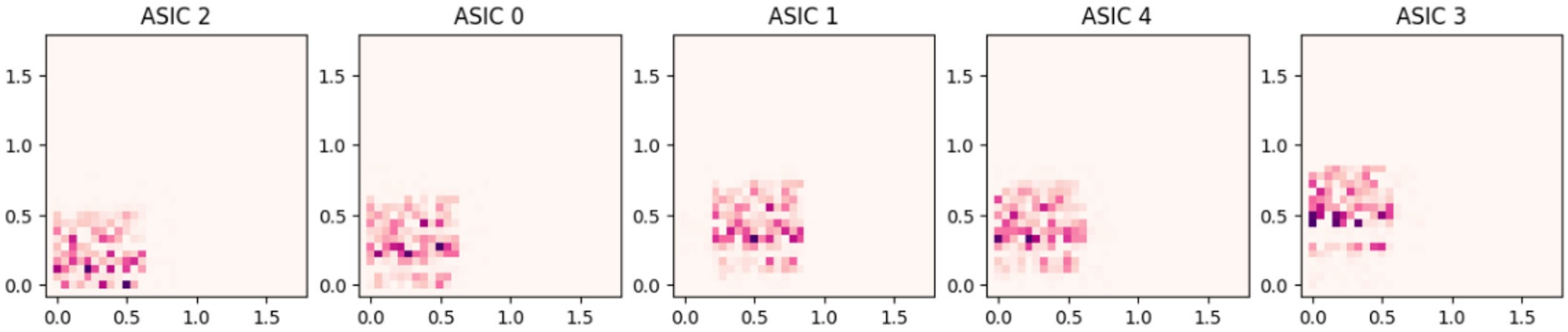
TEST beam @SPS, May 2023

A tracker demonstrator (5 stations)





Preliminary results from the TimeSPOT telescope tests



track hits from the 5 stations

1. **First ever tracks with a 28-nm based system** were acquired and reconstructed.
2. The space-tracking was satisfactory. **Tracking efficiency was as expected** (≈ 80% of geometrical efficiency, see L. Anderlini's talk @FAST May 2023, *Recent results on 3D diamond pixel detectors for 4D-tracking*)
3. Several aspects related to **system operation** have been explored and **better understood**. They give extremely **useful suggestions** for the next ASIC developments
4. The tests have been **dominated by system issues**:
   - The silicon hybrids were not biased properly, due to high leakage current in the sensor matrix, probably due to un-bonded pixels
   - The ASIC matrix was not fully operated, as this caused instabilities in DAQ. Only ¼ of the matrix was switched on
   - A circuit metastability bug on the TDCs was identified, causing them to stuck often (need of global reset to restart)
5. **First-sight results on timing performance appear much poorer than expected (≈ 200 ps). Detailed analysis is in progress.**

Lessons learned, conclusions and perspectives

- The **TimeSPOT ASIC** has been only a **first step** on the hard climb of high intensity 4D-tracking. Many things have been understood and many issues are still to be solved
- At the pixel level, we found **good circuit solutions** both for AFE and TDC, which will be basically confirmed (with some improvements) in the next version of the ASIC. A few bugs were identified and already corrected at the design level.
- In the next design we will tendentially **simplify** front-end circuits as much as possible (our «zen principle»). Complexity is a nest for bugs. A single high-resolution circuit is a radically different task than a **high resolution system made of million of channels working together**.
- A high-intensity complex test @SPS was important to further **stress the devices** and reveal specific issues to care about
- Internal and external timing and in general **global routing** (both power and clock) was not completely under control in the Timespot1. These are extremely delicate aspects which will considerably **worsen on larger size devices**. Verification techniques are decisive for the success of such designs and mandatory on nominal-size ASICs.
- A new ASIC is in preparation, where the architecture will be drastically changed, and the **global organization «localized»** by means of vertical interconnections (**TSV**), ***but this is matter for a different talk.***