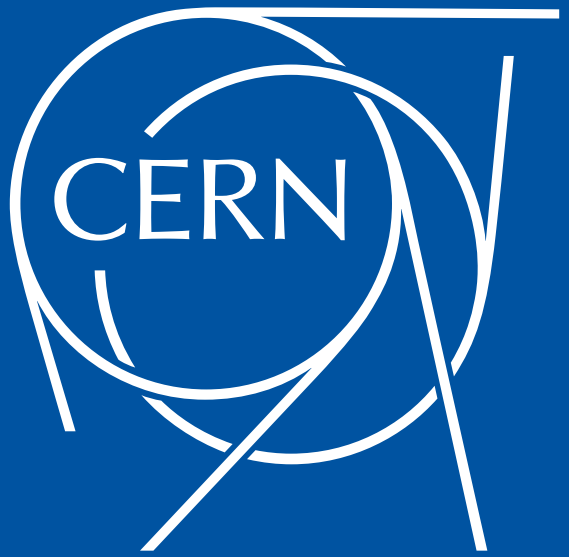
CERN

Analog IP Blocks in 28nm CMOS for the High Energy Physics Community

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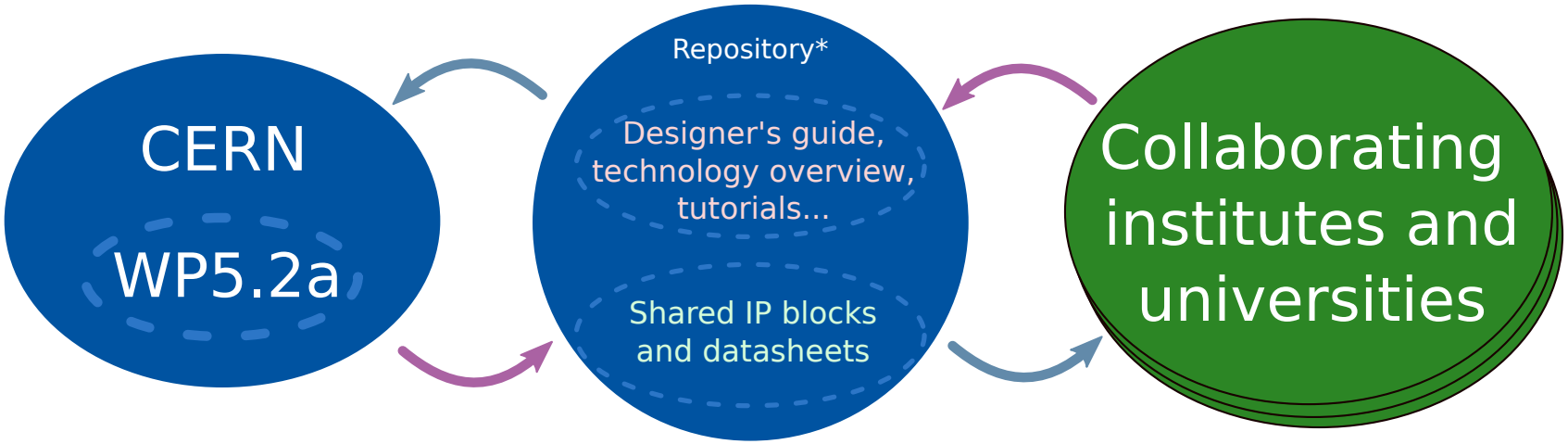
Why IP blocks in 28nm for HEP Community?

This technology is a strong node and will be available in the long term (as 130 nm and 65 nm).



Intellectual Property (IP) blocks design

Intellectual Property (IP) blocks use

IP block example: DAC, ADC, voltage reference, transmitter, receiver, PLL...

*thanks to CERN ASIC Support Team: A. Caratelli and M. Andorno

Challenges

Challenges from the technology:

- Low Vdd reduces voltage headroom for analog design (threshold does not scale down).
- DRC rules are very strict:
  - Only vertical poly is allowed (enclosed layout is not possible).
  - Density rules are tough (diffusion, poly, metals...).
  - Dummy filling is required quite early.
- Lot of corners, high mismatch, layout dependent effects...

Challenges as a part of a community:

- Communication is important: silicon dimension=90 % drawn dimension.
- Shared IP block should be compatible among them:
  - Several transistor flavours and metal stacks.

Challenges from the specifications:

- A TID up to 1 Grad on 10 years lifetime for the future upgrades of LHC.

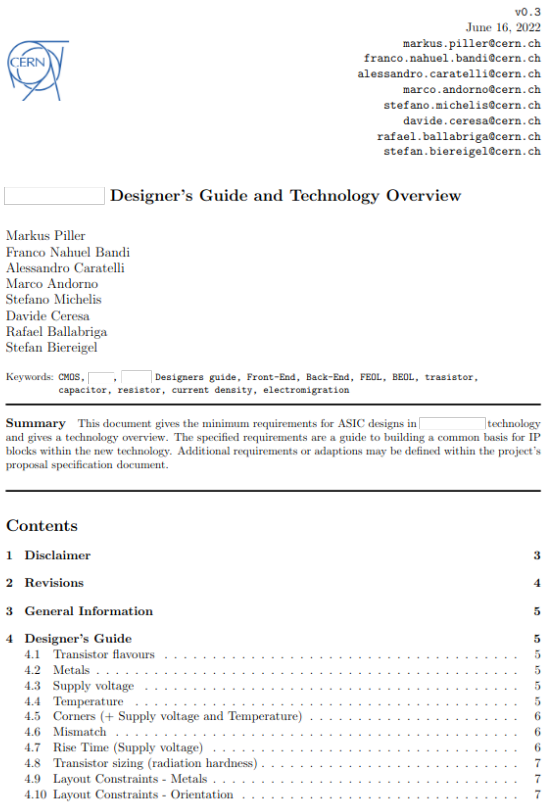
Documentation

Analog IP Blocks

Summary

Motivation

- Familiarize new designers with the technology (short document with practical information)[1].
- These documents DO NOT substitute the foundry documentation.
- We propose guidelines to homogenize choices and enable block sharing.



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Designer's Guide and Technology Overview

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Keywords: CMOS, , Designers guide, Front-End, Back-End, FEOL, BEOL, trasistor, capacitor, resistor, current density, electromigration

Summary This document gives the minimum requirements for ASIC designs in technology and gives a technology overview. The specified requirements are a guide to building a common basis for IP blocks within the new technology. Additional requirements or adaptions may be defined within the project's proposal specification document.

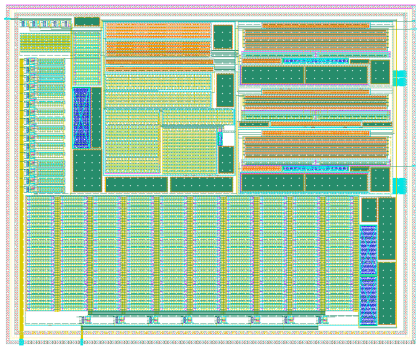
Contents

[1]The documentation is available (thanks to CERN ASIC Support Team: A. Caratelli and M. Andorno):

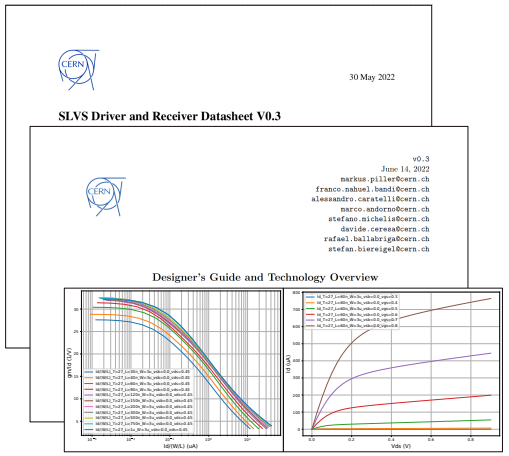
- Web page: https://asicsupport.web.cern.ch/
- Forum: https://asicsupport-community.web.cern.ch/

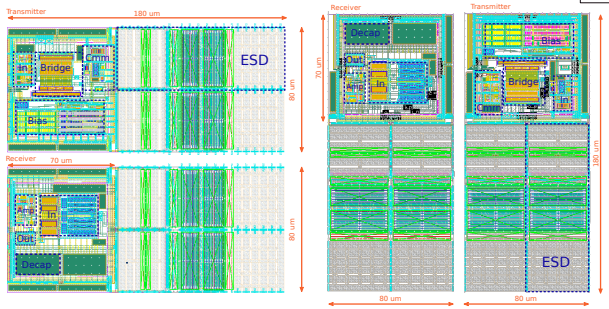
Designers Guide, Technology Overview, Datasheets...

- We have prepared the document with selected technical information and proposed design guidelines that facilitate collaborative design work.
- It is based on the foundry design manual, personal experience and experimental data.
- Several people have contributed to improve and expand the content of the document.

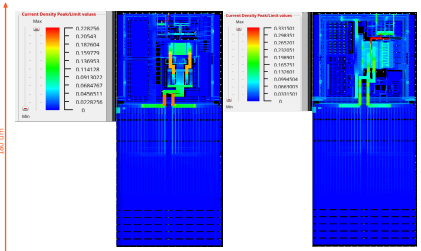


8-bit DAC layout (M. Piller)





Transmitter and receiver layout



Electromigration analysis

Documentation

Analog IP Blocks

Summary

IP Block Library (Design Finished)

Circuits to share	Notes
Bandgap voltage reference and temperature monitor	Block submitted in January 2022. Development lead by **G. Traversi (Bergamo/Pavia) collaboration with the INFN Falaphel project** with support from CERN engineers.
Digital to Analog Converter (8-bit)	Core block submitted in January 2022. Development lead by M. Piller.
SLVS driver and receiver	Block submitted in January 2022. Development lead by F. Bandi
Fast Rail to Rail Operational Amplifier	Completed. To be submitted in Sept. 2023. Development lead by J. Kaplon
Radiation tolerant ESD protections	Design outsorced to Sofics.
CMOS IO pads	Design outsorced to Sofics.

Design followed guidelines for radiation hardness from the initial technological characterization. Testing ongoing for validating the design.

Characterization Set-up

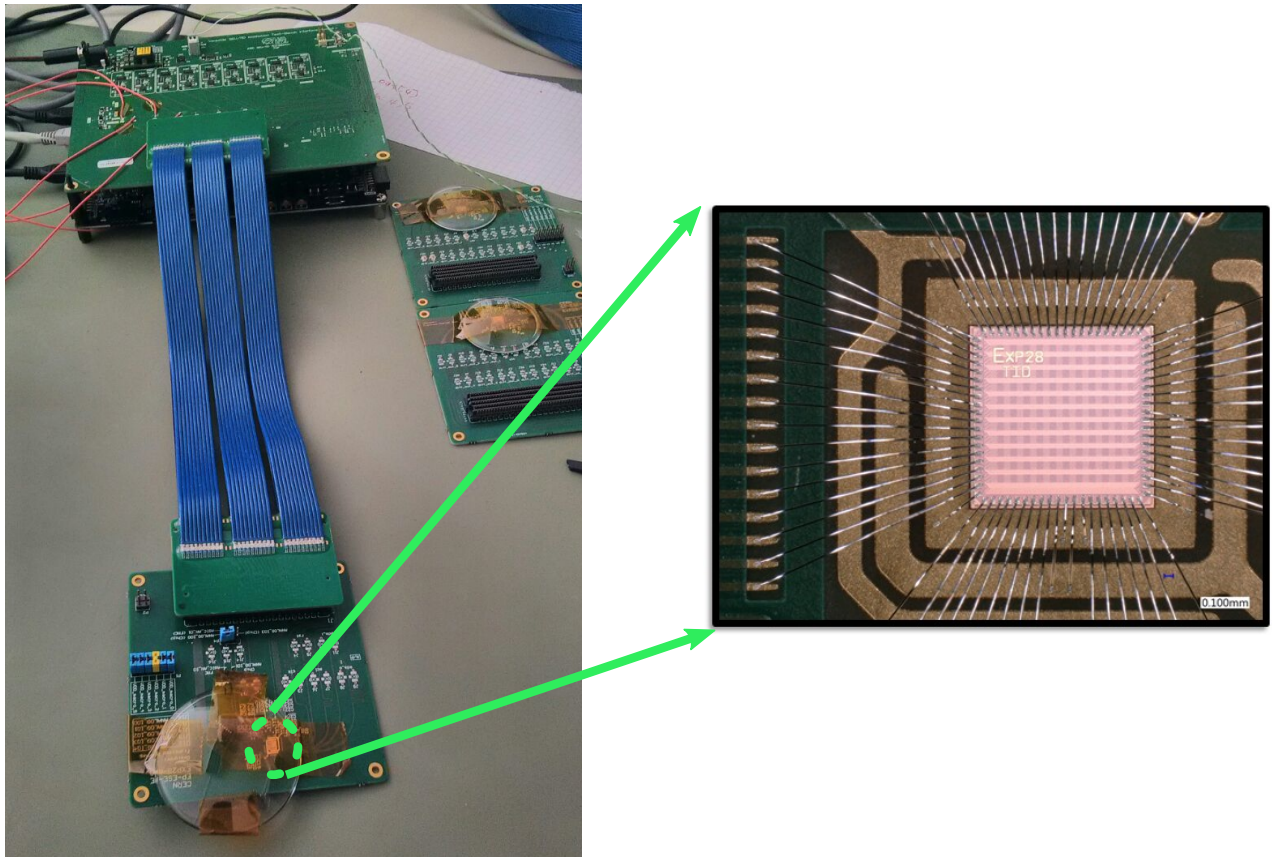
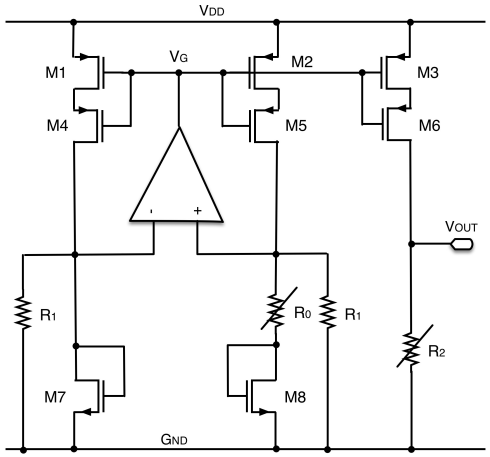
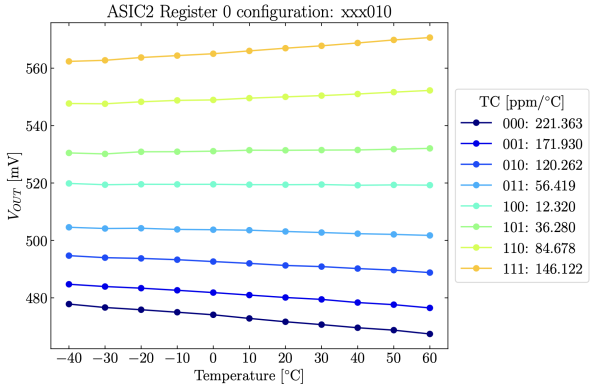
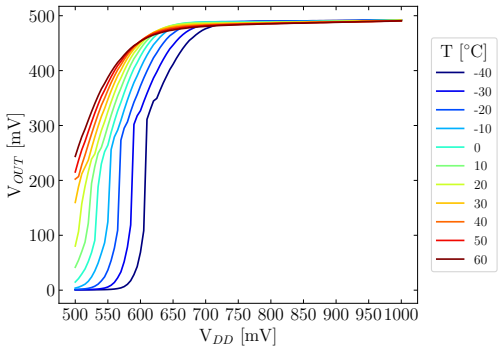


Figure: Left, PCB with wire-bonded chip (bottom) and common test system (top). Right, microphotography of the chip. Acknowledgment: Giulio Borghello, Davide Ceresa, Francisco Piernas Díaz, Risto Pejasinovic.

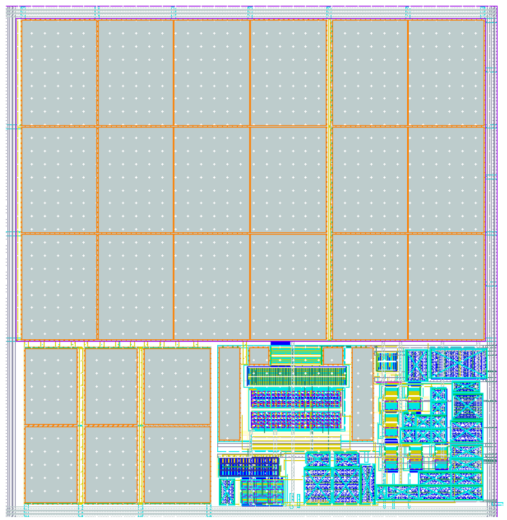
Bandgap Voltage Reference (by G.Traversi: U. Bergamo-Pavia/INFN Falaphel project) [2]







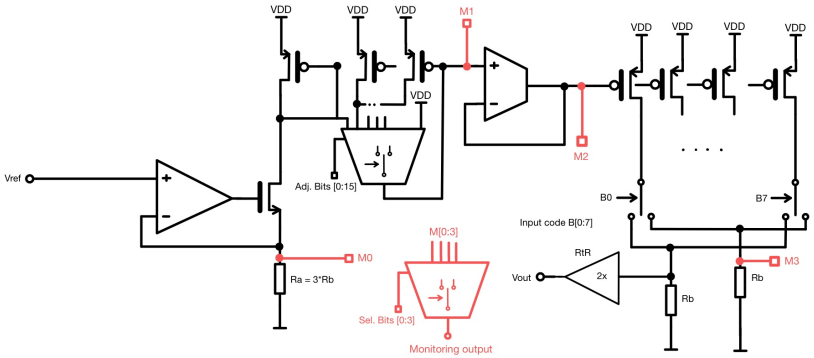
Parameter	Min	Typ	Max	Unit
Voltage supply	0.81	0.9	0.99	V
Output voltage		480		mV
Current supply		100		µA
Temperature	-40	25	60	°C
ΔVref max vs Temp		3		mV
ΔVref max vs Vdd±10 %		2		mV
Target PSR (low frequencies)		40		dB
Active element	lvt in weak inversion			

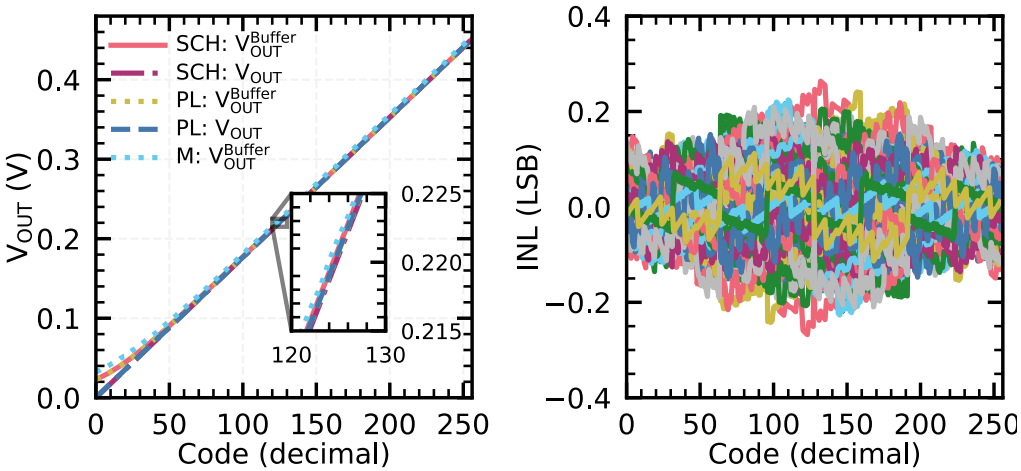


8 Bit DAC (by M. Piller) [3]

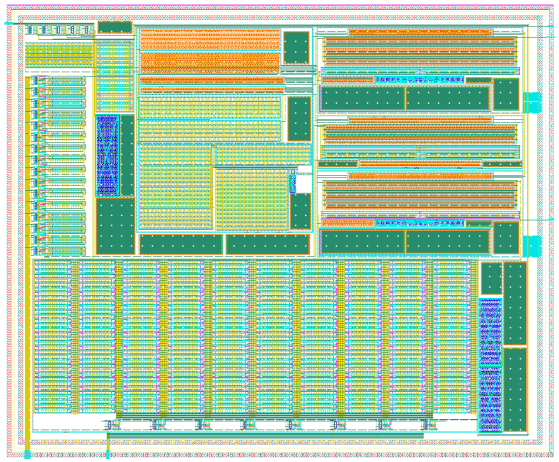
The 8 bit digital-to-analog converter is intent to be a IP block for biasing purposes.

- 8 bit digital-to-analog conversion.
- Output voltage before RtR 0 to $V_{DD}/2$.
- INL < 0.5.
- $I_{LSB} = 50\,nA$ (digitally adjustable)





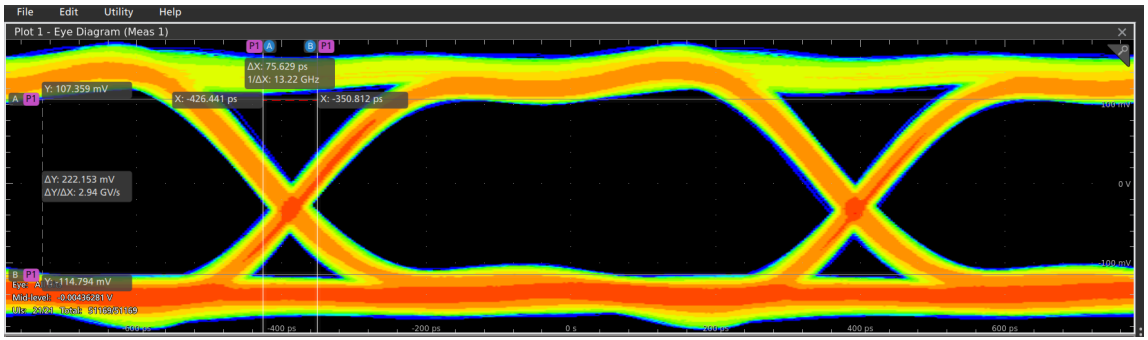
(a) (b)

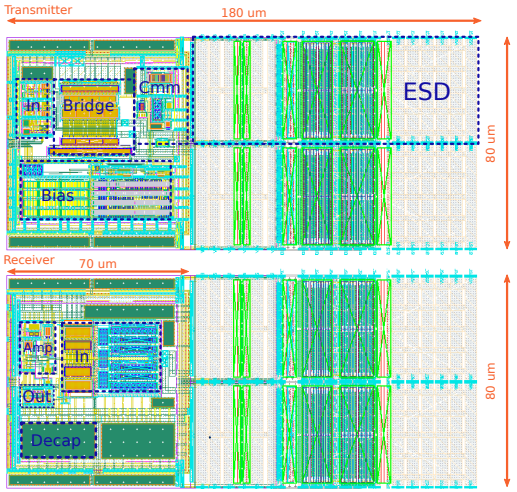


(a) DAC output voltage results from schematic and post layout (PL) simulations and measurements (M) (b) Calculated INL from Monte Carlo simulations.

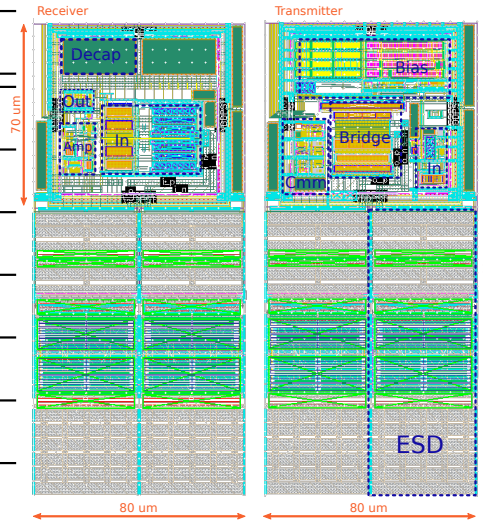
SLVS Driver and Receiver (by F. Bandi) [4]

The design targets mainly on-board chip-to-chip communication in rad-hard applications (1 Grad). Therefore, only thin-gate transistor should be used to ensure higher radiation tolerance [1].





Parameter	Min	Typ	Max	Unit
IO voltage supply	1.08	1.2	1.32	V
Core voltage supply	0.72	0.9	0.99	V
Data rate	0		1.28	Gbps
Temperature	-40		80	°C
Area with ESD		180×80		μm^2
Metal stack		1-2-3(4 power)		metals



Fast Rail to Rail OPAMP (by J. Kaplon)

Parameter	Min	Typ	Max	Unit
Open loop Gain	70	75		dB
GBP (uncompensated)		1.6		GHz
Current supply			400	µA
PM (unity gain for 0-1nF load and 10 Ω series resistor required)	66	74		°
Settling time (1 %)[2]			35	ns
Output noise (unity gain)			150	µV
Offset rms (unity gain)			1.5	mV
Area (amplifier and bias)		$44 \times 70 + 44 \times 90$		μm^2
Area (amplifier, bias, decoupling and compensation)[2]		140×160		μm^2

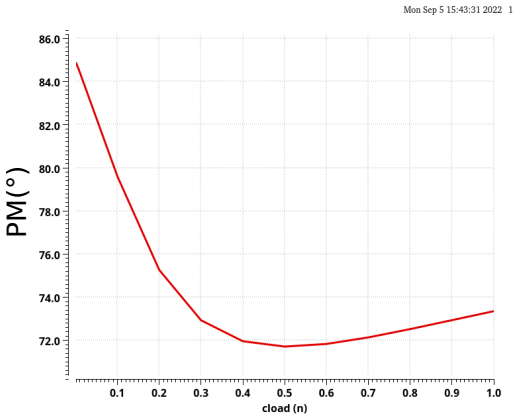
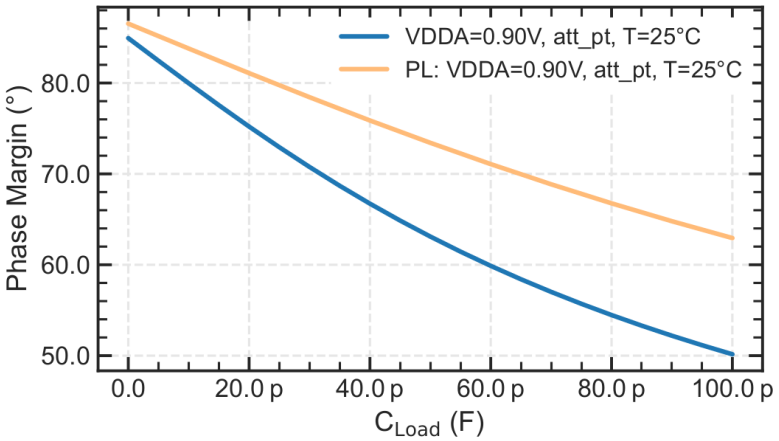


Figure: Phase margin as a function of load capacitance for unity gain configuration.

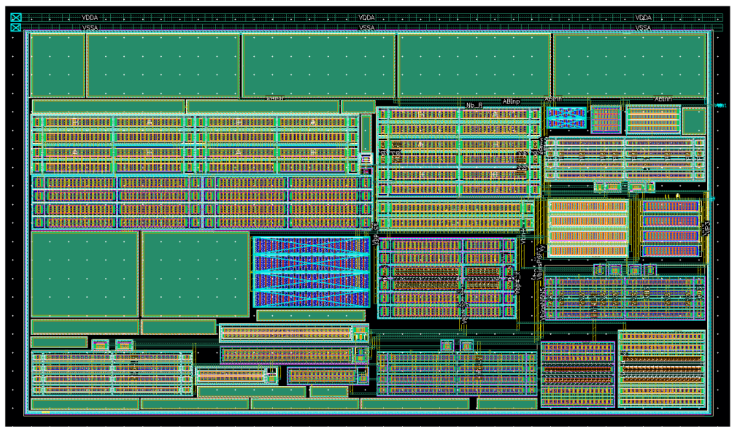
[2] Unity gain configuration.

Slow Rail to Rail OPAMP (by M. Piller)

Parameter	Min	Typ	Max	Unit
Temperature	-40	25	80	°C
Supply voltage	0.81	0.9	0.99	mV
Power		8.4		µW
GBW	130	300		kHz
PM	65		75	°
PSRR	16.5	90(@ 10 Hz)		dB
CMRR		118		dB
Area		186 × 105		μm^2



(a)



(b)

Figure: (a) Phase margin for different load capacitances. (b) Layout.

IP Block Library (Work In Progress 1/2)

Circuits to share	Notes
ΣΔ ADC for monitoring (12b incremental/16b free running; Volt/curr mode)	To be submitted in Nov. 2023. Development lead by T. Hofmann.
Digital to Analog Converter (rail to rail; 8-bit)	To be submitted in Sept. 2023. Development lead by V. Sriskaran.
Slow Rail to Rail Operational Amplifier (low power, e.g. monitoring in unity gain)	To be submitted in Sept. 2023. Development lead by M. Piller. Implemented as part of the 8-bit DAC.
ΣΔ DAC (12-bit)	To be submitted in Sept. 2023. Development lead by O. C. Akgun.
Digital PLL	Specifications closed, design will start Q3 2023. Collaboration with WP6.
Ancillary OPAMPs (small, general purpose amplifiers)	Development lead by M. Piller. Implemented as a part of bigger blocks.

IP Block Library (Work In Progress 2/2)

Circuits to share	Notes
TDC (multichannel; ∼25 ps time resolution)	Collaboration with University of Ulm. Development lead by C. Rudorf.
TID monitoring	To be submitted in Sept. 2023. Development lead by G. Borghello.
DCDC converter ($V_{in,max}$= 5V; V_{out}=0.8-1V; I_{out}=0.5 A)	In progress. Development lead by S. Michelis and G. Ripamonti
LDO ($V_{in,max}$= 1.2V; V_{out}=0.8-0.9V; I_{out}=0.2 mA)	In progress. Development lead by TU Graz, supervised by S. Michelis
Shunt LDO (SLDO) for serial powering solutions (mainly inner tracker pixels)	In progress. Development lead by M. Karagounis (FH Dortmund)

Documentation

Analog IP Blocks

Summary

Summary

- The IP blocks are accompanied by datasheets. A designer's guide and other support documents have been prepared to assist designers.
- Analog IP blocks will have the following view: schematic, abstract, layout, dspf, symbol, .lib, power grid view, verilog...
- CERN ASIC Support Team (A. Caratelli and M. Andorno) is helping designers to create these views.
- Next submissions are planned for September and November 2023 (including rail to rail 8b DAC, a respin of the SLVS TX/RX and the bandgap reference).
- We have created synergies with other groups in the community. Feel free to spread the word and contact us!

Bibliography

[1] Giulio Borghello, *Advantages of 28nm technology in ultra-high-TID environments*, Forum on 28nm CMOS (CERN), Login and access required., 2020. https://indico.cern.ch/event/970389/contributions /4097899/attachments /2141534/3608590/Advantages%20of%2028nm %20CMOS%20Technology%20in%20Ultra-High-TID%20Environments %20-%20Giulio%20Borghello.pdf

[2] G. Traversi, et al., "Design of a Radiation-Tolerant Bandgap Voltage Reference for HEP applications", *2022 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Milano.

[3] M. Piller, et al. , *"Generic Analog 8 Bit DAC IP Block in 28nm CMOS for the High Energy Physics Community"*, Austrochip 2022 - 30th Austrochip Workshop on Microelectronics. Institute of Electrical and Electronics Engineers, 2022. p. 5-8 (Austrochip 2022 - 30th Austrochip Workshop on Microelectronics), doi: https://doi.org/10.1109/Austrochip56145.2022.9940783.

[4] F. Bandi, et al. , *"Analog IP Blocks in 28nm CMOS for the High Energy Physics Community: SLVS Transmitter and Receiver"*, Journal of Instrumentation, vol. 18, no. 01, pp. C01039, 2023, doi: https://dx.doi.org/10.1088/1748-0221/18/01/C01039.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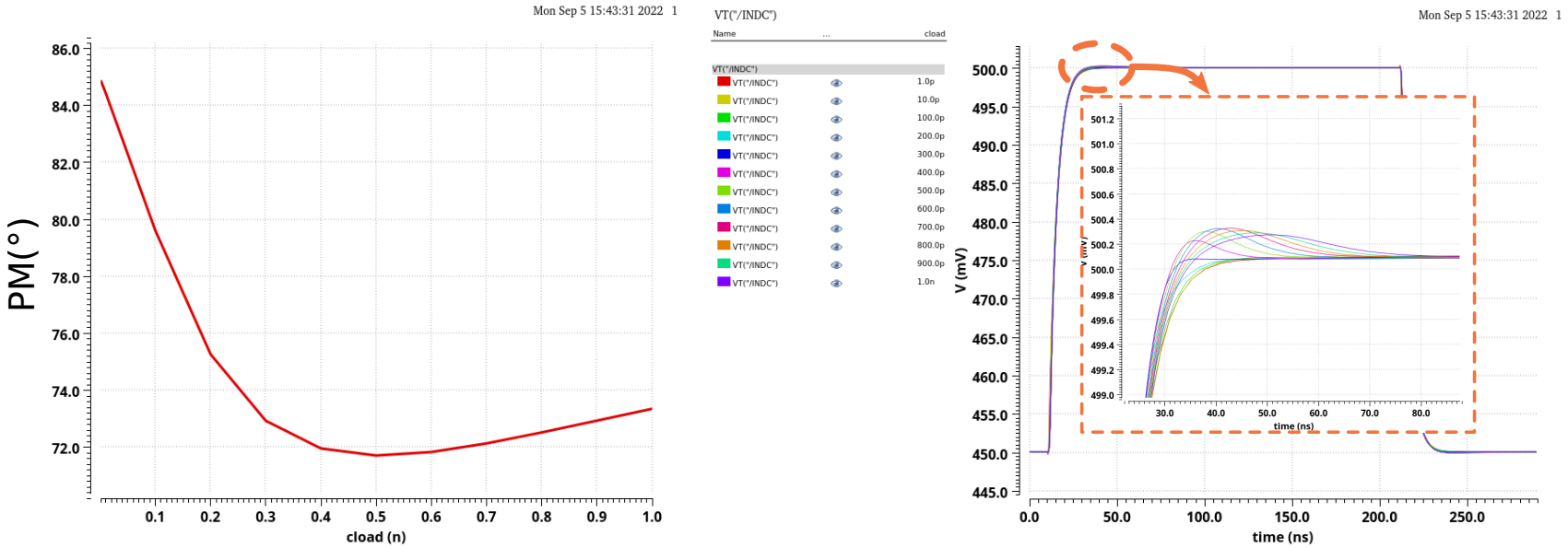
Fast Rail to Rail OPAMP: Simulation Results



(a) (b)

Figure: (a) Phase margin as a function of load capacitance for unity gain configuration. (b) Transient response for unity grain configuration for 50mV step at the input.