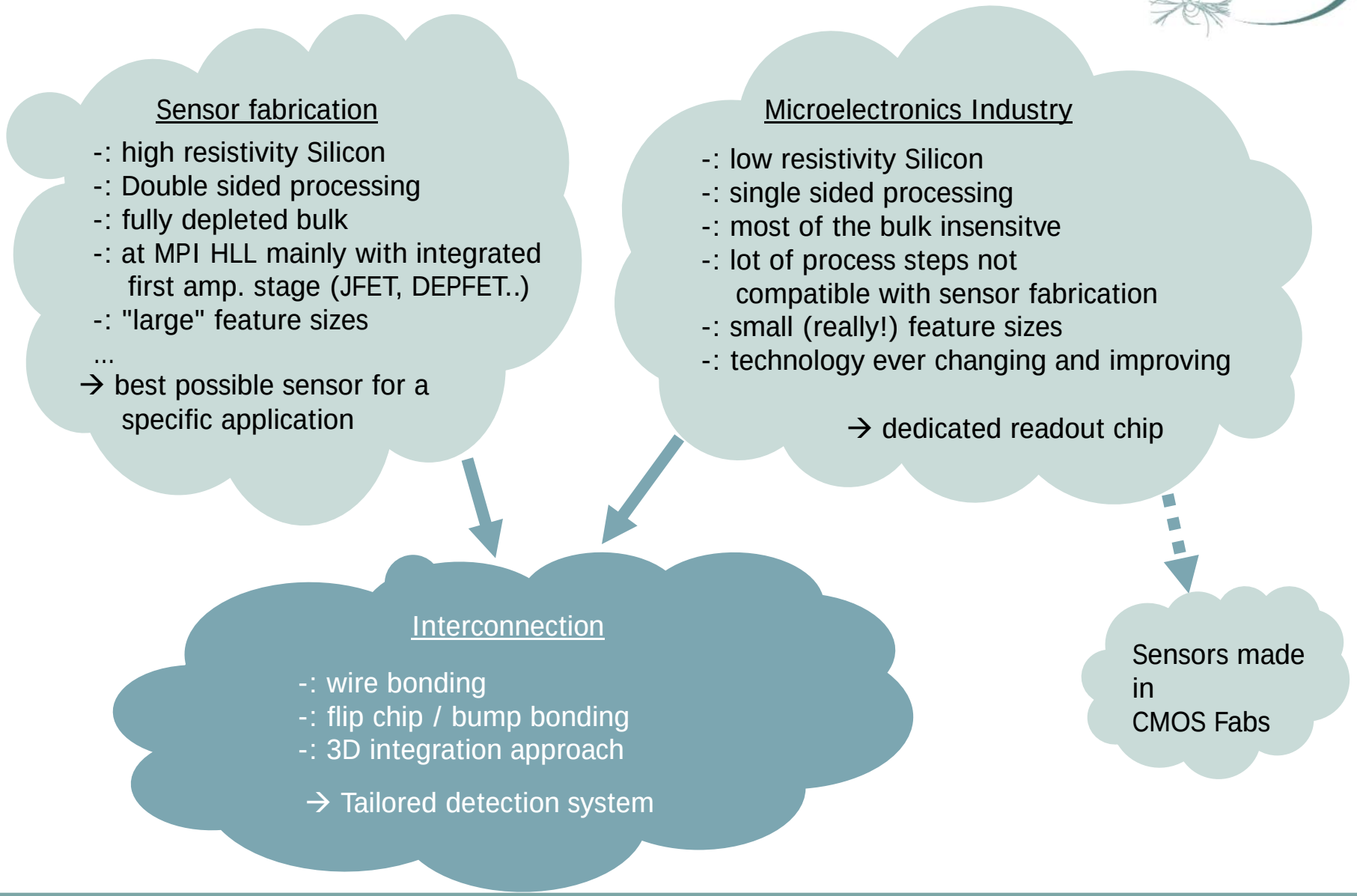
Interconnections

the link between sensors and r/o electronics

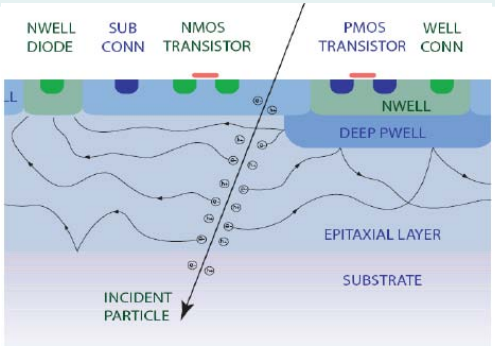
- **conventional wire bonding**
- **bump bonding / flip chip**
  - ↳ **DEPFET all-silicon module at Belle II**
  - ↳ **DEPFET at XFEL**
- **bump-less interconnection**
  - ↳ **SLID and TSV for ATLAS upgrade**

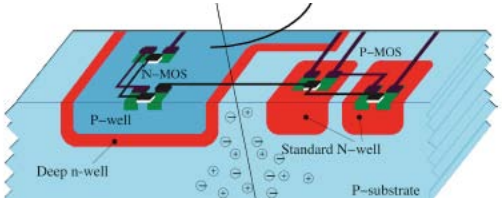
Ladislav Andricek, MPI für Physik / MPI Halbleiterlabor, München

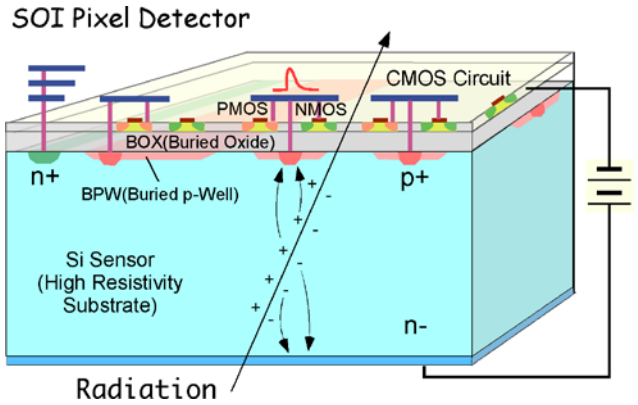
different “worlds”



Sensors made in "CMOS" ... compromises ...







CMOS sensors→ MIMOSA, FAPS, INMAPS, APSEL..

(adoption of the CMOS Sensors for optical consumer cameras)

-: n-well as collecting Anode, collection by diffusion
-: mostly on epi wafers, recently on HiRes wafers
-: started with only use pMOS transistors in the p-well
-: additional wells: double, triple, quadruple well ..

→ first applications in STAR, CBM ...

CMOS on SOI wafers

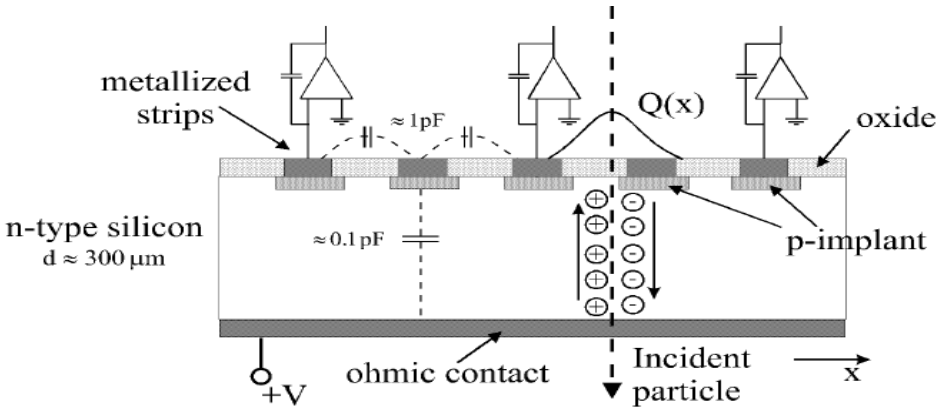
major players: ROHM Lapis (OKI), American Semiconductor

-: use thin silicon layer on top for the r/o circuit
-: thick handle wafer (separated by the BOX) as detector
-: can use full CMOS in top layer
-: processing and handling of the back side still somewhat delicate for standard CMOS lines

→ in R&D phase, first promising results...

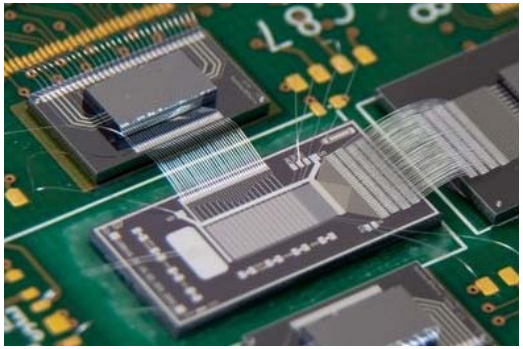
CMOS process compromises detector properties. It is definitely not the "best of both worlds"!
→ try the modular approach.....

wire bonding I



- each strip ("PiN diode") connected with input of r/o ASIC
- used for tracking detectors in HEP experiments
- ASIC: f/e CSA + filter+ ADC + pipeline ...
- typical number: ~ few thousand bonds per module

- interconnect type: wire bonding

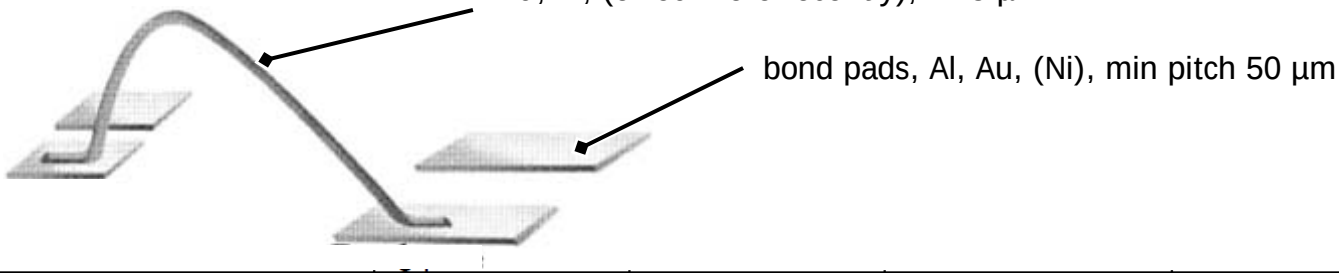


DEPFET matrix with row-wise connected to steering and r/o chip

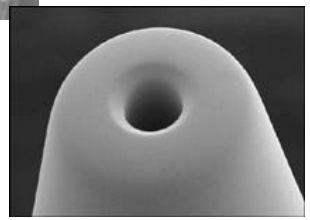
ATLAS Forward SCT strip detector connected to six r/o ASIC "ABCD"

wire bonding II

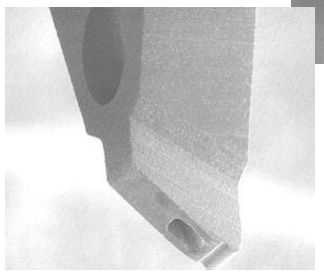
- micro welding process: a thin wire is brought into contact to a metal pad
- using thermo-compression, thermo-sonic and/or ultra-sonic energy an electrical and mechanical connection is formed

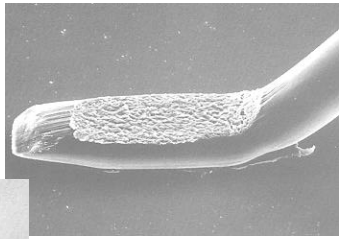


Wirebonding	Pressure	Temperature	Ultrasonic energy	Wire	Pad
Thermocompression	High	300-500 °C	No	Au,	Al, Au
Ultrasonic	Low	25 °C	Yes	Au, Al	Al, Au
Thermosonic	Low	100-150 °C	Yes	Au	Al, Au



ball bonding





wedge bonding

wire bonding → bump bonding

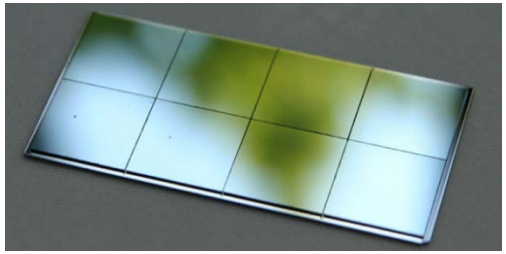
pro:

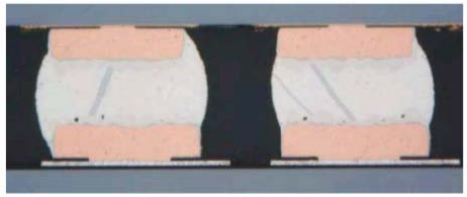
- ❑ no chip (sensor or ASIC) modification is needed
- ❑ relatively cheap technique, small setup costs
- ❑ technique is widely established (you certainly have at least a manual bonder in your lab)

con:

- ❑ all pads have to be at the periphery of the chips → I/O and space problem!!
- ❑ min. pitch is ~50µm
- ❑ losses due to stray capacitances (~1pF/bond) and inductance of the wire (~1nH/bond)

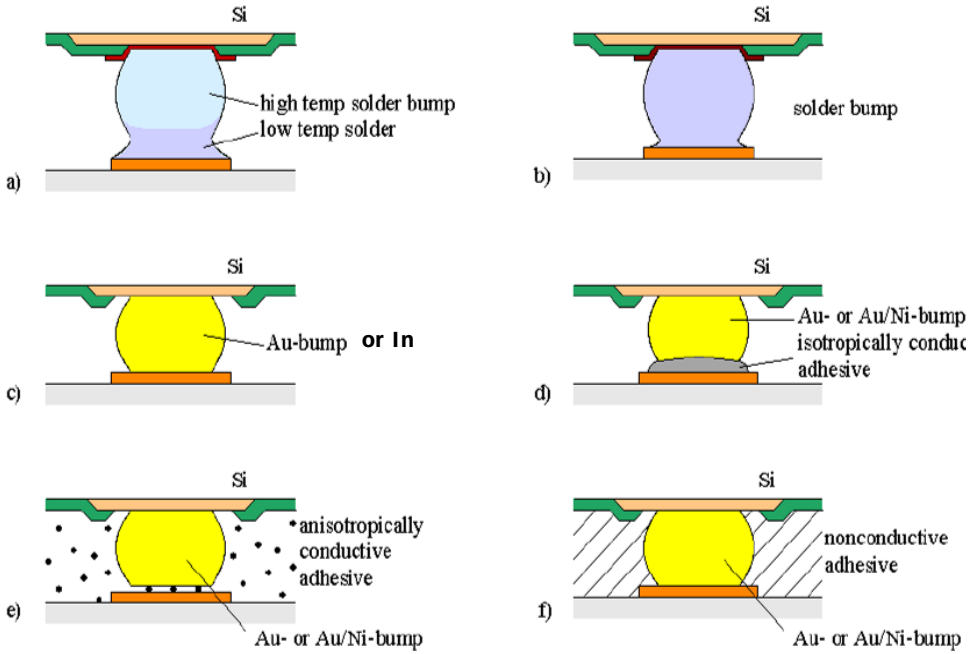
Flip-Chip bump bonding

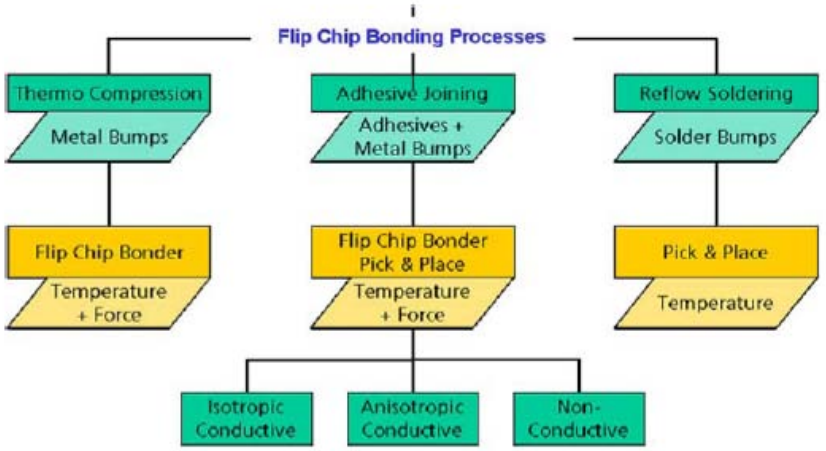




è for more and denser interconnections
è more compact modules
è individual pixel connections of 2D detectors
è reduction of stray capacitance, resistance and inductance of the joint

Flip-Chip Technologies





In general there is always:

1. Bumping of the ASICs
2. Preparing the landing pads on the substrate (sensor)
3. Flip-Chip ASICs to sensor and join electrically and mechanically

→ commercially available solder bumps (PbSn or SnAg or SnAgCu)

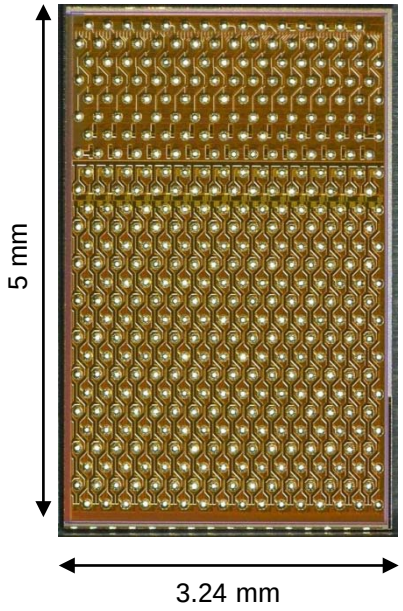
-: Wafer process, commercially available in MPW runs
- IBM C4 : 200 µm pitch
- UMC, TSMC : by external bumping fabs (SPIL...) 150 - 180 µm

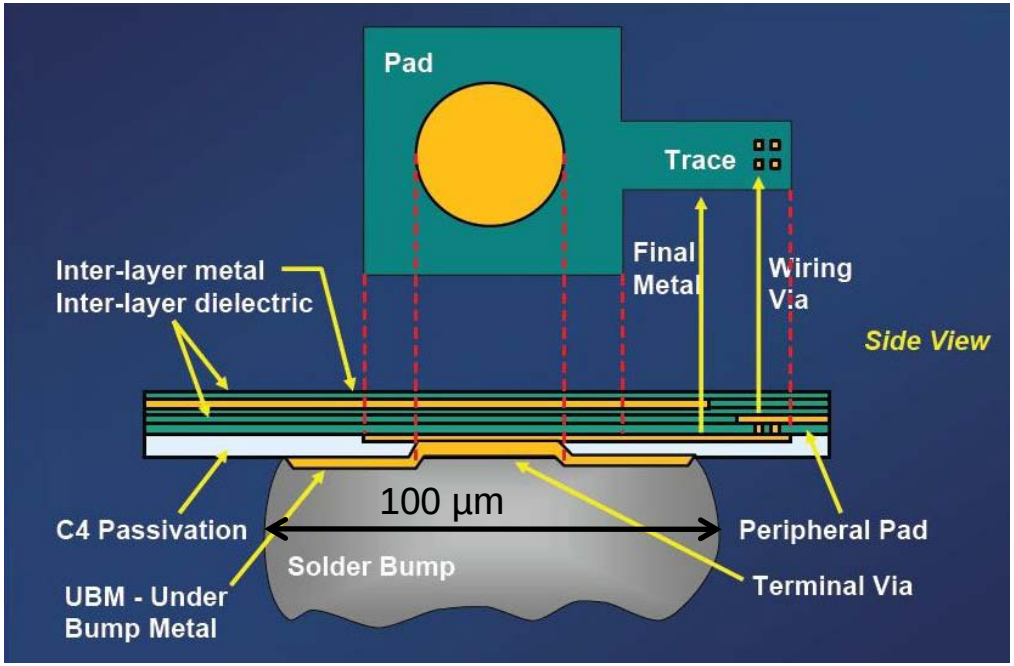
-: ITRS Packaging road map says: pitch ≅ 100 µm until 2015

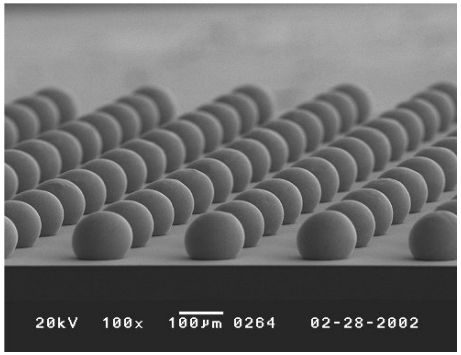
-: non-industrial processes ~50 µm and below as of today

as an example: C4 Bumps on the ASIC from IBM

C4: controlled collapse chip connection (invented by IBM in the 1960s)

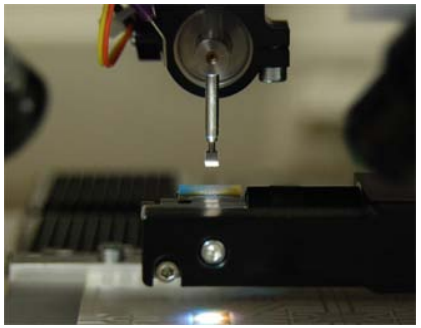


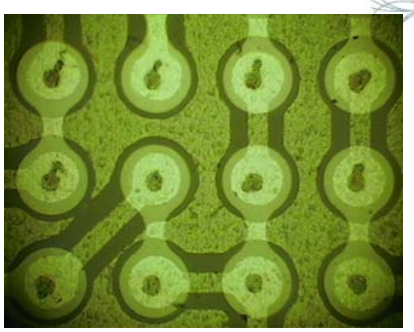


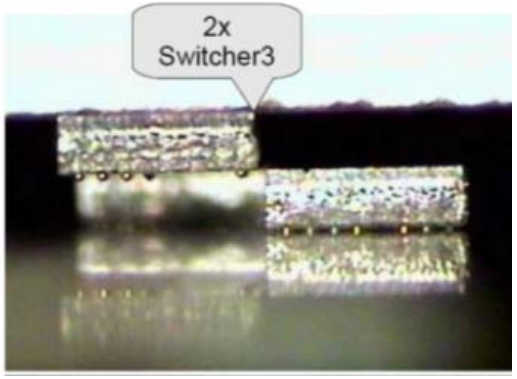


- Bump compositions
  - High melt (ceramic substrate applications)
    - Pb-3Sn, Pb-5Sn, Pb-10Sn
  - Low melt (organic substrate applications)
    - Sn-37Pb, Pb-free compositions (SnAg, SnCu)
  - "Duplex" bumps (low melt on high melt base)

Flip Chip Bonding → "pick-and-place“ and soldering







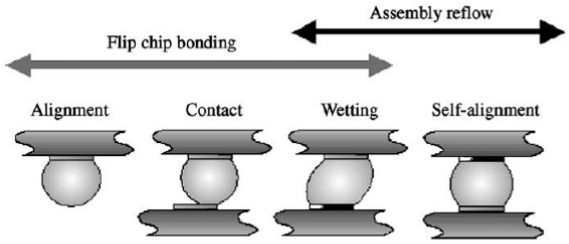
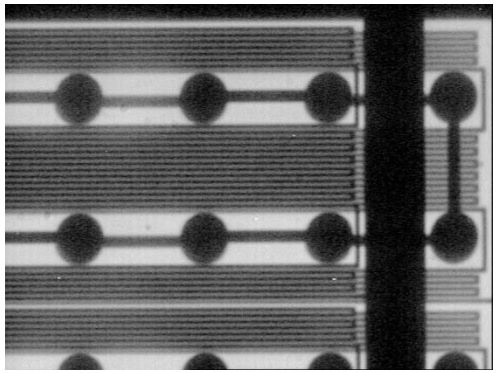


Fig. 3. The principle of the assembly reflow.

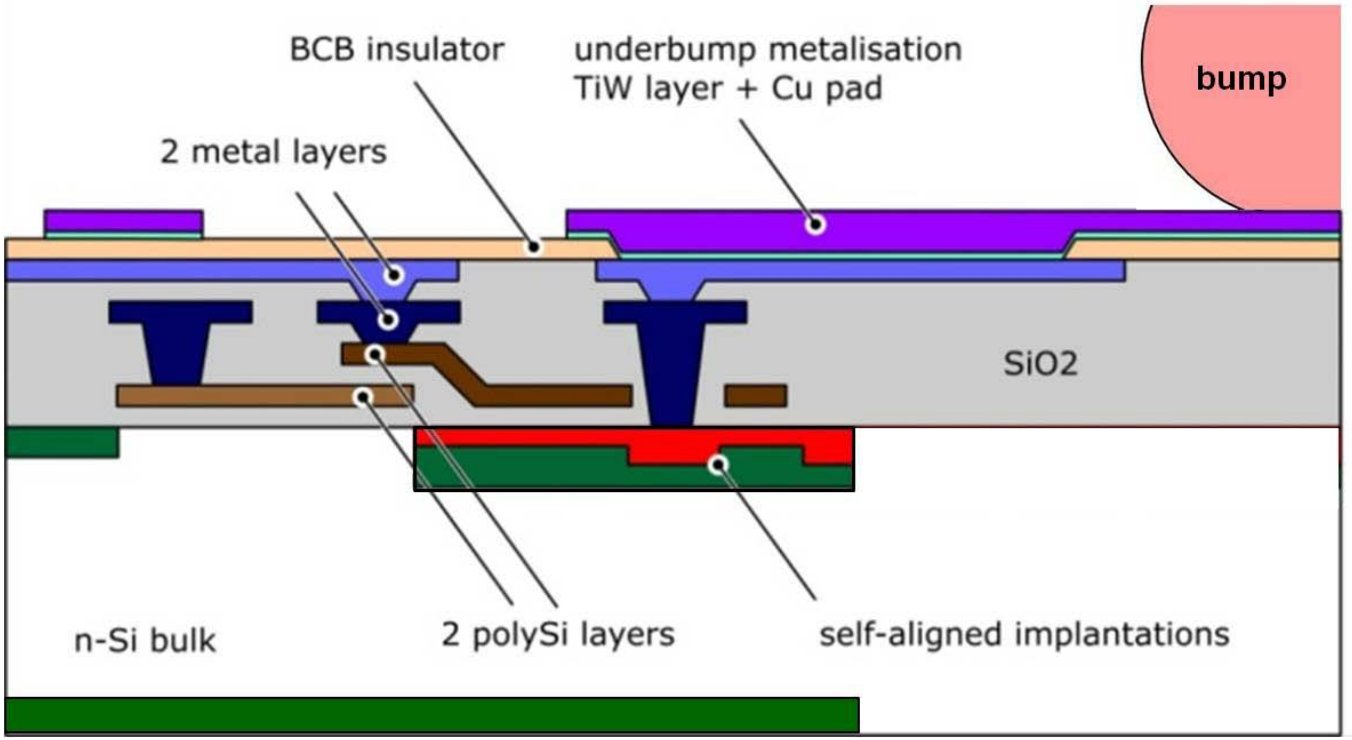


-: dedicated machine for chip-to-chip or chip-to-substrate assembly
-: alignment accuracy ~1 µm (3 sigma)
-: basically no pressure needed
-: in situ reflow for single chip, ~200 °C
-: optionally additional reflow in furnace for multi-chip assemblies

→ allows thousands of connections per chip and very compact arrangements

disadvantage: needs additional processing on the sensor wafer: solder wetable landing pad!!

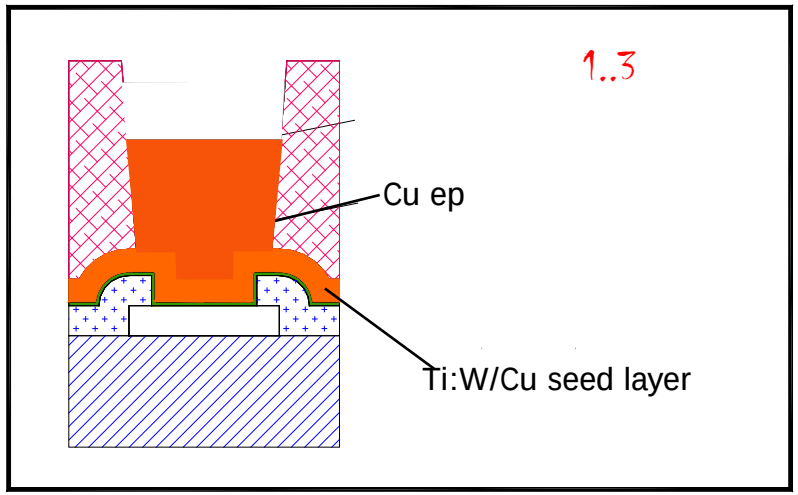
Copper for the bump landing pad on the sensor



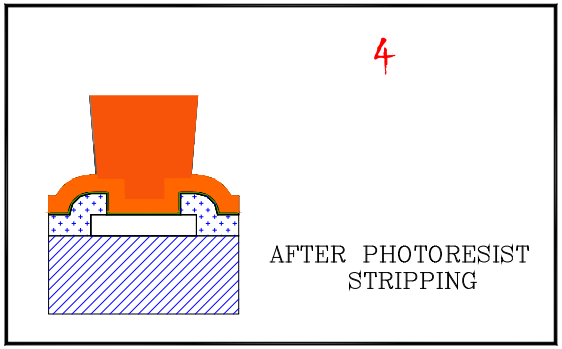
- Standard at MPI HLL: two poly layers + two Al layers → add Cu
- the Cu layer is effectively a 3rd metal on the sensor – ρ(Cu) / ρ(Al) ≈ 0.63
  → low impedance wiring layer and additional routing freedom

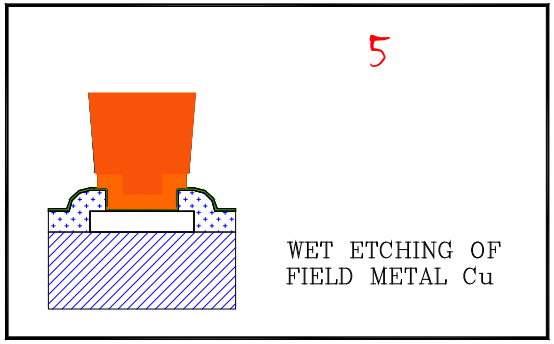
The UBM Process – additional Cu process on wafer level

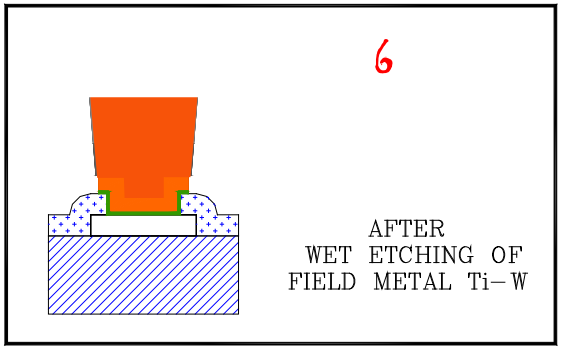
Sensor wafer, last metal Alu2, BCB passivated , from clean room



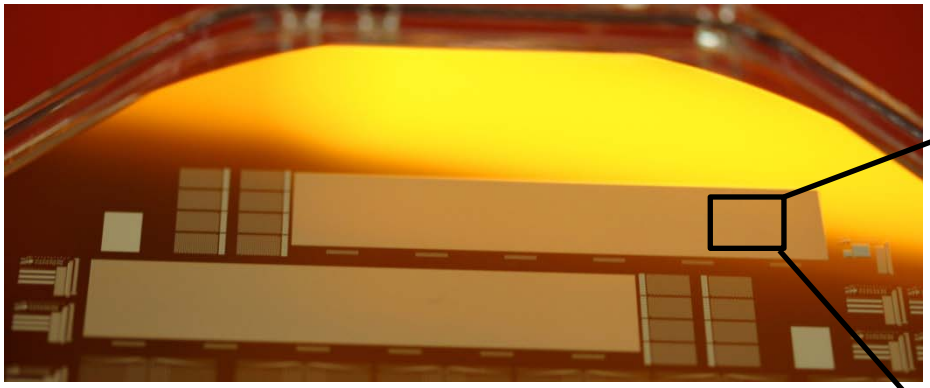
1. Sputter Ti:W (~100nm) und Cu (~200nm)
2. Lithography: thick photo resist (~10µm)
3. Through mask EP: 3-5 µm Cu
4. Resist strip
5. Wet etch Cu ($FeCl_3$, HCl ..)
6. Wet etch Ti:W: H_2O_2 (with additives)



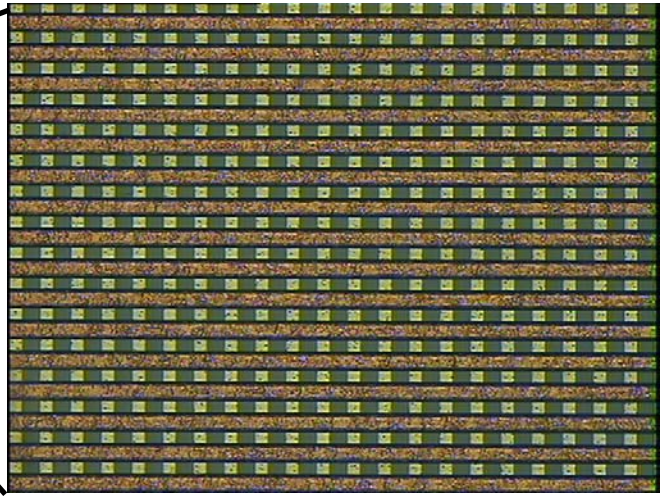


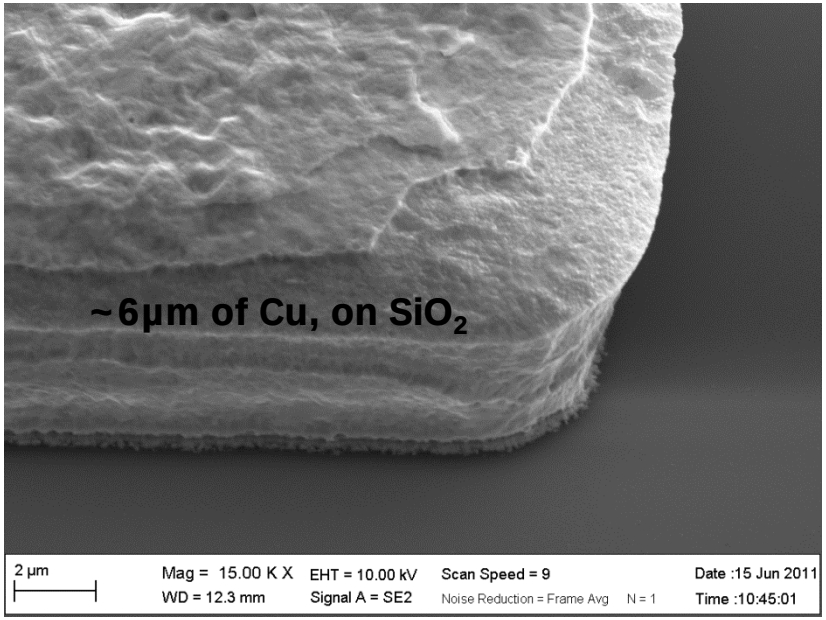


3rd Metal in Cu at MPI HLL



5000 Al-Cu crossings in ~6cm^2





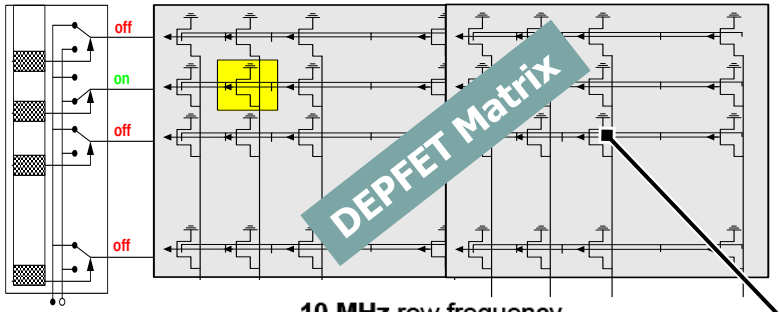
- resistivity of Cu close to ideal (17µΩ.cm)
- BCB ILD stands 150 V, no shorts seen on 6cm^2
- tests on active devices (pin diodes and MOS)
  - ↳ no effect on device performance
- FC tests with dummy chips on Cu samples
  - ↳ Cu is solderable in reducing atmosphere

an example: DEPFET pixel vertex detector for Belle II

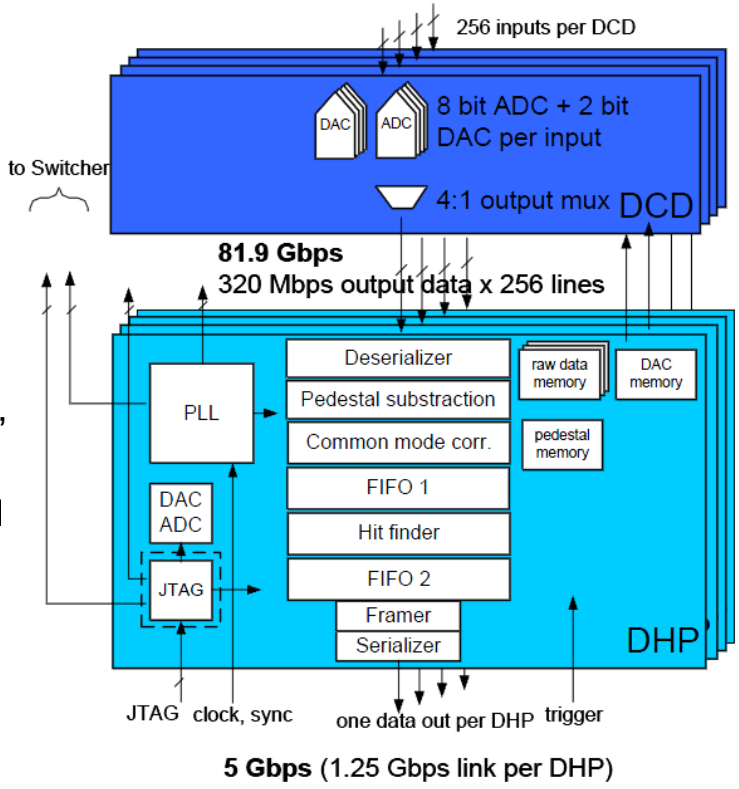
Switcher:
180nm HVCMOS AMS
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV up to 20V

DCD:
"Drain Current Digitizer"
UMC 180nm
f/e and ADC

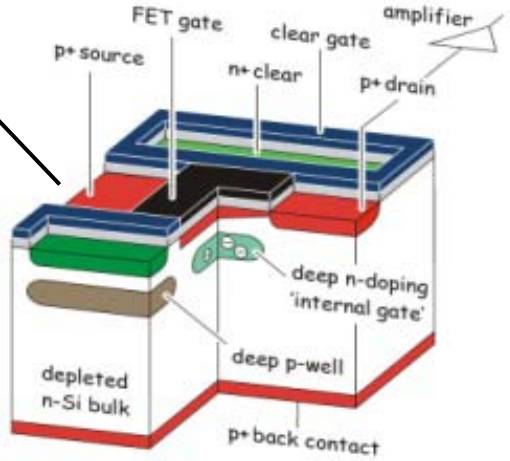
DHP:
"Data Handling Processor"
IBM 90nm → TSMC 65nm
Digital control chip



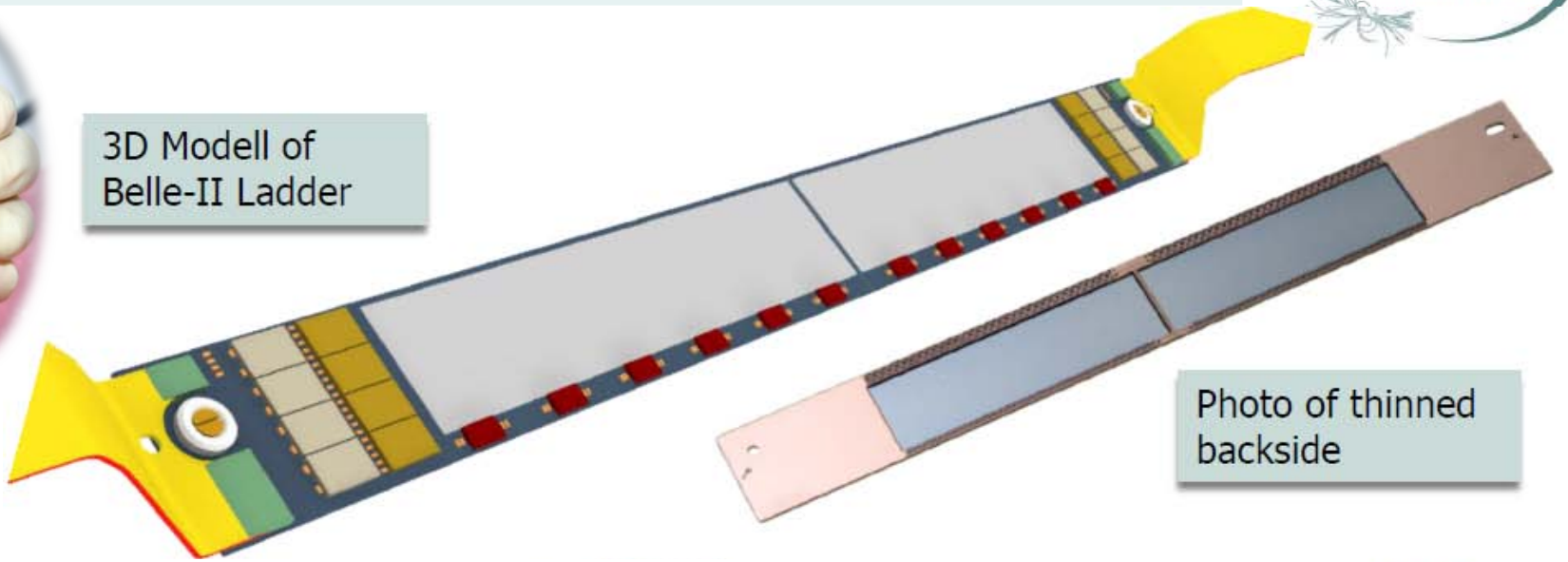
10 MHz row frequency
100 ns ADC conversion time



5 Gbps (1.25 Gbps link per DHP)

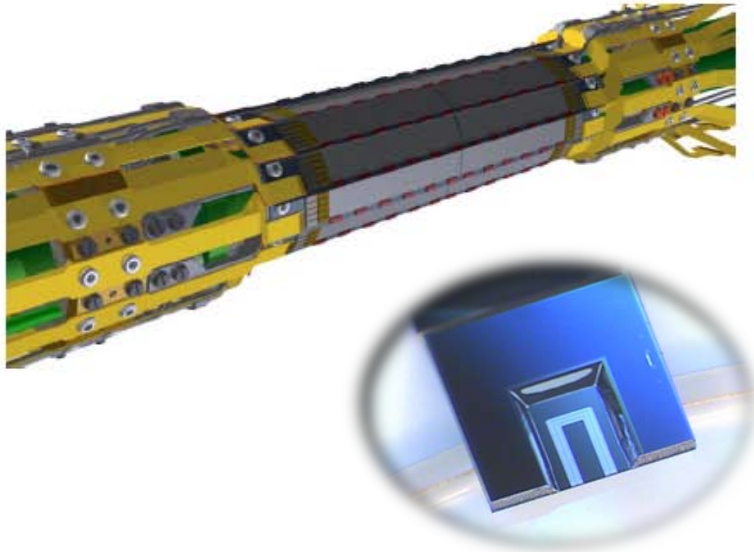


DEPFET vertex detector at Belle II

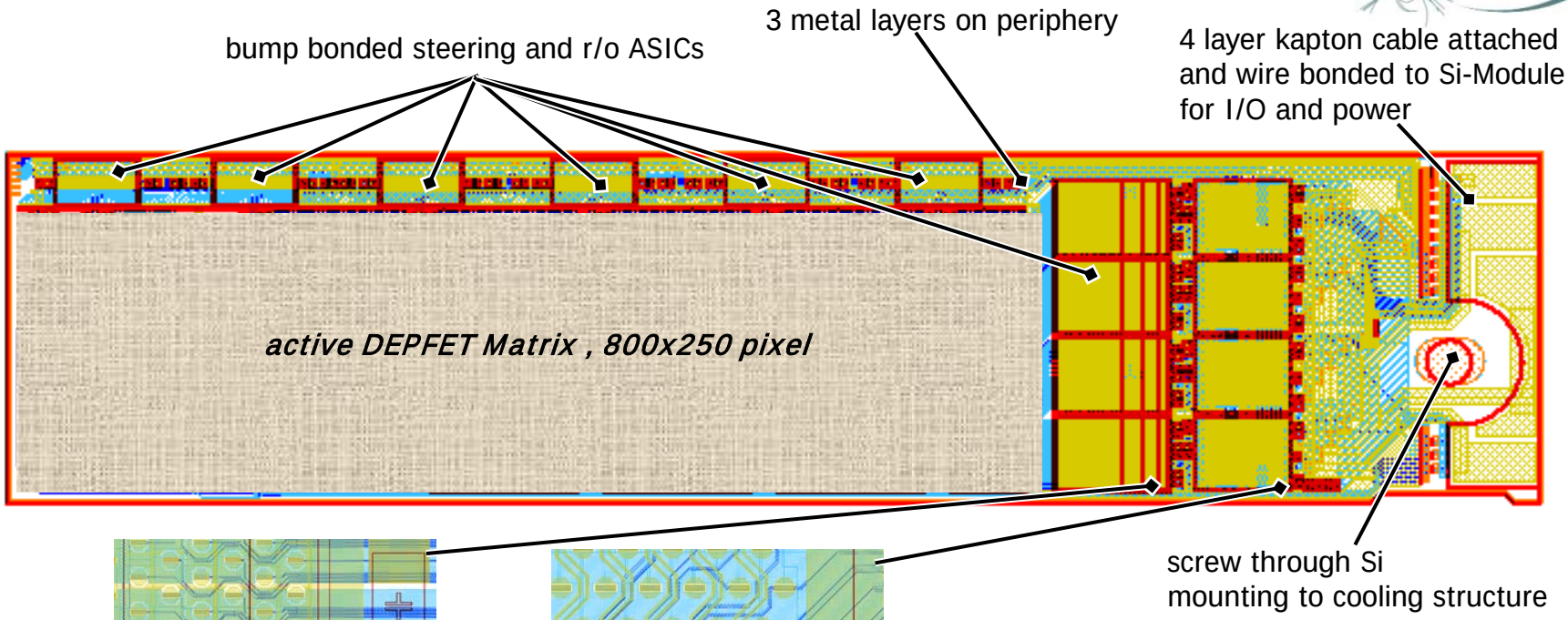


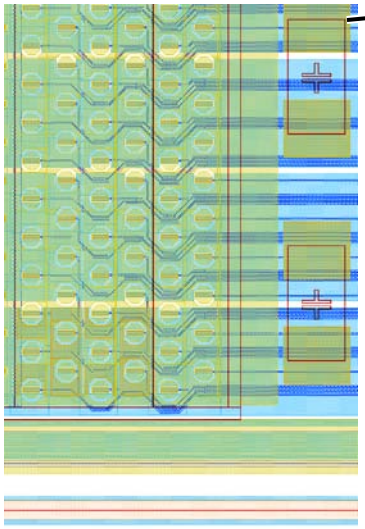
Belle-II PXD Module (two modules form a ladder)

- three metal layers, Cu as LM
- 4 DCD, 4 DHP, 6 Switchers → ~3000 bump bonds/module
- Cu as UBM, bumps partly on thinned perforated frame
- passive components soldered (or glued to) substrate
- I/O and power over kapton cable

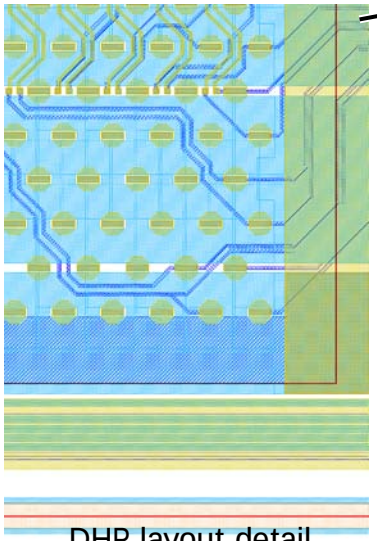


layout at the periphery

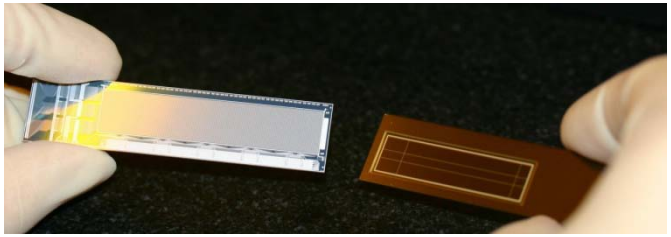




DCD layout detail



DHP layout detail

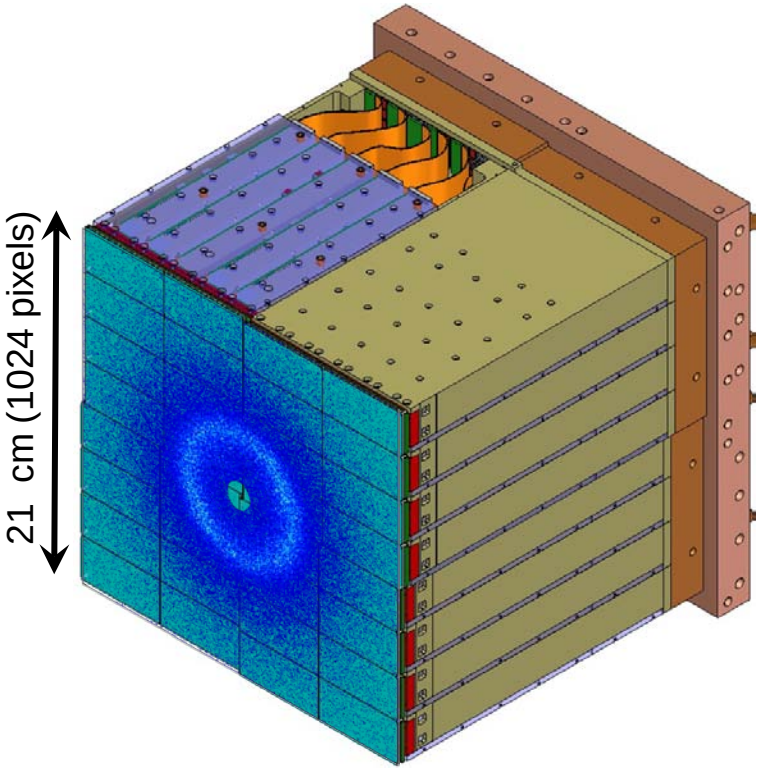


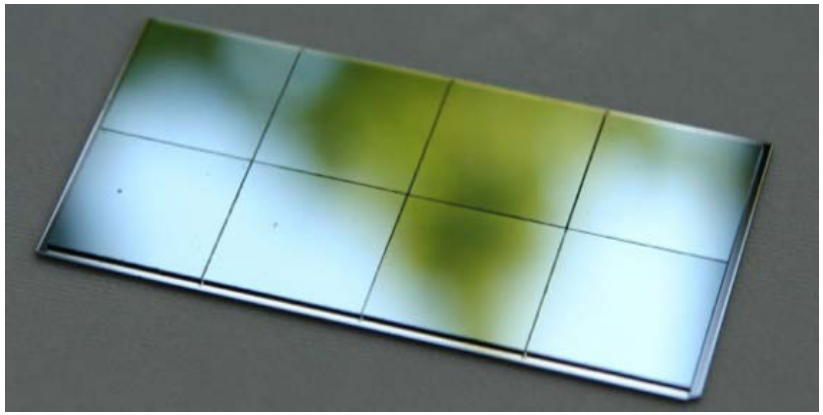
status:
thin double metal prototypes done
next step:
full size samples with complete metal system

another application: DSSC – DEPFET for the XFEL

- Flip chip with one bump per pixel opens the way to fully parallel processing

- each pixel has its own r/o channel, ADC and memory, bump bonded in the sensitive area
  ↳ 1 Megapixel with Megaframe read-out: 1 picture/220 ns





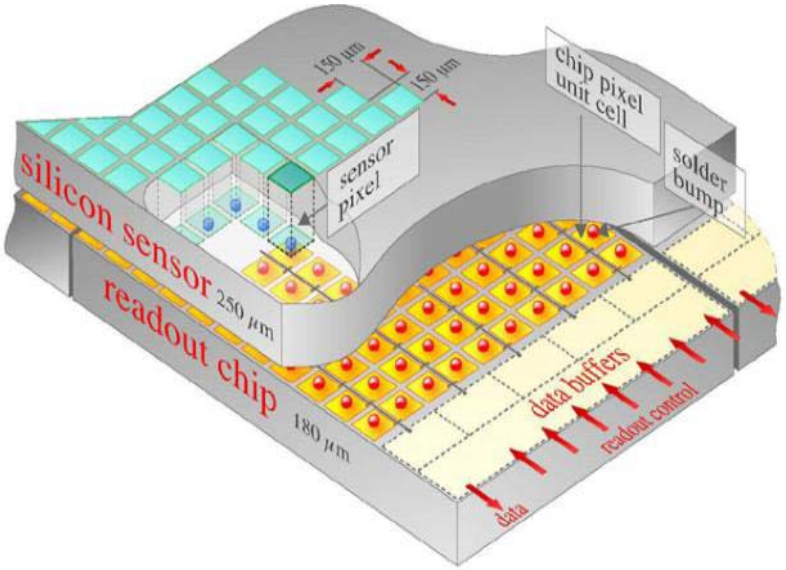
- dedicated development of the DEPFET sensor
- bumped custom made r/o ASICs

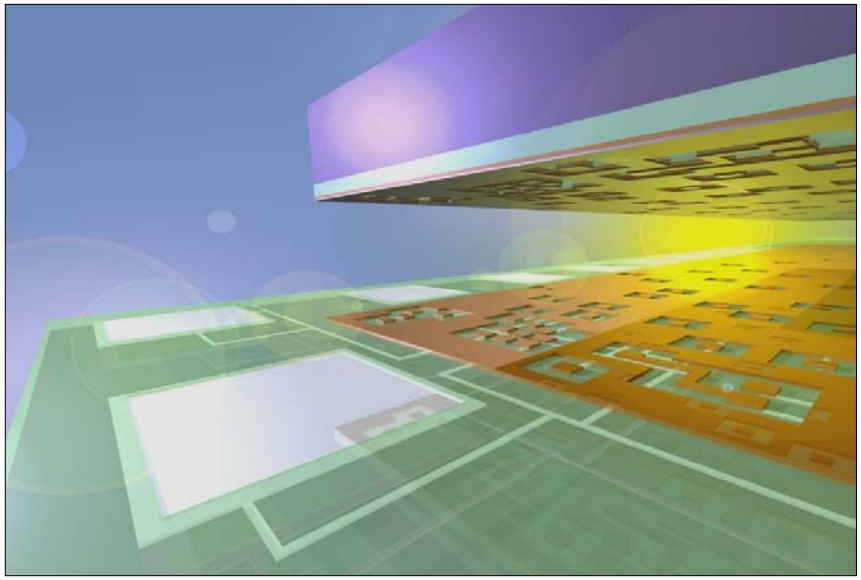
- bump bond technology basically the same
  ↳ 200 µm pitch, PbSn bumps to Cu pads

→ optimal detector system for specific application

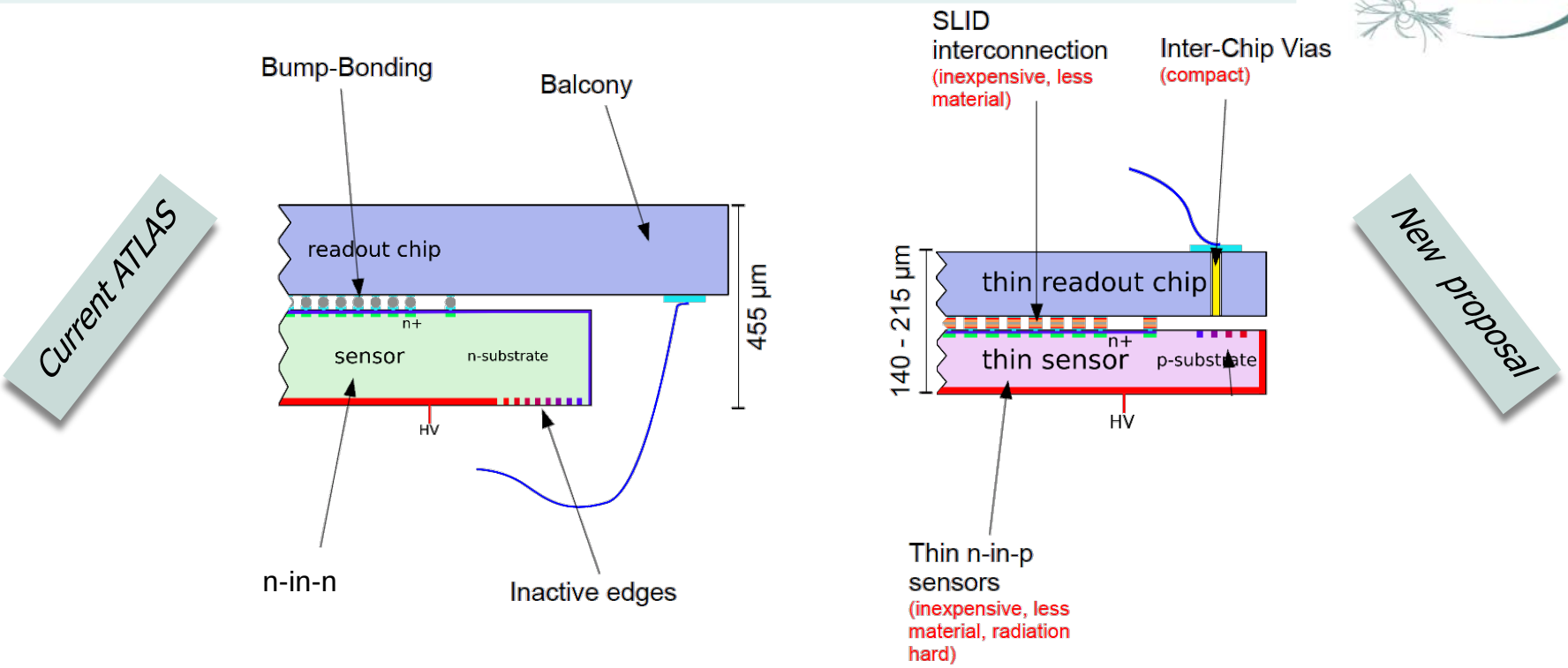
solder bump bonding – in summary

- Solder bump bonding is widely used in industry and for 2D pixel detectors in HEP and photon science
- commercial vendors for bumped chips deliver pitches down to ~150µm
- R&D labs (IZM Berlin, VTT Finland..) go down to 50 µm, recently micro-bumps in the 20 µm range were reported, technologically limited by the bumping process
- potentially, **bump-less interconnects** offer the opportunity to have an even finer pitch and a better mechanical joint between the two layers (important for ultra-thin chips and/or sensors)
- bump-less means direct Cu-Cu bonds or Cu-Sn eutectic bonding





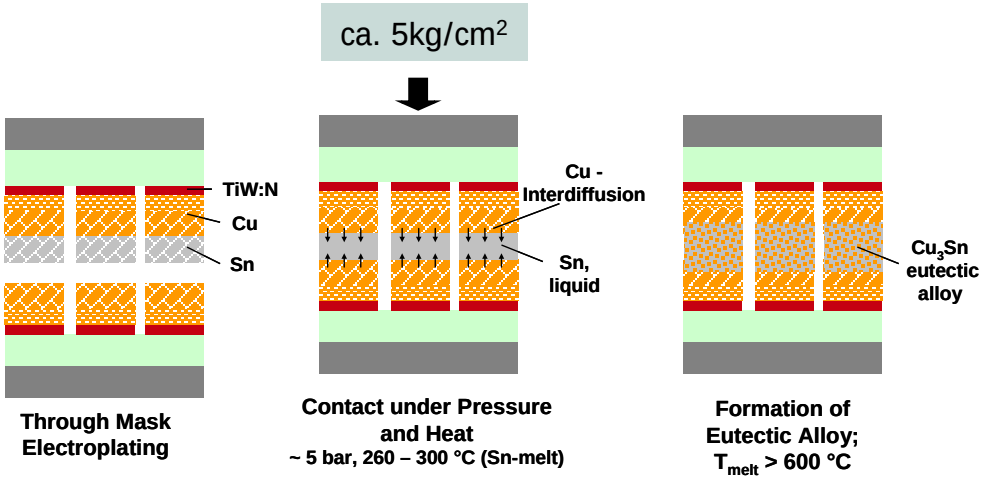
The ATLAS Pixel Detector Upgrade



Objectives of the project (MPP Munich & Fraunhofer EMFT Munich)

- Design and build thin pixel sensors on p-type FZ material
- Show compatibility and radiation hardness of sensors with SLID metal system
- Show feasibility of the post-processing of existing r/o electronics (ICV and thinning)
- Build demonstrator module with thin sensors, using SLID and ICV through the r/o Chip

"SLID" - "SOLID" – bump-less Cu-Sn eutectic bonding



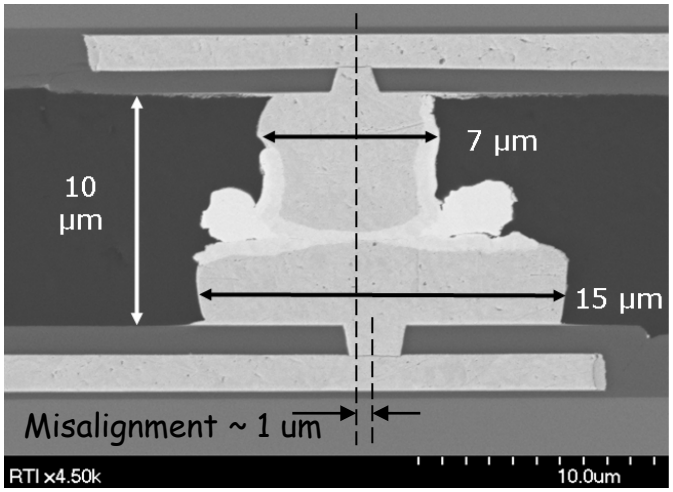
SLID: Solid Liquid Interdiffusion

- alternative to conv. bump bonding
- Cu+Sn layers → Cu_3Sn alloy
- for electrical and mechanical connection
- min. pitch given by pick and place (~few µm)

- However: no rework possible!

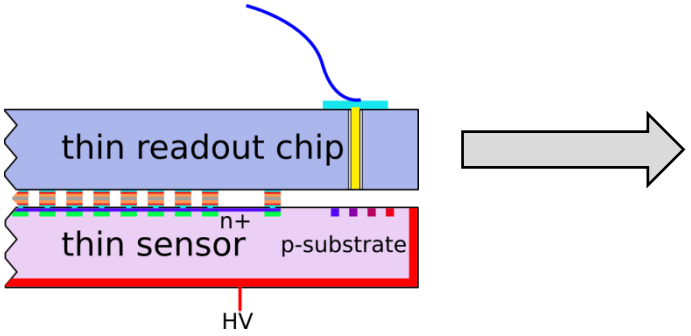
post-processing for sensor and ASIC wafer

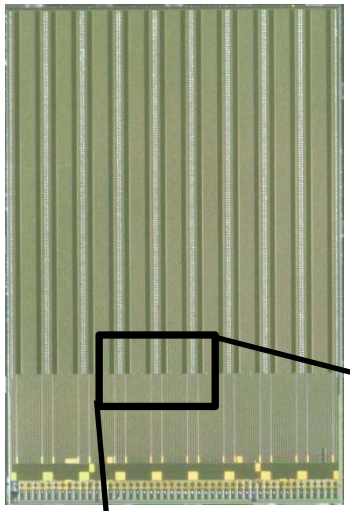
- BCB layer to define TiW/Cu/Cu(/Sn) System
- Metal system on both:
  - 100 nm TiW, sputtered
  - 200 nm Cu, sputtered
  - 5 µm Cu, through mask electroplated
- on sensor wafers add: 3 µm Sn
- basically the same process steps as for std. solder bumps



RTI with direct chip-to-chip attach

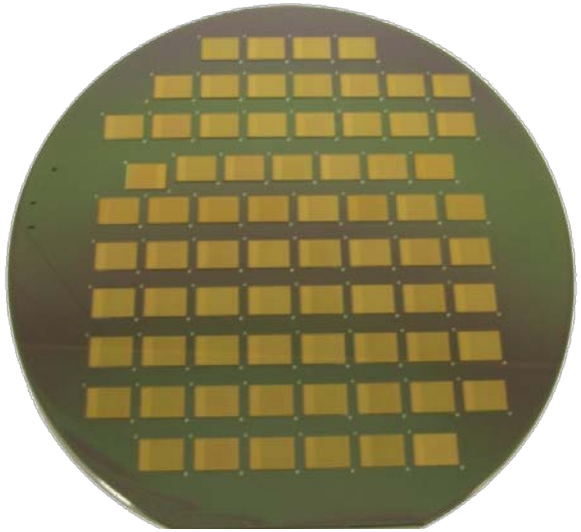
reconfiguration of the ASIC wafer FEI3



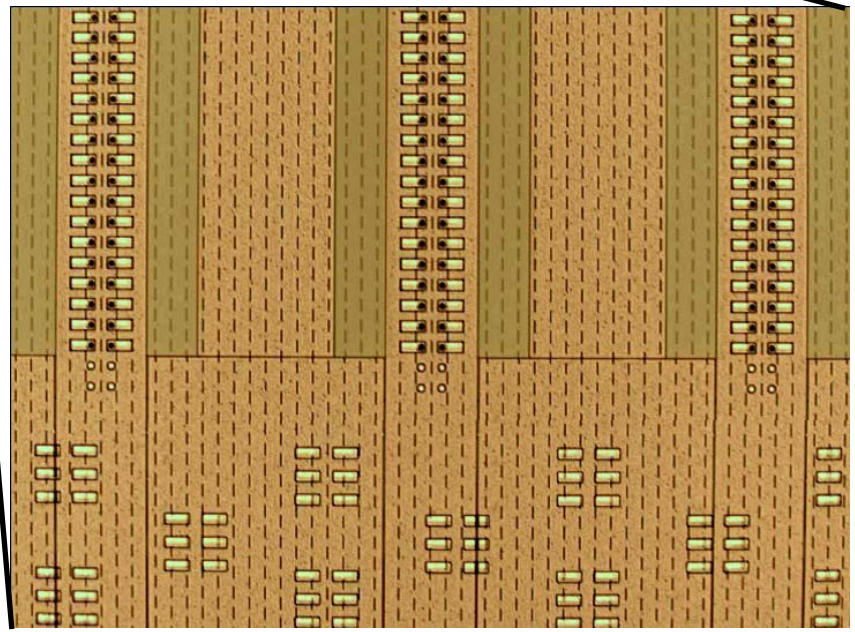


FE-I3 read-out chip

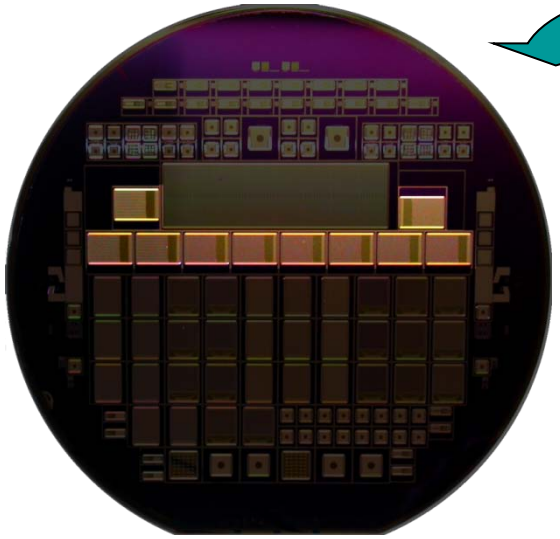
- 0.25 µm IBM, rad. hard design
- 7x11 mm^2, 2880 channels
- post processing on wafer level
- 5 µm Cu pads for SLID
- Pad size: 27 x 60 µm^2
- pitch in y: 50 µm



- diced chips placed face up on a handle wafer



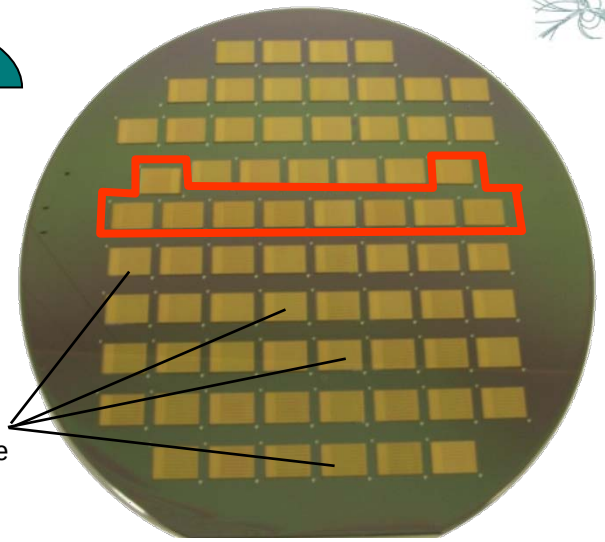
SLID: FE-I3 to Sensors



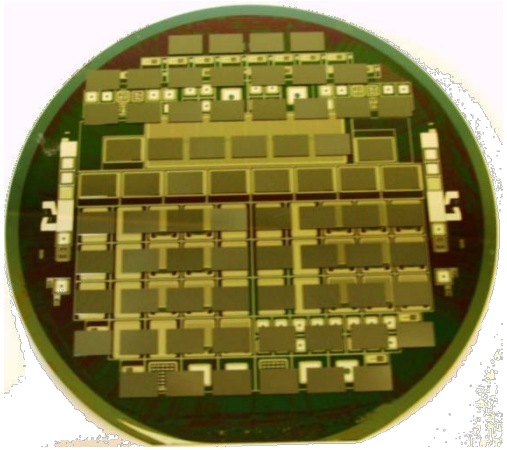
Sensor wafer, 75 µm active thickness

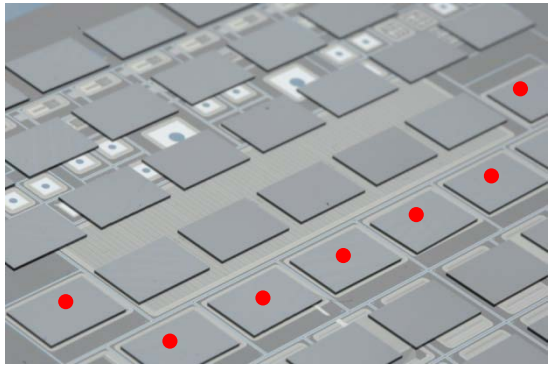
Fraunhofer EMFT

dummy chips to equalize pressure distribution

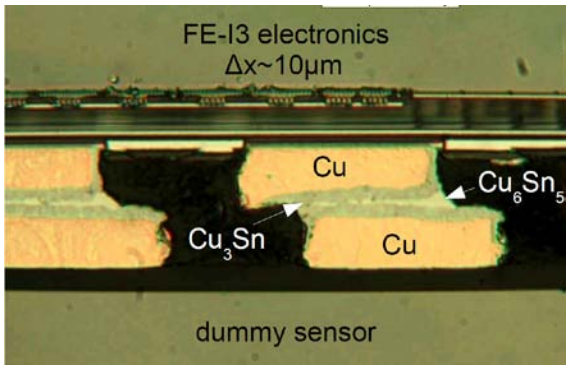


FE-I3 chips reconfigured on a 6” handle wafer



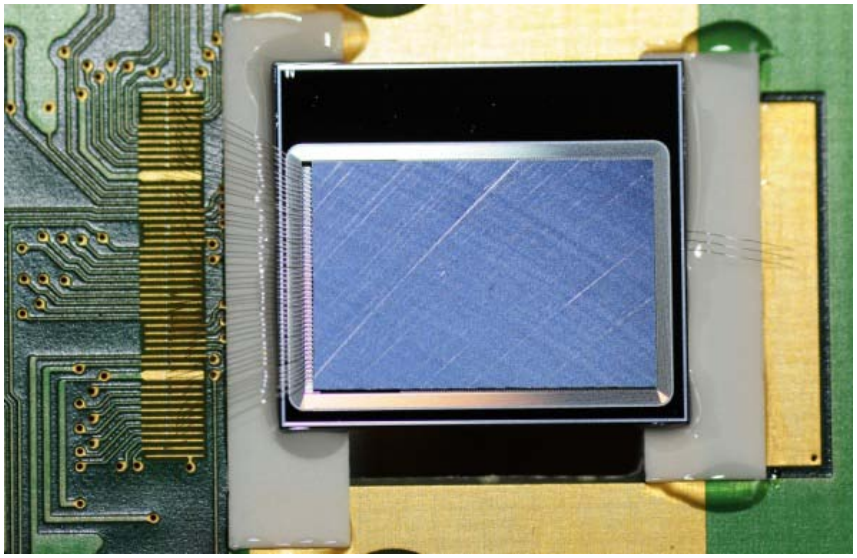


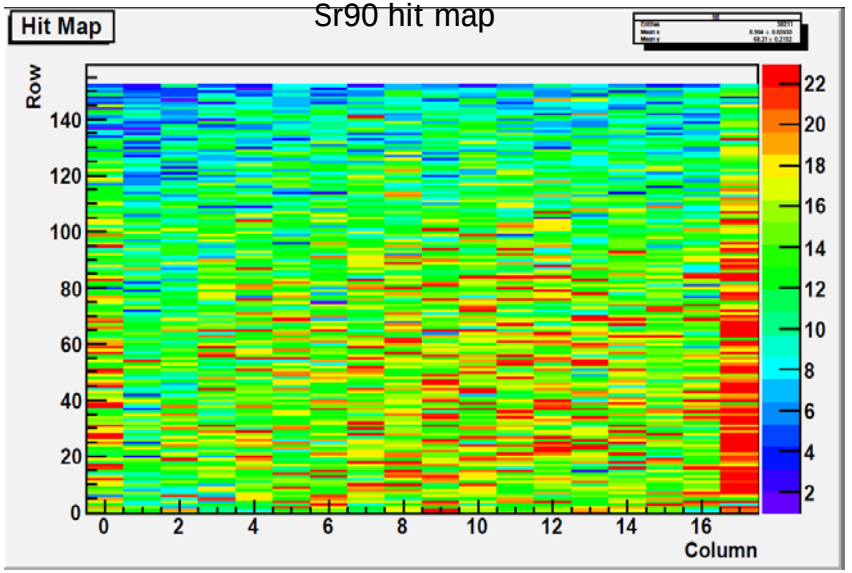
After SLID and handle wafer removal



Lab tests

- Five sensor/chips pairs mounted on single chip read-out cards (SCM)
- → all SCMs are functional!

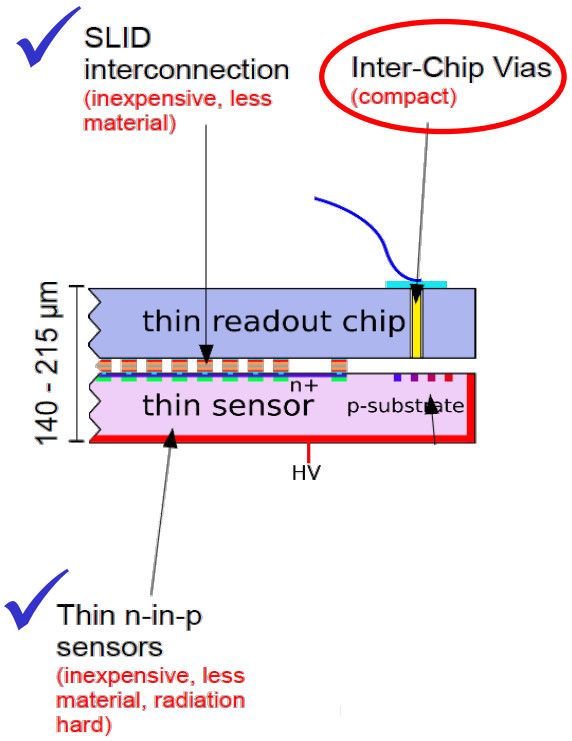


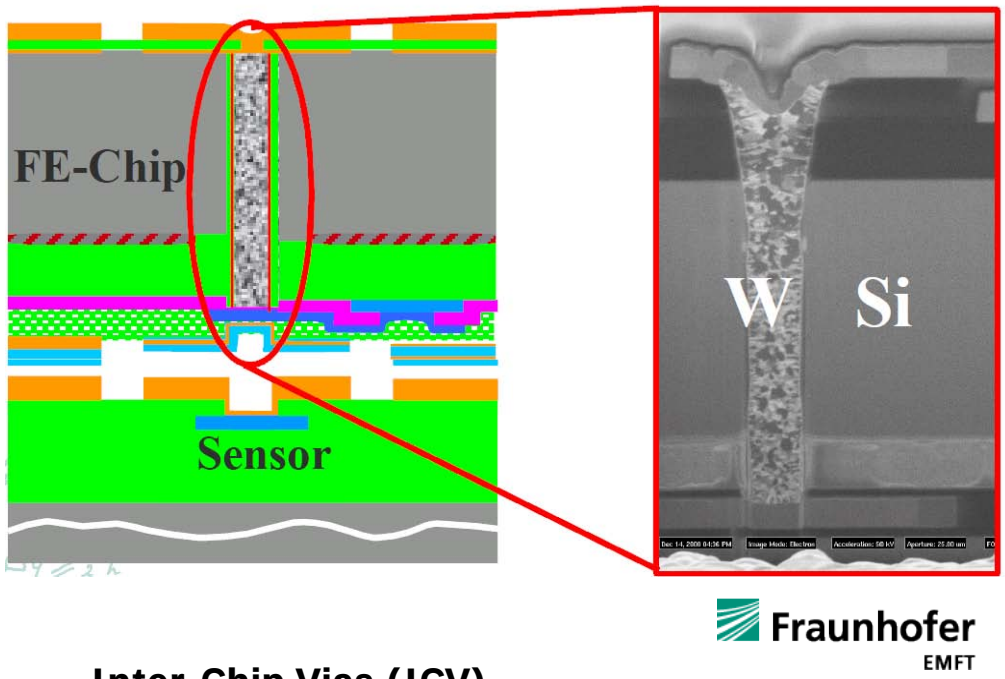


- contact yield measured on a precursor production: 99.95%
- pull and shear test results similar to conv. bump bonding (~0.01 N/connection)

- beam tests at CERN followed → no difference to conv. bump bonded modules

Inter-Chip Vias ICV → TSV



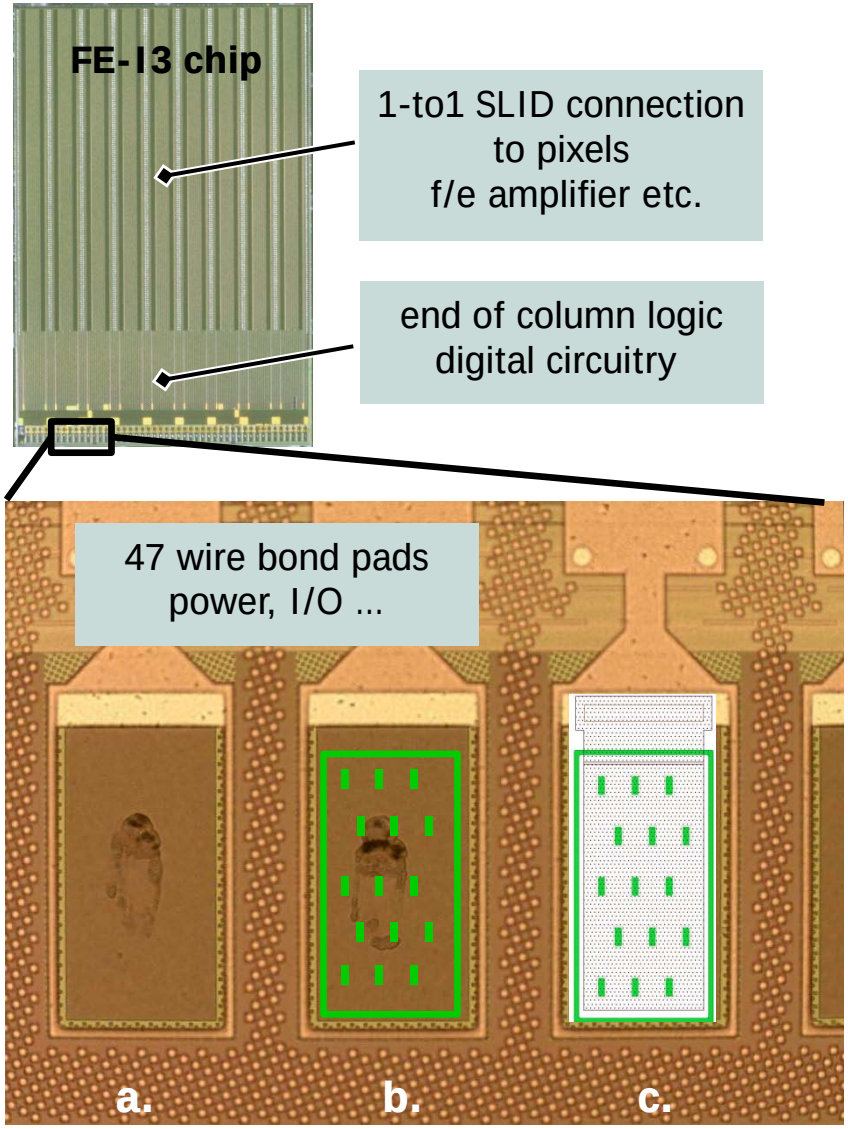


Inter-Chip Vias (ICV)

- Allow for vertical signal transport through Si structures
  → Compact pixel modules

- post-processing of the FE-I3 wafer (“via last” approach)
  - via etching on front side (Bosch-process), isolation, and tungsten filling
  - back side thinning of the wafer
  - isolation and metallization for the back side contact (wire bonds)

Location of the vias (for the demonstrator)

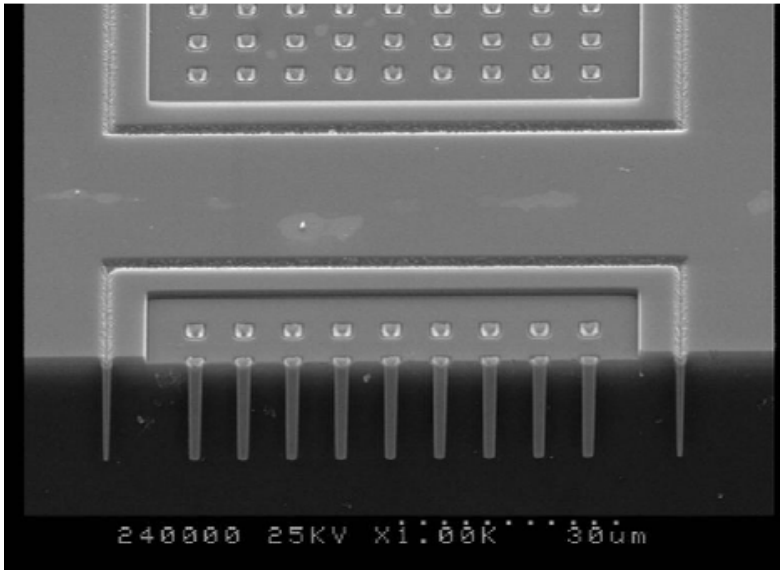


wire bond pads → back side of the chip

a.) remove pad metal (Alu)

b.) etch blind vias from the front side
3x10 µm², ~70 µm deep

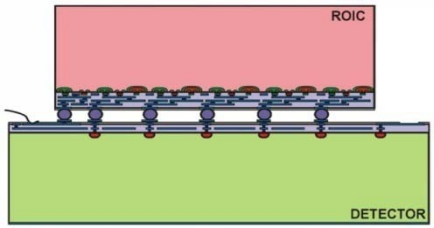
c.) connect via metal to pad metal on the front



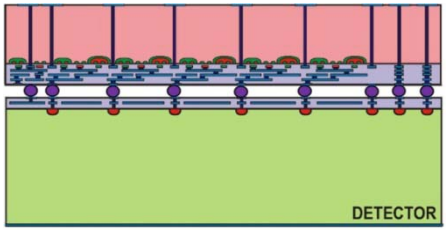
FIB image of test samples showing the structure of the vias and the trench around them.

In Summary

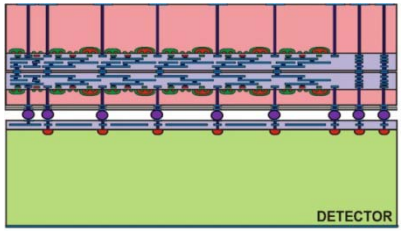
- Hope I convinced you a about the importance and significance of the link between sensors and read-out electronics
- And I hope that you got a little bit of the taste of this field of R&D and processing
- I had to skip a lot: TAB Bonding, different bump materials, various techniques of bumping...
- And I did not talk at all about 3D integration, a very active field of R&D and innovation, both in industry and in the detector community



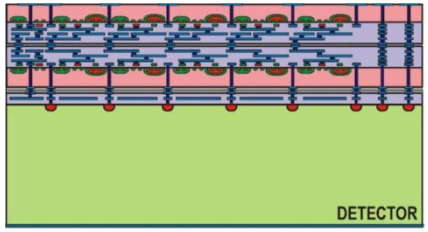
wire and bump bonding



through silicon vias



chips stacking with TSV



bump-less interconnect with chip stacking and TSV

- integrated silicon frame