Triggering Philosophies for Large Nuclear Physics Experiments

ANSIP 2011, Acireale

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Overview of talk:

- ***Introduction:***
  - *Why do we make triggers?*
- ***How do we make triggers?***
  - *Examples of Trigger Systems from 1980 to 2011*
- ***Time stamped systems and software triggers***
  - *Time stamping data and software triggers*
  - *Advantages of software triggering.*
  - *TS components and problems to consider.*
- ***Examples of time stamping systems***
- ***Living in the real world***
- ***Conclusions***

Why do we make triggers? (1)

- ***Why don't we just save everything from all detectors?***
  - *Volume of data (storage + writing bandwidth)*
  - *Computing power to replay it*
  - ***Correlation- what happened when?***
  - ***What data belongs together?***
  - *All the data is useless unless correlated.*
- ***Triggering is about correlation.***
- ***To correlate we need to know the time***
  - *Hardware coincidence (defines time window)*
  - *Software coincidence using time stamps (on/offline)*

Why do we make triggers? (2)

- ***Triggering is about correlation.***
  - *To select interesting data from background*
    - *e.g. Multiplicity requirements for high spin gamma*
  - *To select coincidences between sub systems*
    - *e.g. Prompt gammas + isomer detector*
    - *e.g. Prompt gammas + focal plane of spectrometer*
    - *e.g. Layers of a particle tracker*

- ***A side effect is that hardware triggering cuts down the rate and volume of data to the DAQ.***
  - *No choice- hardware trigger selects data*

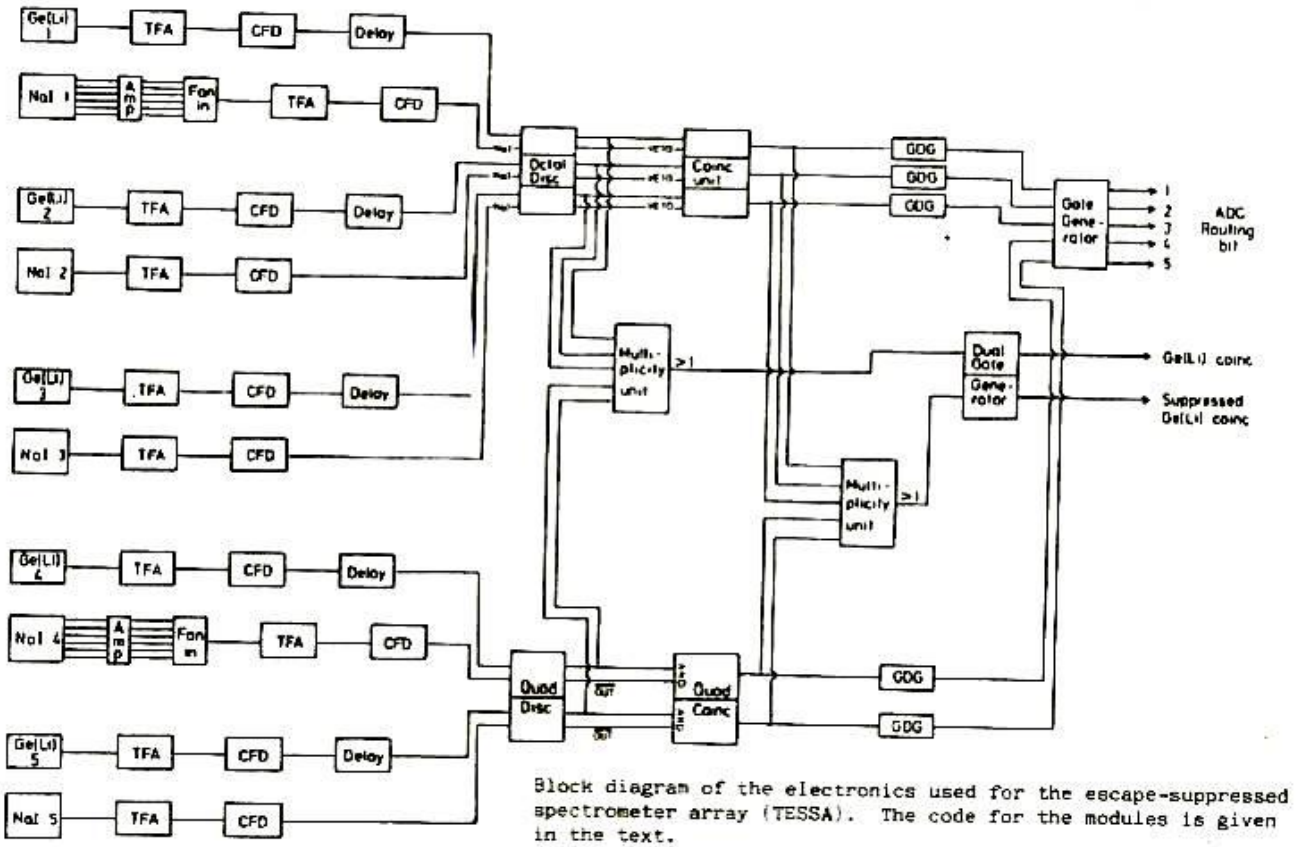
How do we make triggers?

Timeline- some NP trigger systems (UK collaborations)

- *TESSA c. 1980 Simple multiplicity coincidence (5 dets)*
- *Eurogam 1990-1994 (Euroball 1994-2002, EXOGAM)*
  - *2 stage trigger/val (allows later decision from recoil)*
  - *Introduced reprogrammable logic (FPGA) to replace cables*
  - *Local intelligence for parallel or pipelined operation as well as normal Common Dead Time*
- *GREAT 2000-> Time stamped data labelling*
  - *Total Data Readout- Read it all and trigger online in software.*
  - *Software front end gate*
- *NUSTAR White Rabbit (Used by AIDA & R3B Si tracker)*
  - *Time stamped (White Rabbit)*
  - *Hardware front end gate*
  - *Software front end gate*
  - *Software trigger*

Examples of trigger systems (1)
Simple hardware coincidence trigger

FIGURE 3.5



Block diagram of the electronics used for the escape-suppressed spectrometer array (TESSA). The code for the modules is given in the text.

TESSA array
@NBI
Circa 1980

5 Ge(Li) with Escape suppression

From J.Simpson's thesis

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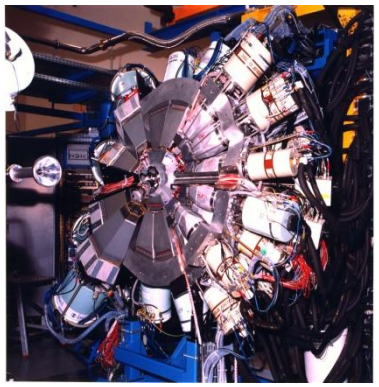
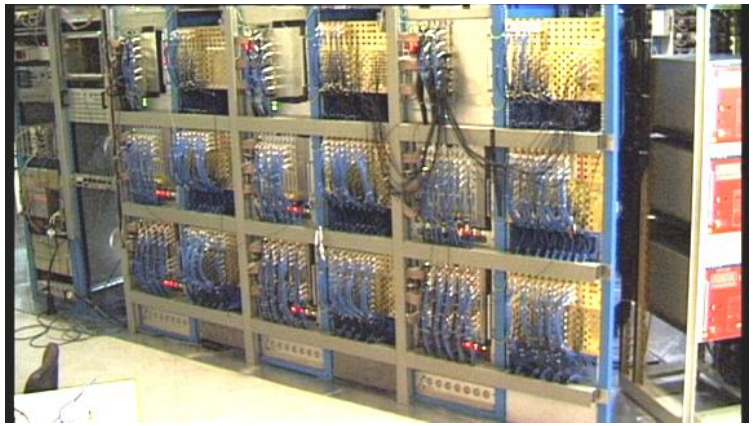
Examples of trigger systems (2)

Eurogam/Euroball (1991 NSS)
Central programmable hardware trigger
Intelligent "local trigger" controls channels





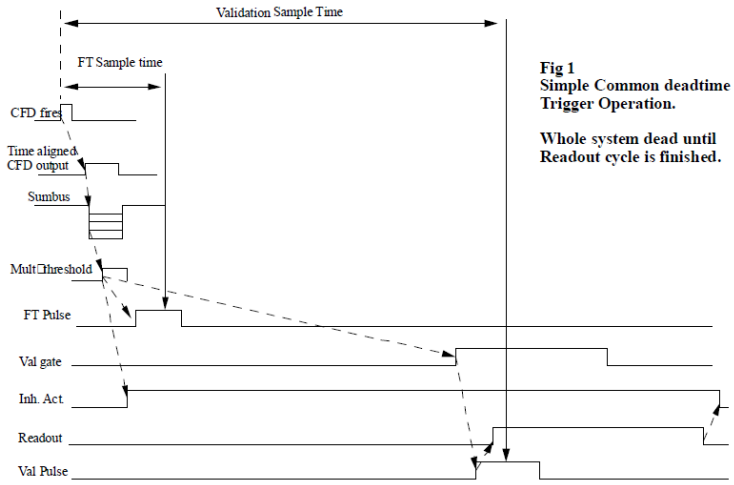
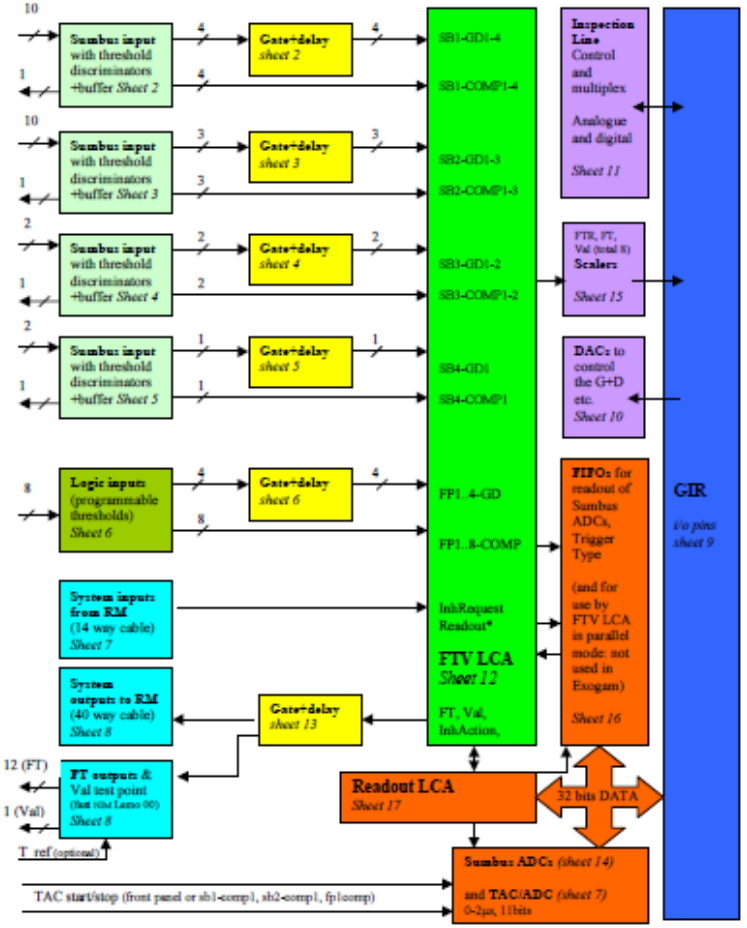


Fig 1
Simple Common deadtime Trigger Operation.

Whole system dead until Readout cycle is finished.



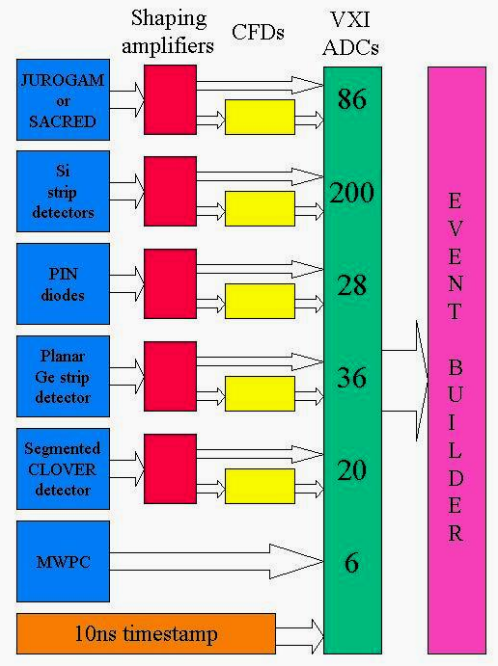
Lazarus et al. IEEE TNS Vol 39 (5) p1352 October 1992

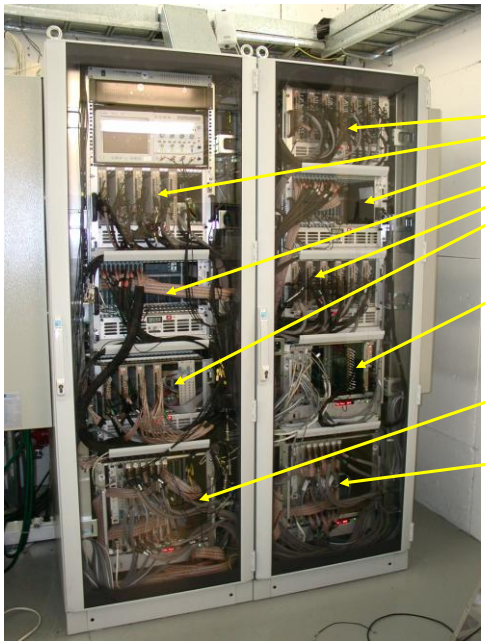
Lazarus et al. IEEE TNS Vol 48 (3) p567-569 JUN 2001

Examples of Trigger systems (3)

GREAT TDR (2000 NSS)

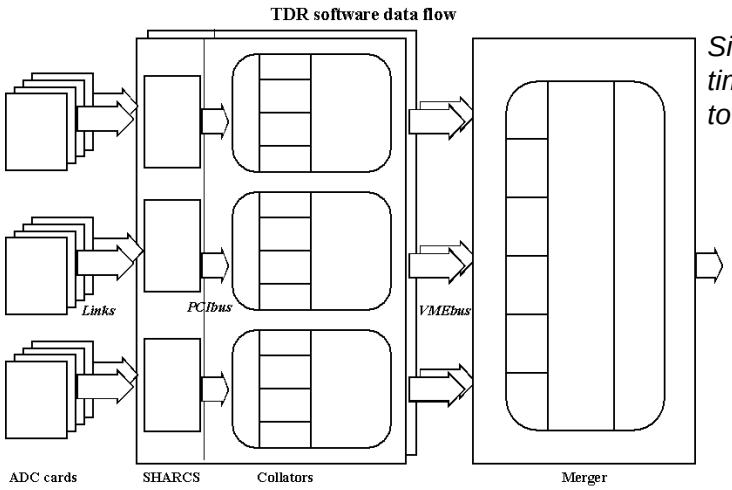
Time Stamped



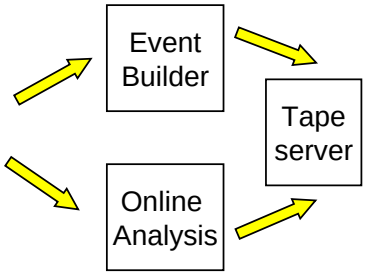


Rack includes

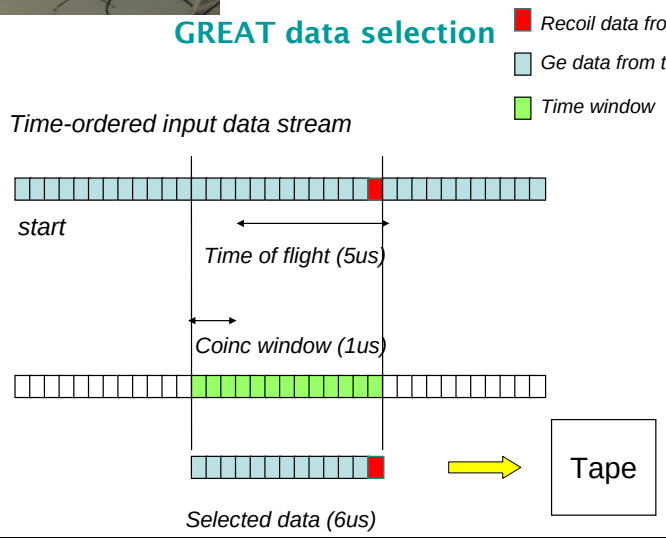
- 4 NIM and 2 CAMAC for front end Amps, CFDs.
- A VME crate (data merger, metronome and pattern unit)
- 2 VXI crates containing between 12 and 15 32 channel cards (up to 480 channels).



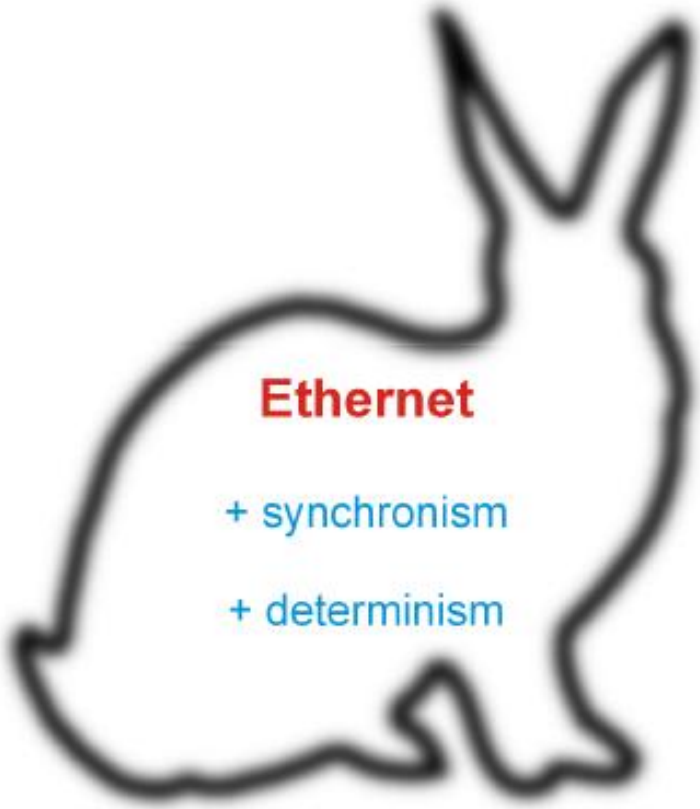
Single stream of time ordered data to event builder.



GREAT data selection



Examples of Trigger systems (4)
NUSTAR (White Rabbit)
Time Stamped over Ethernet



Time Stamped Trigger Systems- Principle

- *Trigger = correlation. Correlate data by sending a time stamp as a label with data from each channel.*

- *Also possible to give one time stamp to each event in a hardware triggered sub-system. (1993 Daresbury RDT setup, later TITRIS, CENTRUM)*

- *Time stamps must have a fixed time relationship to the moment when the channel fired or event generated.*

Software Triggers for time stamped systems

Now that all data is labelled with time stamps...

... we need to decide- how much data will my experiment generate? Is it possible (or useful) to collect all the data?

Yes. *Just write it all to disk. Use offline data selection.*

- *Can be repeated with different trigger algorithms*
- *Usually used for testing and development only*

*Normally **no**- so use online data selection = software trigger*

- *Save only useful data- cuts down data volume to analyse*
- *No second chances*

Advantages of software triggering (1)

- *Huge increase in trigger flexibility:*
  - *Time travel! Software can look back/forward in time (time =buffer size)*
  - *Perfect for low rate data in delayed coincidence with high count rate (e.g. Recoil Decay Tagging- GREAT)*
- *Eliminates trigger dead time, But...*
  - *Doesn't help with pileup (signal shaping vs count rate)*
  - *Doesn't help with readout dead time if DAQ is too slow*

Advantages of software triggering (2)

- *Less cables, less connectors = more reliability*
  - *Need only 1 fibre or cable per crate or card.*
  - *Correlate multiple systems without cross-triggering cables (no delay/ground problems over long distances)*
  - *Removes NIM "spaghetti" cabling*
  - *Cutting out hardware trigger connections improves reliability (no problems from cables, ground/isolation)*

If it's so good why doesn't everyone do it?

- *Needs new hardware to insert time stamps*
- *Some experiments are so simple that they don't gain a lot.*
- *Software trigger can't be set up by oscilloscope- a different way of working. (Trust the software!)*

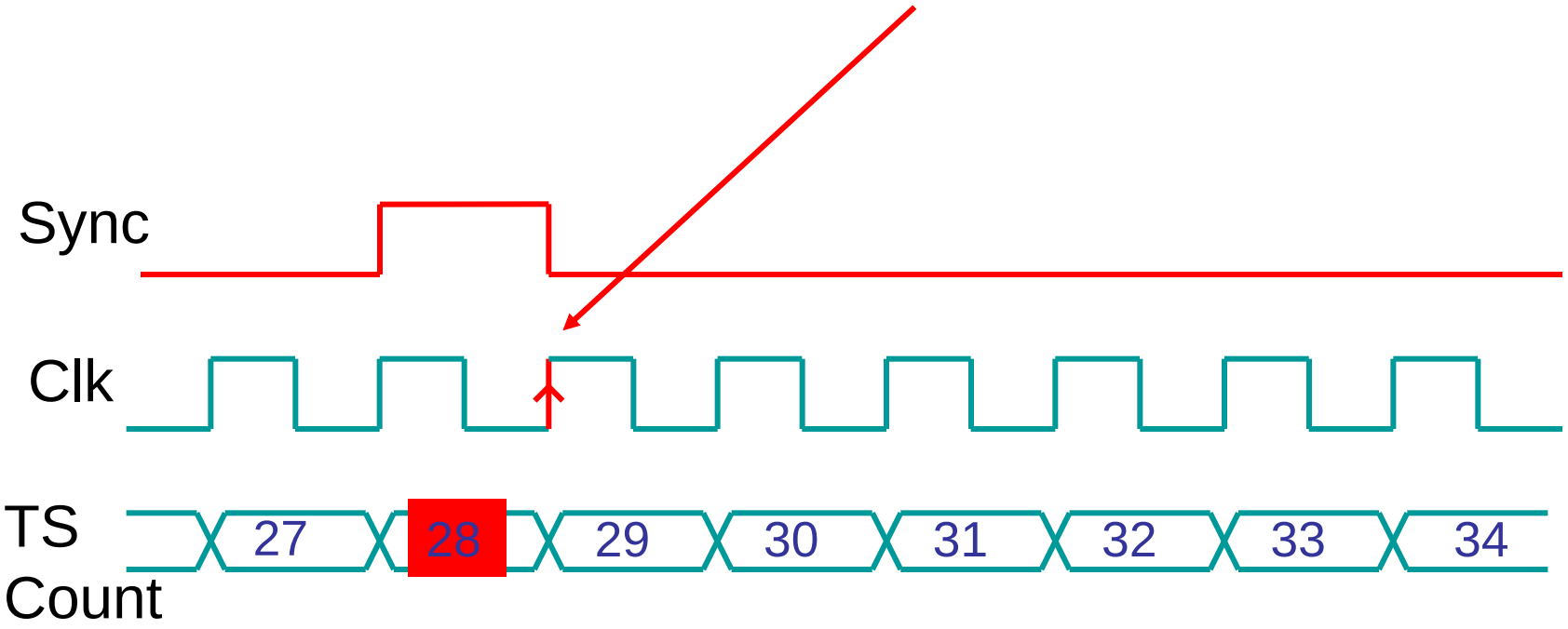
Summary so far

- *Triggering is all about correlation of data*
- *Time stamping data allows versatile correlation (less limits than hardware triggers)*
- *Software triggering selects data online or offline. Must be a trigger selection sometime.*
- *Software triggering increases flexibility and reliability- time travel is possible!*
- *Now- how do we actually do time stamping?*

Time stamp components (1)

- *Clock (very well matched) to all FEE*
- *Data must be time stamped with good timing*
  - *e.g.CFD on a channel*
  - *e.g.Trigger from subsystem (many channels)*
- *Sync is needed (to give a time value to clock)*
  - *Time value can be preloaded or sent with sync*
  - *Time frames for the data **and for no data***
  - *Set up TS, check TS, insert timing frame to data*

GREAT Sync protocol
Insert timeframe in data
and check local TS count now.



Time stamp components (2)

- *Data format must include TS with enough bits to avoid ambiguity from:*
  - *Buffer depth or throughput variation (low/high rate)*
  - *Signal processing differences*
  - *Physics processes (decays can take many hours)*
  - *16 bits @ 100MHz = 655us*
  - *32 bits @ 100MHz = 42.9 seconds*
  - *48 bits @ 100MHz = 32.6 days*
- *Don't always need to send all TS bits (e.g. use headers/packets)*

Problems to overcome (1)

- *Need **time stamps in ASICs** (or timing outputs) some designs include this now*
  - *N-XYTER*
  - *CALICE and PIMMS MAPS (in-pixel TS)*
  - *AIDA (via timing outputs)*
  - *R3B Si ASIC...*
- ***Latency**- doesn't matter until making connections to other sub-systems using analogue triggers (see later)*
- ***Buffer edge effects** (true for both time and physical channels- the end of time!)*

Problems to overcome (2)

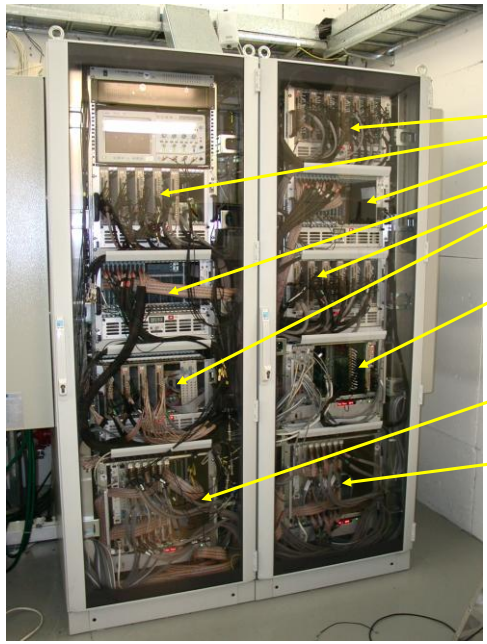
- ***Time alignment*** *(setup) is critical*
  - *sub ns for AGATA PSA*
  - *for simple coincidence must be better than half a clock across all systems*
  - *if using for ToF then must be few tens of ps (or equivalent stability and well calibrated)*
- ***ToF*** *using clock as stop is only as accurate as the TS clock after alignment and jitter errors.*
  - *For ps ToF timing we still need to use TAC/TDCs*
  - *Should also calibrate the ToF channels for clock alignment errors*

Examples of NP Time Stamping Systems

- *GREAT TDR (UK/Finland, Jyvaskala)- working*
- *TITRIS (GSI)- working*
- *CENTRUM (and ATOM) (GANIL)- working*
- *AGATA GTS system (Europe) working*
- *White Rabbit (GSI/FAIR/CERN) Partially Built*
- *White Rabbit + AIDA (NUSTAR DeSpec) Mostly built*
- *R3B Si tracker (+ links to CALIFA)- Under design*

Time Stamp example 1 - GREAT TDR (2000 NSS)

Operating since 2003



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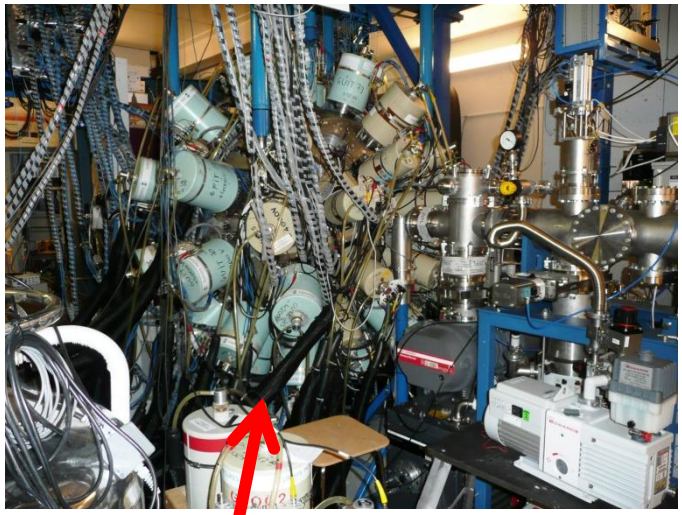
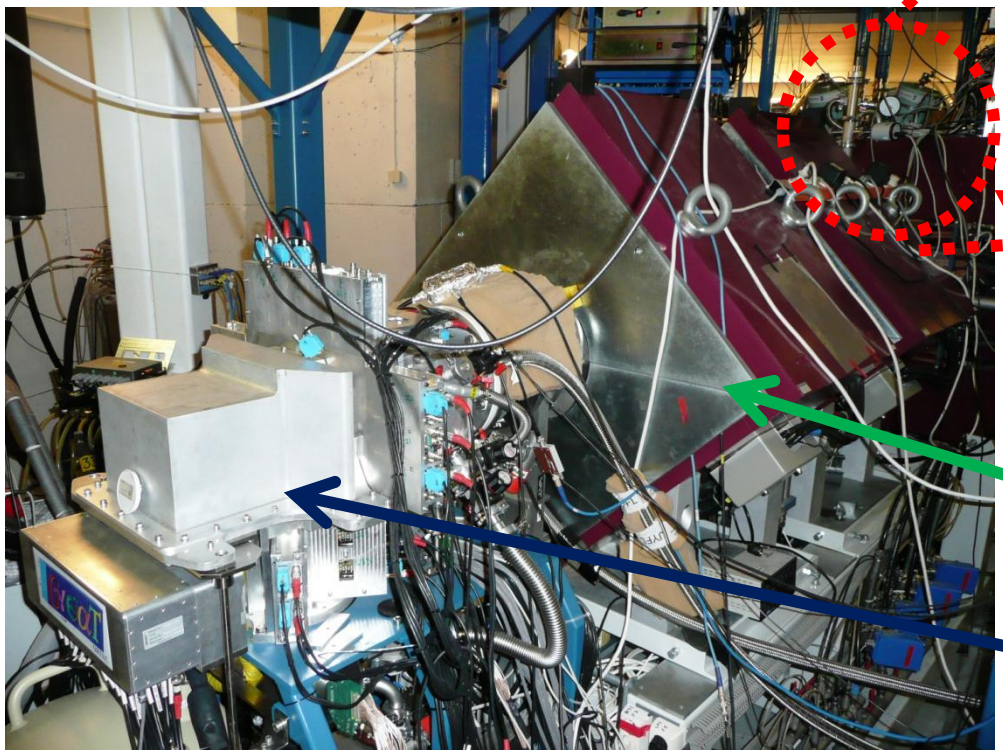


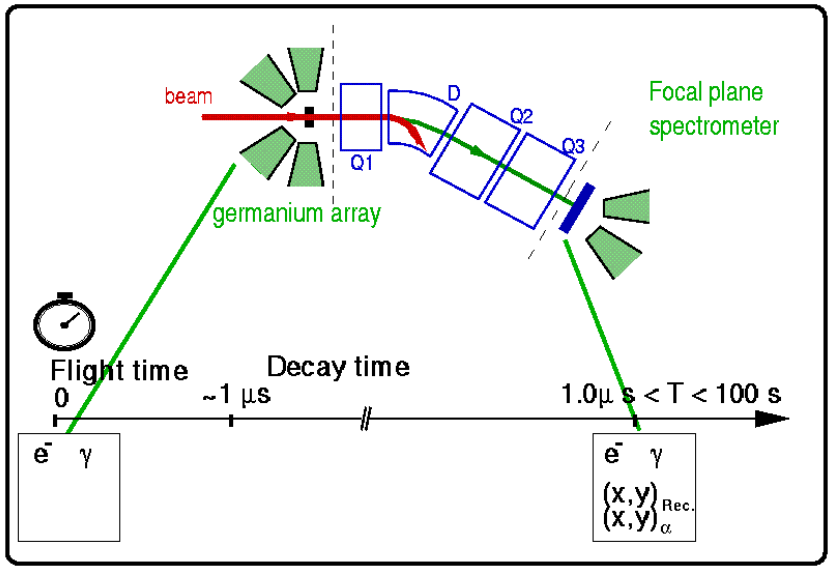


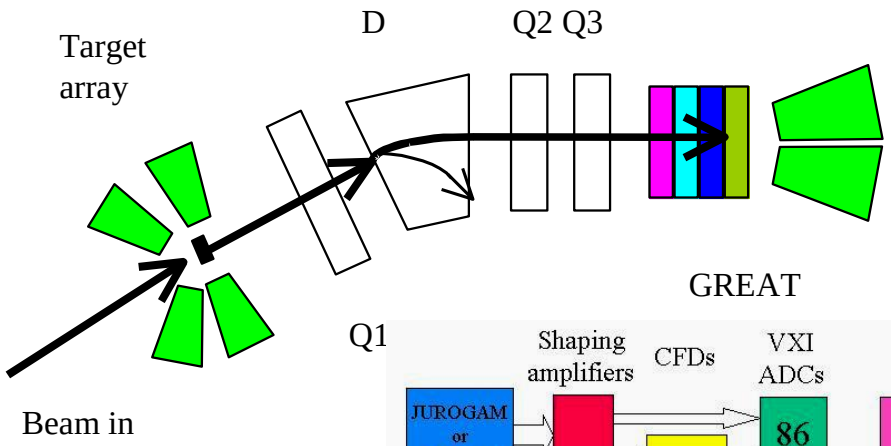
Target Position Jurogam

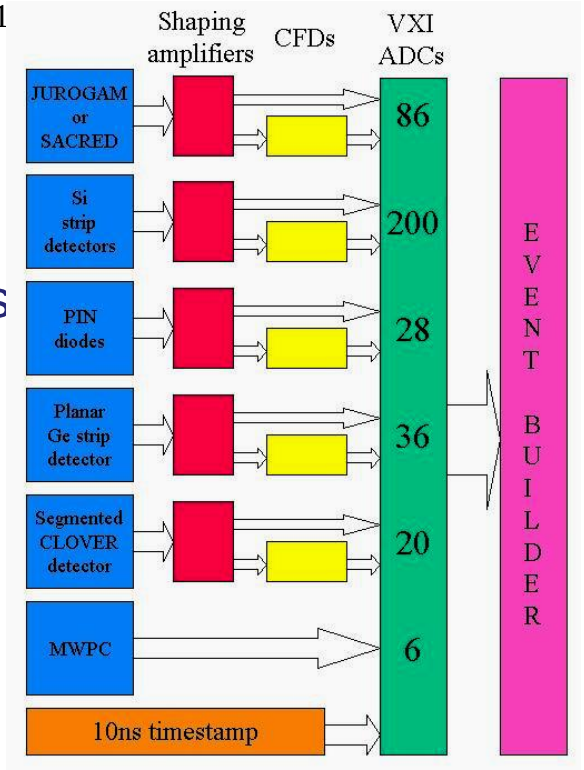
RITU separator

Focal plane- GREAT

GREAT- example of software triggering







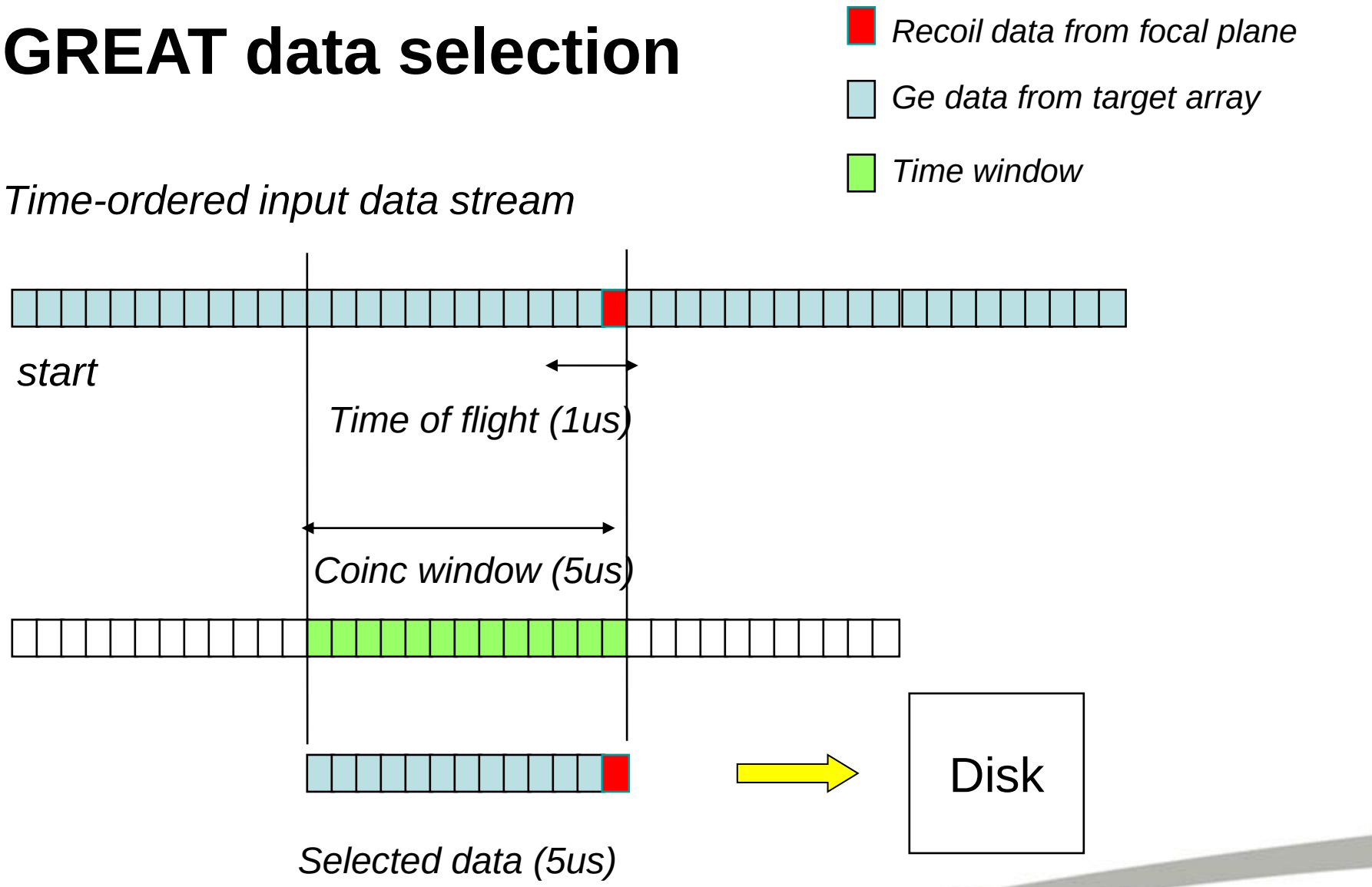
Gamma/electrons at target. GREAT at focal plane has Recoil ID, conversion electrons, alpha, beta, gamma.

Analogue signal processing- time stamp with CFD

Software trigger rejects single gammas from target.
Accepted data meet one of these 2 criteria:

1. n-gamma > 2 (regardless of focal plane)
2. Everything in a 5us window before focal plane TS

GREAT data selection

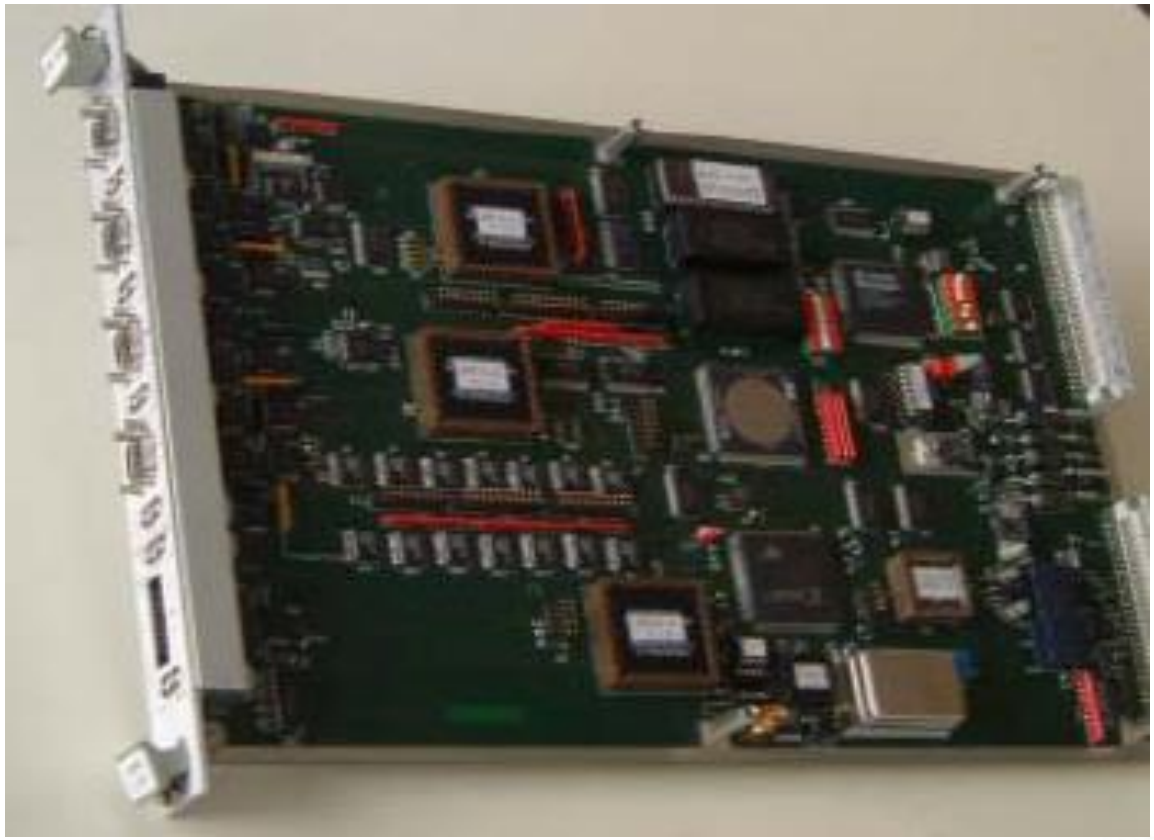


GREAT software trigger and data rates *(from Pete Jones, ex-JYFL)*

- Target position: 10-30kHz singles, 111 Ge crystals, generating 10 to 30Mbytes/sec (max 40 Mbytes/sec)
- Time of flight through RITU- approx 1us
- FP detectors- approx 10-30kHz rate (of which 3-9kHz is implant/decay rate in Si). Corresponding FP data rate is 150-450kBytes/sec from all FP detectors.
- Data filter removes about 20% of data from tokens, flags, overflow etc. and looks for s/w triggers in 8-24Mbytes/sec.
- Output rate to disk recoil+5us coinc window events at 0.5-1.5MBytes/sec or gamma doubles too at 5.5-16.5Mbytes/sec
- Filter Machine- quad core 9950, 2.6GHz, few GB memory (4096 buffers of 64k are used)

Time Stamp example 2
CENTRUM (Spec 2001, h/w 2003)

- *CENTRUM Time Stamps Events (not channels)*
- *Correlates EXOGAM with VAMOS and TIARA*
- *ATOM upgrade adds channel time stamp functionality*
- *Gilles Wittwer (GANIL)*



Time Stamp example 3- AGATA design 2001-6 physics from 2009

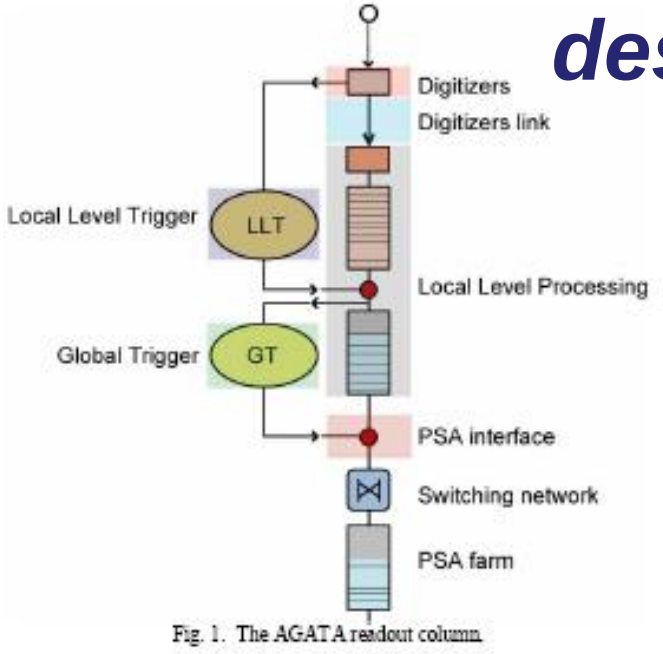
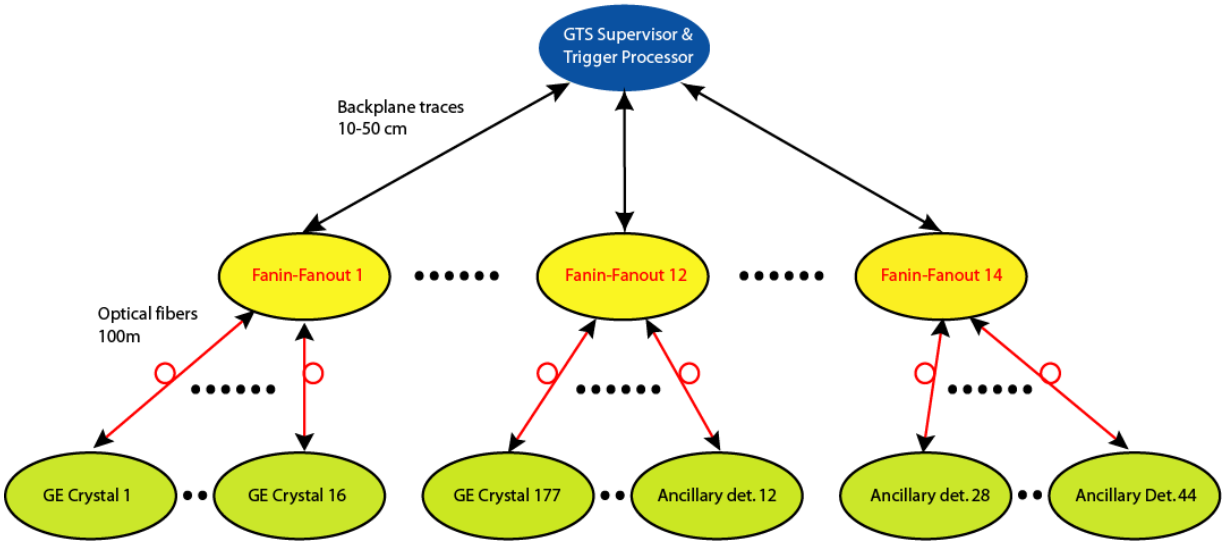
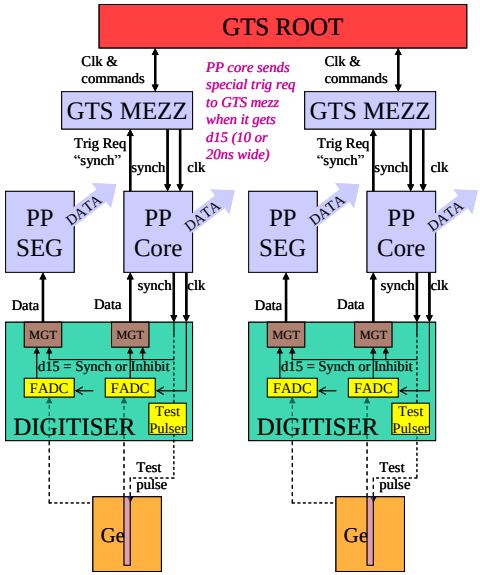


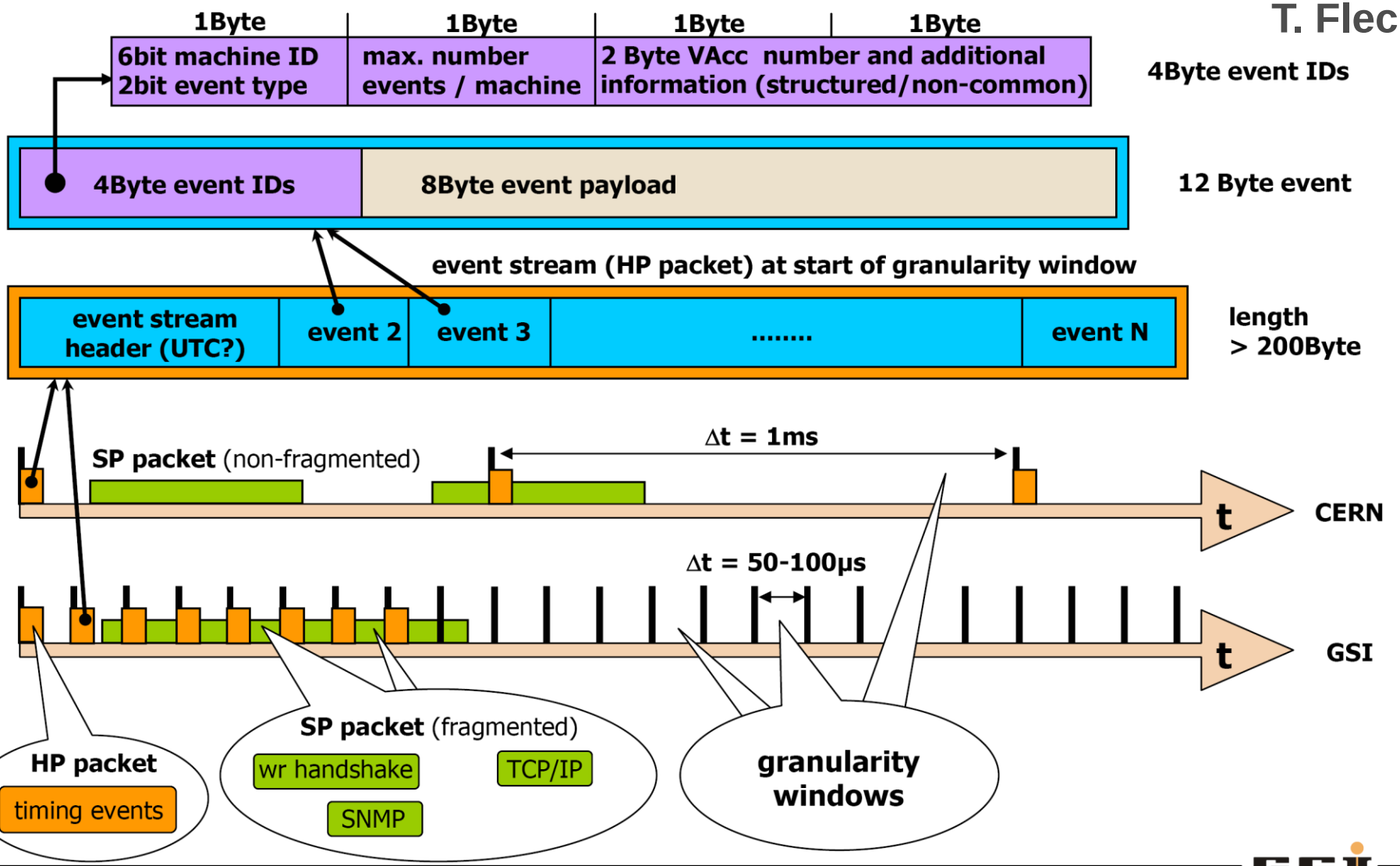
Fig. 1. The AGATA readout column





Bellato et al.
IEEE TNS Vol 55 (1) p91-98 FEB 2008

T. Fleck

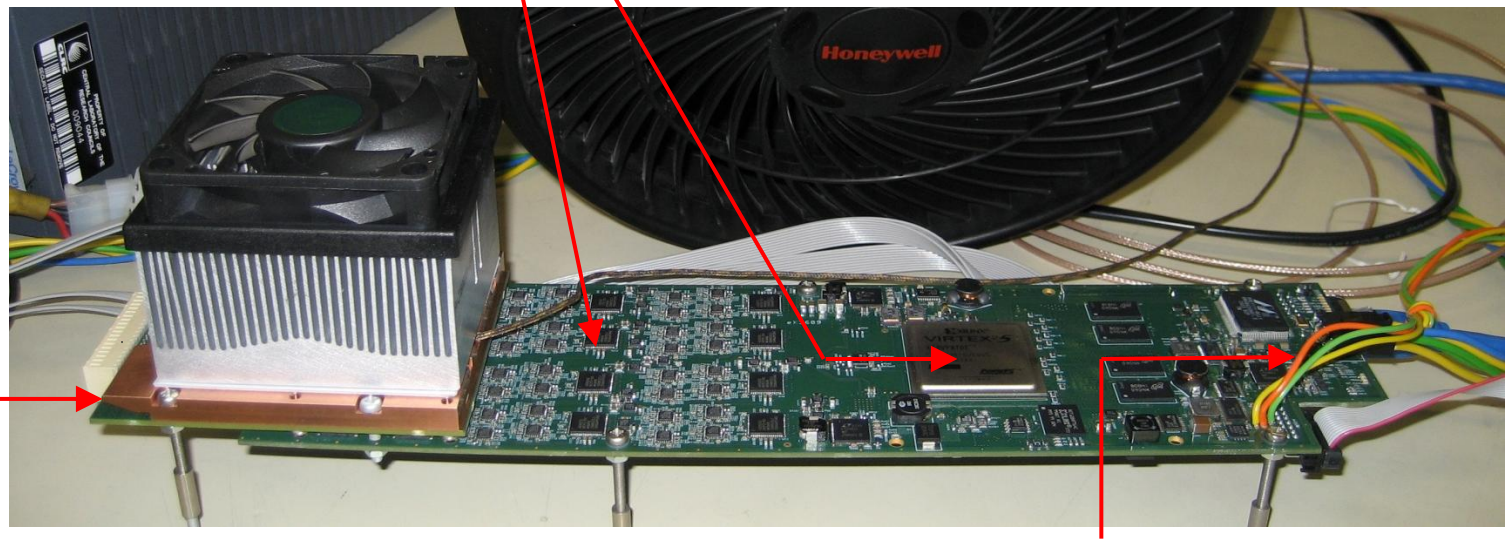


Time Stamp example 4 – White Rabbit

Time Stamp example 5
AIDA (NUSTAR, DeSpec)

Mezzanine:
- 4x 16 channel ASICs
- Cu cover
  - EMI/RFI/light screen
  - cooling

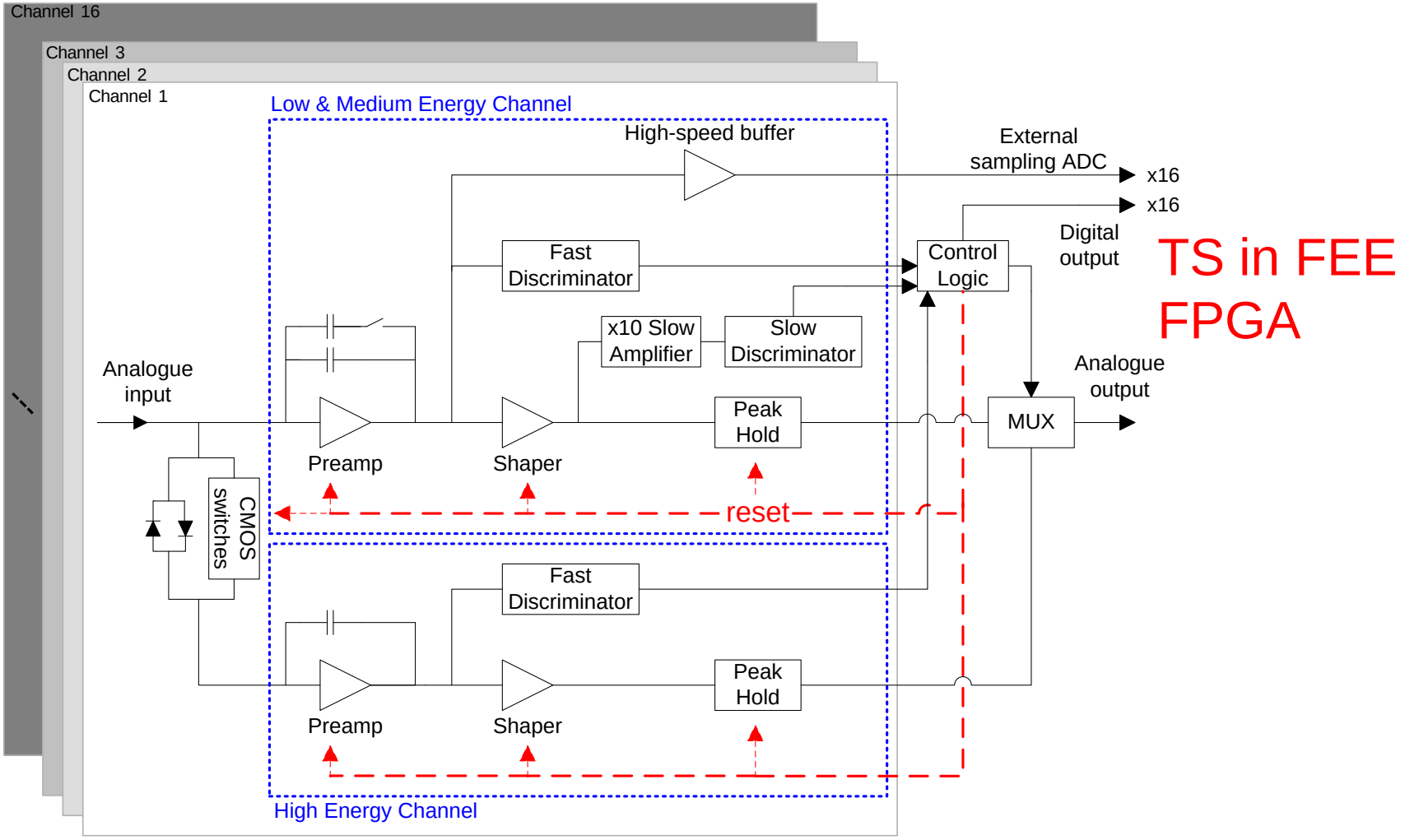
FEE:
- 4x 16-bit ADC MUX readout (not visible)
- 8x octal 50MSPS 14-bit ADCs
- Xilinx Virtex 5 FPGA
  - PowerPC 40x CPU core/Linux OS – DAQ



FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power

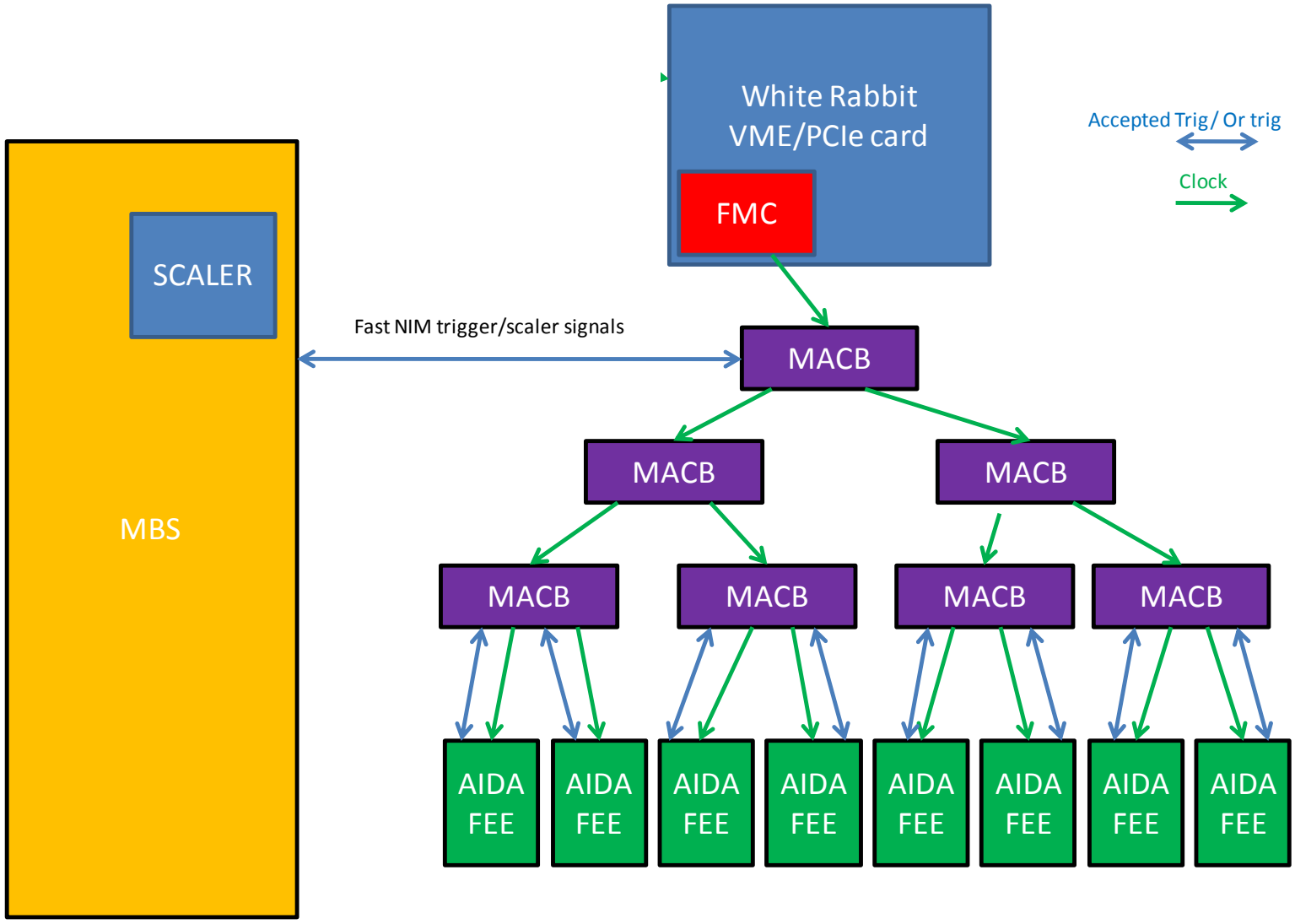
Time Stamping example 5
AIDA (NUSTAR)

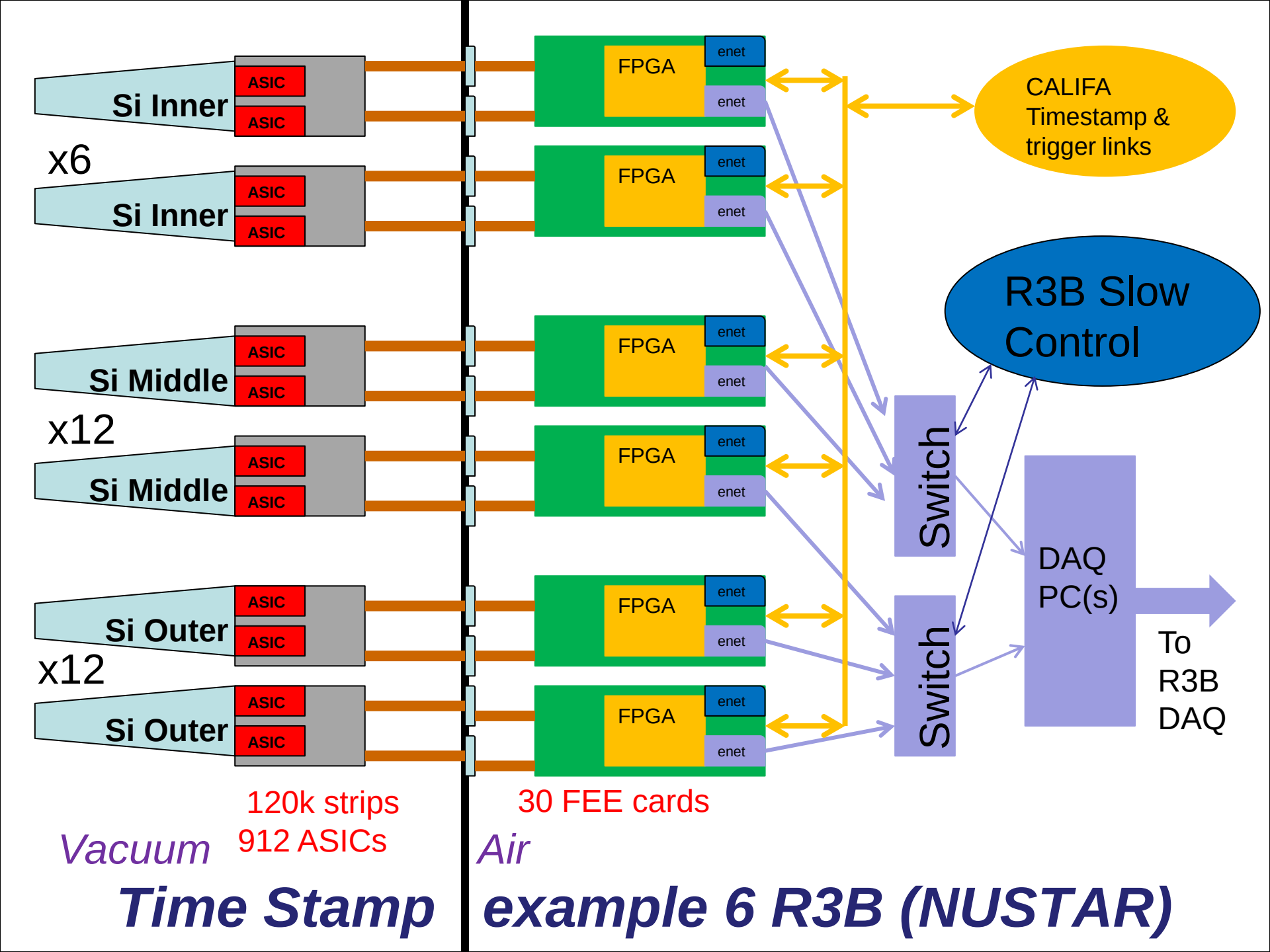


TS in FEE FPGA

Braga et al. 2009 IEEE NSS conf record, VOLS 1-5 P 1924-8

Time Stamp example 4/5 – NUSTAR (White Rabbit)




Si Inner
ASIC
ASIC
x6
Si Inner
ASIC
ASIC
Si Middle
ASIC
ASIC
x12
Si Middle
ASIC
ASIC
Si Outer
ASIC
ASIC
x12
Si Outer
ASIC
ASIC
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
CALIFA
Timestamp &
trigger links
R3B Slow
Control
Switch
Switch
DAQ
PC(s)
To
R3B
DAQ
120k strips
912 ASICs
30 FEE cards
Vacuum
Air
Time Stamp
example 6 R3B (NUSTAR)

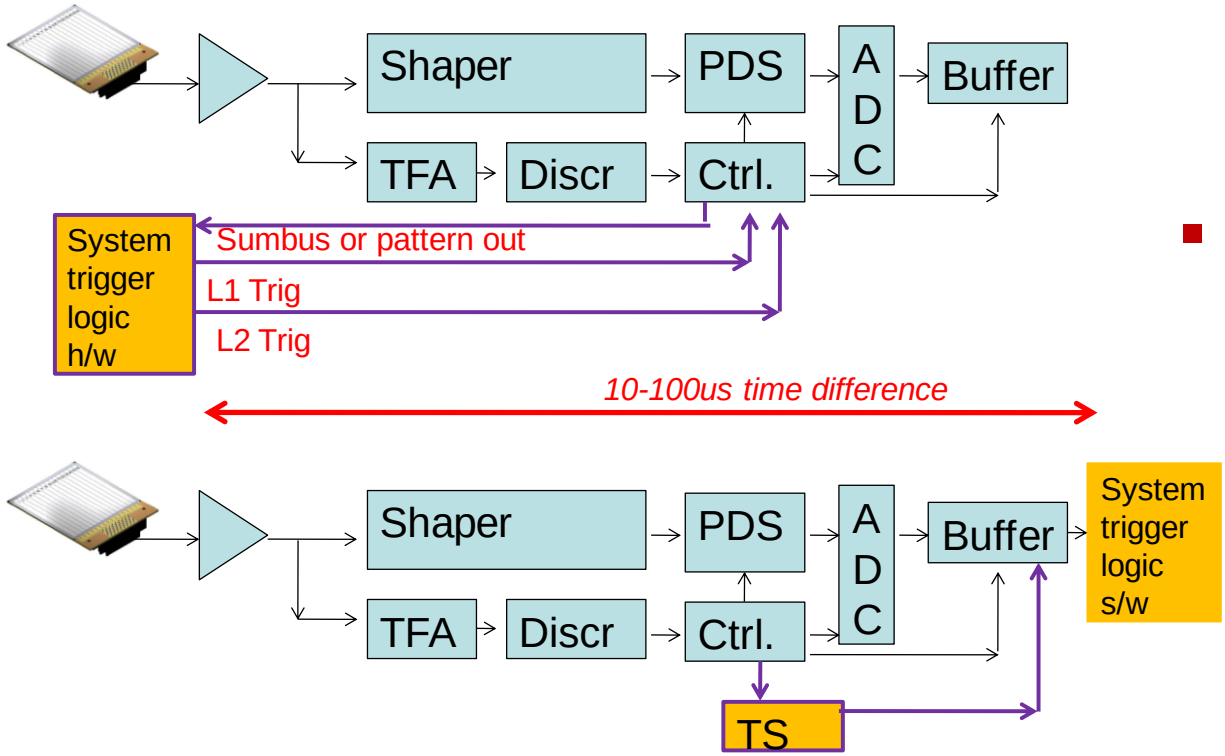
R3B Si tracker- possible s/w triggers

Examples of possible software triggers:

- *>= 2 Si layers fired within programmed coincidence window*
- *>= 2 Si layers fired and hits are on compatible faces (i.e. track, not random)*
- *>= 2 Si layers fired **AND** TS from CALIFA local processing fits the same time window*
- *TS from downstream detectors within fixed time window of Si hits.*

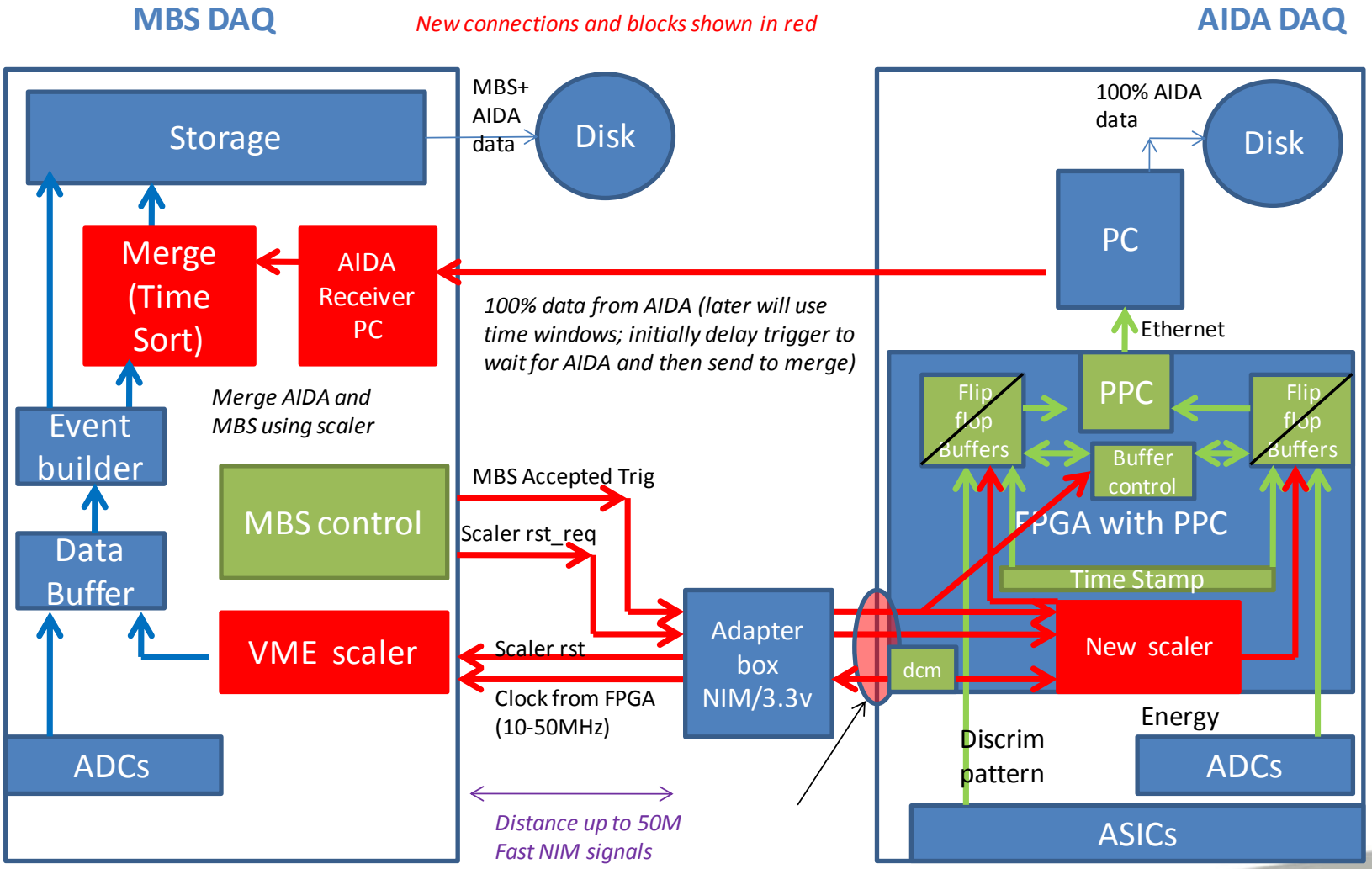
Living in the real world (1)

Legacy equipment needs an early coincidence trigger. But TS software trigger has latency. There are 2 solutions:



- *Run independently with common scalers*
- *Add extra "compatibility" output.*

Conceptual design follows discussion between Ian , Nik and Stephane at GSI and discussion at DL between Vic, Patrick, Simon and Ian



Linked scalers to correlate 2 systems

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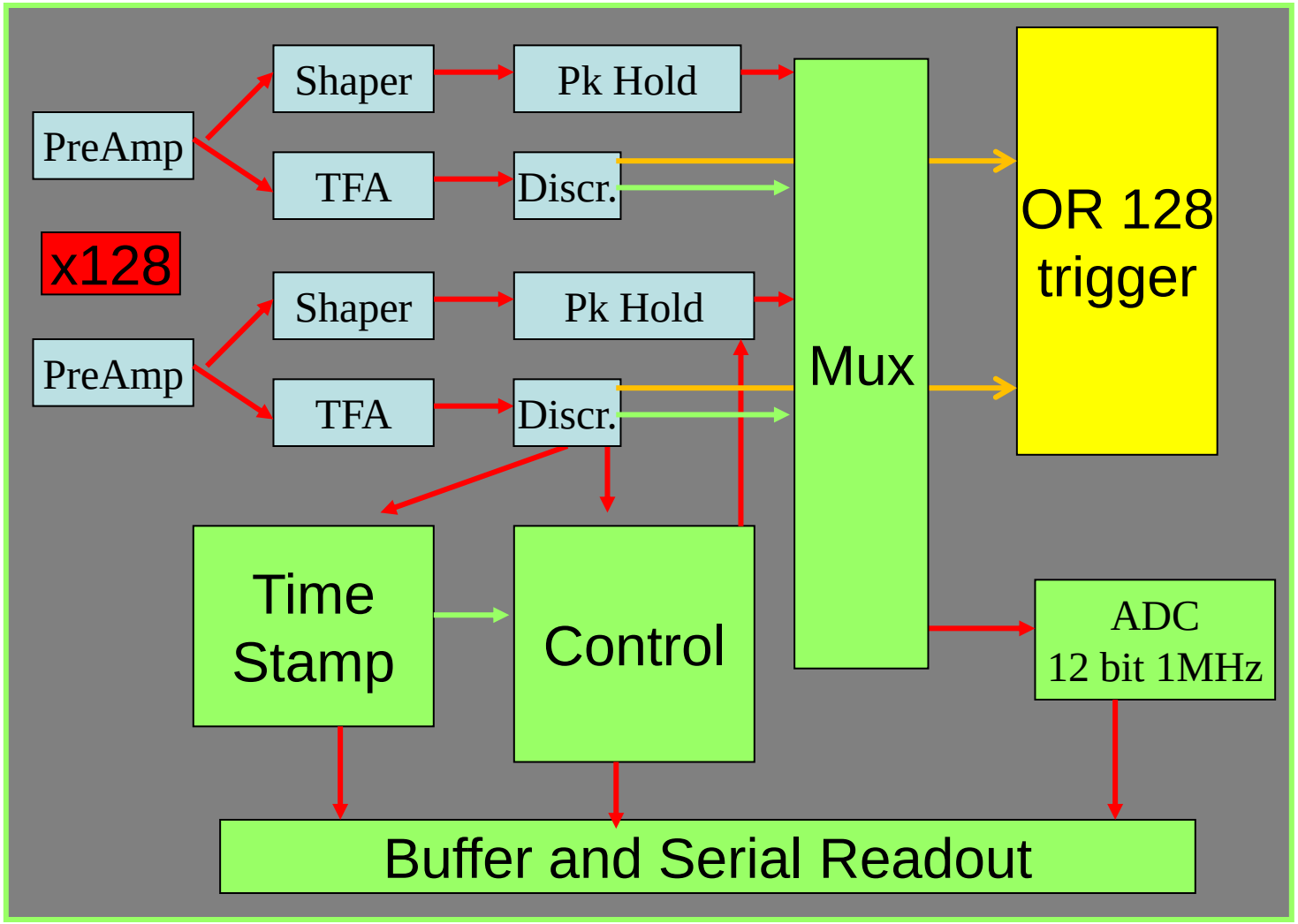

ASIC features:

- Time Stamp
- Zero Suppress
- On chip ADC

R3B Si Tracker ASIC (mid-design)

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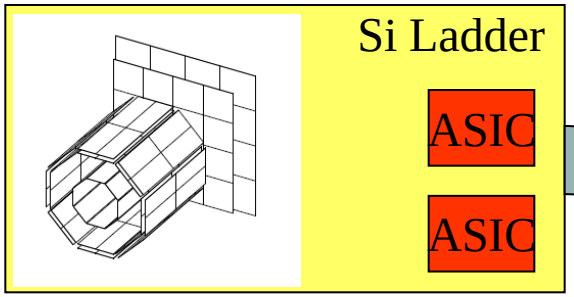
Nuclear Physics Group

R3B conceptual design for Si tracker FEE and DAQ with simulated data rates



100um Gold shield-
Max 210 MBytes/sec
100-300kBytes/sec/ASIC,
ave 225kBytes/sec/ASIC

NUSTAR Common DAQ

R3B input code module

Gbit Ethernet fibres

Total Data Rate:
No shield 5.7Gbytes/sec
(at least 189 fibres)
Gold cone 210Mbytes/sec
(at least 7 fibres)

FEE Card

Number determined by the data rate (depends on shielding)

With Au shield-30 cards

Fibre Ethernet

Slow Control

HDMI links

White Rabbit

HDMI link

MACB Fan out

Grey boxes show common NUSTAR elements

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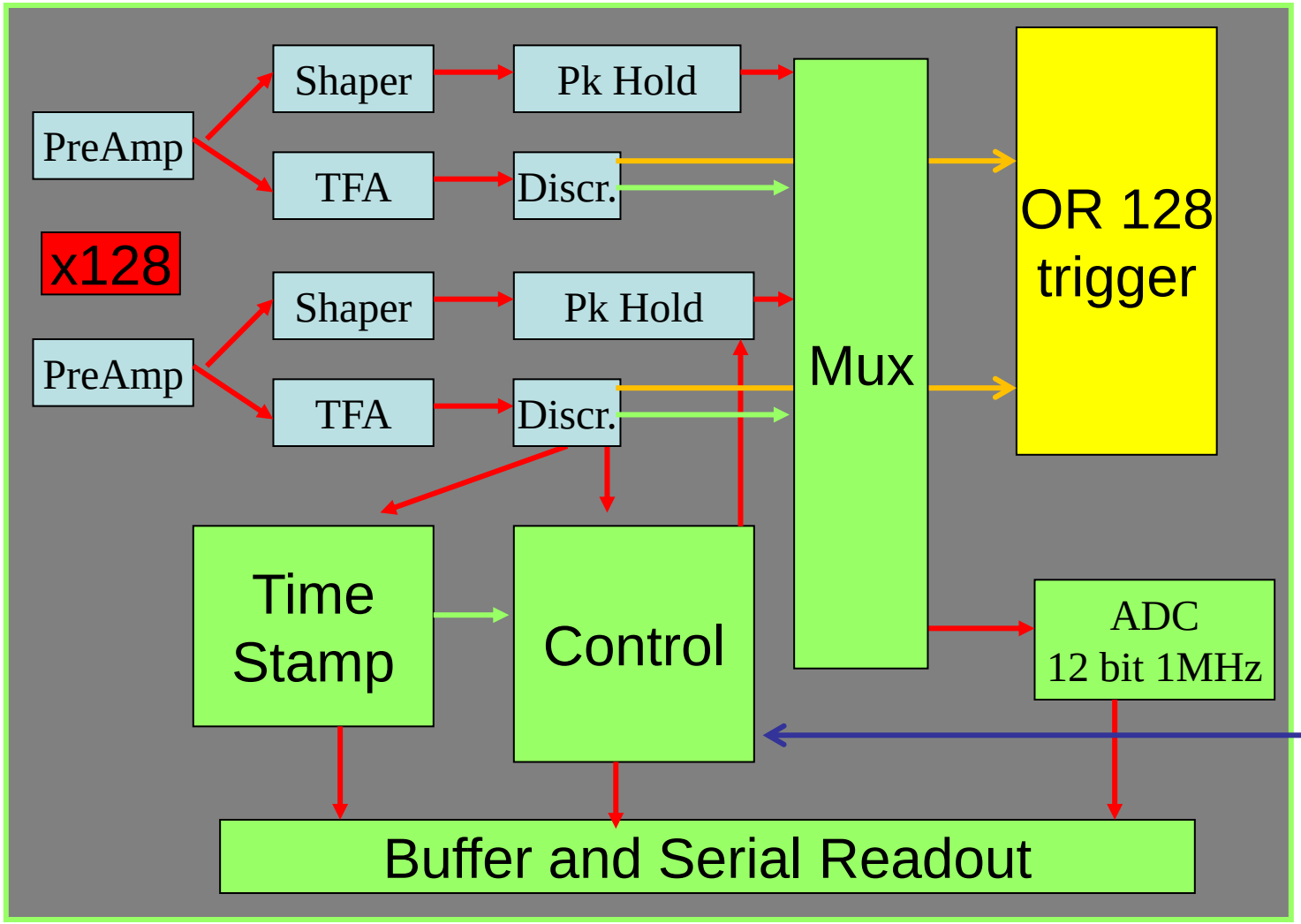
Living in the real world (2)

The problem- in R3B Si tracker the delta electrons give a very high background count rate; much higher than protons

Solutions:

- *Enable ASIC peak hold only if protons reach calorimeter (previous slide)*
- *Shielding detectors with thin foil*
- *Exchange time stamps with calorimeter before readout of data buffers*



ASIC features:

- Time Stamp
- Zero Suppress
- On chip ADC

Optional Gate from Califa

R3B Si Tracker ASIC (mid-design)

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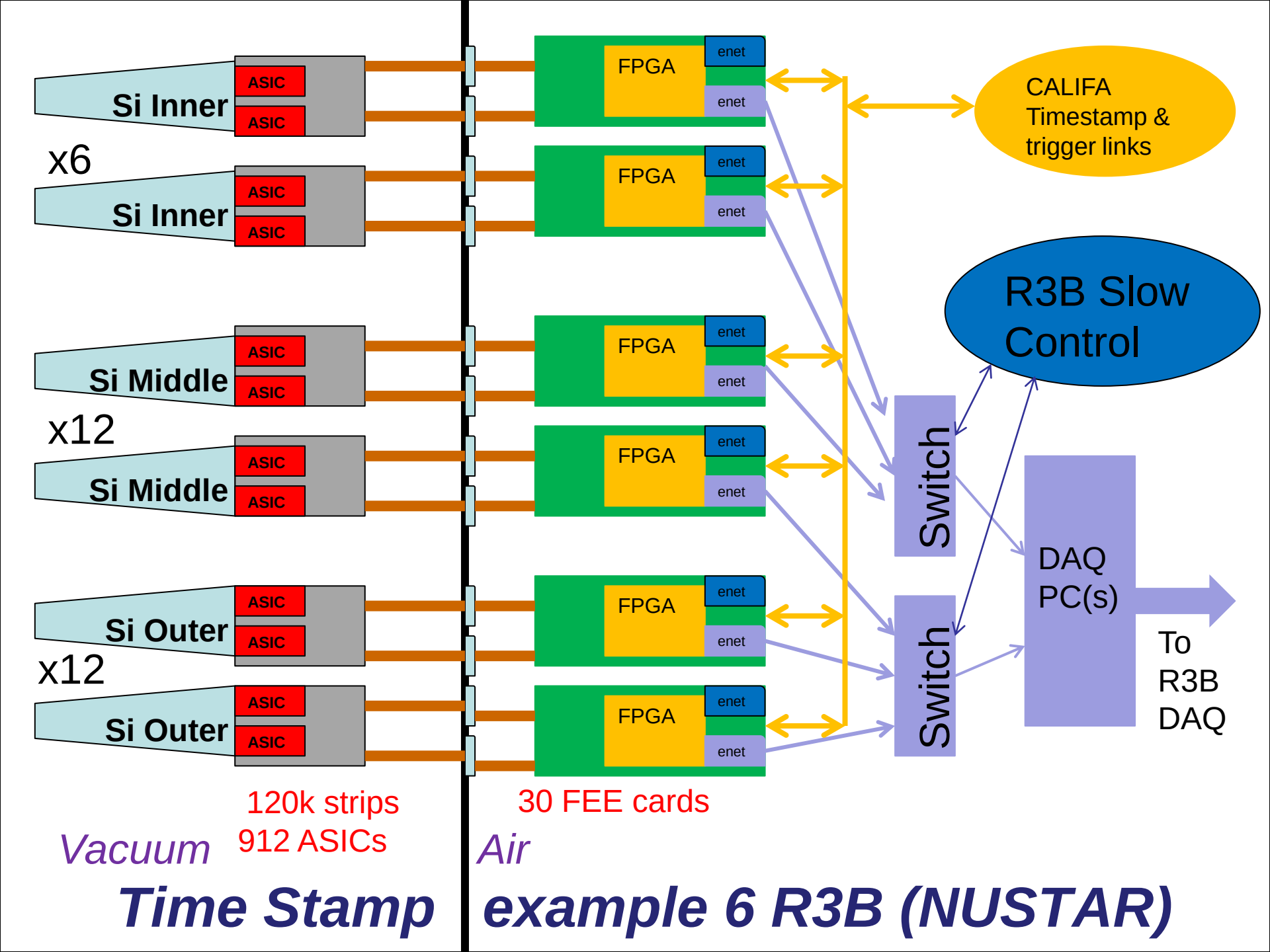
Si Inner
ASIC
ASIC
x6
Si Inner
ASIC
ASIC
Si Middle
ASIC
ASIC
x12
Si Middle
ASIC
ASIC
Si Outer
ASIC
ASIC
x12
Si Outer
ASIC
ASIC
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
CALIFA
Timestamp &
trigger links
R3B Slow
Control
Switch
Switch
DAQ
PC(s)
To
R3B
DAQ
120k strips
912 ASICs
30 FEE cards
Vacuum
Air
Time Stamp
example 6 R3B (NUSTAR)

Conclusions

- ***Introduction:***
  - *Triggers are all about correlating data (essential)*
  - *Side effect reduce DAQ speed/costs*
- ***How do we make triggers?***
  - *Hardware correlation or time stamp data labelling*
  - *Now have choice about DAQ speed/cost.*
  - *Software trigger can be online or offline*
- ***Time stamped systems and software triggers***
  - *Advantages- flexibility, time travel*
- ***Living in the real world***
  - *Latency problem- partition system or add extra signals*
  - *Rate reduction with hardware gate*
  - *Timestamp based data buffer filter in readout*