AIDA introduction for S3 AIDA comparison 2011, Acireale

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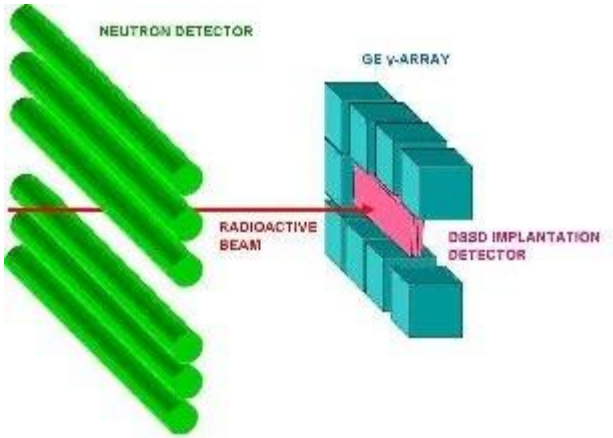
AIDA: introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*



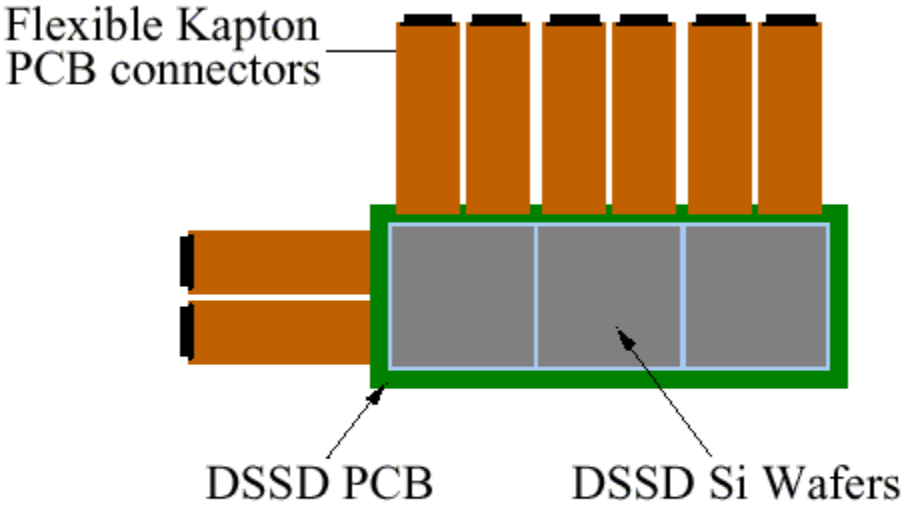
- SuperFRS
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

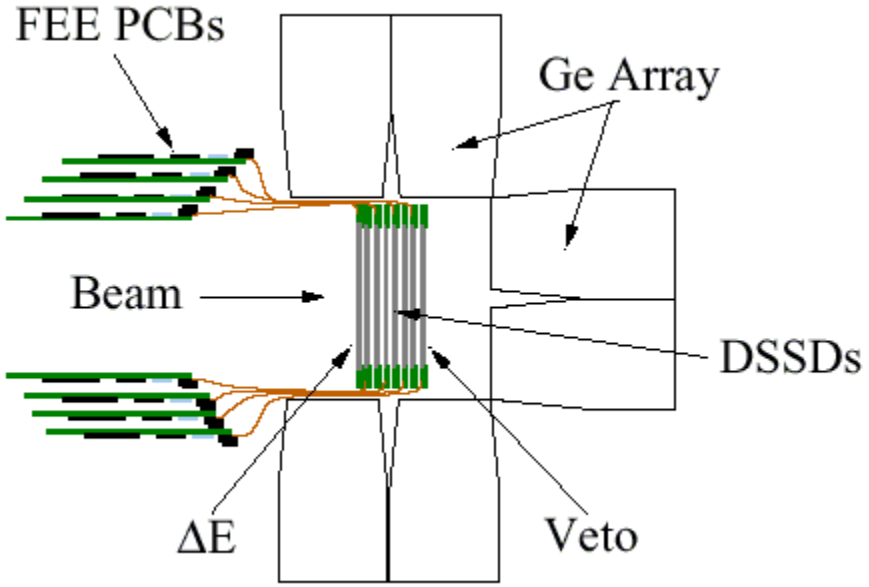
Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

Science & Technology Facilities Council
Nuclear Physics Group

AIDA General Arrangement

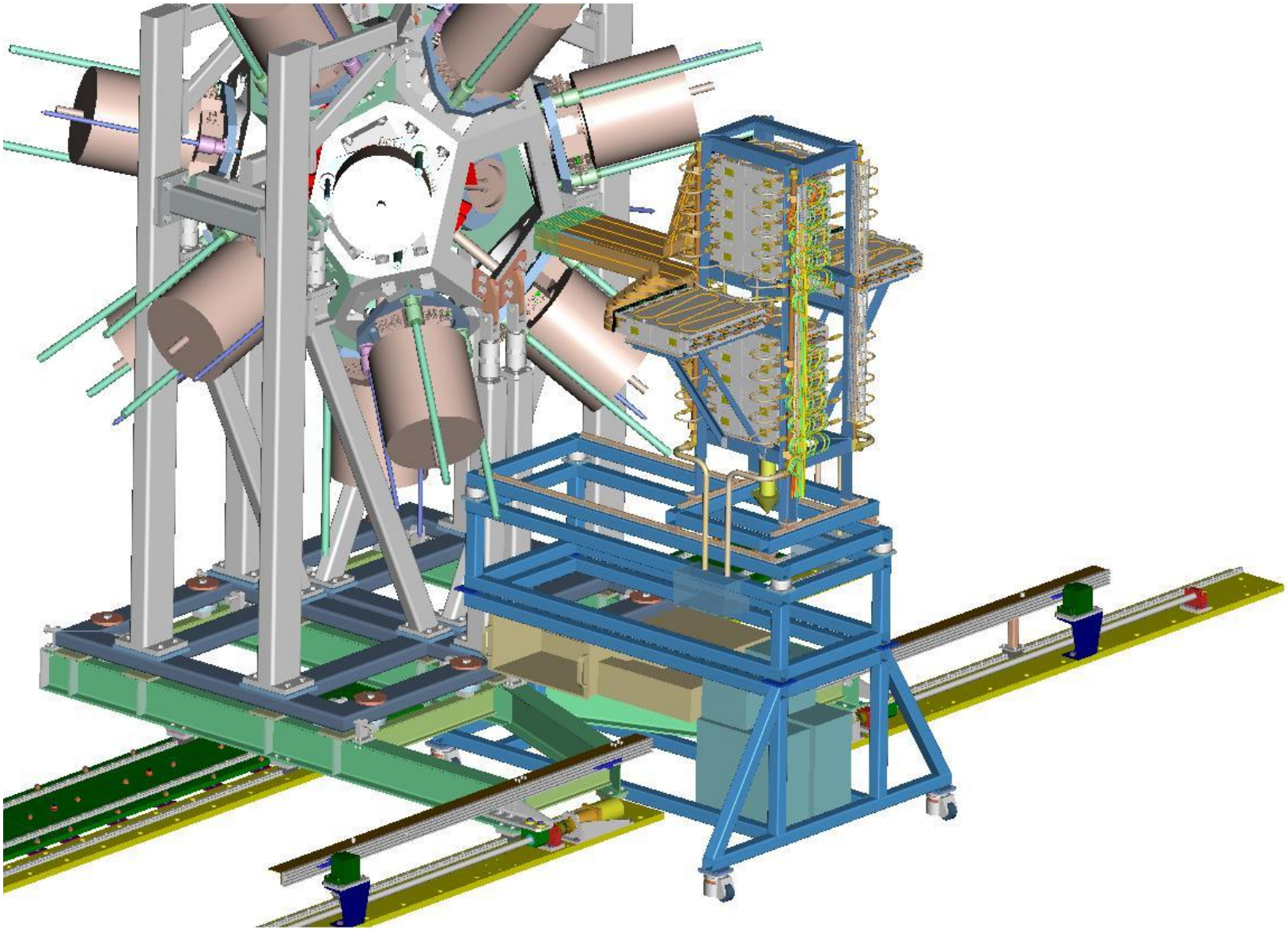




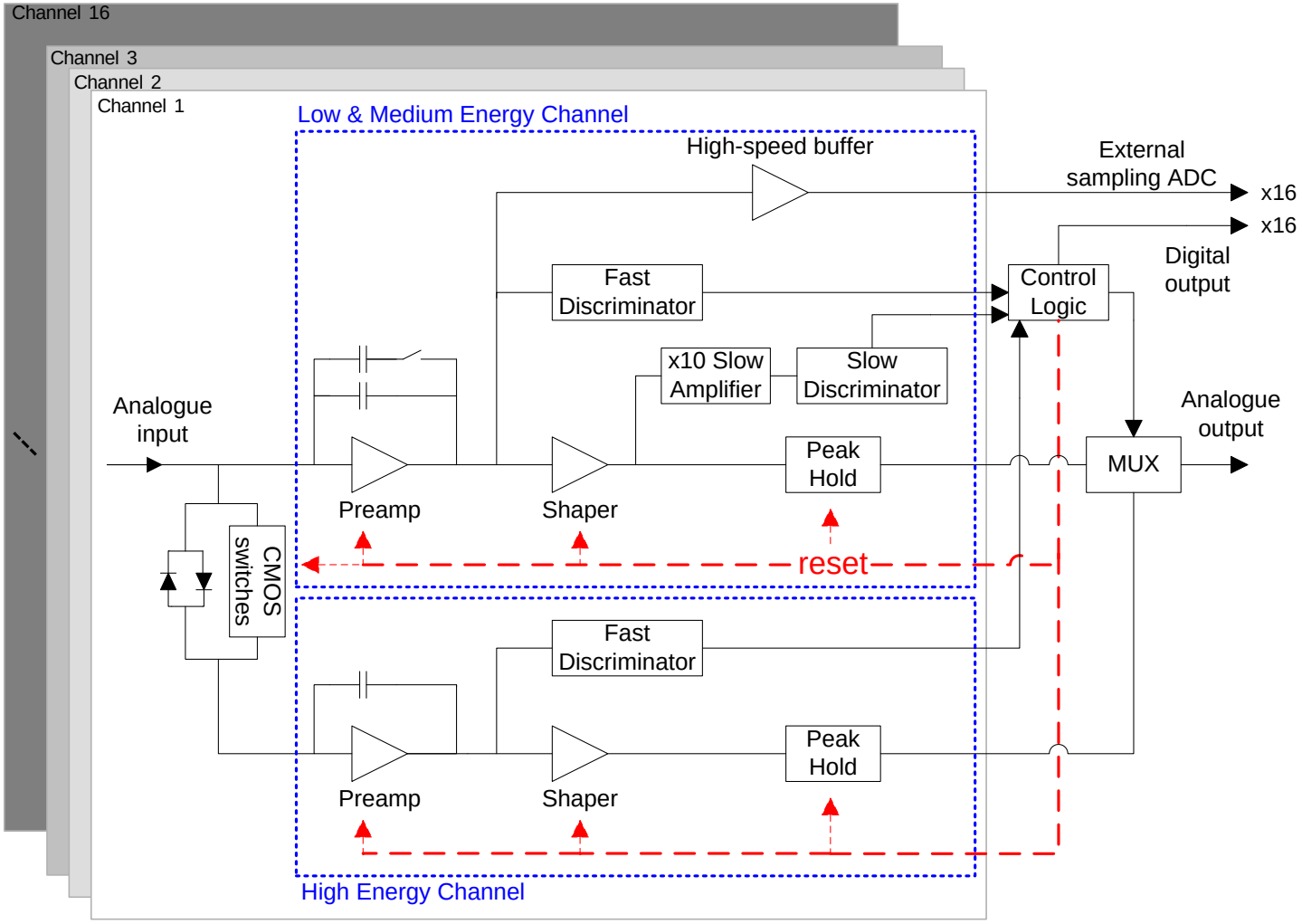
Implantation detector for RDT

Slide from Tom Davinson

AIDA Mechanical

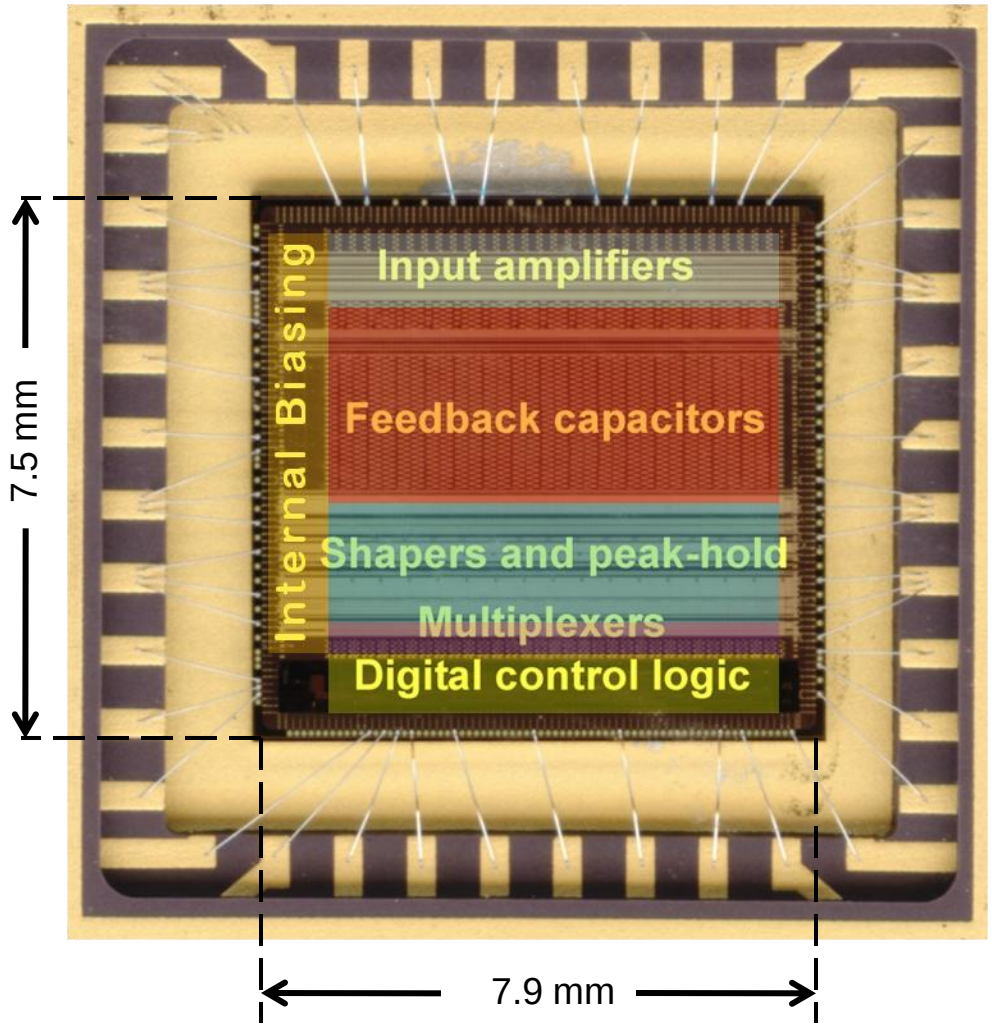


AIDA (NUSTAR)



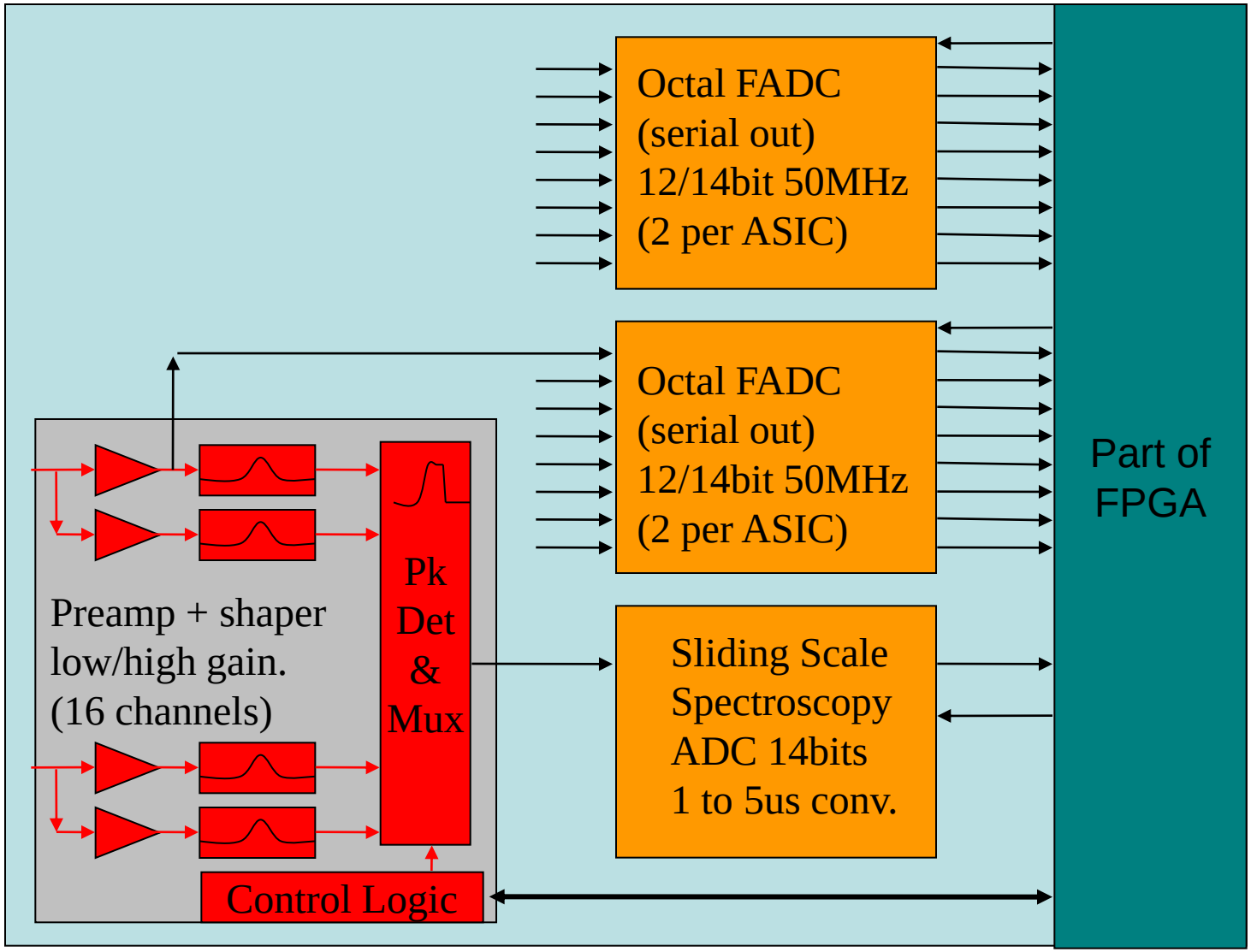
Braga et al. 2009 IEEE NSS conf record, VOLS 1-5 P 1924-8

Layout



AIDA ASIC:

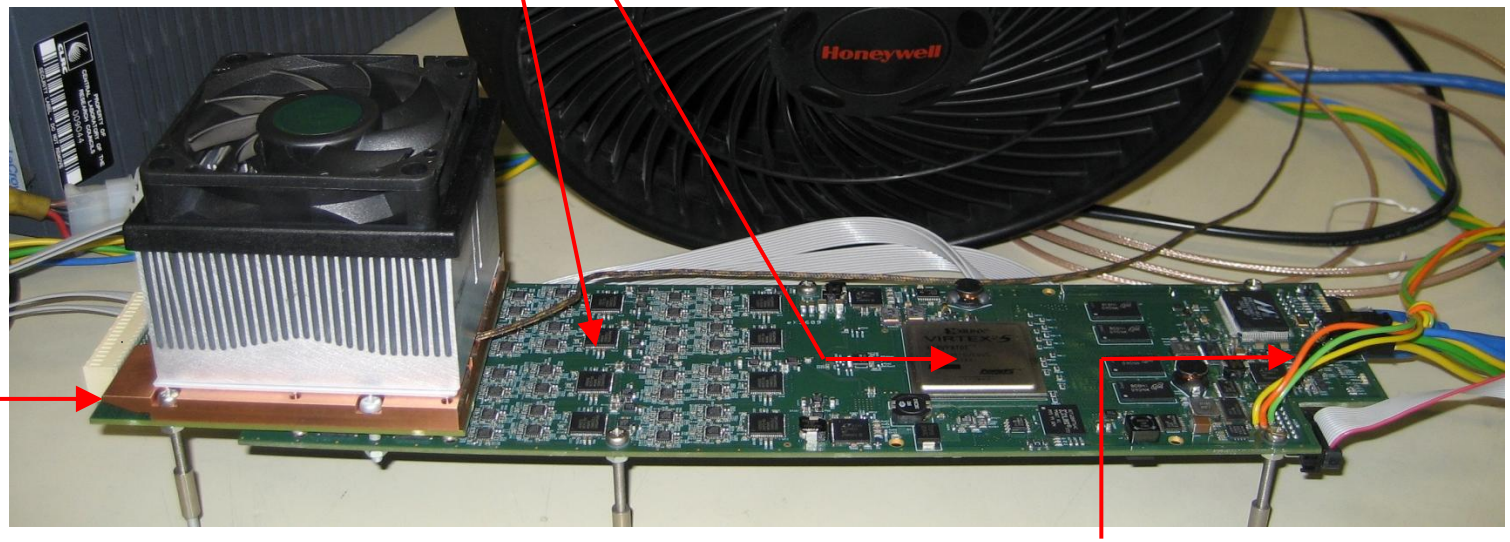
- 625um pitch
- 16 channels
- 2 channels/strip
- Mux'ed analogue output
- Direct digital output for external FADC
- 2 ranges: 0-20MeV/1GeV (switchable) and 0-20GeV (fixed)
- AMS 0.35um CMOS


Octal FADC
(serial out)
12/14bit 50MHz
(2 per ASIC)
Octal FADC
(serial out)
12/14bit 50MHz
(2 per ASIC)
Part of
FPGA
Preamp + shaper
low/high gain.
(16 channels)
Pk
Det
&
Mux
Sliding Scale
Spectroscopy
ADC 14bits
1 to 5us conv.
Control Logic

AIDA (NUSTAR, DeSpec)

Mezzanine:
- 4x 16 channel ASICs
- Cu cover
  - EMI/RFI/light screen
  - cooling

FEE:
- 4x 16-bit ADC MUX readout (not visible)
- 8x octal 50MSPS 14-bit ADCs
- Xilinx Virtex 5 FPGA
  - PowerPC 40x CPU core/Linux OS – DAQ



FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power