Introduction to FPGAs

A. Kugel, Heidelberg University / ZITI

Application Specific Computing

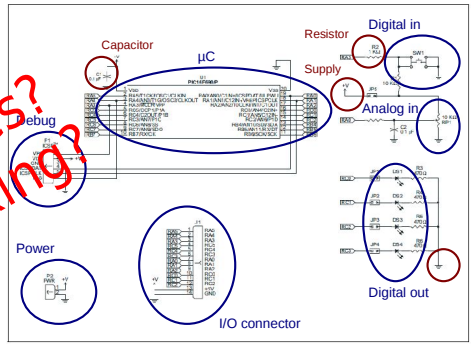
www.ziti.uni-heidelberg.de/ziti/index.php?option=com_content&view=article&id=131&Itemid=76

FPGA: **F**ield **P**rogrammable **G**ate **A**rray

- What?
  - Technology
- Where?
  - Applications
- How?
  - Tools
  - Build or buy
- Summary

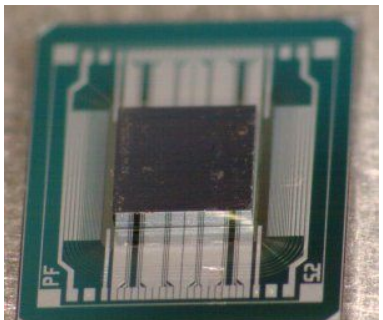
Known Technologies

- Custom Hardware
  - Schematic design
  - Discrete Components



Speed!
Upgrades?
Bug-fixing?

- Chip Design



sus.ziti.uni-heidelberg.de/

- Software
  - General Purpose HW
    - CPU, GPU
  - Custom Program
    - Sequential execution
    - Some Parallelism

Flexibility!
Speed?
Timing?

Something in Between

- Programmable Hardware
  - PLDs were first: „sum-of-products“, early '70s
    - Logic function defined by AND-OR connection matrix
    - Fuses (OTP), EPROM, FLASH
  - Mid '80s: simple „logic“ + programmable interconnects, volatile: FPGA
  - Growing market since ...
- Today
  - Flash (e.g. Lattice), Antifuse (e.g. Actel [+mixed sig]), SRAM (e.g. Altera, Xilinx)
- Focus here: Xilinx

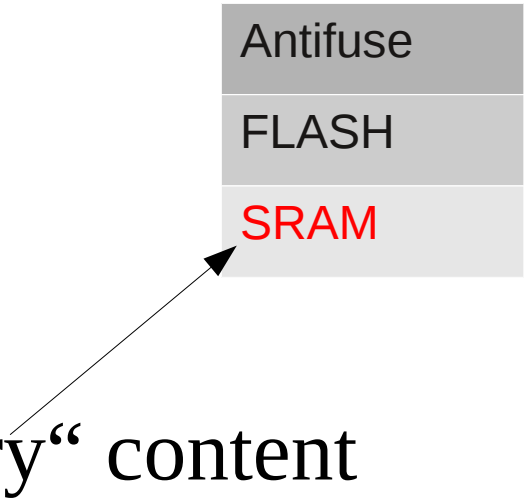
Digital logic

Advantages

- Custom electronics without ASIC-like cost
  - No submission, no MPW
  - Single chip affordable
- Solves „all“ digital interfacing problems
  - Up to ~ 1GHz arbitrary signals
- High bandwidth
  - ~ 1Tb/s
- High processing power
  - Parallelism! Application specific operations
- High density, flexible SoC
- Programmability

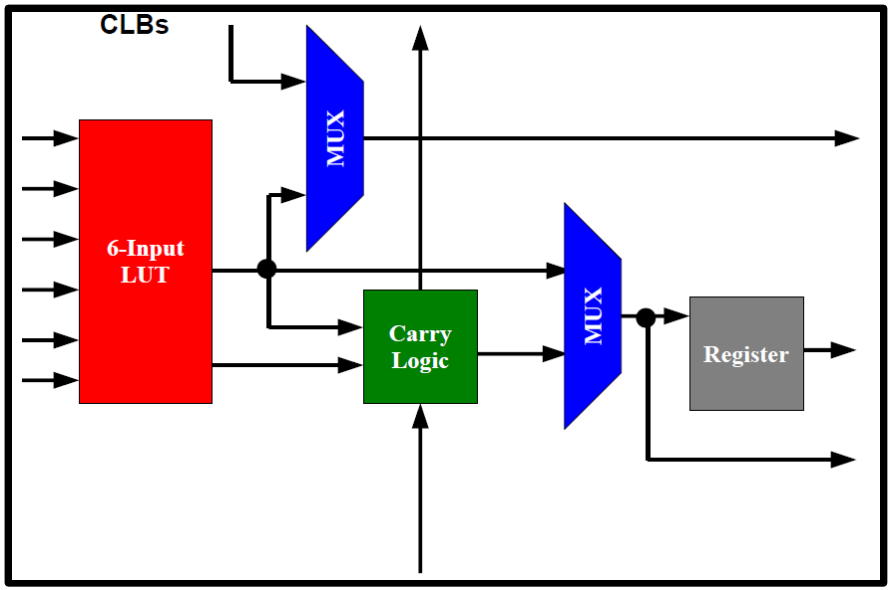
Basic Technology

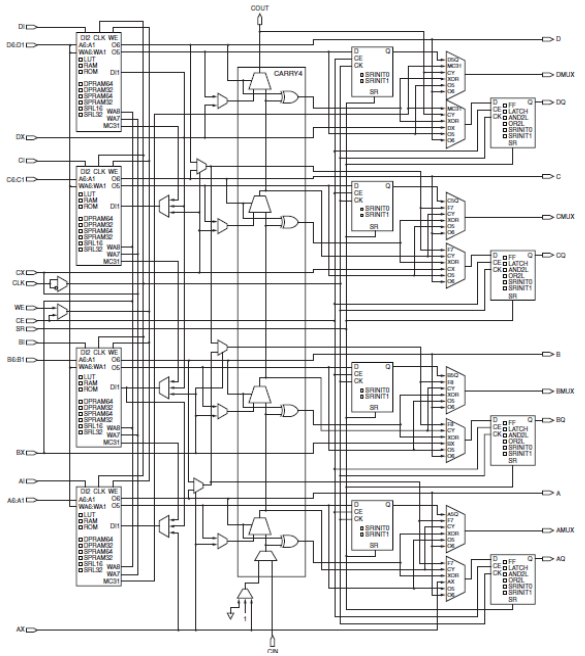
- Logic Elements (LE)
  - Can implement any digital logic via LUT + FF
  - 10^4 – 10^6
- IO
  - 100 – 1000 Pins
  - Multiple I/O Standards + Voltages
- Interconnect
  - Local, regional, global „routing wires“
- Configuration memory
  - All above: defined by on-chip „memory“ content



Logic Elements

- Look-up-table (LUT)
  - 6(4) inputs
- Output register (FF)
- Carry IN/OUT
- Multiplexer options
  - Bypass LUT, FF
- Grouped in
  - Slices (4 LEs)
  - CLBs (2 Slices)
- *Some variants*

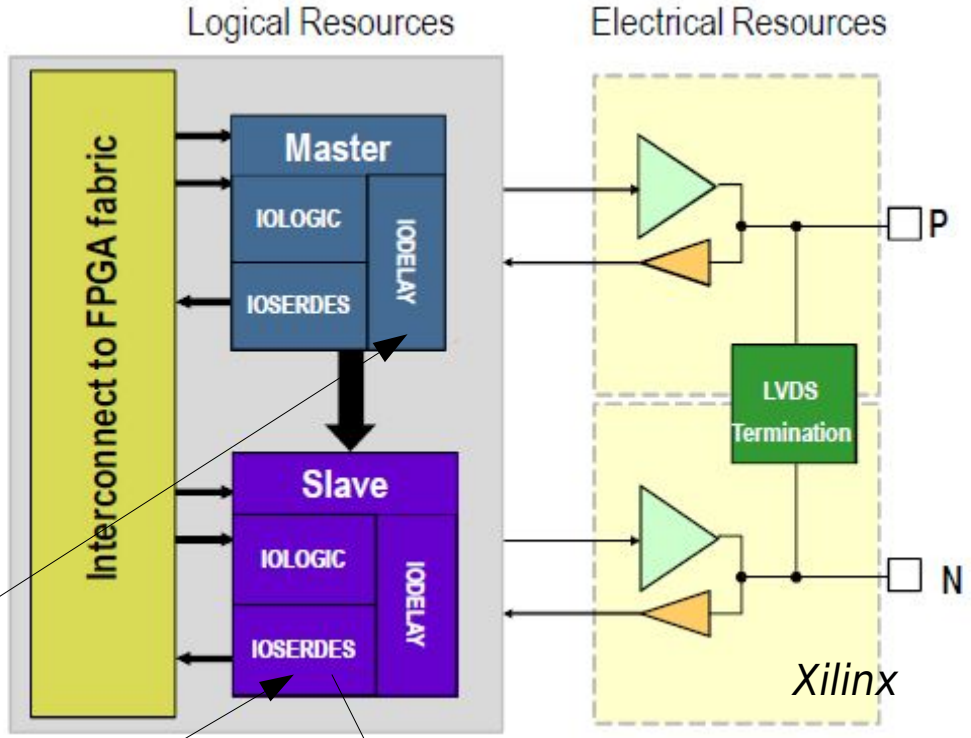




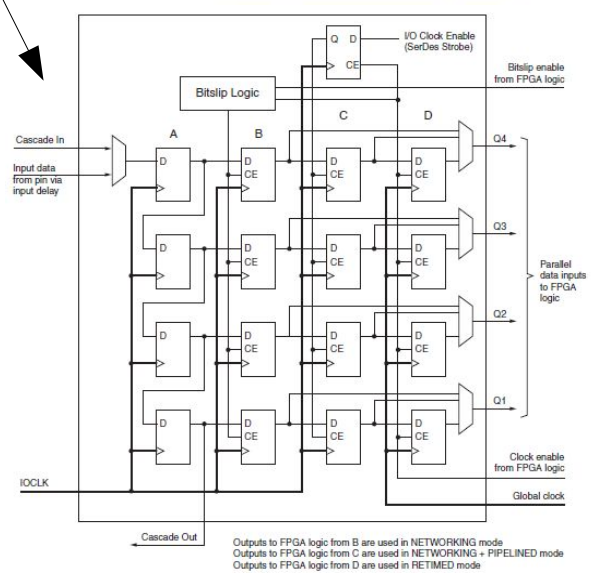
Xilinx: Spartan-6 SLICEM

I/O Cells

- IN/OUT buffer
  - Tri-state option
  - Differential option
  - Termination
  - Levels: I/O „bank“ supply
- Programmable delay
  - ~ 100ps resolution
  - Few ns max delay
- SerDes
  - 1:2, 1:4 ratio
  - Multiple clocks



Xilinx



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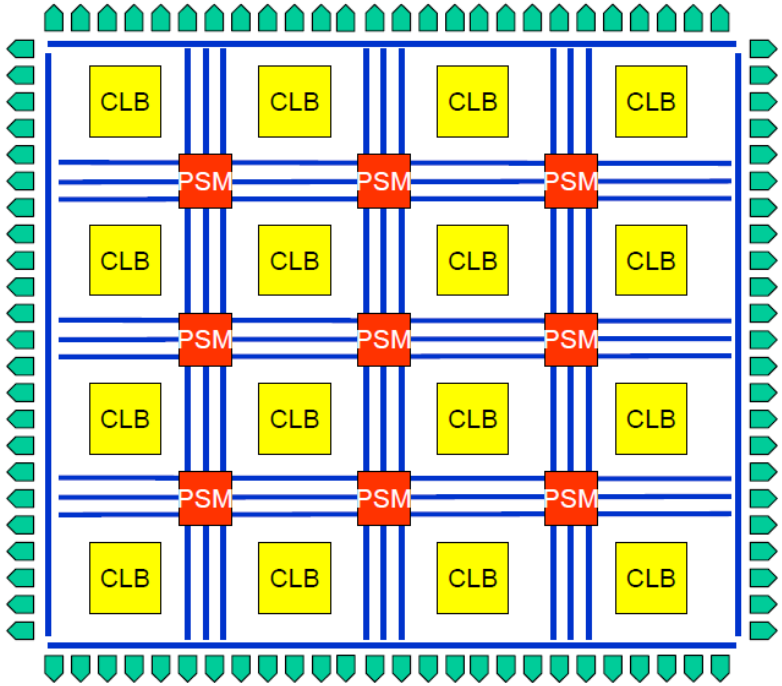
Fabric Interconnect

- All CLBs and I/O-cells connect to „switch matrix“
  - Local routing (neighbours)
  - Regional (banks, columns)
  - Global (clocks)



PSM: Programmable Switch Matrix

CLB: Configurable Logic Block

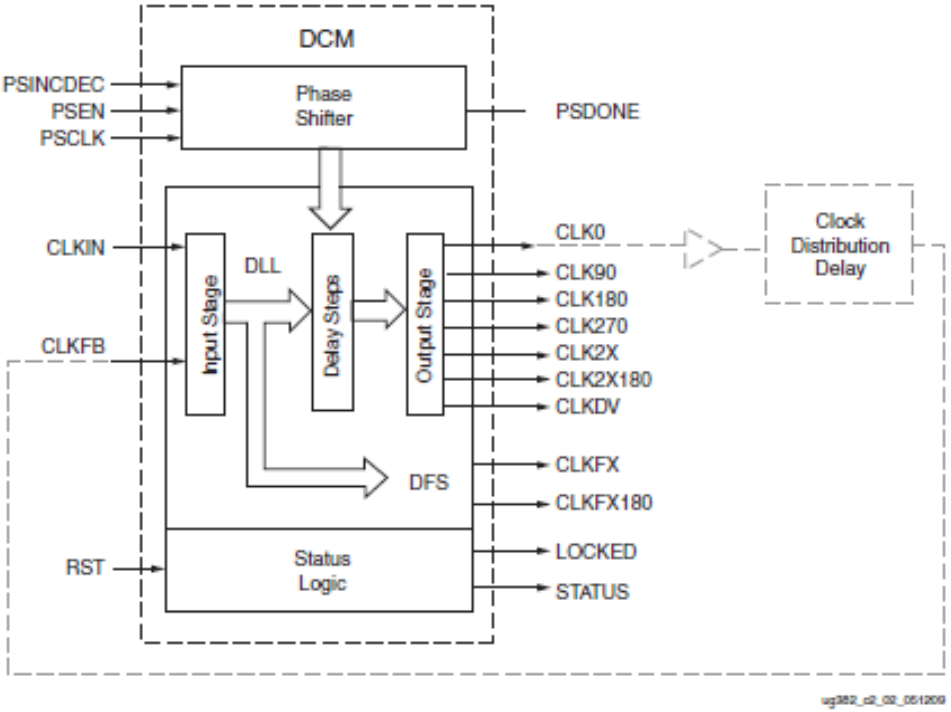
Xilinx

Advanced Technology

- IP-Blocks *(Intellectual Property)*
  - Hard IP: portion of chip with special function (~co-processor)
  - Soft IP: functionality implemented in FPGA fabric (~library)
- IP Blocks
  - Clocking
  - Memory
  - DSP
  - Processor
  - Ethernet
  - MGT

Clocking

- DCM
  - Phase shift
  - Clock alignment
  - Frequency synthesis
  - Multi-phase clocks
- PLL
  - Frequency synthesis
  - Jitter filter
- Variety of clock buffers
- *Limited resources*



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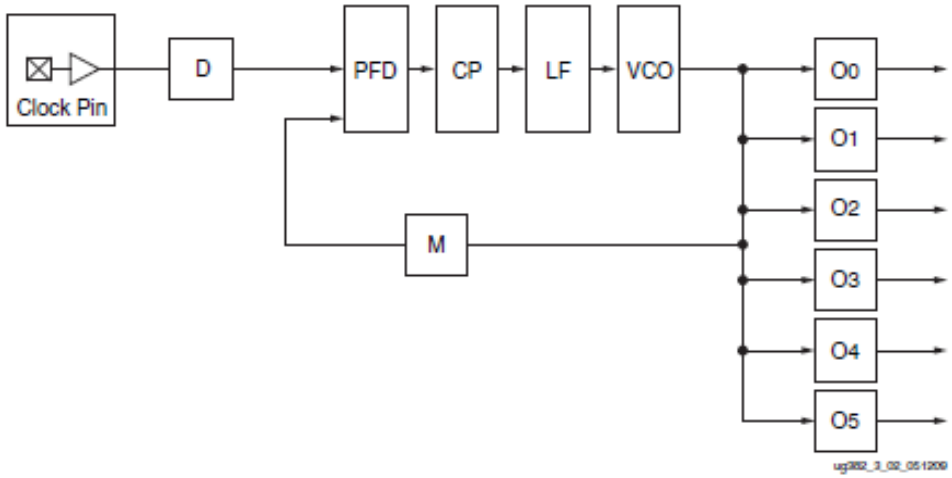
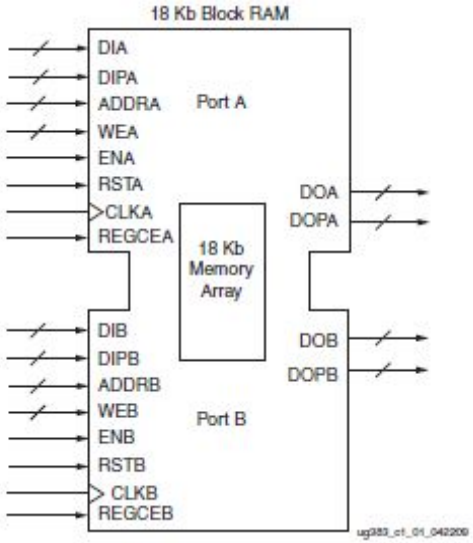


Memories

- LUT memory
- Hard-IP memory blocks (18kB)
  - FIFO
  - Dual ported RAM
  - Configurable (A, D)
- Memory Controllers
  - Soft-IP
    - DDR1,2,3 + IO-Delay
  - Hard-IP
    - Multi-port, high speed



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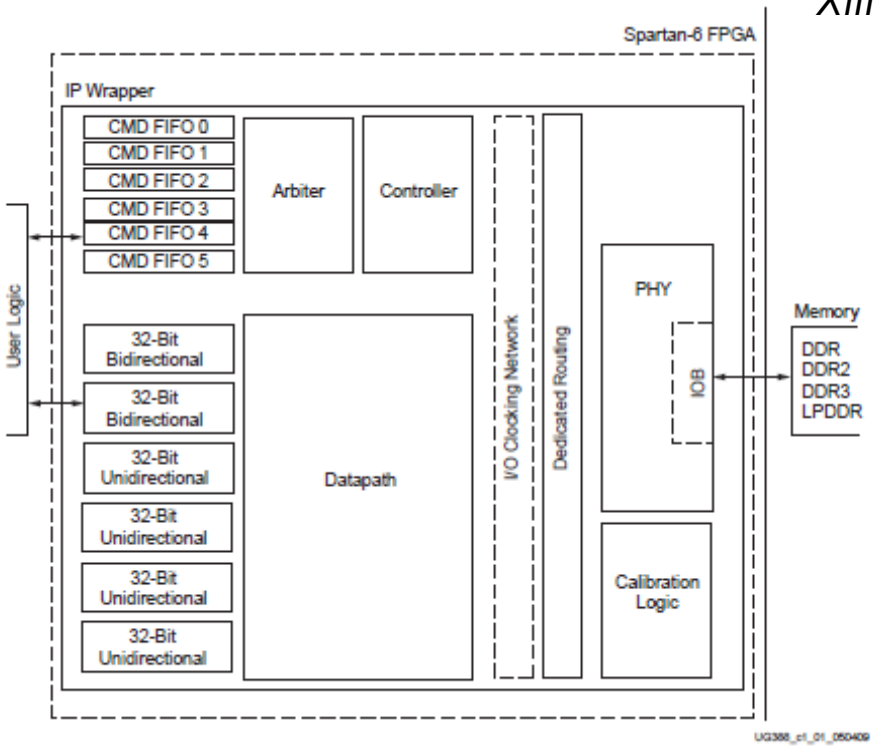
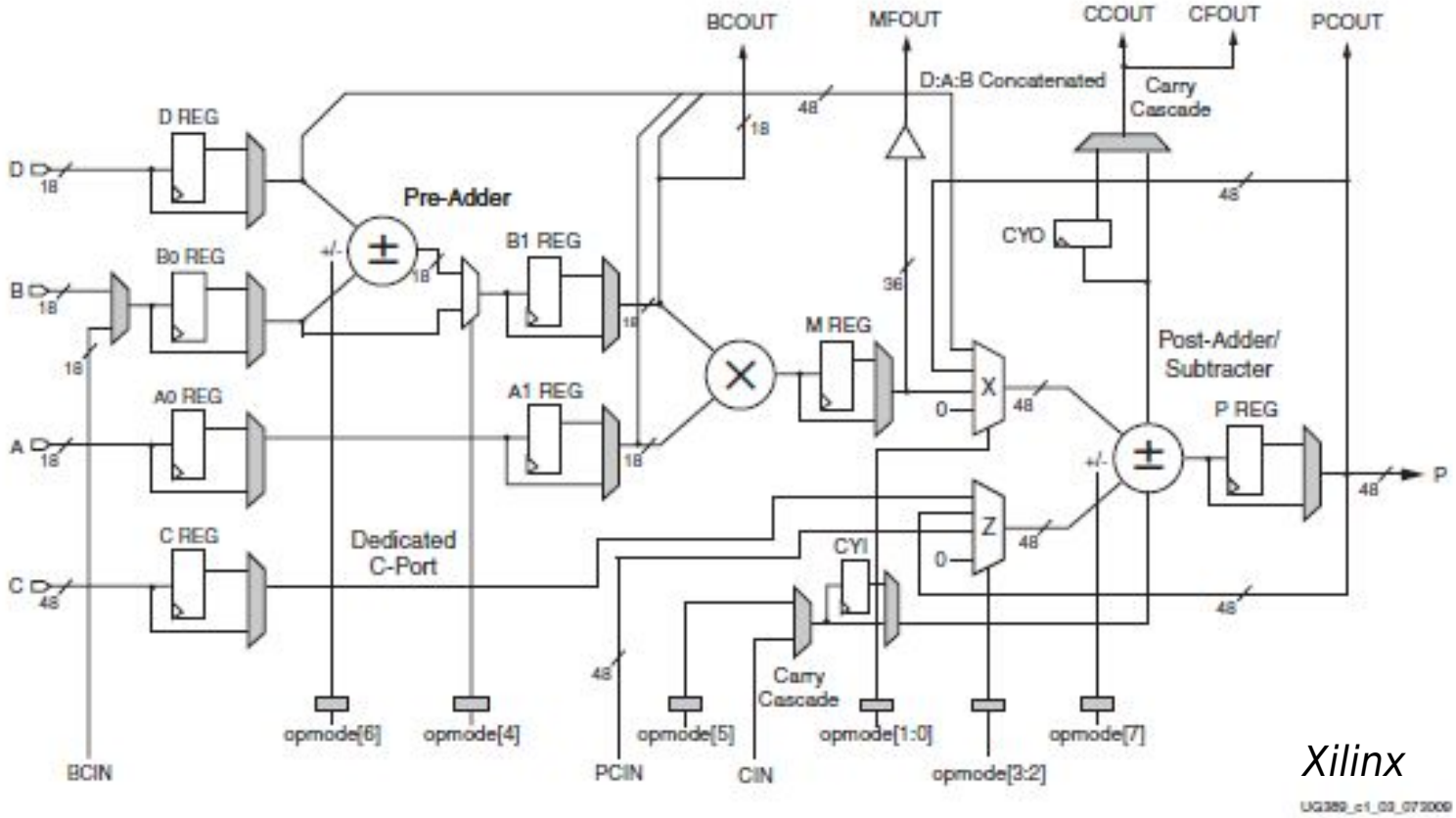


DSP

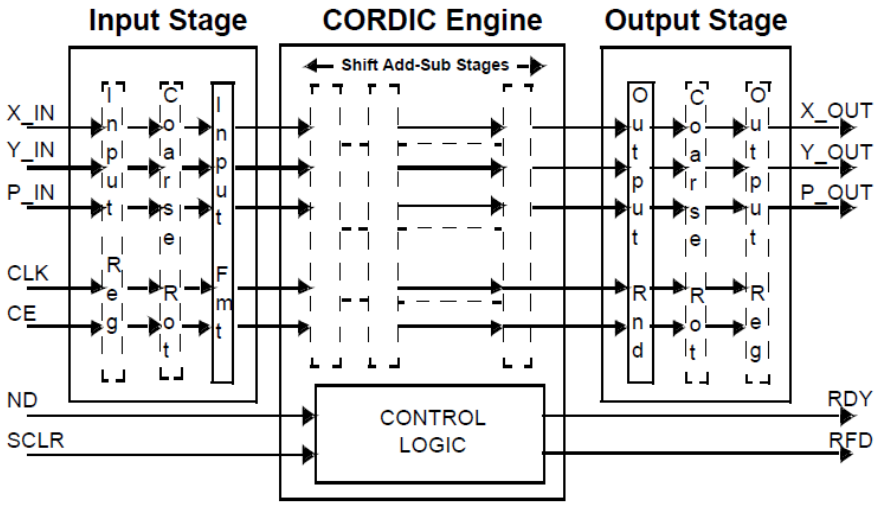
- 18x18 (24x24) ADD – MUL – ADD
- Cascadable
- Filters, Processing, barrel shifters, ...

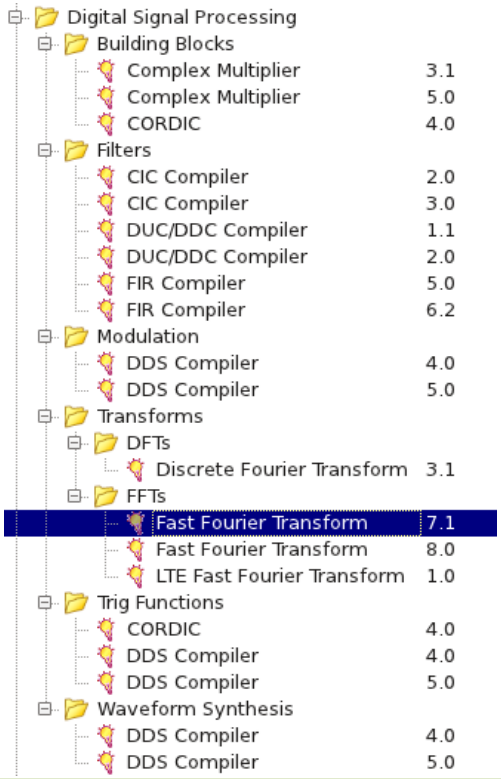
Xilinx: TOPS/s

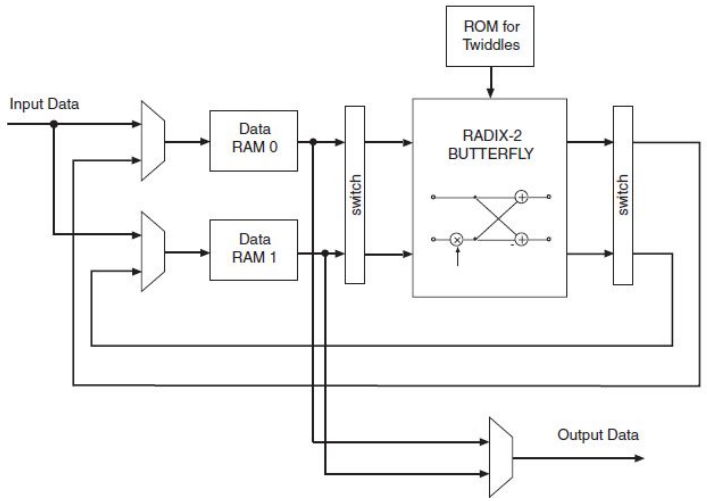


DSP Soft-IPs

- CORDIC
  - Vector operations
  - Sin and Cos
  - Sinh and Cosh
  - Atan and Atanh
  - Square root
- DFT, DFT^{-1}
- FIR
- DDS
- ... via CoreGen



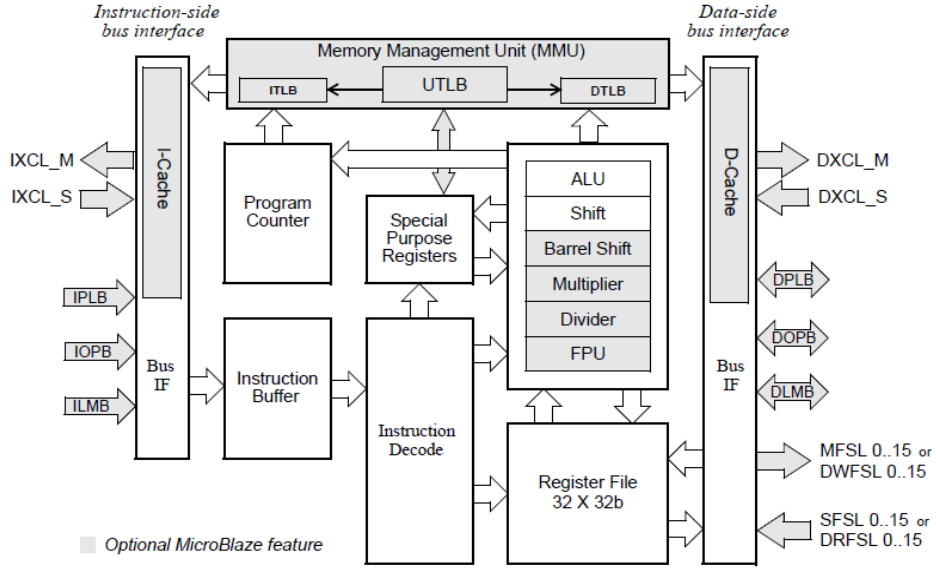




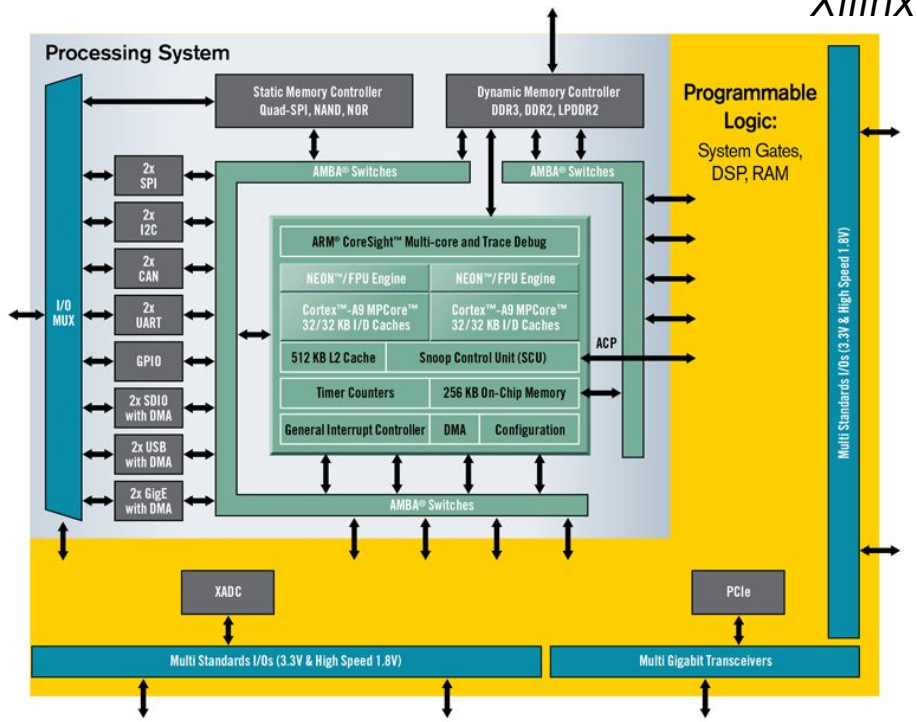
$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-jnk2\pi/N}$$

Processors

- Soft-IP
  - „Full custom“ µC
  - 32 bit RISC (µBlaze)
    - Linux
  - 100 .. 400MHz
- Hard-IP (depends)
  - PowerPC 440
    - 550 Mhz
  - Arm M9, dual core
    - 800 Mhz
    - FPU
    - Peripherals

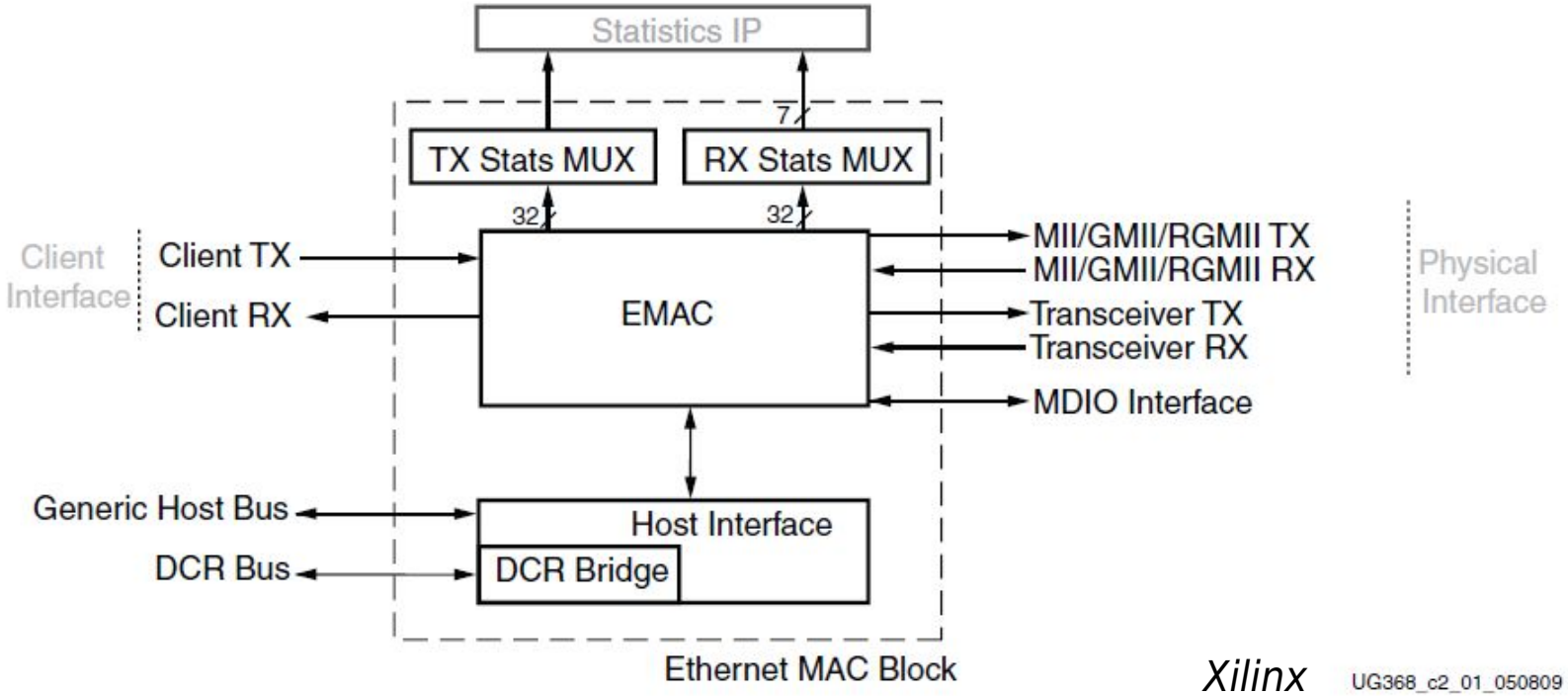


Xilinx



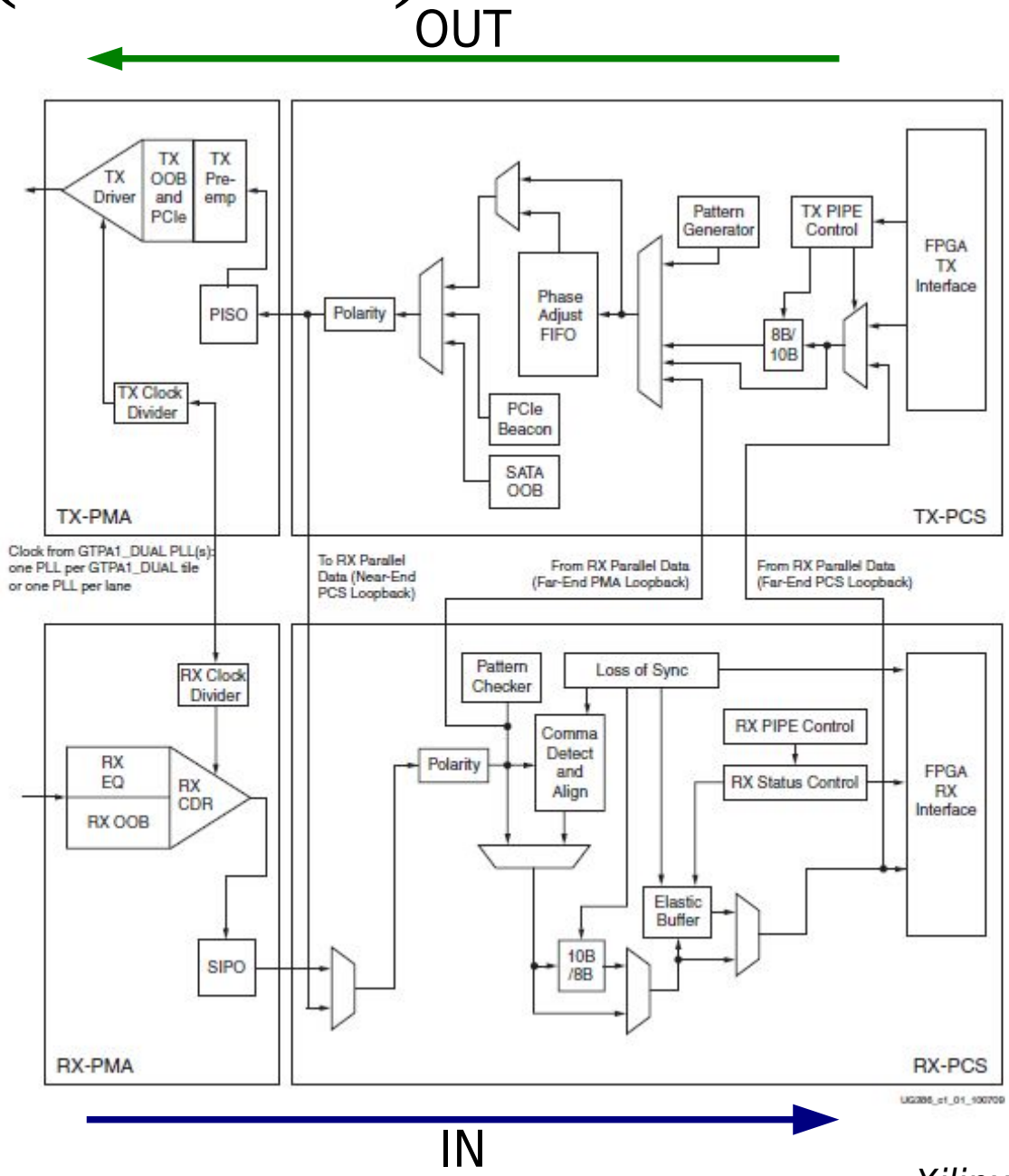
Ethernet

- Ethernet MAC
  - Soft-IP, any modern FPGA (resource consuming)
  - Hard-IP, selected FPGAs (1..few / FPGA)
- Ethernet PHY (serial only/ no CAT5)



MGT (GTP/H/X)

- Multi-Gigabit-Transceivers
- Serial bitrates up to 28Gbit/s
- Many protocolls
  - FC, GE, XAUI, SATA, PCIe
- Custom (e.g. low latency)
- Channel bonding



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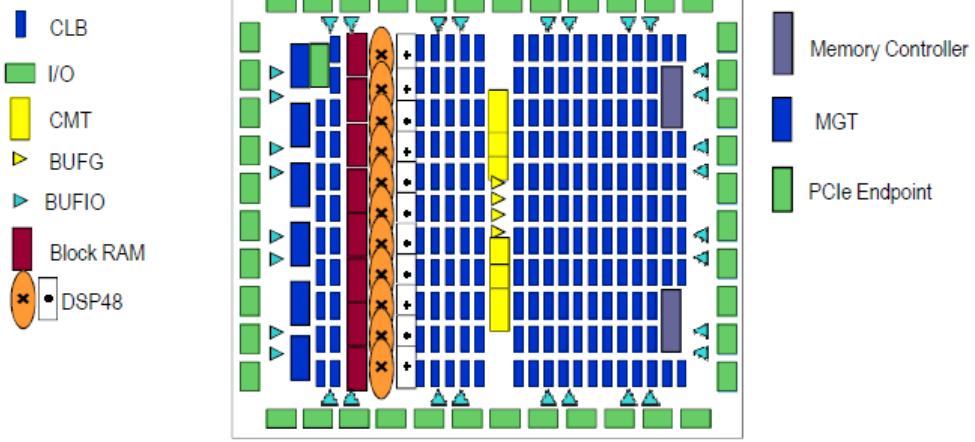
Full View



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- Block diagram
- Floorplan

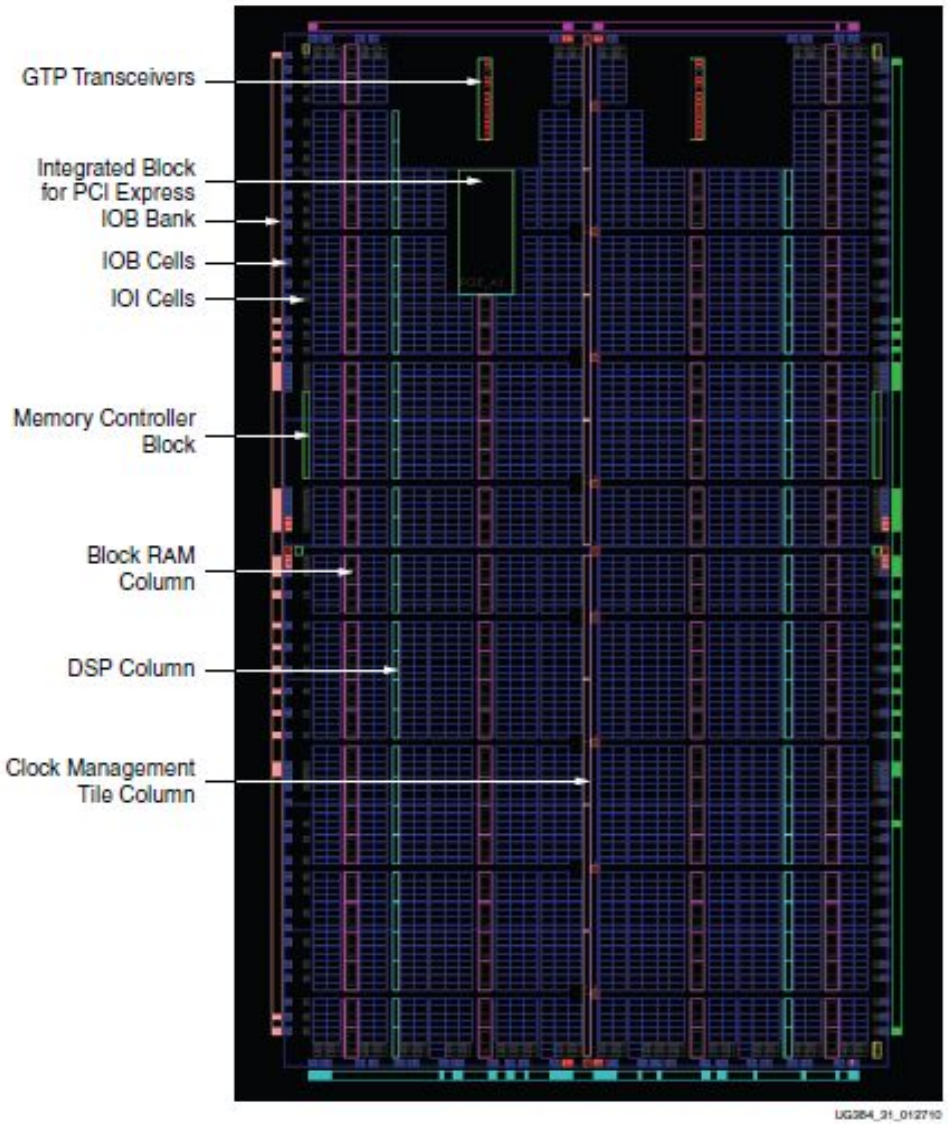


Figure 31: **XC6SLX45T Floorplan View in PlanAhead**

Xilinx

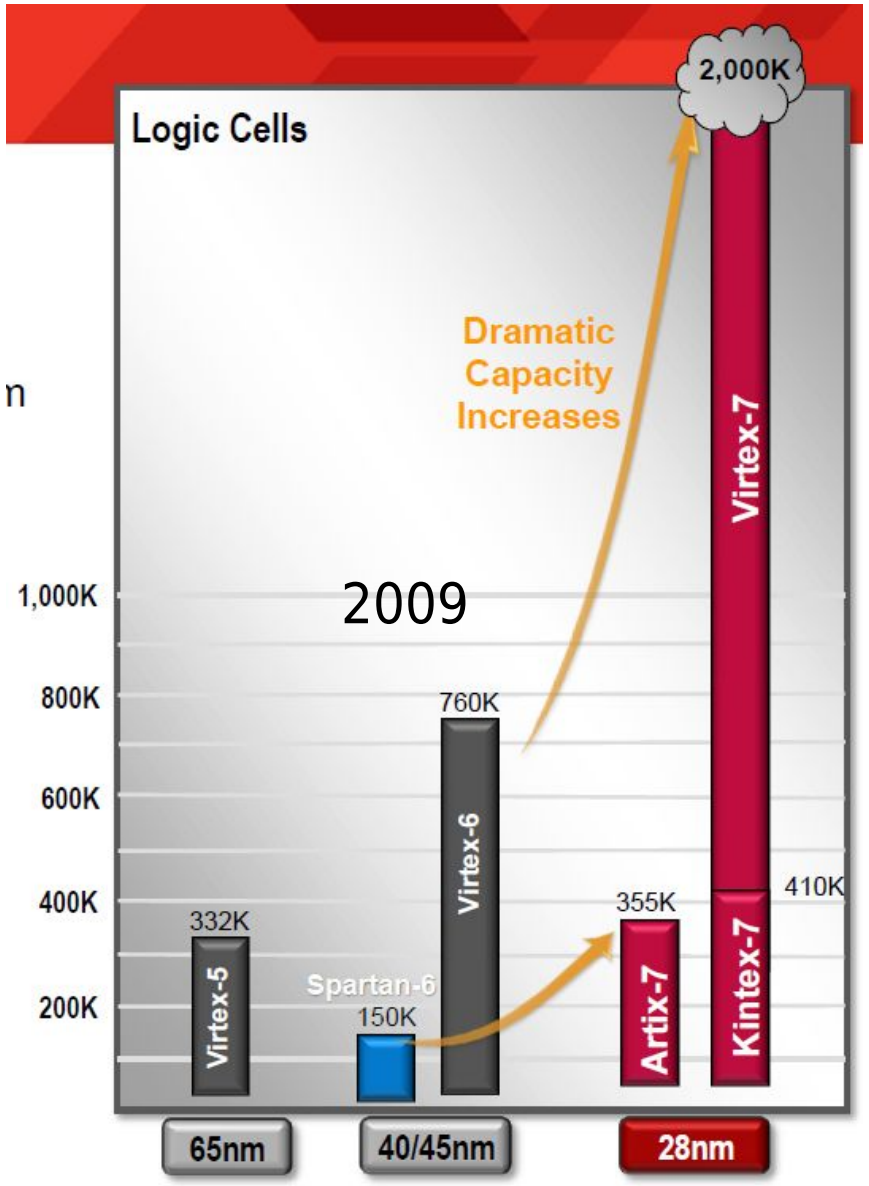
Devices

- Low cost: Spartan-6
  - 150k LEs
  - 180 DSP
  - 260 BRAM
  - 8 MGT, 3Gbit/s
  - 500 I/O
- High end: Virtex-7
  - ~2M LEs
  - ~4k DSP
  - ~4k BRAM
  - 72 MGT, 28Gbit/s
  - 1200 I/O

Typ. speed ~200MHz

Typ. speed ~400MHz

10€ .. 10k€



Xilinx

Applications

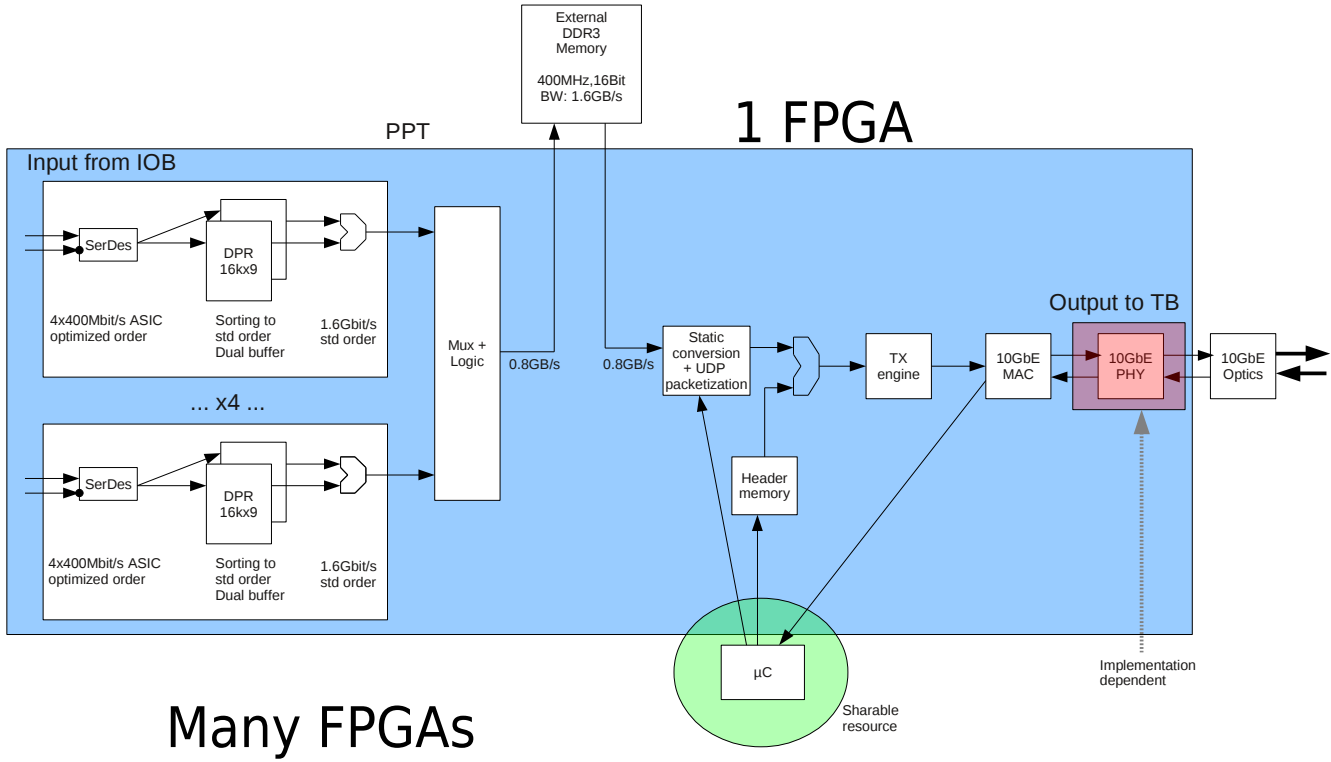
- Tasks
  - „Glue“ Logic, Custom I/O, Custom Processing
- Areas
  - Data Acquisition, Signal Processing, Image Processing, Computing, Communication, Embedded Systems
- Systems
  - Stand-alone, Accelerators/Co-Processors, Hybrid

„Glue“ Logic

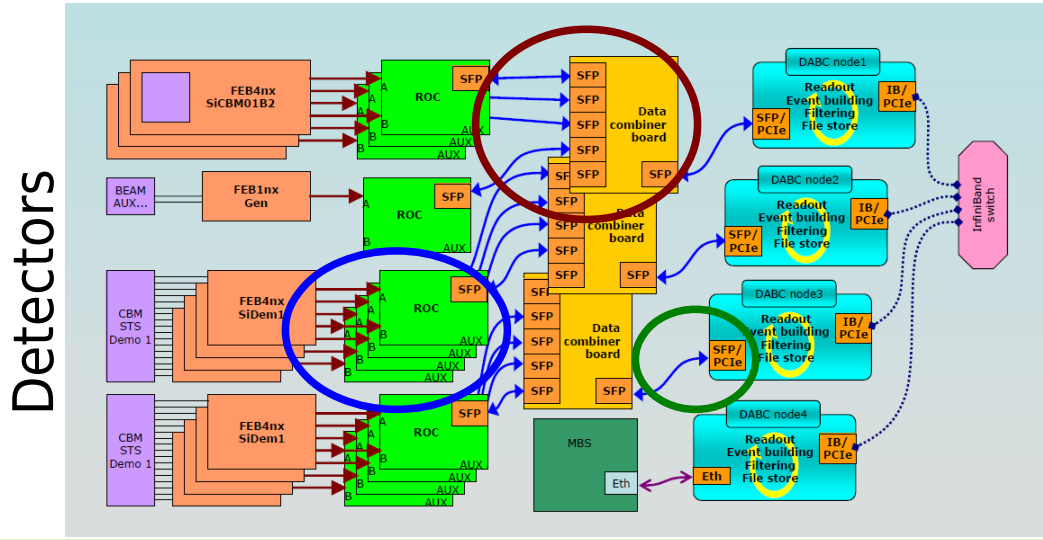
- Interfaces
  - Unlikely to find digital device FPGAs cannot handle
  - 0.8 ..3.3V, PECL, LVDS, CMOS, termination (DCI)
- Protocol engines
  - Standards: I2C, SPI, PCI ...
  - Custom handshakes: Converters, Peripherals, ...
- Timing
  - Synchronisation
  - Mutliple clock domains

DAQ Examples

- XFEL
  - Mpixel sensor
  - 10GE slice (16)
  - Control

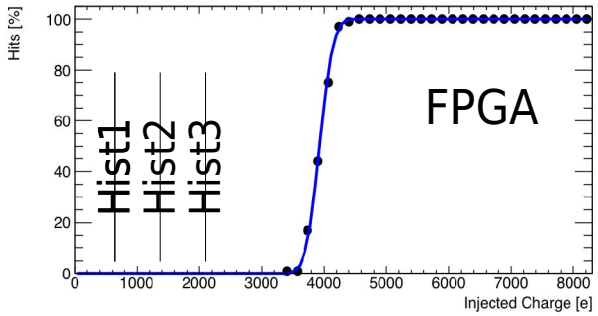


- CBM
  - 1 TB/s
  - 1k links @ 10G
  - Determ. Latency
  - ROC,DCB,ABB

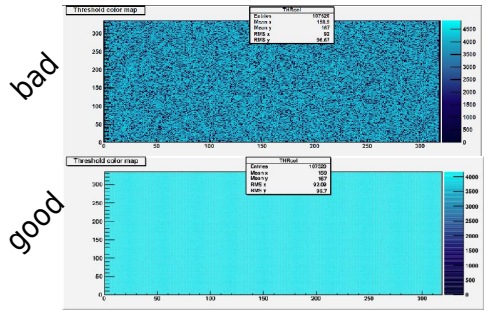


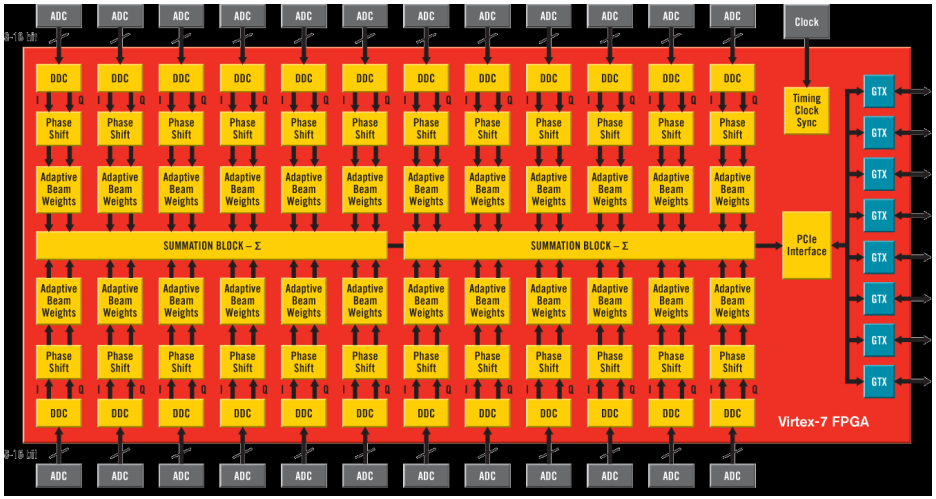
Processing Examples

- Histogramming
  - Pixel calibration
  - Hybrid
- DSP
  - Radar data preproc.
- SPH
  - 60 FOPs
  - Pipeline
  - 1 cycle

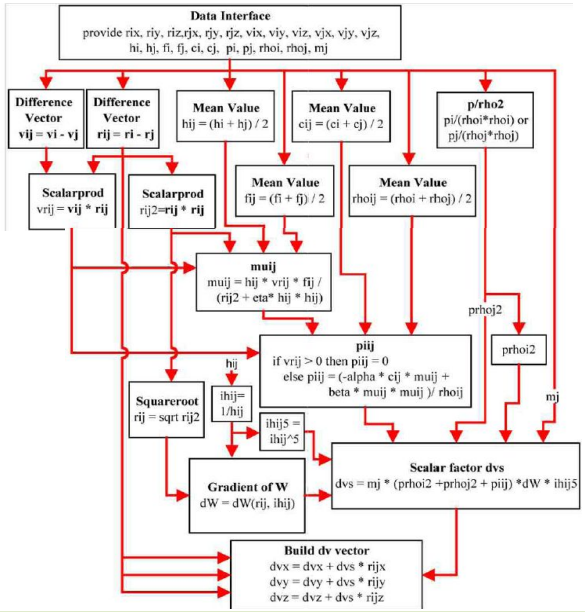


CPU





Xilinx: Radar signal processing



Parallel implementation VERY different from CPU/SIMD

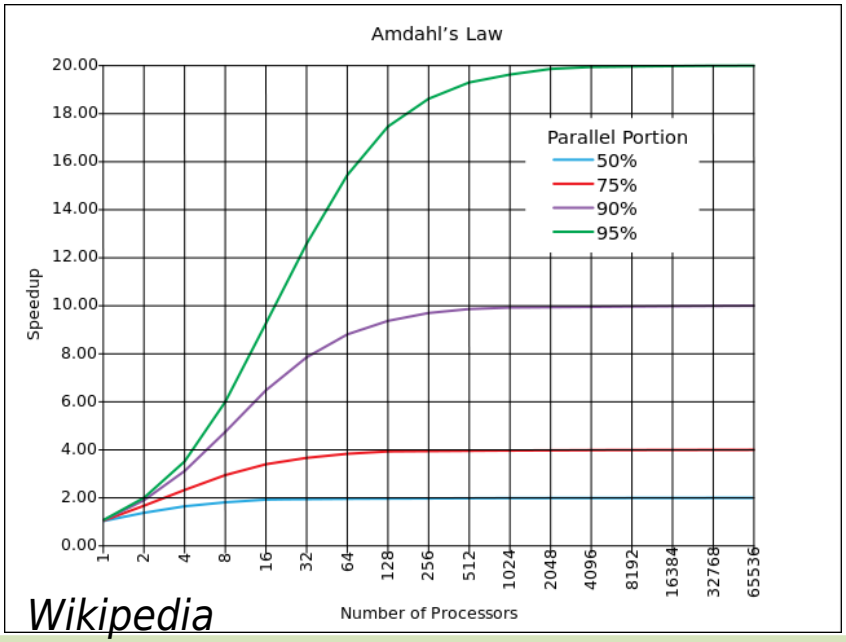
More Processing

- Key issue is parallelism
- FPGA parallelism can be any order (few .. 1000)
  - Application specific
  - Typically, avg. performance = max. performance
- For SIMD-like apps, maybe GPU is better
- Watch Amdahls law!
  - Fewer+longer pipelines++

GPUs, FPGAs and all that

	CPU	GPUs			FPGA	ASIC
	Intel Core i7-960	Nvidia GTX285	Nvidia GTX480	ATI R5870	Xilinx V6-LX760	Std. Cell
Year	2009	2008	2010	2009	2009	2007
Node	45nm	55nm	40nm	40nm	40nm	65nm
Die area	263mm^2	470mm^2	529mm^2	334mm^2	-	-
Clock rate	3.2GHz	1.5GHz	1.4GHz	1.5GHz	0.3GHz	-

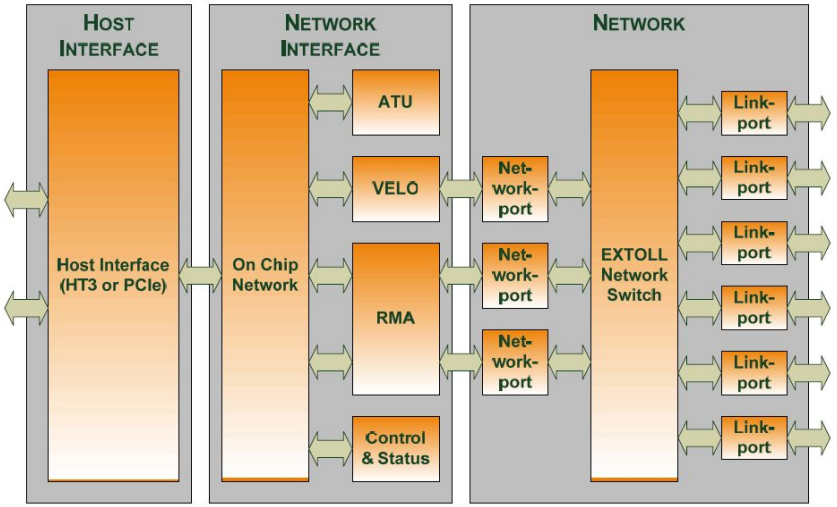
E.S Chung et al., 2010



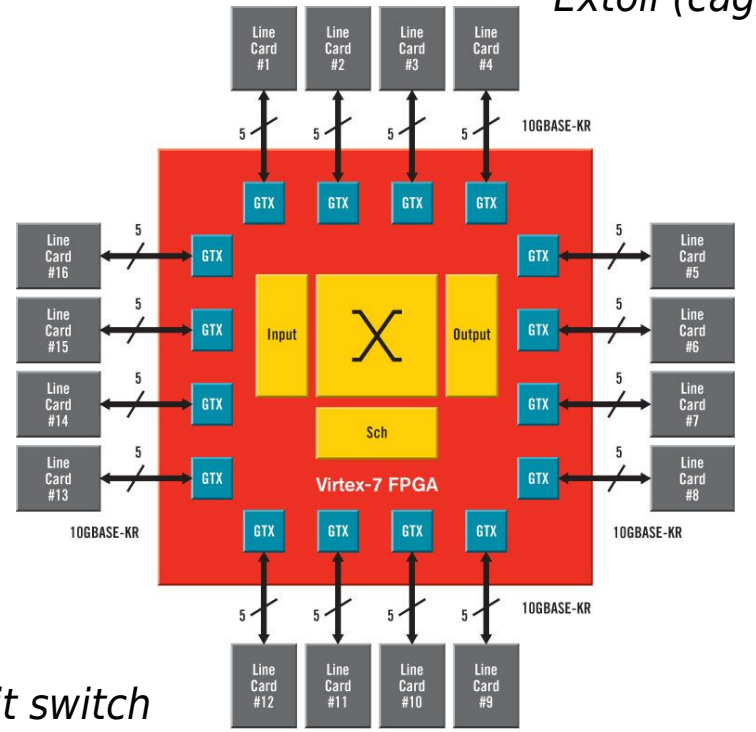
Wikipedia

Communication Examples

- Custom „networks“
  - Deterministic, low latency (Extoll)
  - HTX, PCIe
- Programmable packet switches
- Realtime packet analyzers



Extoll (cag, ziti)



Xilinx: terabit switch

Tools

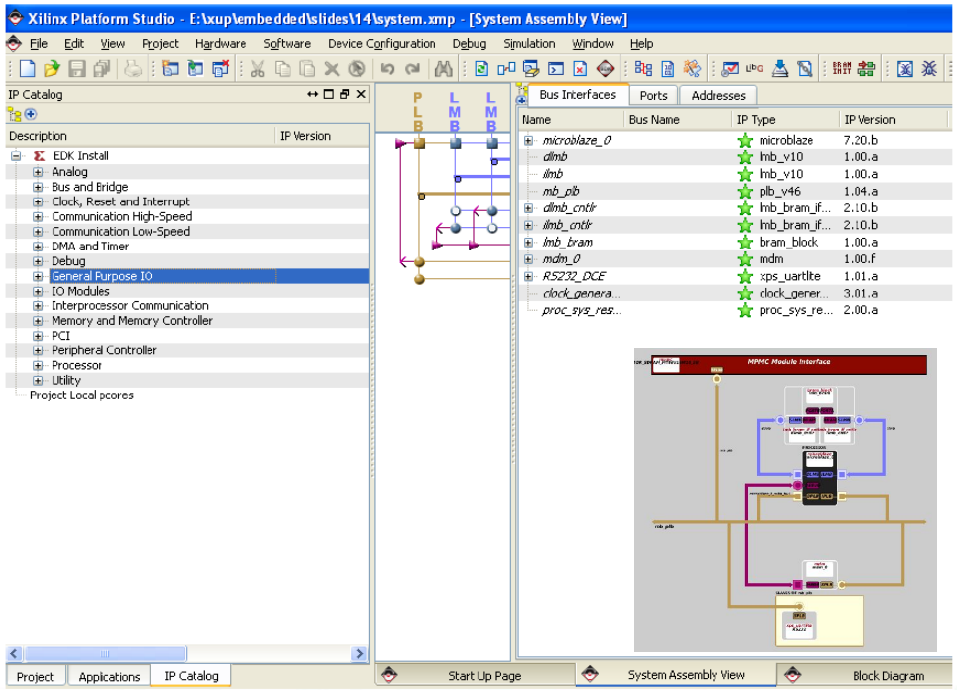
- Specification
  - HDL
  - Codesign
  - Others
- Verification
  - Simulation
  - Debugging
- Radiation
- Programming

Hardware Description

- Basic HDL (...sine qua non)
  - VHDL, Verilog
  - Plus IP-Cores
  - *Don't be afraid!*

```
Begin
Wait until rising_edge(clk);
C <= A + B after 5 ns;
End process;
```

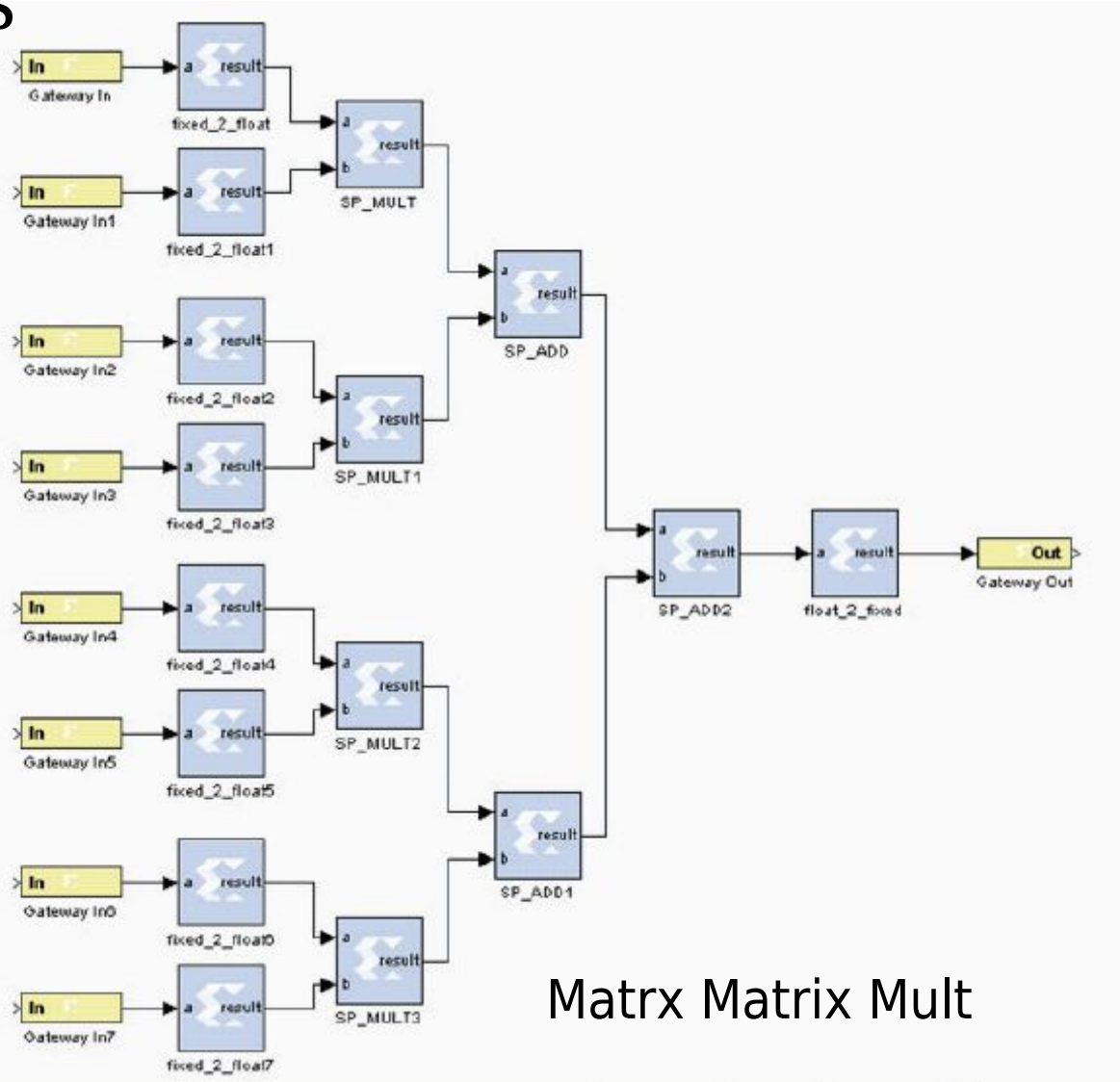
- Embedded: EDK



- Higher level
  - Custom pipeline generators
  - C-based
    - Some general tools
    - FCUDA
  - System-Verilog/C
- All very application dependent

System Generator

- Configurable „macros“ for Matlab
  - Format conversion
    - Integer, fix, float
  - Arithmetic
  - Image processing
  - Filters
  - FPGA IP-cores
  - Utilities
- Simulation models
  - Matlab, HDL



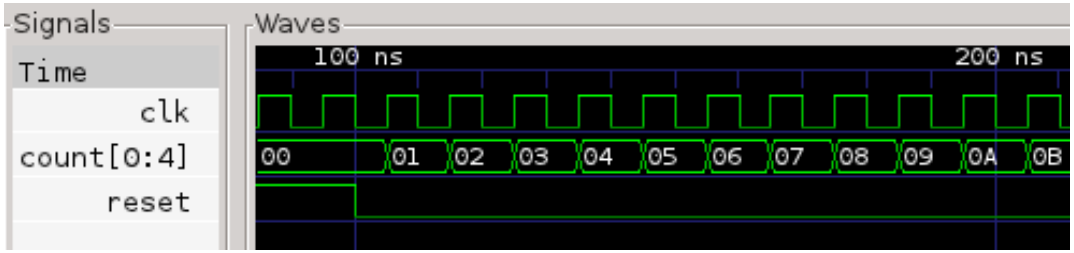
Matrx Matrix Mult

Xilinx

Simulation/Debugging

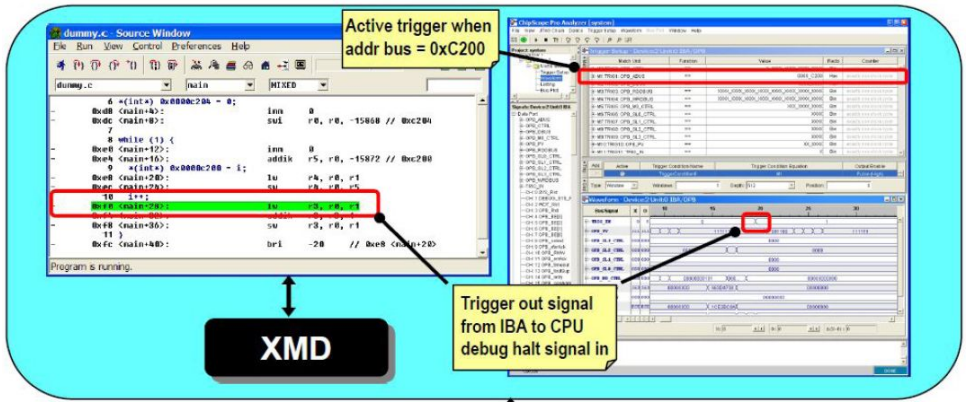
- Simulator „runs“ the HDL description
  - Waveform output
  - Breakpoints
  - Verification
    - Text-I/O
    - Assertions
    - API (FLI) + testprog.
  - Incl. processor

Fast turnaround
Slow execution



- ChipScope
  - Access FPGA internal state + memory content
  - Trigger + Control
  - Waveform display
  - Incl. processor

Slow turnaround
Fast execution



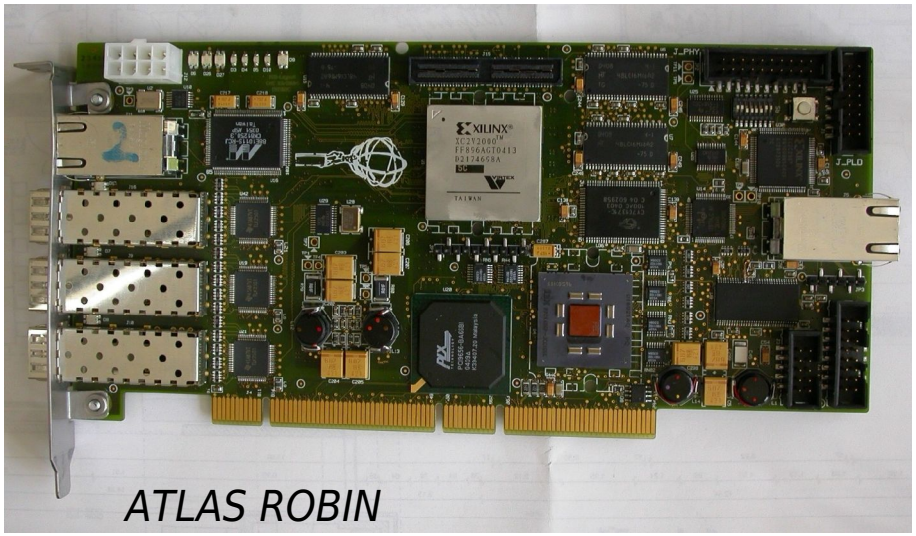
Programming

- JTAG (4-wire test access port)
  - Most basic: download config data via JTAG programmer
  - Debugging support (Chipscope, Gdb)
- FLASH
  - Powerup boot from serial/parallel FLASH
- Configuration access port
  - Memory interface for µC/CPU
  - Can be internal access (e.g. from soft processor)
  - Can be partial reconfiguration (depends)

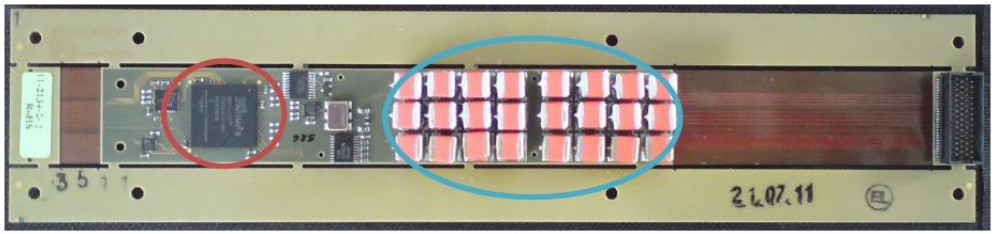
Radiation Protection

- Problem: SEU errors in configuration SRAM
- Work-arounds
  - Radiation tolerant devices
    - Special devices (limited resources, higher cost)
      - Space applications
  - TMR (triple mode redundancy)
    - Design effort, resource consumption
  - Scrubbing
    - Rewrite config memory from external, rad-hard subsystem
    - Full „refresh“ at regular intervalls
    - On-demand – (partial) rewrite on ECC errors

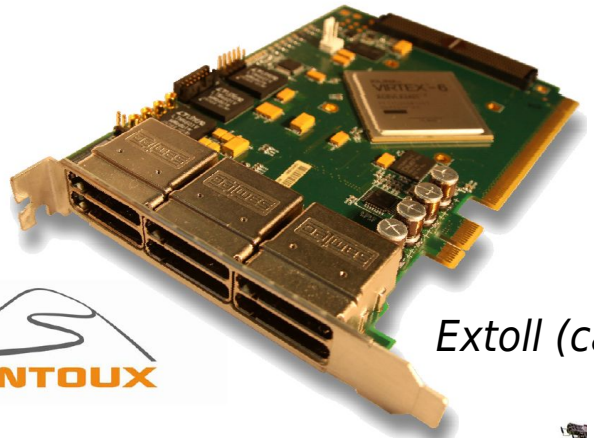
Build or Buy?



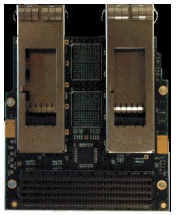
ATLAS ROBIN



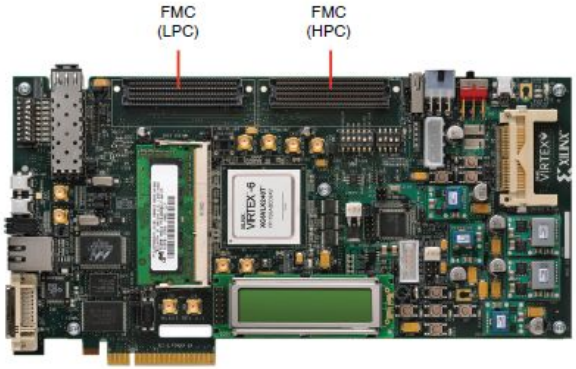
XFEL IOB



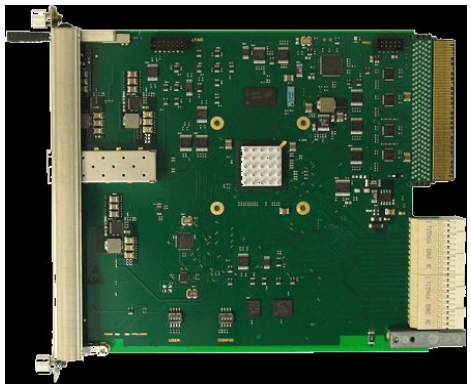
Extoll (cag, ziti)



PCIe + FMC



VXS



mTCA

Summary

- Very interesting technology
  - Flexible I/O
  - High performance
  - ASIC „replacement“
- Well suited for experimental Physics
  - Custom systems
  - Off-the-shelf expansions/systems
  - Lifetime HW bug-fixes „in the field“
- Tools: need to get used to ...
  - ... but worthwhile

Remember: it's PROGRAMMING