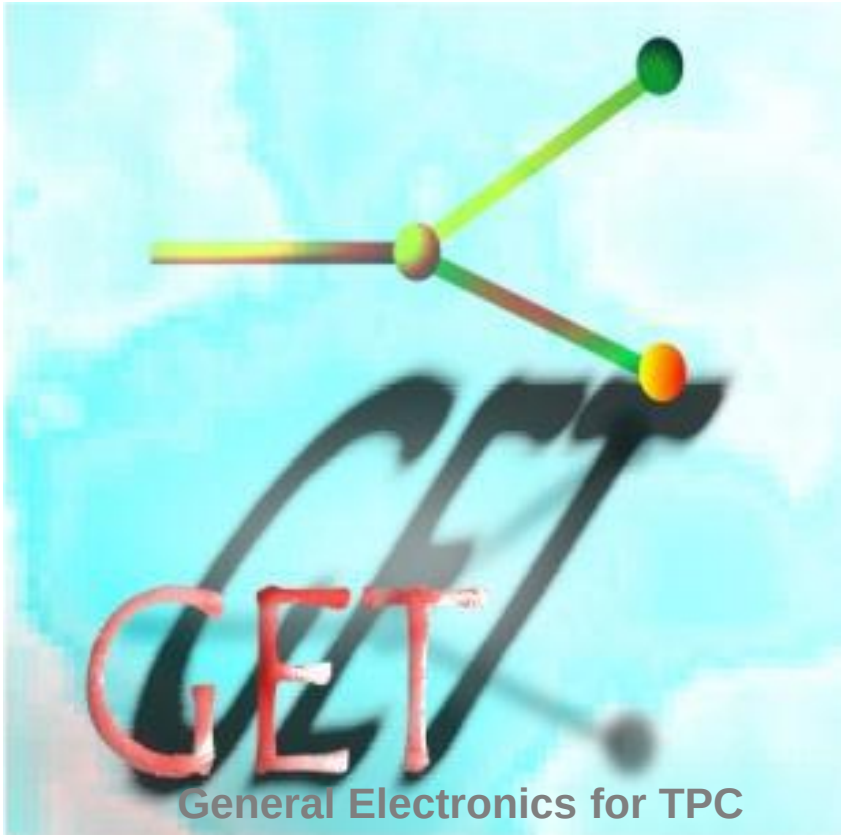
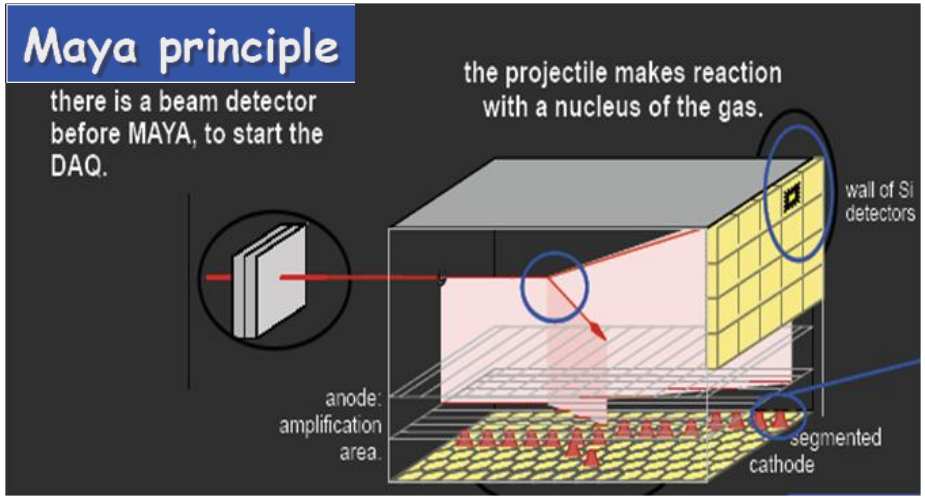


A new architecture based on the µTCA™ standard

With a short introduction to µTCA for physics …

Gilles Wittwer

TODAY: 32x32 = 1024 channels



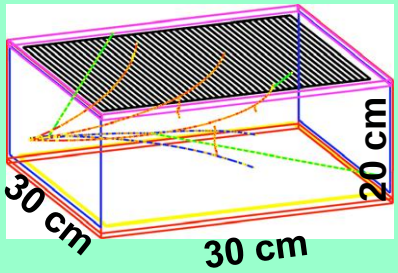
DAQ based on GASSIPLEX ASICs

- ⇨ **Long dead time** (max. counting rate ≈ 100 Hz)
- ⇨ **Low integration** (16 channels/circuit)
- ⇨ **Old technology** (Availability, Quantity ?)

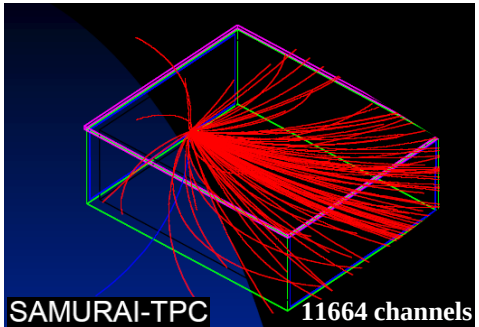
Do not fit with the requirements of the new generation TPC

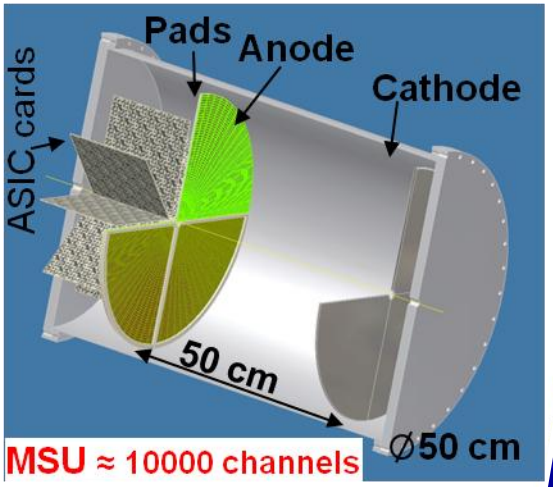
- ➔ **High number of channels (> 5000)**
- ➔ **+ one order of magnitude in terms of counting rate**

ACTAR ≈ 16000 channels @ GANIL

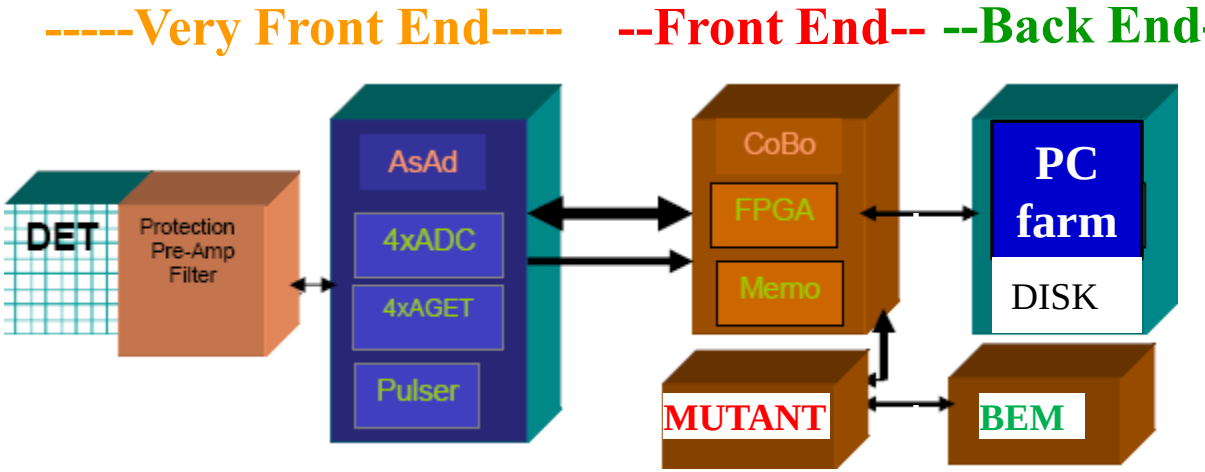


TOMORROW: 10000 channels or more … @ 1KHz (ICR)





DAQ block diagram



AGET: Asic for GET – 64 analog channels - 512 cells/channel

ASAD: AGET Support for Analog to Digital – 4 AGET

COBO: COllection BOard – 4 ASAD - 1024 digital channels

MUTANT: MUtiplicity, Trigger ANd Time (3 trigger levels)

BEM: Back End Module (coupling, logical inspections, …)

IRFU*

CENBG*

MSU

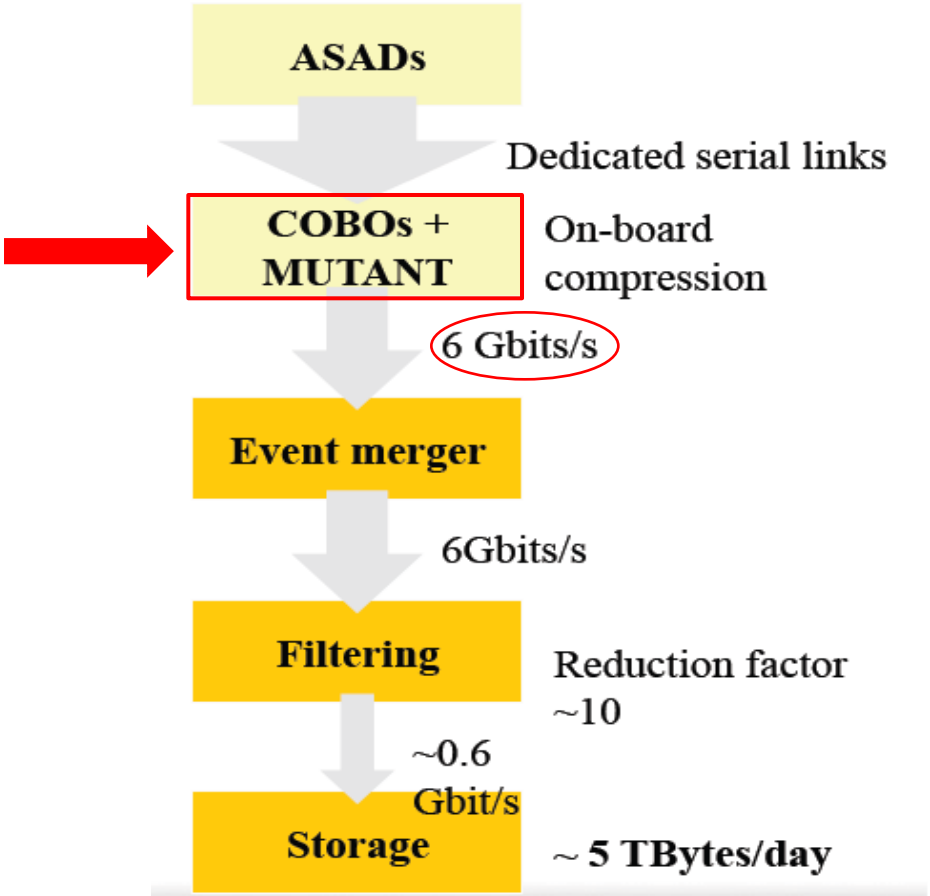
* GET project funded in these labs by the French ANR

Example of data rate for ACTAR TPC

In a CoBo: 64x512x4x4=512 Ksamples
Data size
- bulk format (24 bits/sample)=12 Mbits
- zero suppr. (32 bits/sample): 16 Mbits

Compression factor=4 =>4Mbits/CoBo

ACTAR (16384 pads)=16 CoBo
=> 6.4 Gbits/s @ 1kHz if 10% hit pads



What type of bus and crate for the front end electronic ?

// BUS

NO BUS or CUSTOM BUS

① NIM Instrumentation System

② Xxx Laboratory standard

SERIAL BUS but which one ?

VITA

VME32 VME64 VME 2eSST VXS VPX

Military, aerospace, rugged applications …

PICMG

PCI EXPRESS

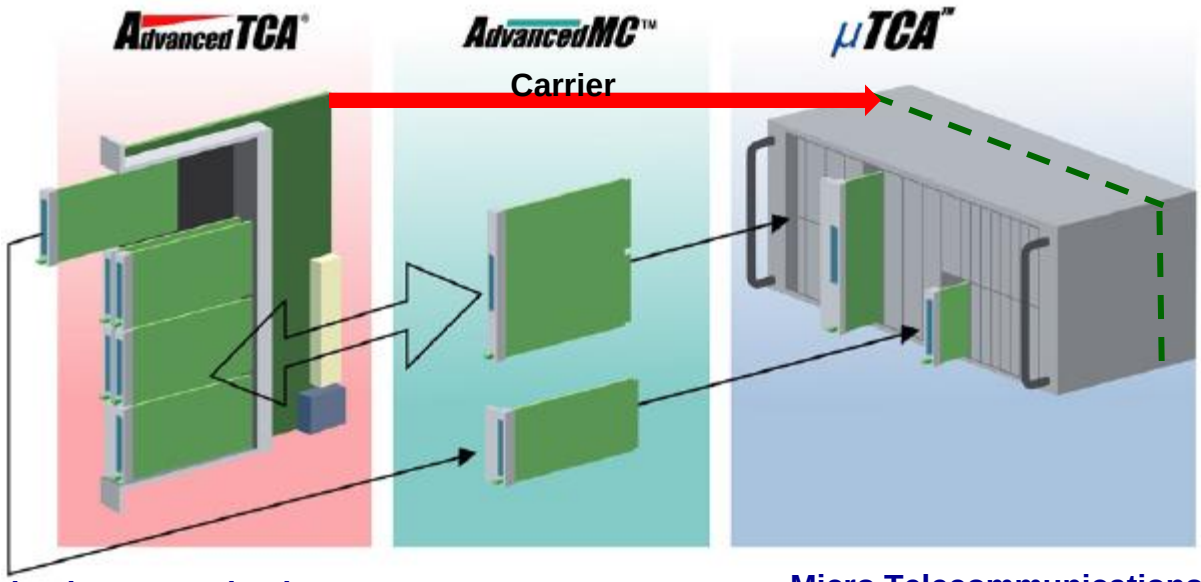
Telecom world

AdvancedTCA™

③ µTCA™

3 choices for a vote held in the GET collaboration…

Why µTCA ?



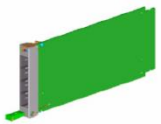
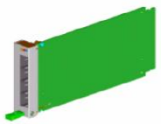
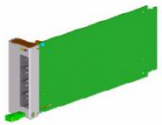
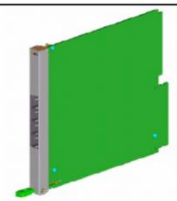
Here the carrier is unique,
It is the backplane !

Advanced Telecommunications Computing Architecture

Advanced Mezzanine Card

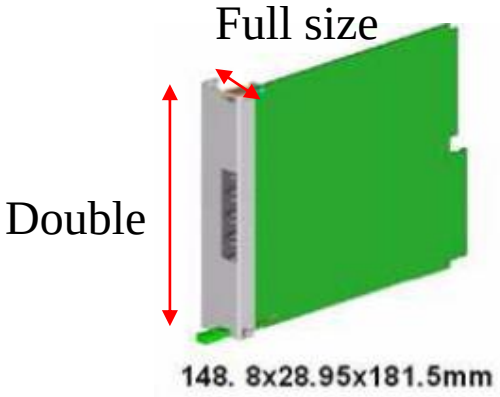
Micro Telecommunications Computing Architecture

Advanced Mezzanine Card configuration examples

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148. 8x18.96x181.5mm	 148. 8x28.95x181.5mm

Advanced Mezzanine Cards (AMC)

The largest one has been chosen for GET electronics



About PICMG

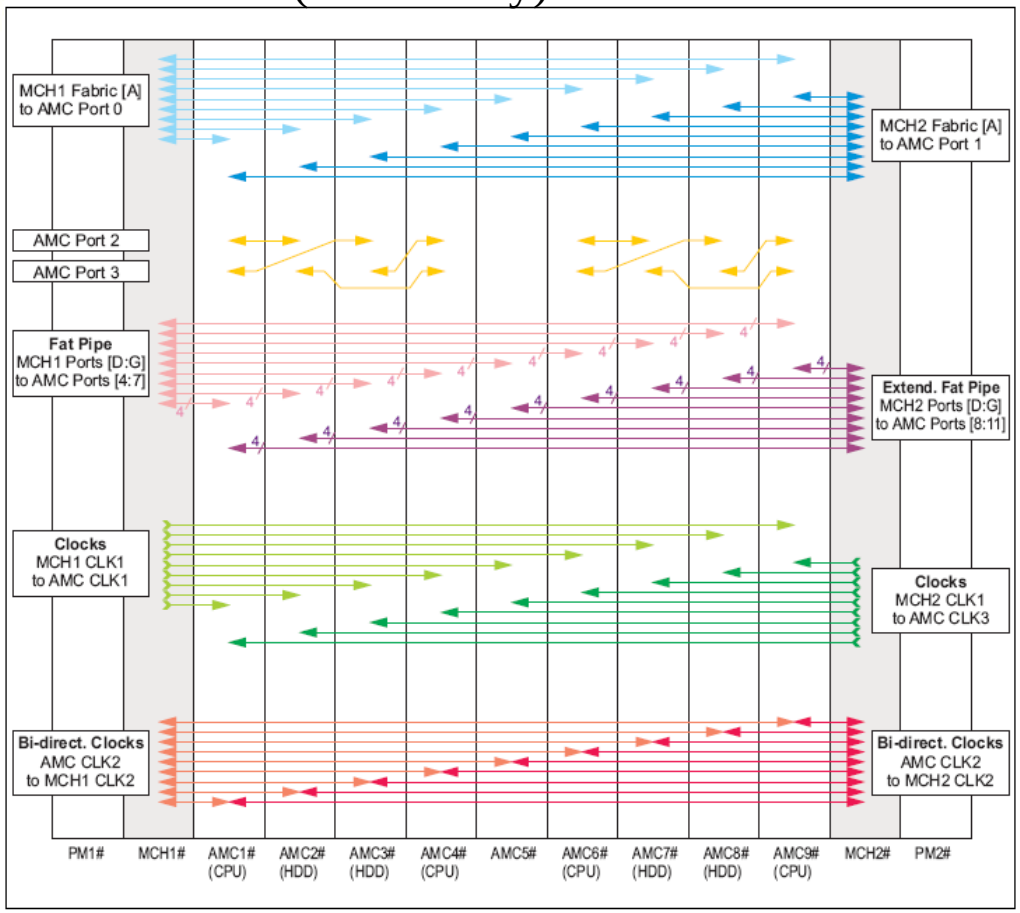
Founded in 1994 as the PCI Industrial Computer Manufacturers Group, PICMG is a consortium of over 250 companies that collaboratively develops open specifications for high performance telecommunications, military and industrial computing applications.

http://www.picmg.org

Choice of µTCA standard for the project

GANIL
⇨Laboratory leader & referent
For µTCA of GET

« Dual Star » topology
(redundancy)



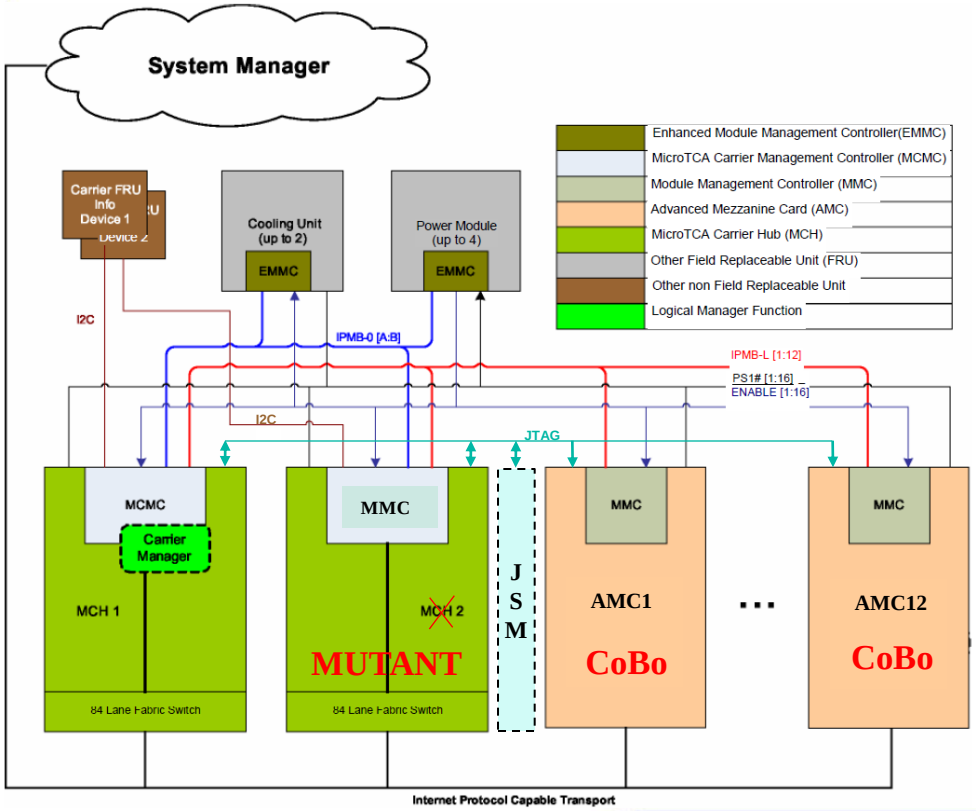
Up to 6.5 Gbit/s by port (1TX/1RX)

1 MicroTCA Backplane
2 Cable Tray
3 Air Filter
4 DC Outputs Power Supply 1
5 Grounding Terminals
6 Power Supply 1 (optional)
7 Fan Tray
8 DC Outputs Power Supply 1
9 ESD Wrist Strap Terminal
10 Slot for Power Supply 2

MicroTCA Carrier Hub (MCH)
Carrier management / Network Switch

Power Module (PM)

Shelf management

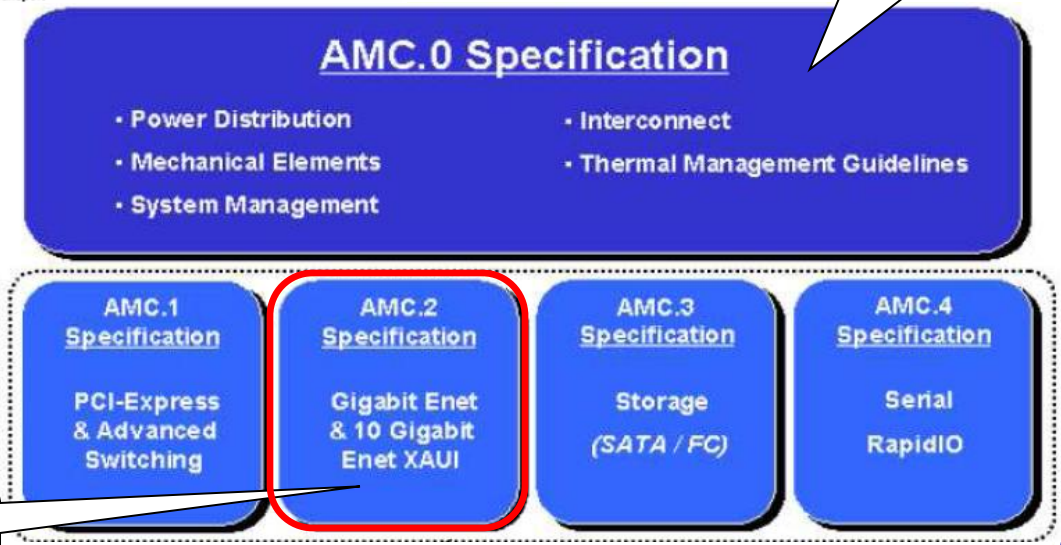


- "Hot Swap" capability
- 80 W max/module
- 2 temperature sensors/module
- Jtag Switch Module option

MUTANT MMC (VT026 from Vadatech)

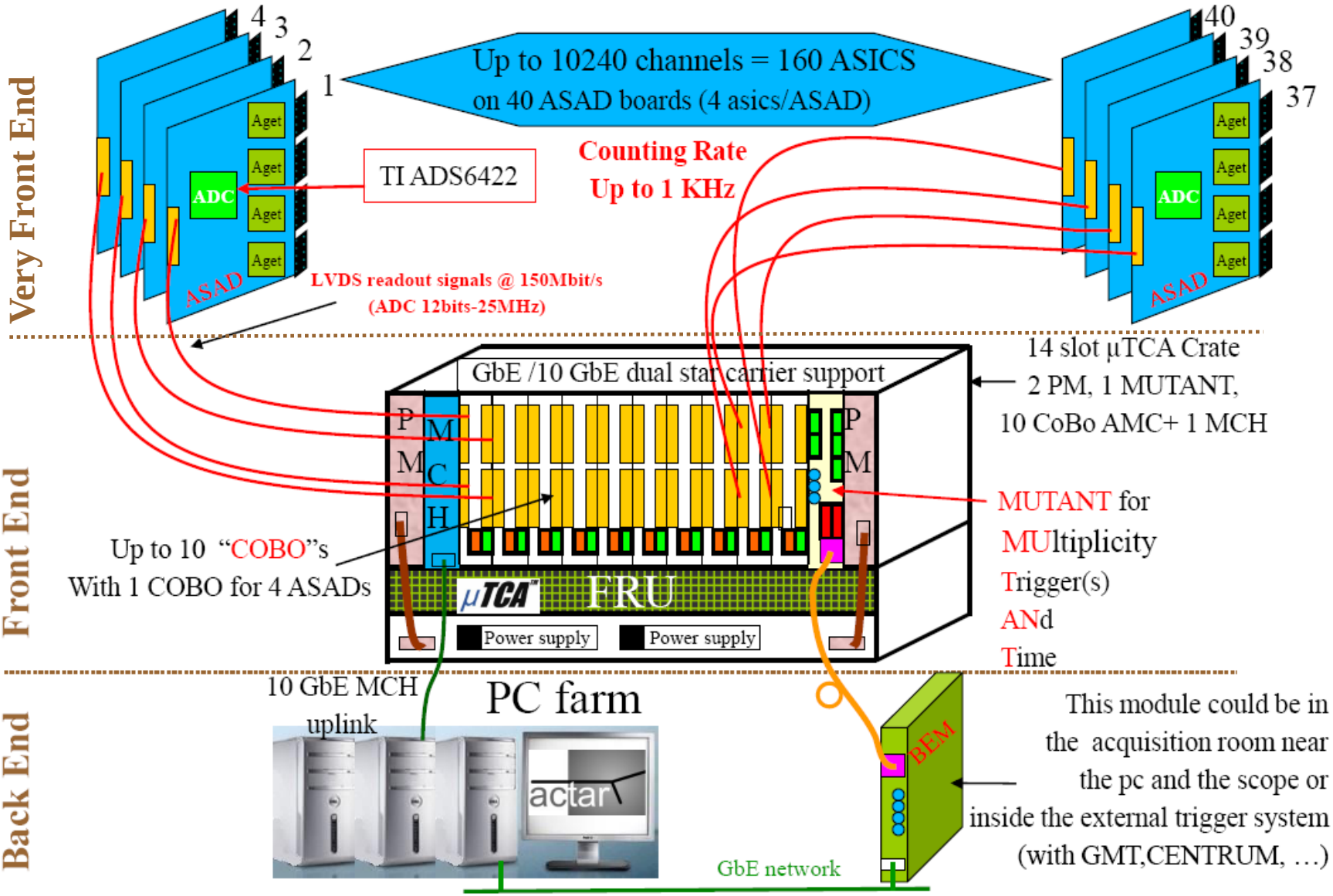
1 - Mechanical
2 - Electrical
3 - Thermal

Several levels of specifications

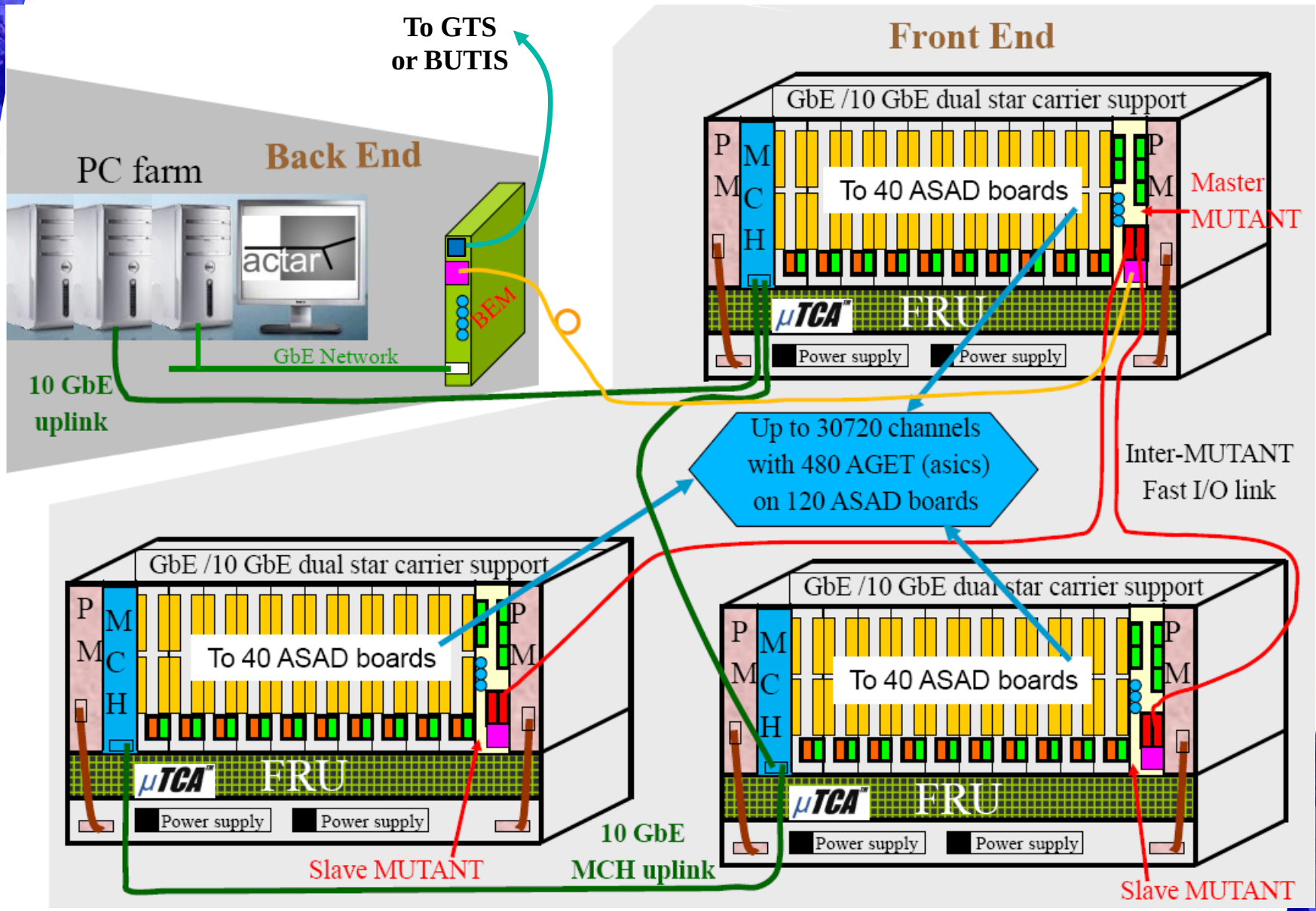


4 – Communication protocols between AMC/AMC & AMC/MCH

1 µTCA shelf typical architecture



Full architecture – 3 µTCA shelves

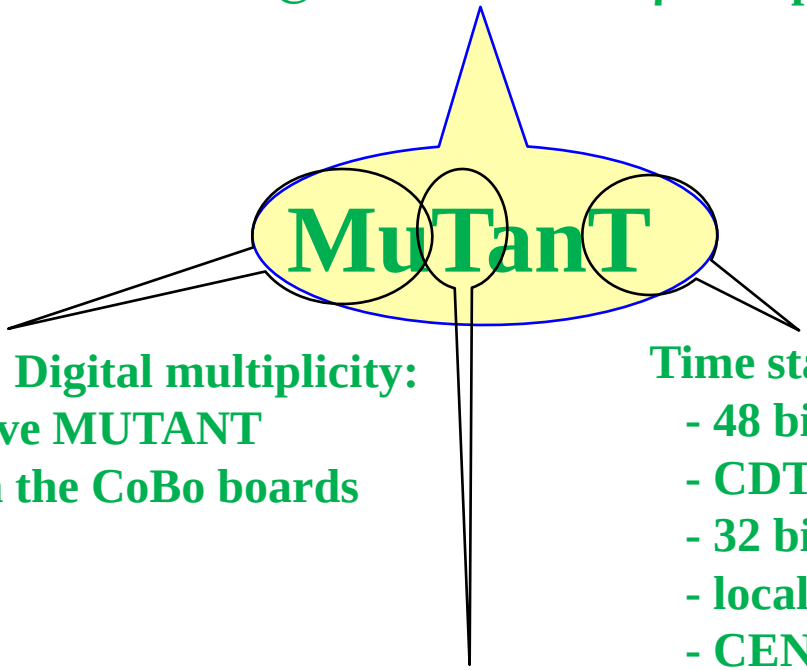


What are the tasks of MUTANT ?

Distribution of a 100 MHz clock to every CoBo of each crate, phase aligned (skew< 1ns - TDC) ⇨ µTCA-CLK1

Distribution of a synchronous start/stop sampling (phase aligned) ⇨ µTCA-CLK2

Exchanging data with the CoBo @ 800 Mbit/s ⇨ 5 µTCA ports (TX/RX)

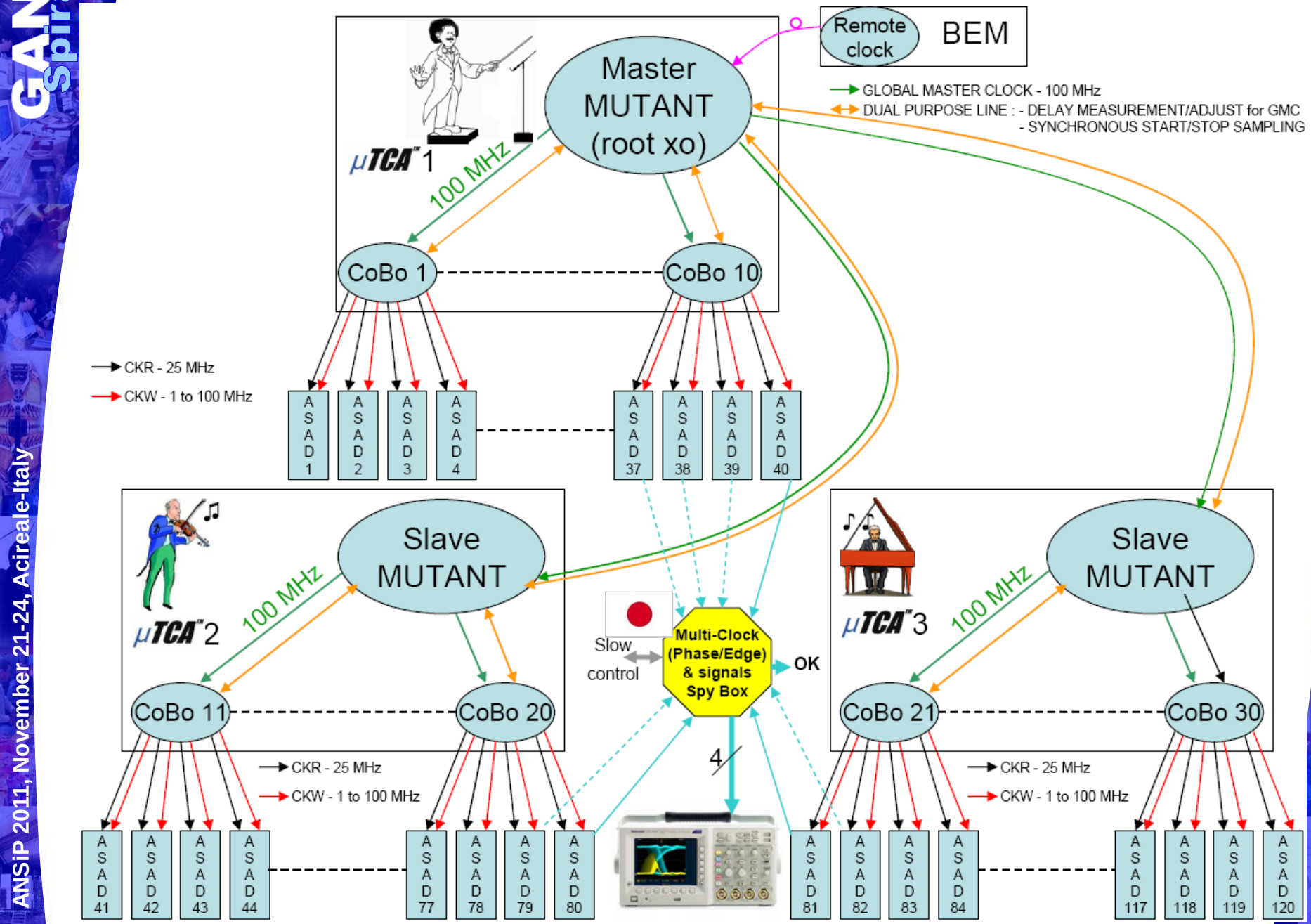


Building the whole TPC Digital multiplicity:
- **Master Mutant + slave MUTANT**
- **Each MUTANT with the CoBo boards every 40 ns**

Time stamp:
- **48 bits / 10 ns**
- **CDT/autonomous mode**
- **32 bit event number (CDT)**
- **local/remote (via BEM)**
- **CENTRUM interface (GANIL)**

3 Trigger levels:
- **-LØ= External Trigger**
- **-L1 = Multiplicity Trigger**
- **-L2 = Hit Pattern Trigger**

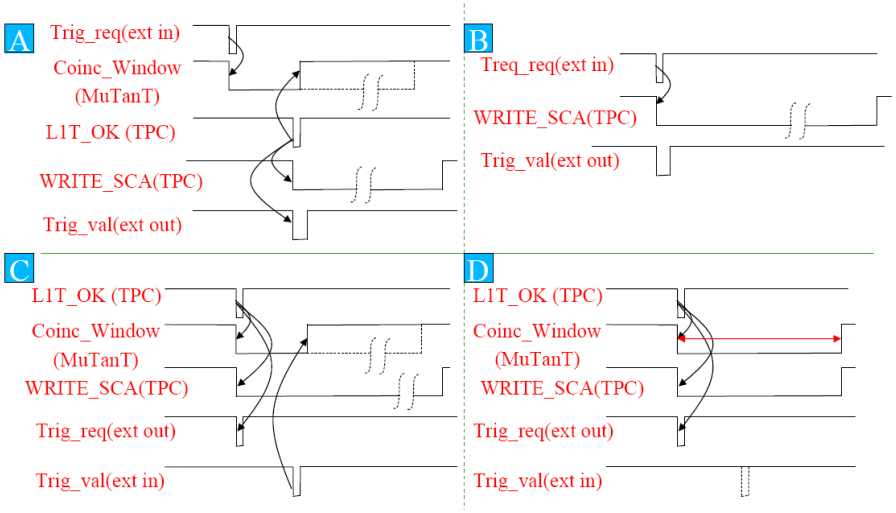
Clock distribution & synchronization



Trigger management details (LØ & L1)

Level Ø = External Trigger

External trigger is the Master trigger

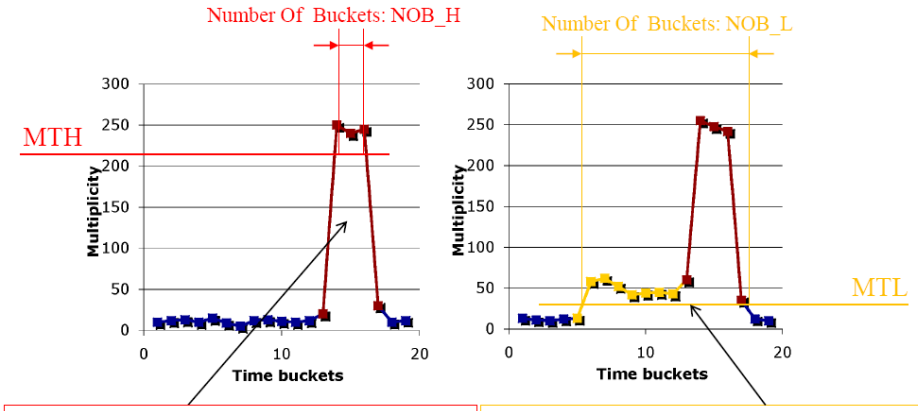


External trigger is slave of MuTanT

Level 1 = Multiplicity Trigger

Digital multiplicity on 16 bits (15 significant bit + 1 parity bit)
Checked by Master MUTANT @ 25 MHz (every 40 ns)

2 programmable multiplicity threshold (high & low): MTH, MTL
with associated programmable number of time buckets



Pure beam event with programmed trigger conditions => MTH = 220 & NOB_H = 3	Beam reject logic with scattered particle detection trigger conditions => MTL = 30 & NOB_L = 12

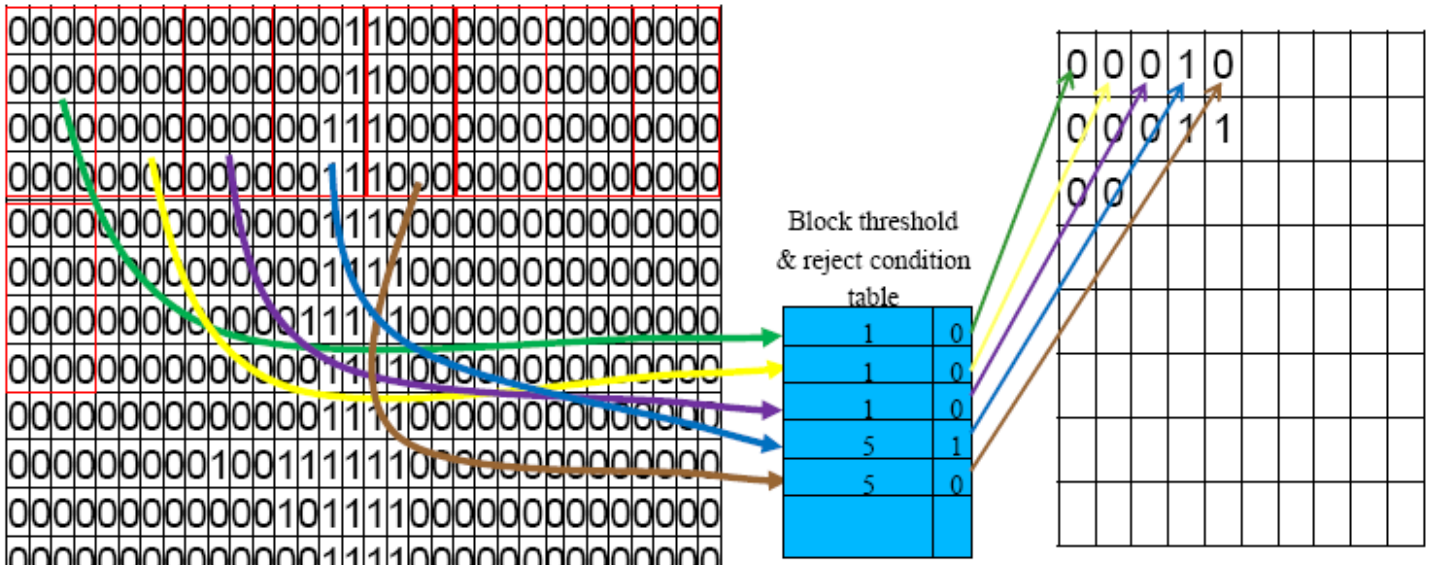
Trigger management details (L2)

with processing

Level 2 = Hit pattern trigger

2 options: - from the raw matrix

- from pads to blocks of pads (macropads)



programmable → Size	Blocks in a COBO	Total blocks N (for 16 COBOs)
4 x 4	64	1024
8 x 8	16	256
16 x 16	4	64

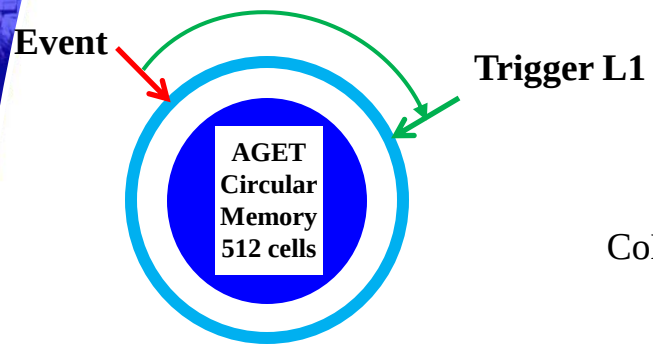
Scanning of the TPC hit pattern
in order to produce
a "macropad" pattern

30720 pads → 1920 mpads
30720 pads → 480 mpads
30720 pads → 120 mpads

MUTANT- CoBos data exchanges

main time values

Full memory



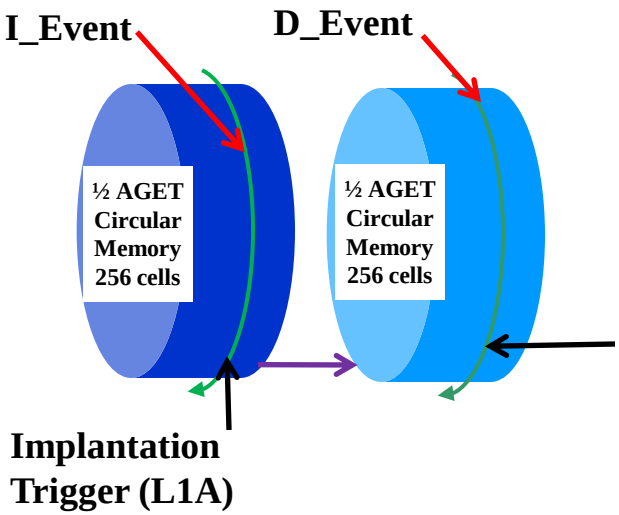
AGET: Sampling Frequency = 1-100 MHz
Trigger roundtrip: 512 x 10 ns = 5.12 µs
to 512 x 1µs = 512 µs

MUTANT Programmable Delay & Gates are 16 bits wide
Attached to GMC (10 ns)

CoBo to MUTANT : L1: new multiplicity value @ 25 MHz max
nothing to do @ MUTANT level for lower frequency
L2: 1.3µs to receive the TPC hit pattern (one shelf)
12.8 µs for added shelves

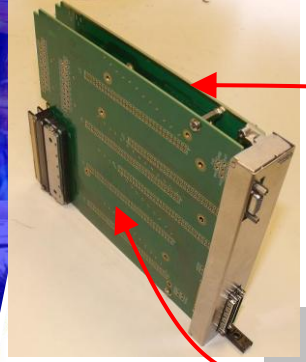
MUTANT trigger "OK" to CoBo "STOP": -LØ : 30 ns/655 µs max
- L1 : 80 ns /655 µs max
- L2 : depends on the algorithm

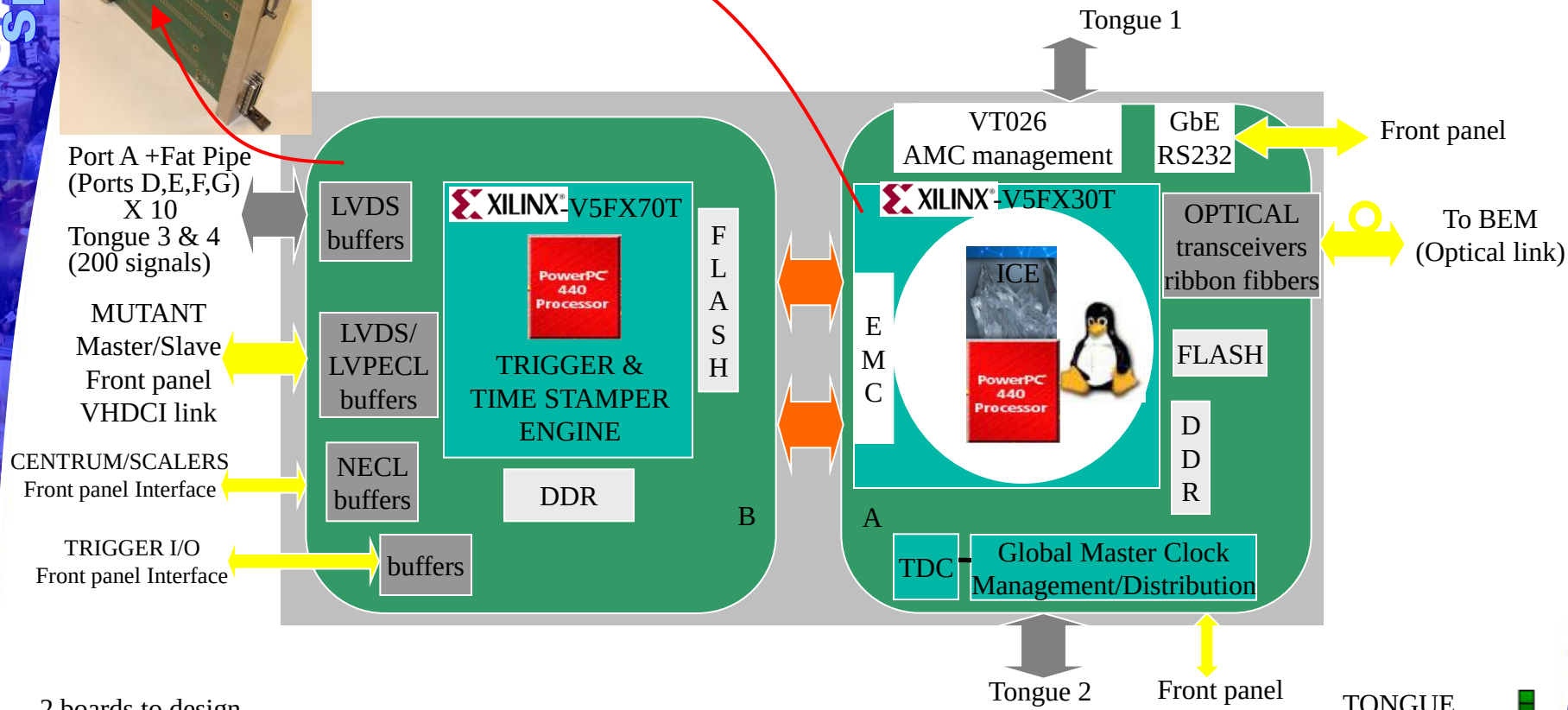
2 x half-memories (2p decay)

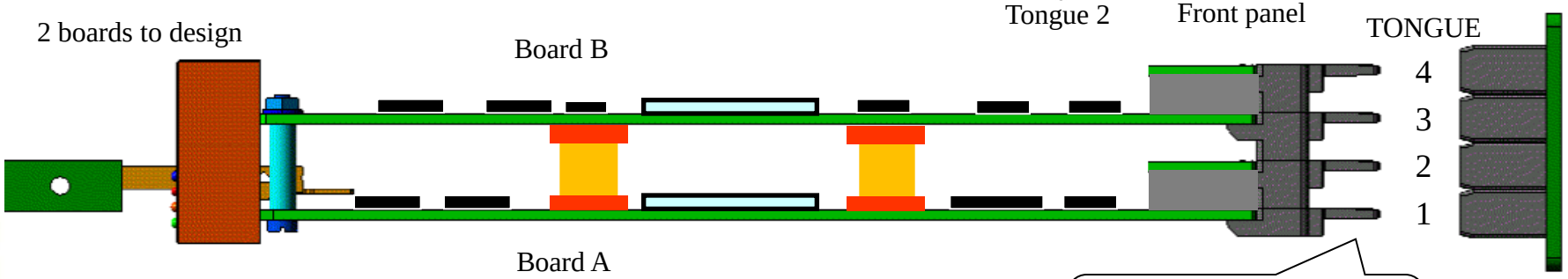


MUTANT information's to CoBo: - L2 mask pattern: 1.3 µs
- Time stamp + Event Number: 120 ns
- Time stamp only: 80 ns

MUTANT block diagram & board assembly

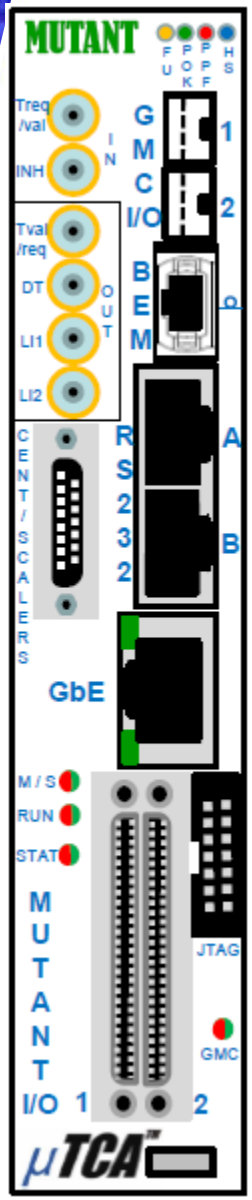




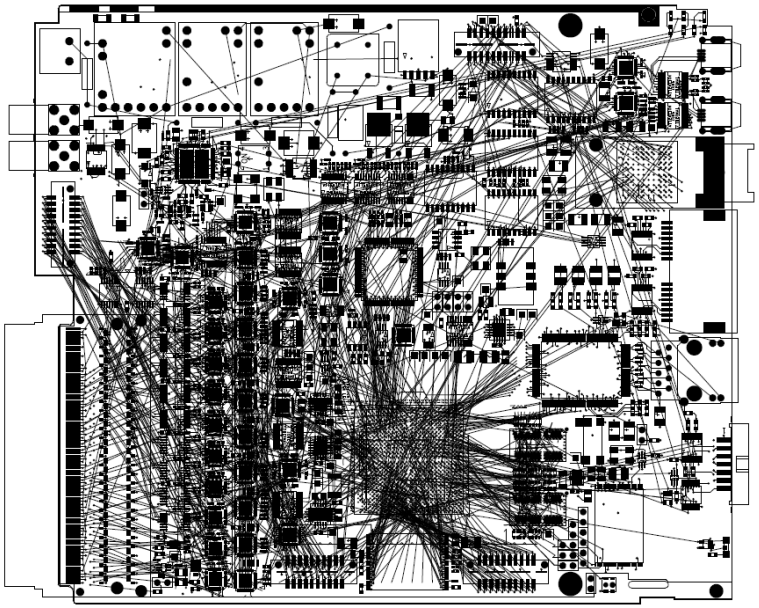


1 tongue = 2 x 85 pins
4 tongues to manage
= 680 pins!

MUTANT – few hardware aspects



Front Panel

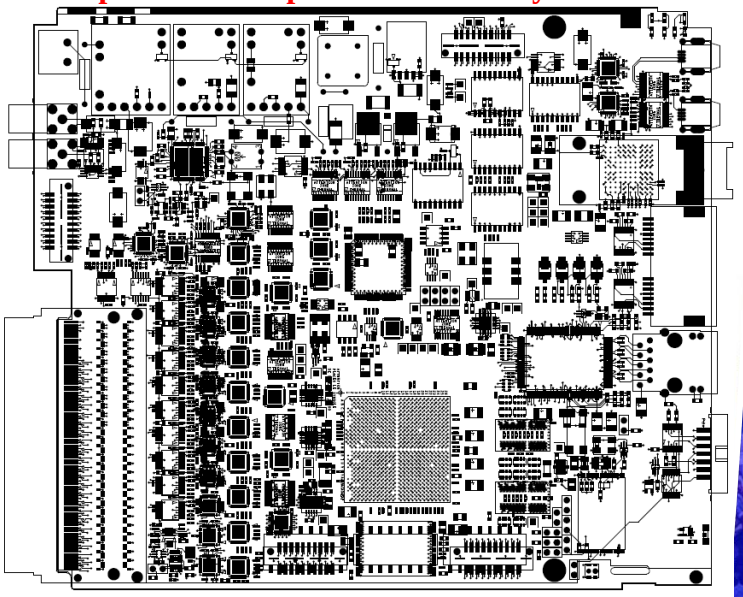


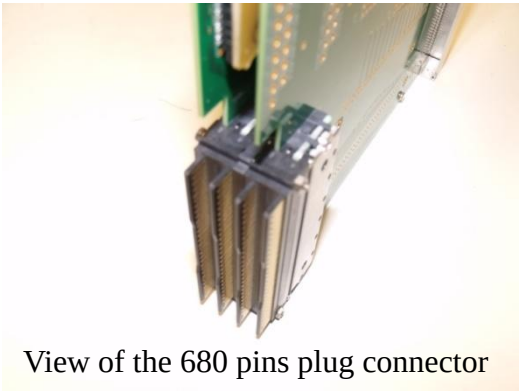
MUTANT board A - PCB routing

≈ 5000 nets including 200 differential pairs (100 Ω)

MUTANT board A - PCB implantation

Up to 1500 components on a 14 layers PCB

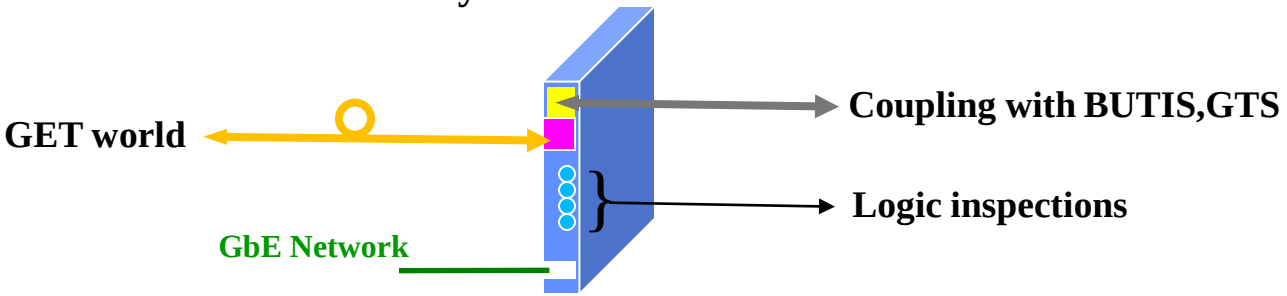




View of the 680 pins plug connector

About Back End Module (BEM)

GET with MUTANT: Ready today for coupling @ GANIL with CENTRUM interface !
But tomorrow ?
Or in another laboratory ?



Goal: Be able to synchronize GET (Clock & Time stamp) by an external system or to be synchronized by GET if ancillary detectors are added to the TPC

Work to do: Writing specifications in 2012, especially the board standard (VME, AMC, …)
Starting design in 2013

Conclusion about GET front end

- 2 sources of µTCA shelf are validated for the project
  - a "9 AMC slot" shelf & an "11 AMC slot + JSM" shelf

- MCH with 10 Gbe uplink was purchased
  - Used in a first step for management and tests
  - Network performance tests have to be made

- MUTANT module is on track
  - Board A is under test

    (as a kit on the table then inside the crate with management)

  - Design of board B is in progress
  - Full MUTANT is expected for mid 2013

- CoBo AMC design is in progress at NSCL/MSU
  - Harmonization of choices in terms of components and µTCA configuration

- First µTCA configuration (CoBos + MUTANT) by end 2013

GANIL Spiral 2

Short introduction to µTCA™ for physics …

Gilles Wittwer

Short introduction to MTCA.4

Working group and press release

What is this new “xTCA for Physics”

The data systems used today to run these research institutions, such as the particle accelerator at CERN near Geneva, are VMEbus systems.

For the next generation of systems, the particle physicists group has committed itself again to an open standard. In future, MicroTCA systems will be used.

The main reasons for changing from VMEbus to MicroTCA are that MicroTCA has implemented an extensive remote management that detects all possible faults on plug-in boards, in the power supply systems and in the ventilation system.

The MicroTCA basic specification forms a very good basis that covers most of the requirements of this research group. However, a number of additional features are required that are not implemented in the MicroTCA basic specification.

For this reason the PICMG working group "xTCA for Physics" was formed to define a MicroTCA sub-specification, MTCA.4 and ATCA RTM Z3A specification.

Recently, PICMG Ratifies new MicroTCA and AdvancedTCA Specifications

WAKEFIELD, Mass., October 18, 2011 – PICMG, a leading standards organization for the communications, military and embedded computer industries, announces the adoption and availability of the two new specifications, The MicroTCA® Enhancements for Rear I/O and Precision Timing (MircoTCA.4) specification, and PICMG 3.8 - AdvancedTCA Rear Transition Module Zone 3A specification.

“Many of the changes introduced by both of these specifications are the result of PICMG’s high energy physics efforts through direct engagement with researchers in this field. This will allow both the MicroTCA and the AdvancedTCA community to better serve these markets or other additional markets that need synchronized data acquisition or greater I/O needs,” said Joe Pavlat, PICMG’s President.

From MTCA.0 to MTCA.4

Reference Specification for Management

PICMG 3.0
AdvancedTCA
Base Specification
(Telco-centric spec)

Reference Specification for Board Implementation

AMC.0
AdvancedTCA
Mezzanine Cards
Base Specification
(Telco-centric spec)

Diverse market segments:

- **Telecom**
- **Defense**
- **Medical**
- **Transportation**
- **Industrial**

MicroTCA
Base System
Specification

MTCA.0
MicroTCA Air Cooled
Base Specification
Environment:
Controlled Telco / Industrial
(Telco-centric spec)

MTCA.1
Rugged Air Cooled
Specification
Environment:
Extended Telco / Industry
(Telco/Industrial-centric)

MTCA.2
Hardened Air Cooled
Specification
Environment:
Extended Telco / Military
(MIL-centric)

MTCA.3
Hardened Conduction
Cooled Specification
Environment:
Extended Telco / Military
(MIL-centric)

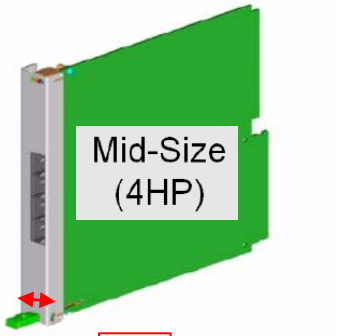
MTCA.4
MicroTCA for Physics
Hardware for
AMC, MicroRTM, Shelf
(High Energy Physics-centric)

MicroTCA Specialized System Specifications

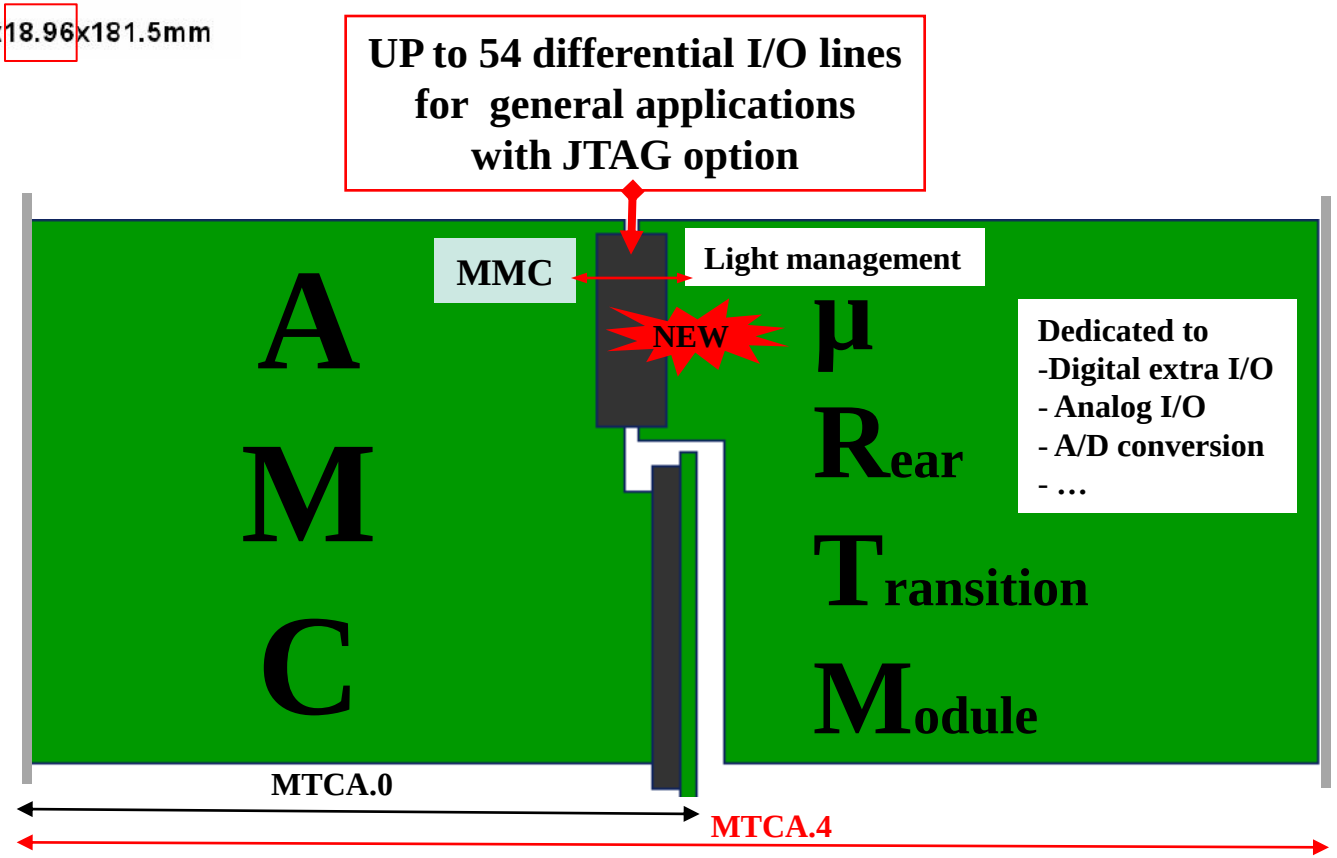
New segment:

- High energy physics and Nuclear physics …

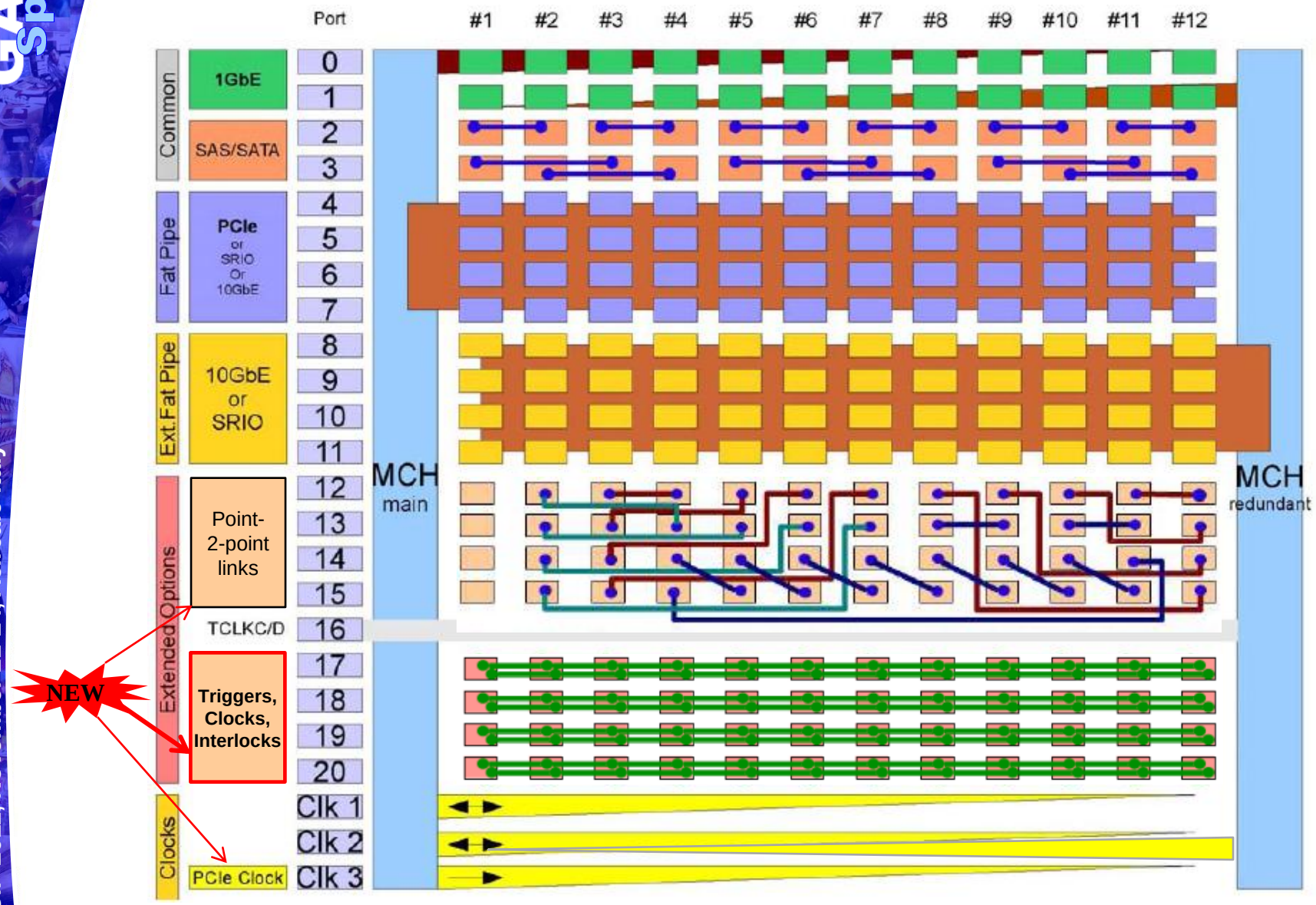
What are the main points of MTCA.4



- ✓ **Specifies rear I/O capabilities for physics applications**
- ✓ **Specify methods for distributing timing synchronization and triggering signals to the shelf, carrier and AMC levels**
- ✓ **Goal:**
  - **Minimal or no changes to the standards**
  - **Maintain backward compliance (with MTCA.0)**
  - **Reuse of COST where possible**



MTCA.4 backplane Topology



First conclusions about MTCA.4

MTCA.4 versus VME

- ❖ **Performances and Management** (Power, temperature, hot swap, …, and redundancy if needed)
- ❖ **No communication protocol attached to the backplane (carrier)**

AMC + µRTM versus VME

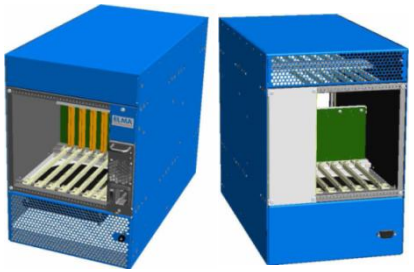
- ❖ Same front panel width as VME boards but + 25% in terms of height
- ❖ ≈ + 25% of PCB surface for components implantation
- ❖ as MTCA.0, hot swap capability (no need to reboot the full system)
- ❖ fully compatible to AMC and previous MicroTCA standards

AMC + µRTM versus VME + Mezzanine(s)

- ❖ µRTM are identified with a standard light management
- ❖ Tasks and designs are easier to separate as form factors are well defined (layout and routing constraints clearly separated)

AMC + µRTM

- ❖ Power budget shared between the 2 boards !
- ❖ No AMC shielding for EMC compared to VXI



Few MTCA.4 shelves are already available …

Thank you very much
for your attention