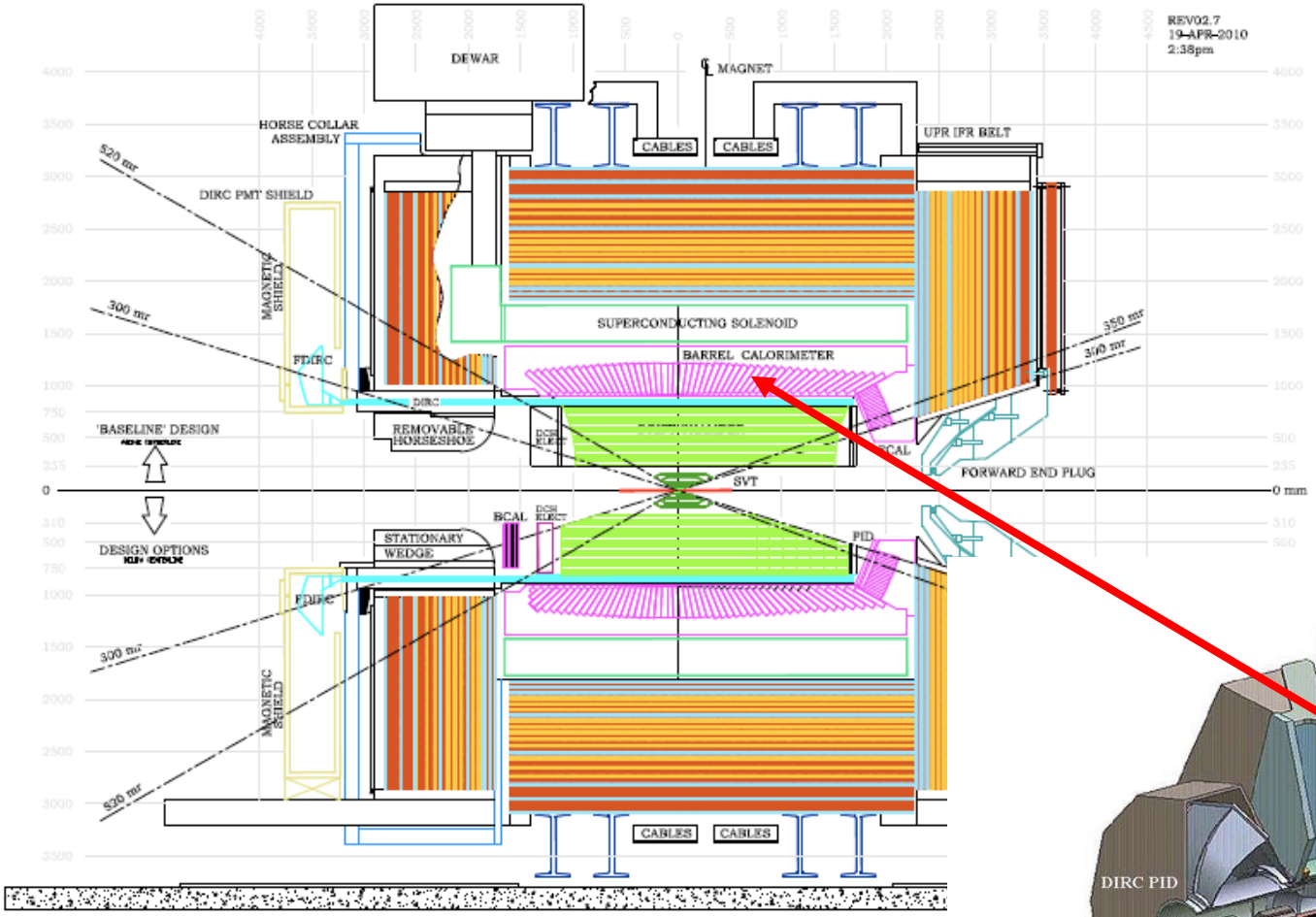
Elettronica di Front End e Trigger del Calorimetro Elettromagnetico di SuperB

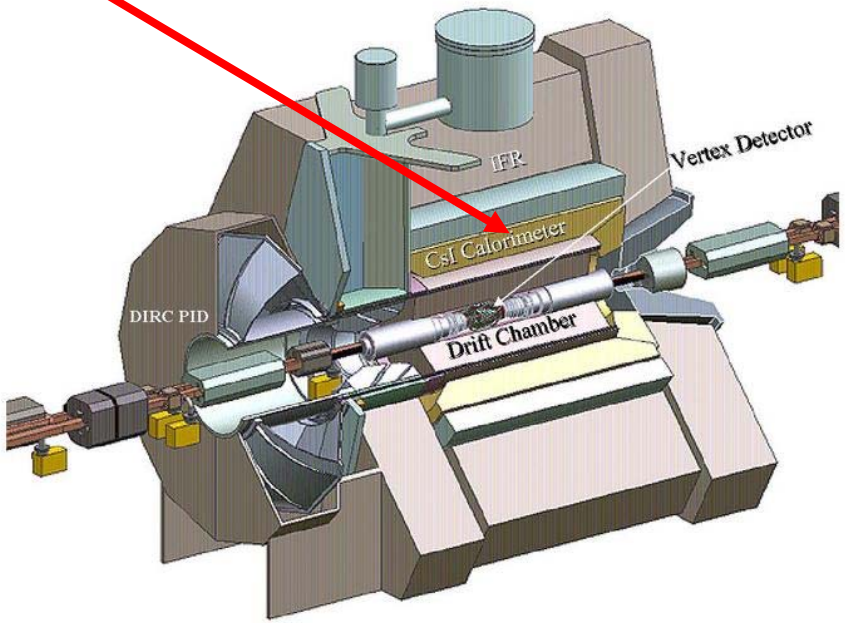
Valerio Bocci INFN Roma

Elettronica: EMC : INFN Roma,INFN Perugia
Trigger: INFN Roma,INFN Perugia,INFN Roma 3,INFN Naples,INFN LNF

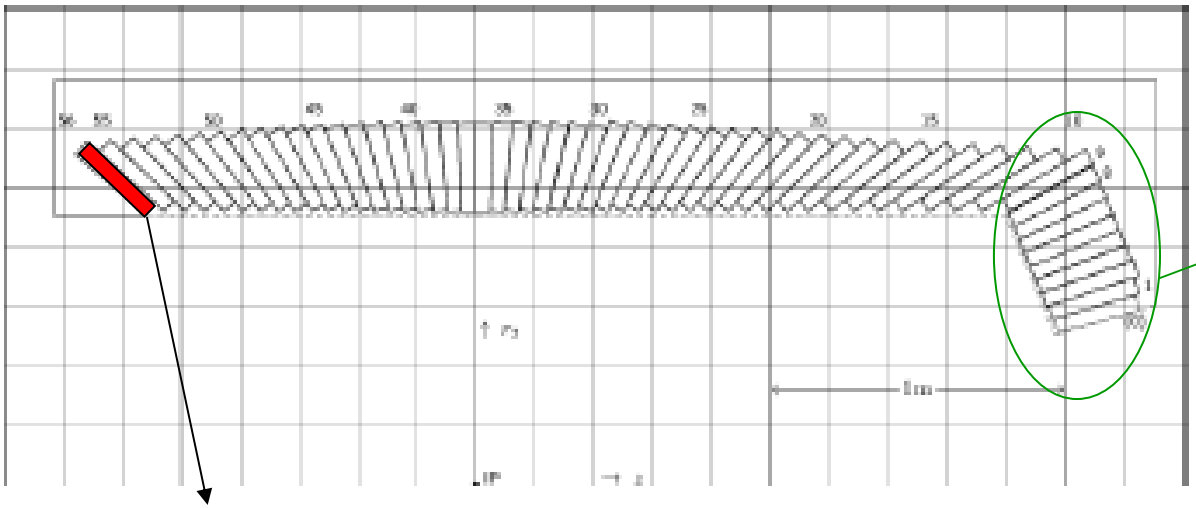
INFN Roma 8 Aprile 2011

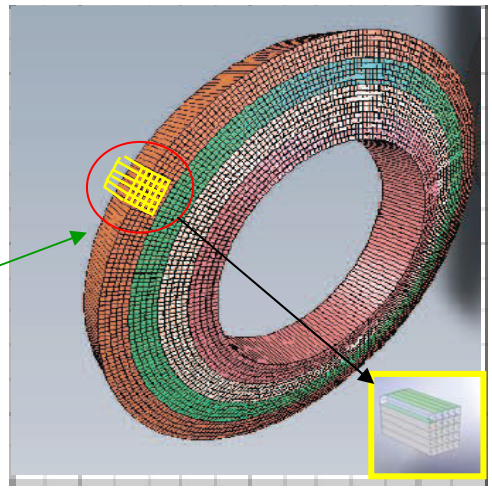
Babar EMC location

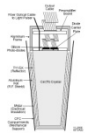




SuperB EMC



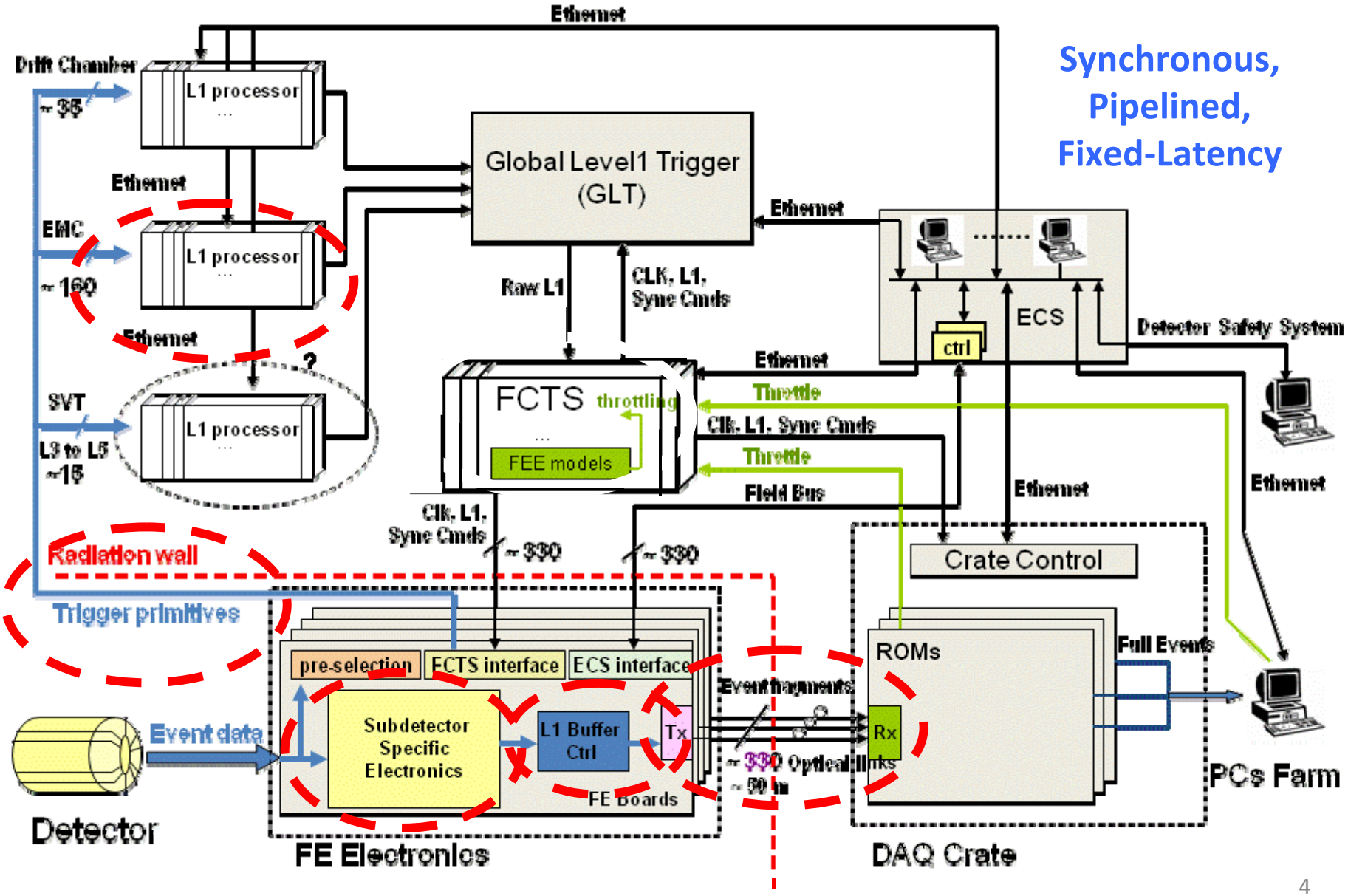




EMC Barrel :
5760 CsI(Tl)
Crystals

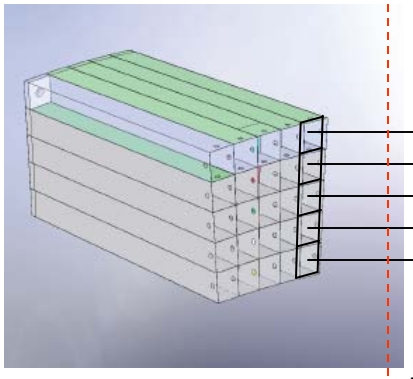
EMC Forward =
4400 Lyso Crystals
(176 modules)

Elettronica SuperB



Synchronous, Pipelined, Fixed-Latency

25 crystals tower readout electronics



Crystals Mechanics

X 5

X 5

X 5

4X

VFE Board

5

Shaper Range Board

Ranges Lvds

5

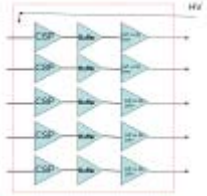
5

Differential ADC Board

ranges analog Coded

ADC CLK

PIN Or APD



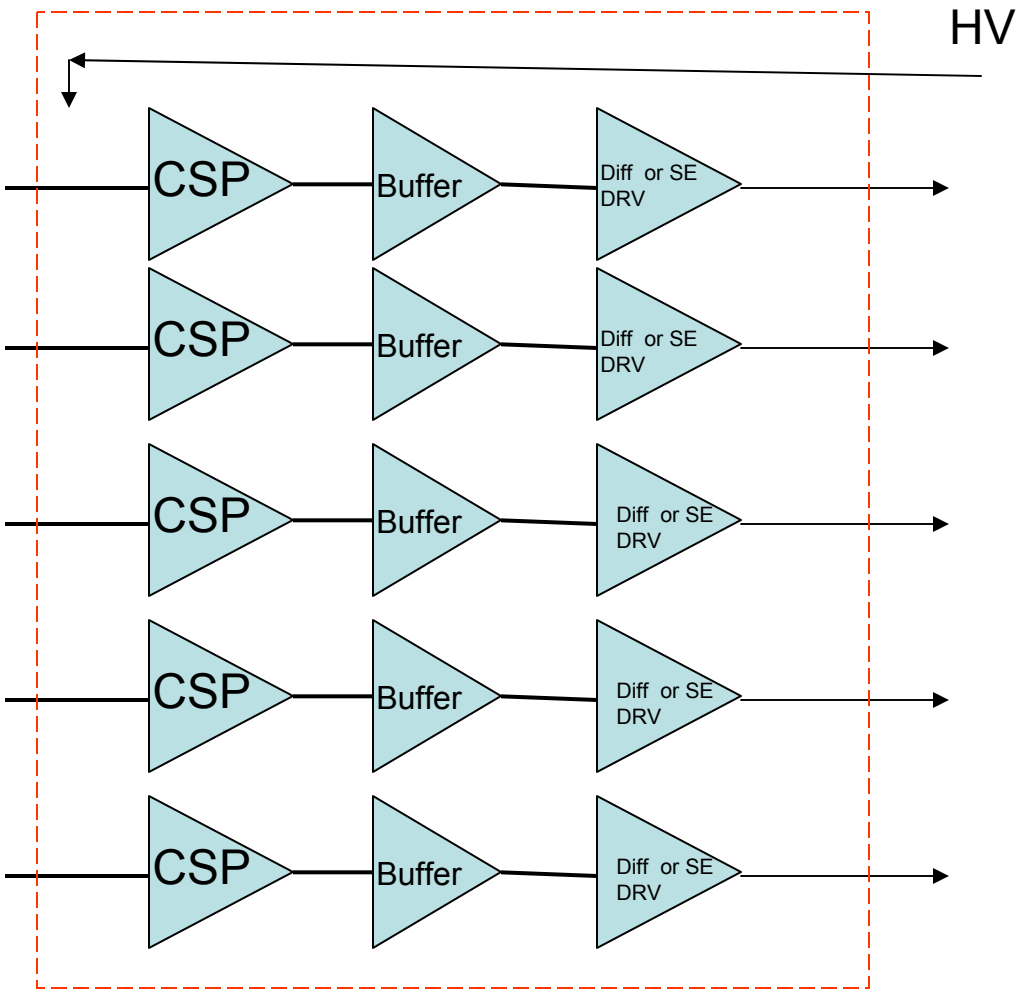
I2c

VME

• 25 channels
(full module readout)
•All boards produced

Very Front End Board

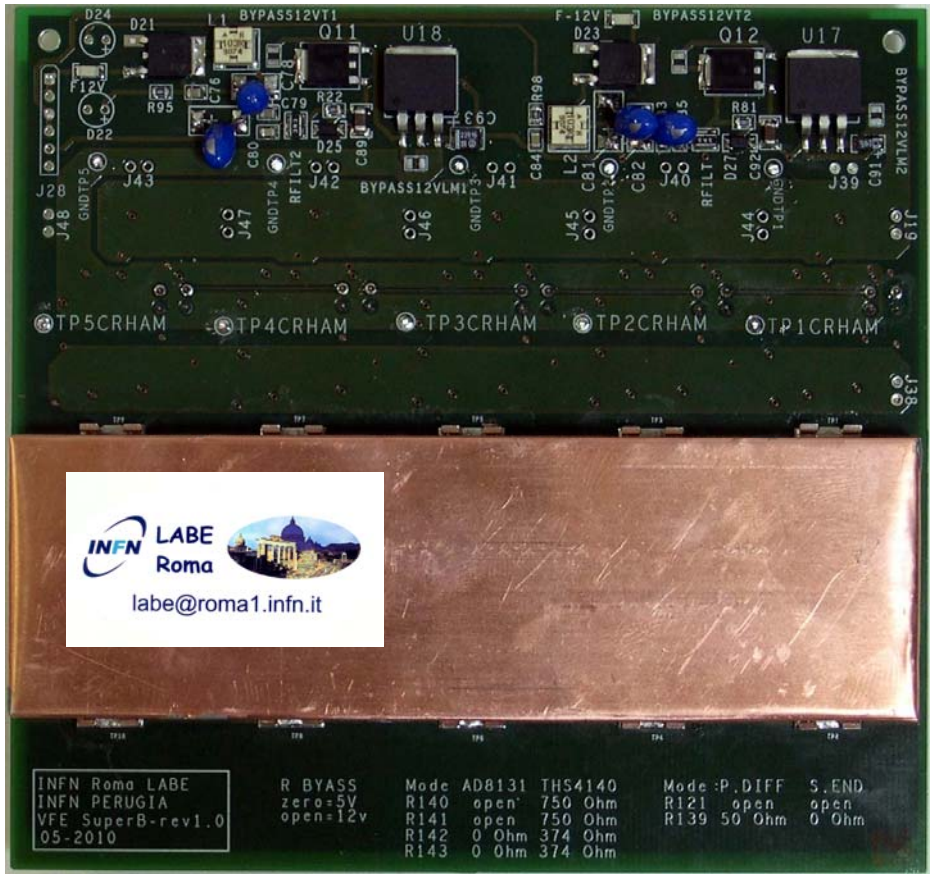
- EMC VFE Board
- 5 CSP Channels
- Enable to mount: Cremat, Hamamatsu, Home Made CSP
- HV distribution



Very Front End Board

(PCB layout D. Ruggieri, A.Papi)

- EMC VFE Board
- 4 Layers
- 5 CSP Channels
- Enable to mount:
  Cremat,Hamamatsu,Home Made CSP
- HV distribution
- Mounted on crystals
- Interface with EMC range Board

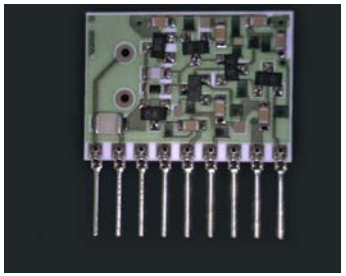


24 May 2010 in production
Estimated delivery time
for test 7 June week

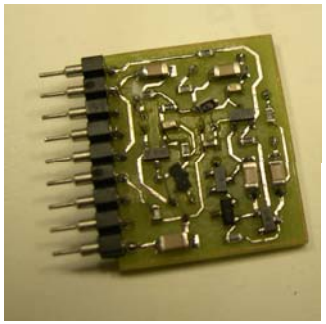
Three Type of CSP under evaluation

Cremat 1.4 V/pC

Hamamatsu 1 V/pC

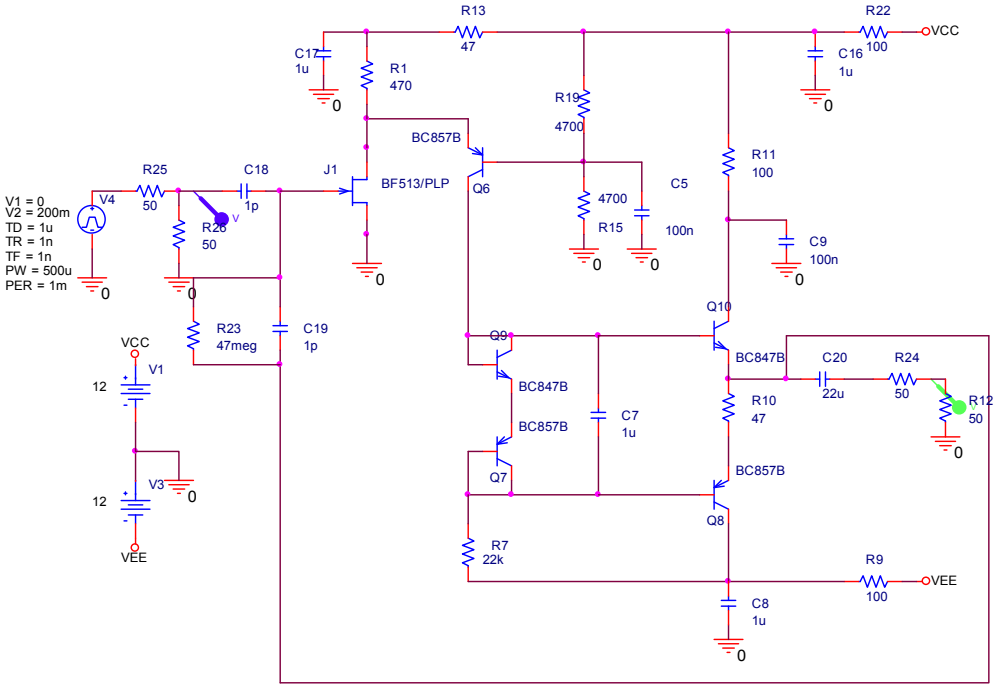


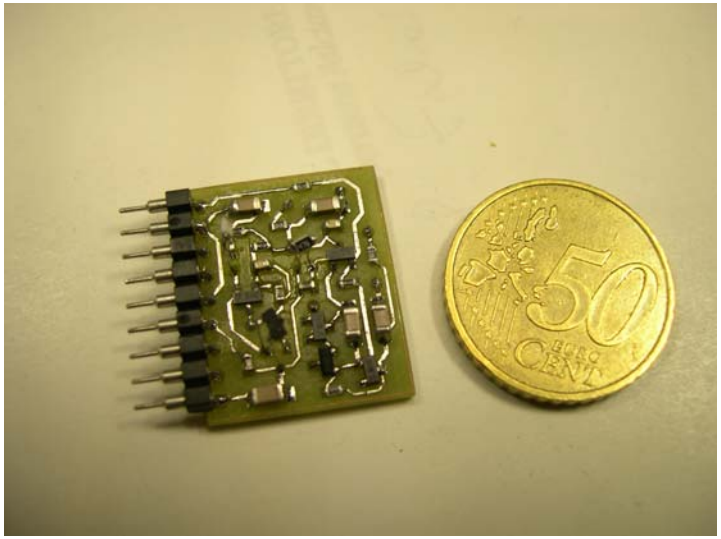
Homemade 1 V/pC



LABE Made Charge preamplifier

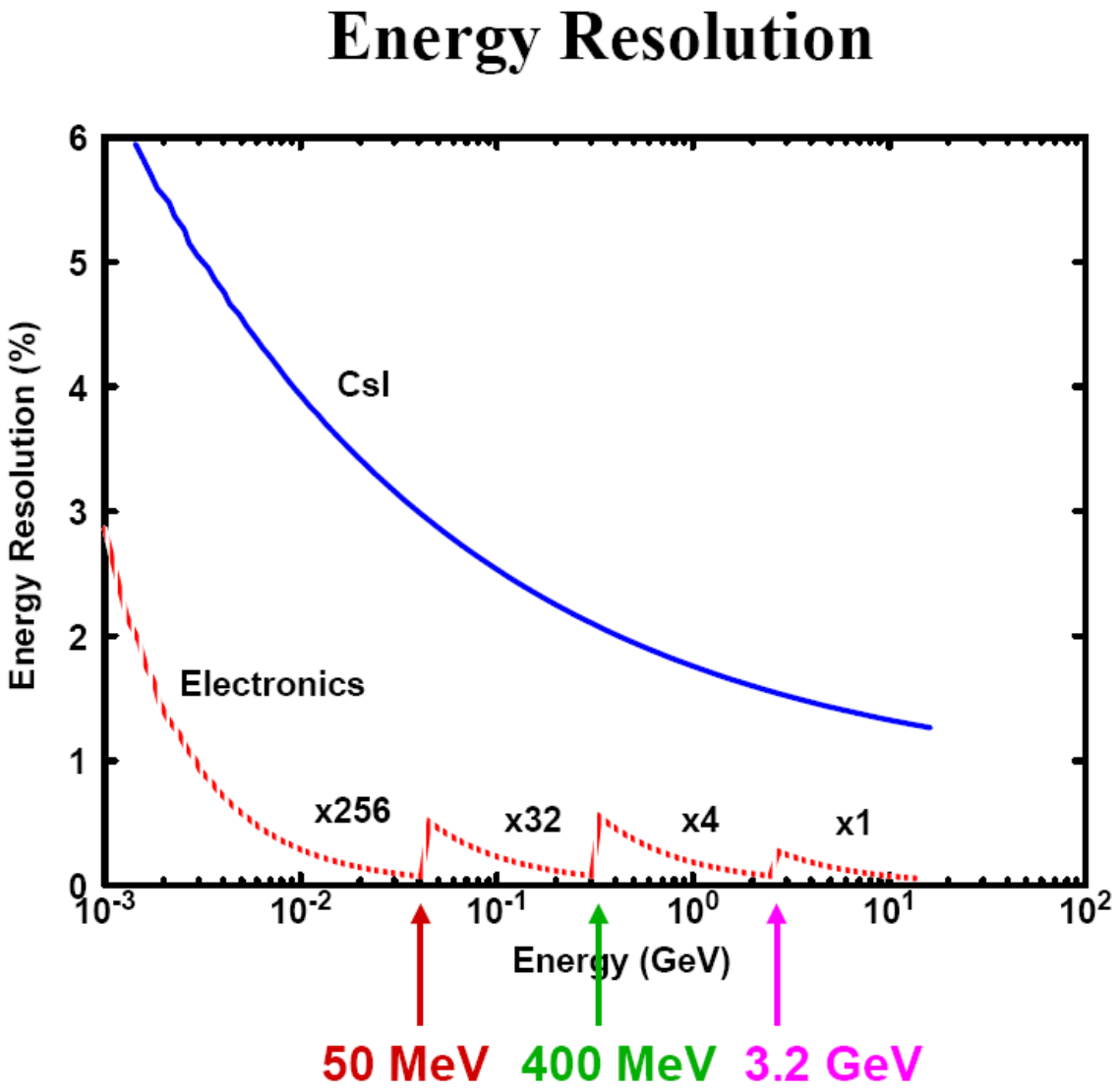
charge sensitive preamplifier in radeka configuration and push pull output



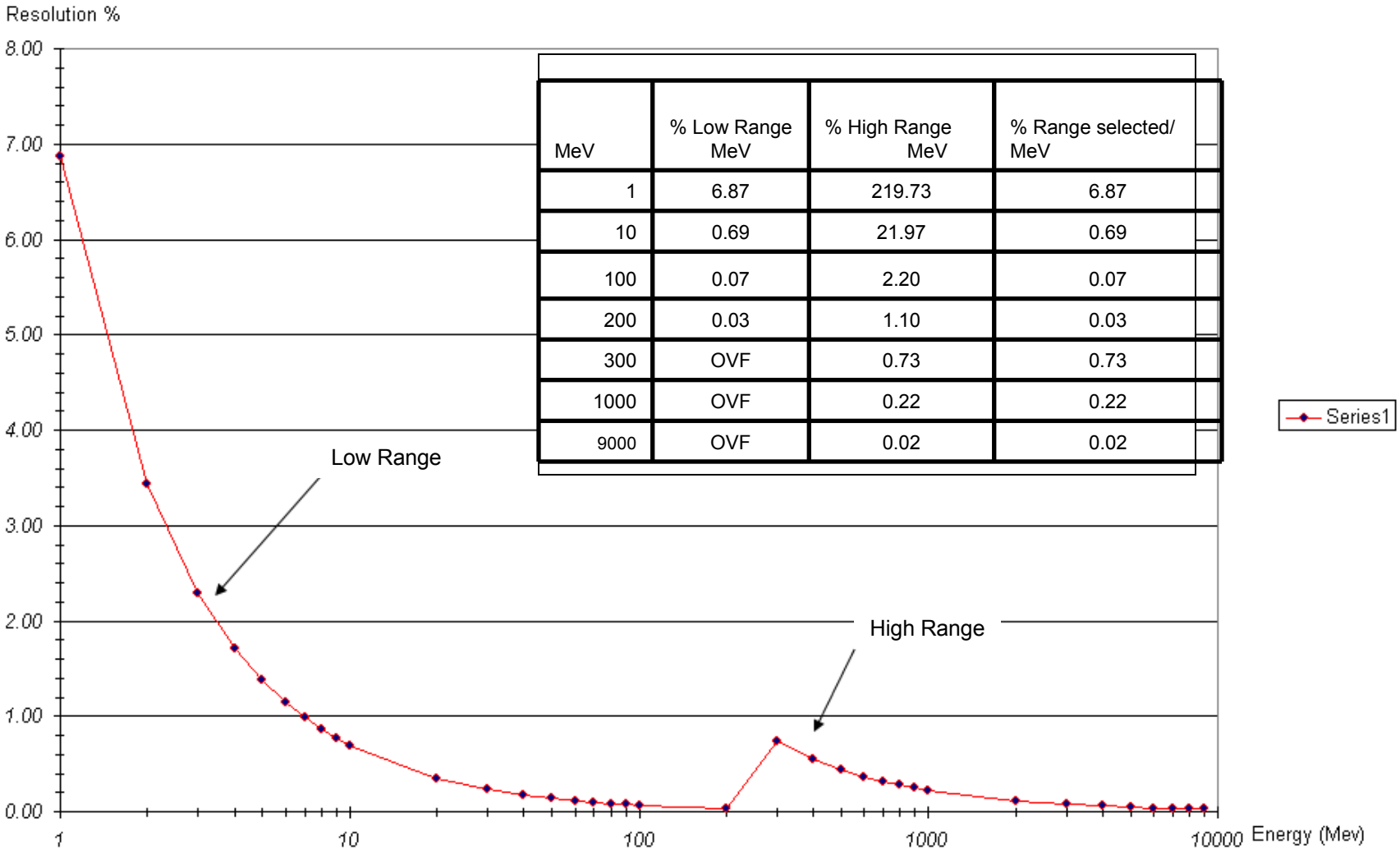


Luigi Recchia & Andrea Papi simulation and optimization.
Home made in LABE (Electronic LAboratory) in Rome.

Babar Energy resolution

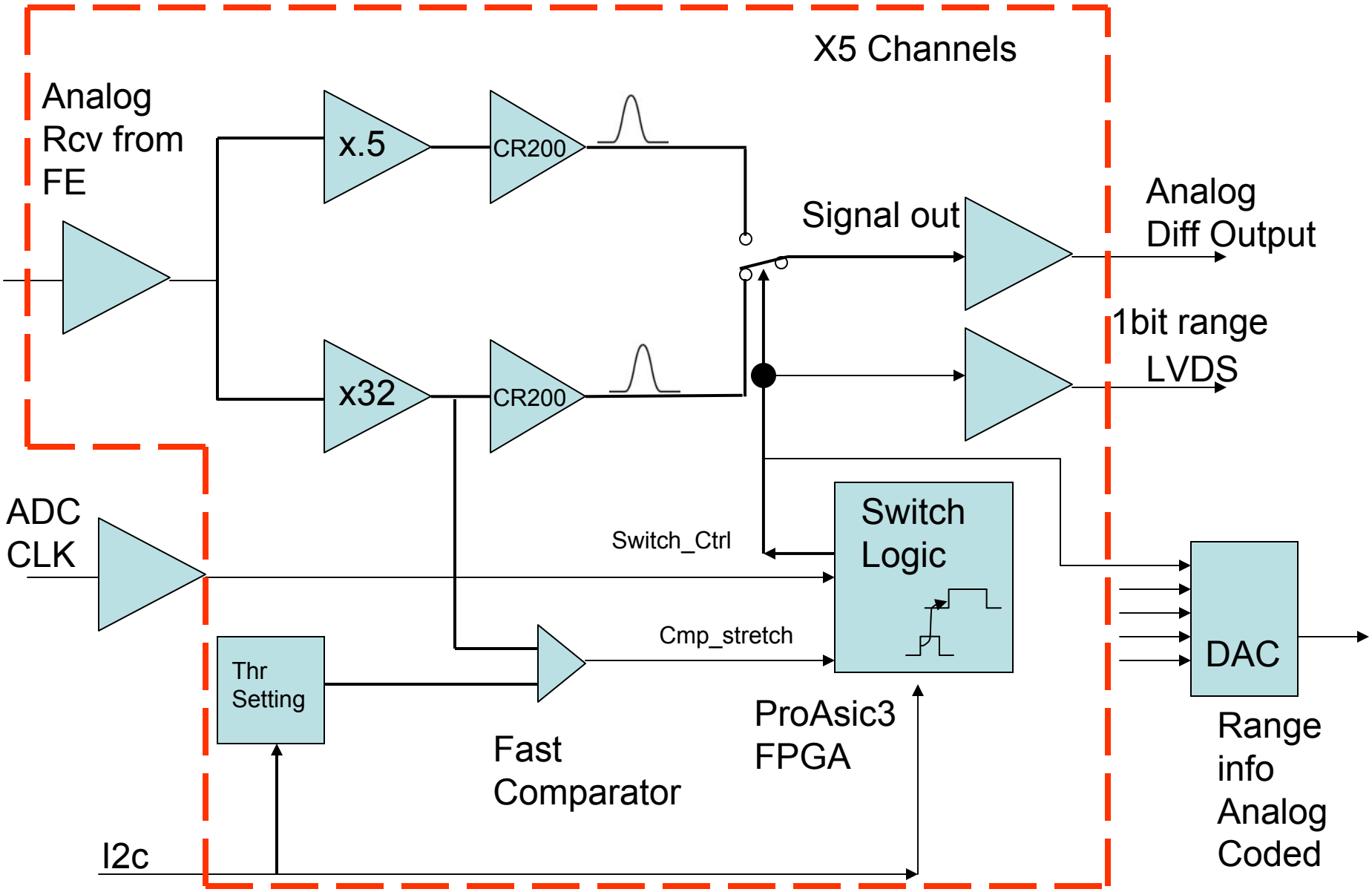


Energy Resolution SuperB



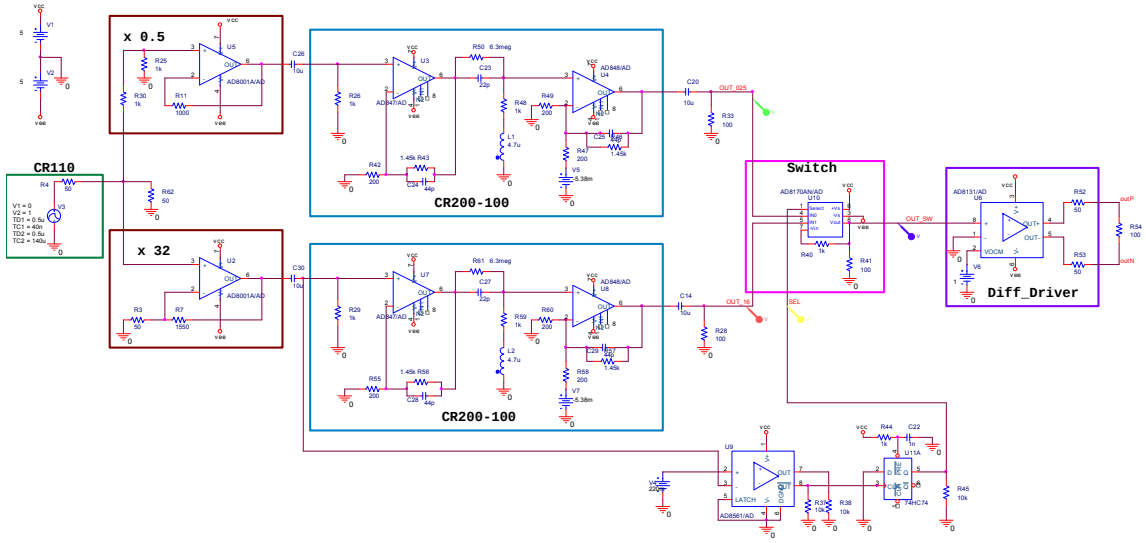
MeV	% Low Range MeV	% High Range MeV	% Range selected/ MeV
1	6.87	219.73	6.87
10	0.69	21.97	0.69
100	0.07	2.20	0.07
200	0.03	1.10	0.03
300	OVF	0.73	0.73
1000	OVF	0.22	0.22
9000	OVF	0.02	0.02

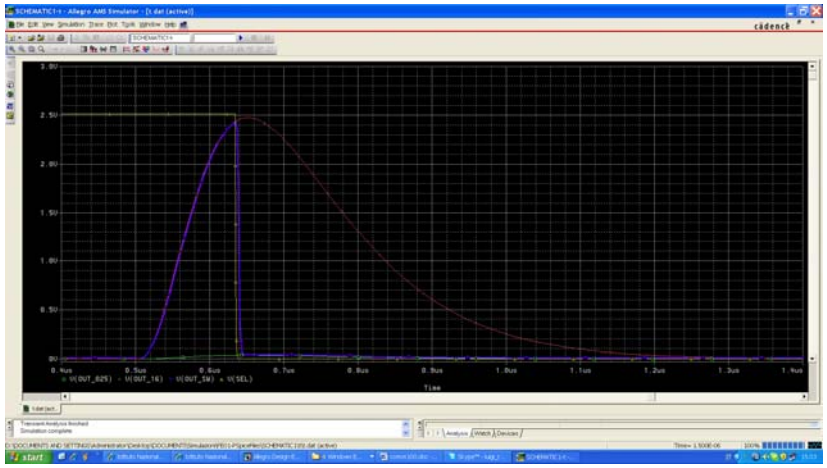
EMC Ranges shaper board



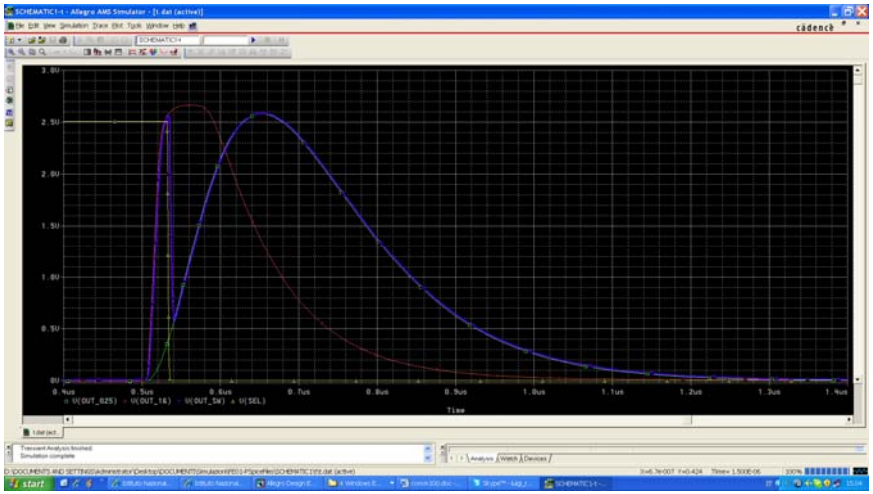
Pspice Simulation

(from Luigi Recchia)





Vin=15mV, Vth=260mV

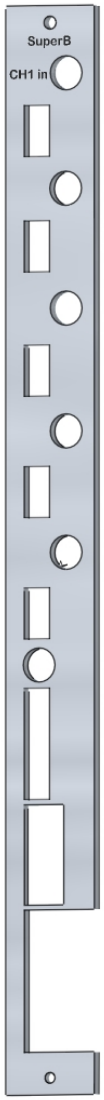


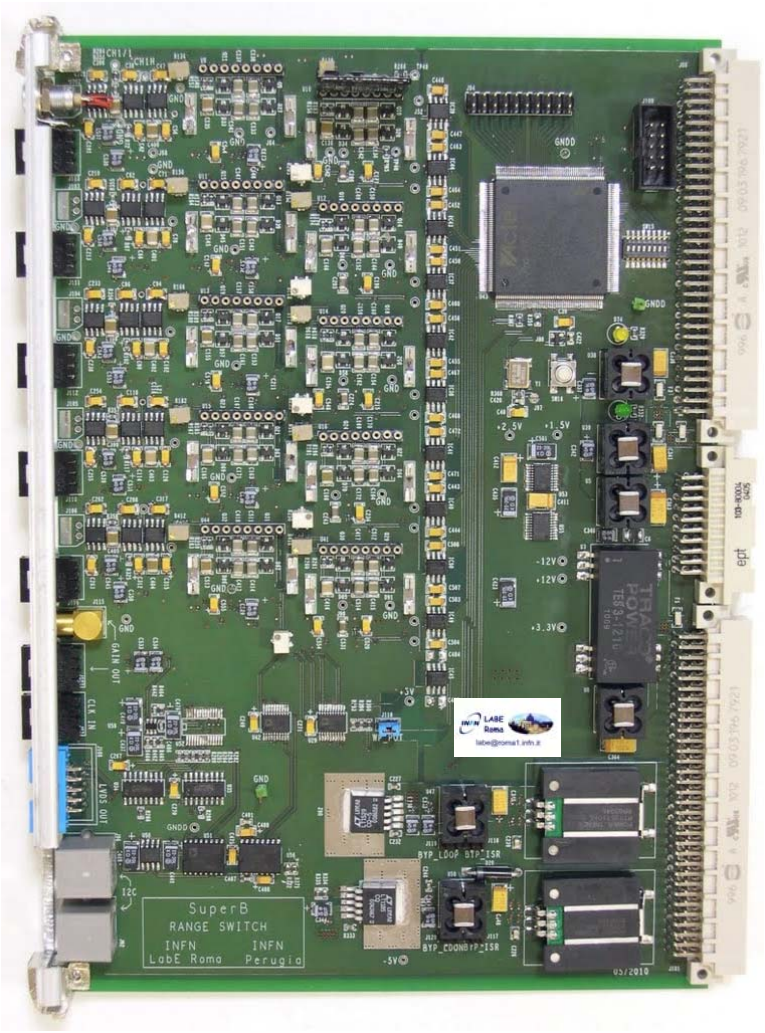
Vin=1V, Vth=260mV

EMC Range Board

(PCB layout R.Lunadei,G.Chiodi)

- EMC Range Board
- 8 Layers VME size
- 5 Channels Analog Differential input
- 5 Channles Analog Differential output
- 1 Main clock input
- Long line I2c control input
- Range info analog coded
- Lvds output for Range bit

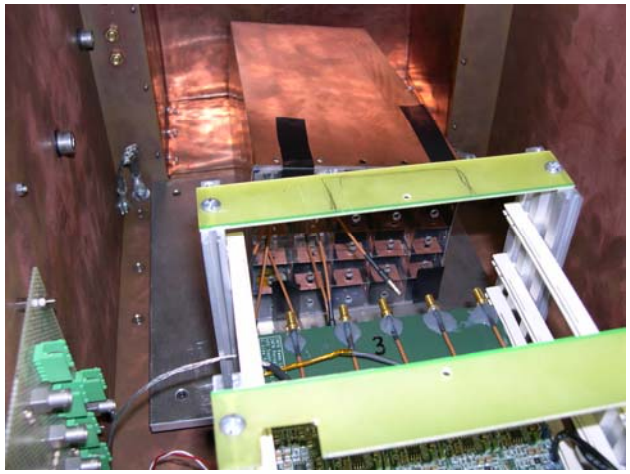


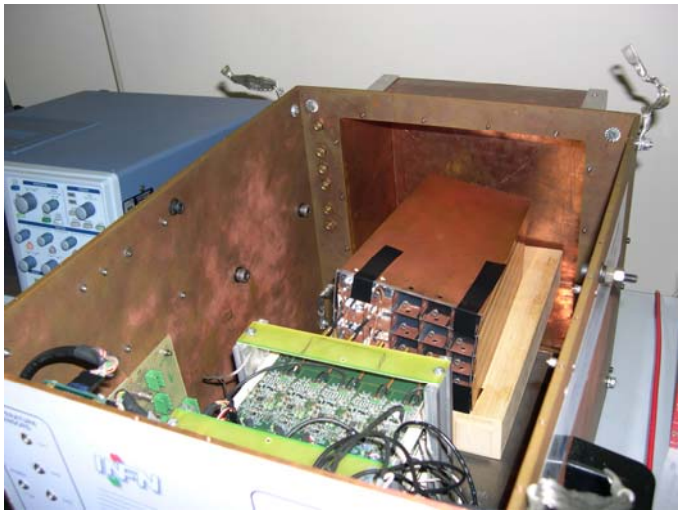


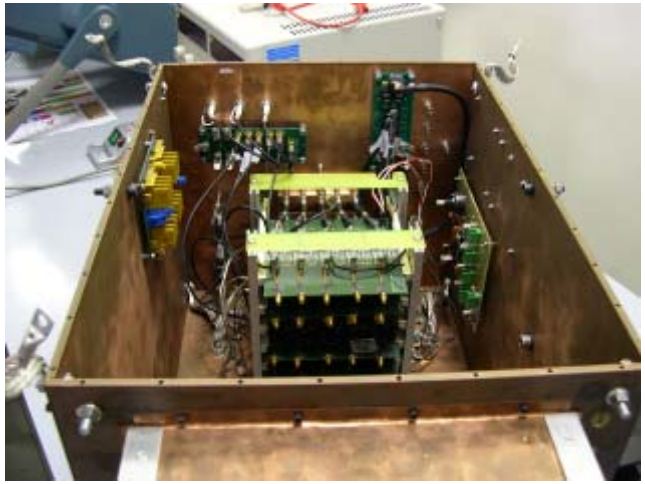
24 May 2010 in production
Estimated delivery time
for test 14 June week.

VFE inside the copper Box

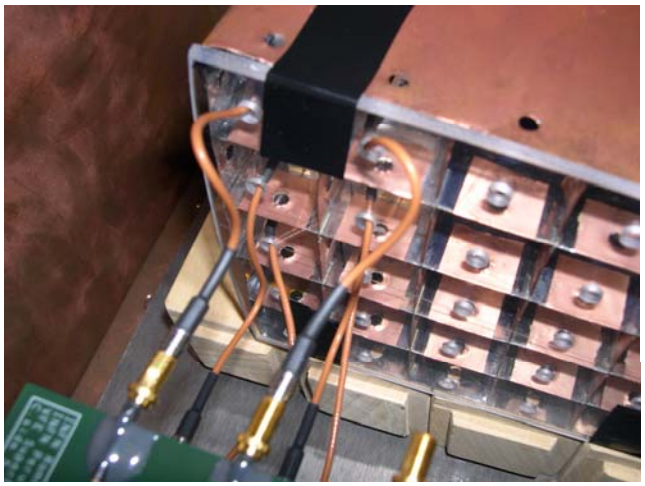
(INFN Perugia,INFN Roma)



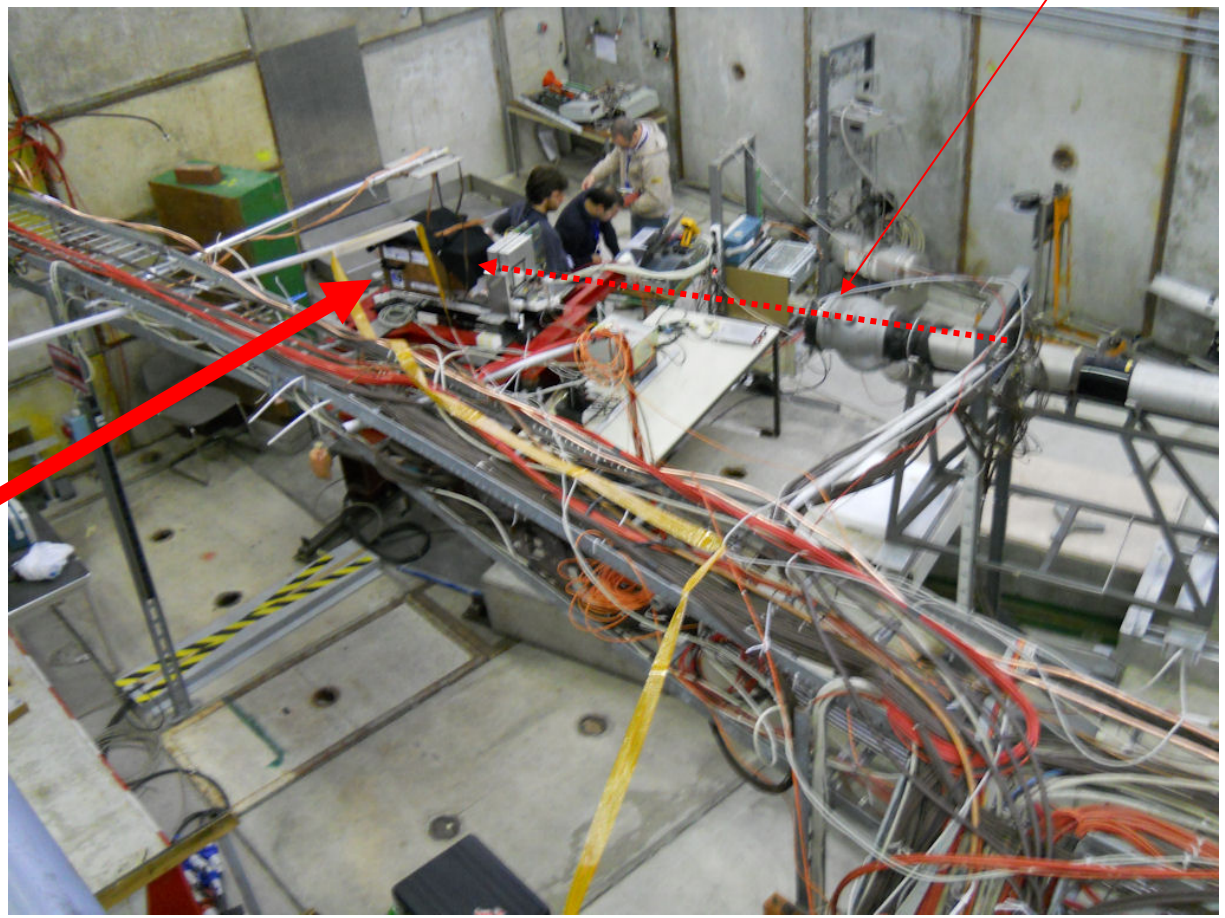




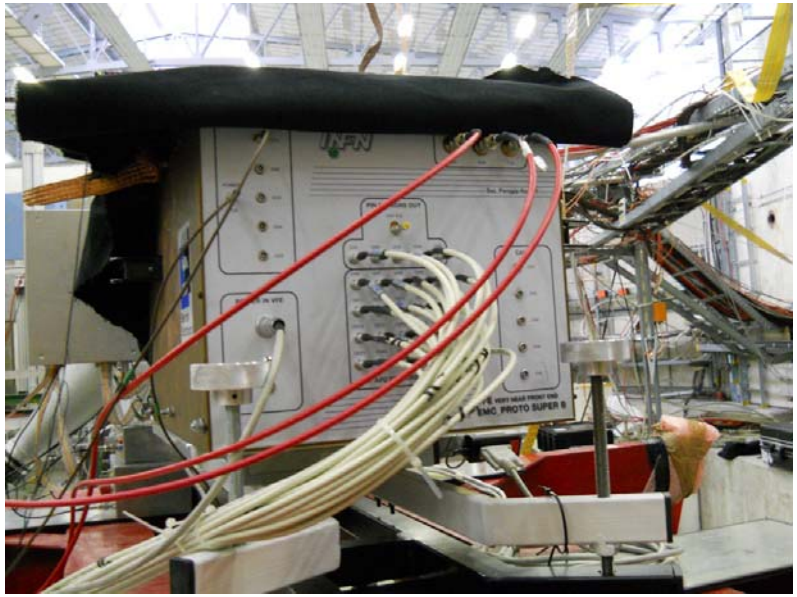
Cabling by M.Bizzarri



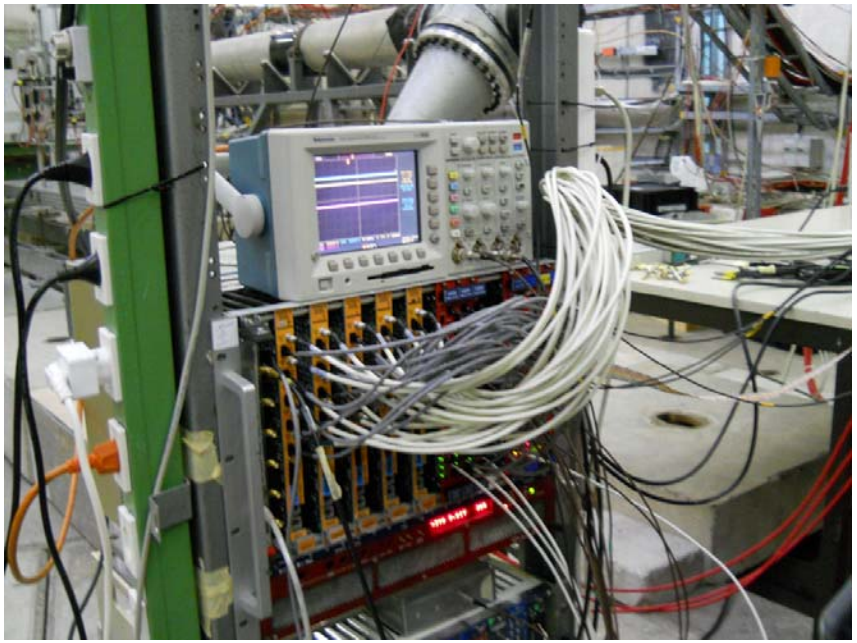
CERN test Beam 1/2



CERN test beam 2/2



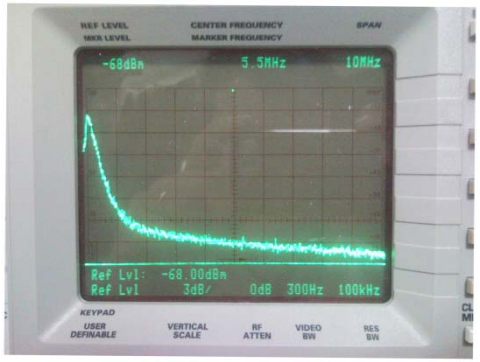
Front End Box



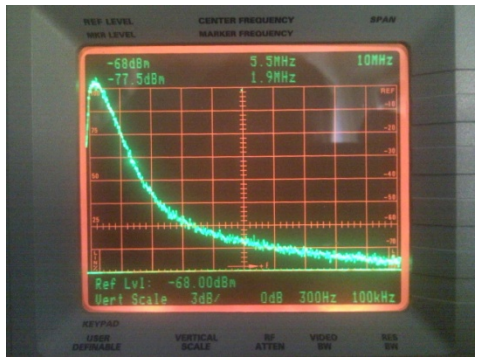
Shaper switch Boards

As we know the noise spectrum depends from the shaping time we do not find any noise source with an heavy contribution.

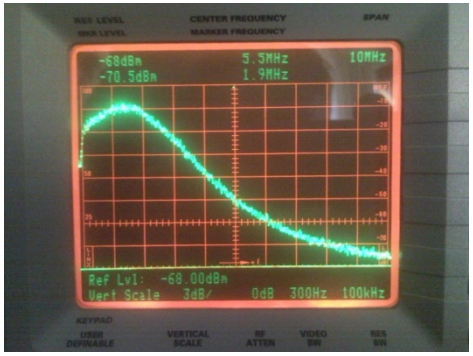
Power Spectrum 500 ns Shaper

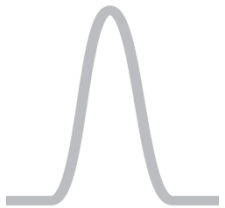


Power Spectrum 250 ns Shaper



Power Spectrum 100 ns Shaper





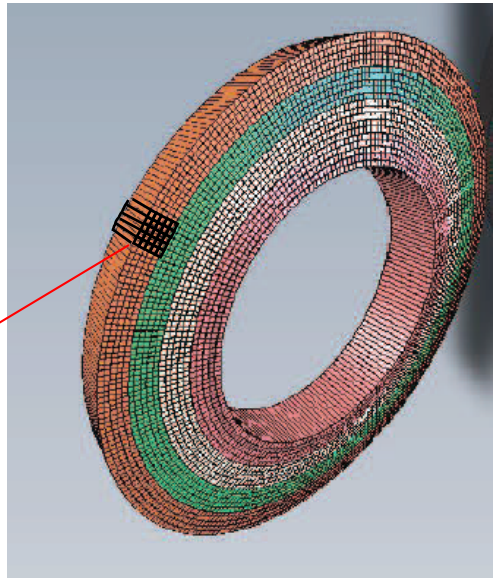
More noise

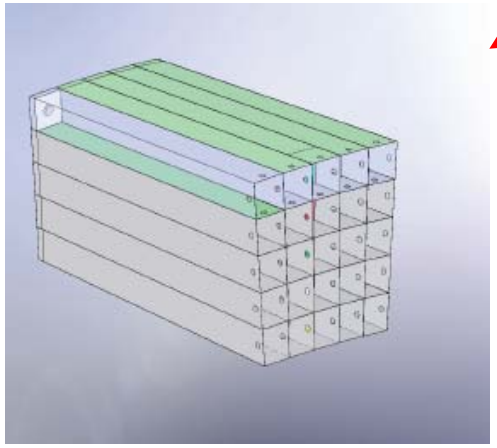
We integrate the noise spectrum and we have evaluated the noise level in Veff

- **100ns -> 745 uVeff**(0.5-10.5 MHz)
- **200 ns -> 565 uVeff** (0.5-3.5 MHz)
- **500 ns -> 418 uVeff (0.1-2.1 MHz**)

1 Mev 600 uv High Gain during CERN test Beam
1 Mev 180 uv Low Gain during CERN test Beam

EMC Forward Trigger Primitives

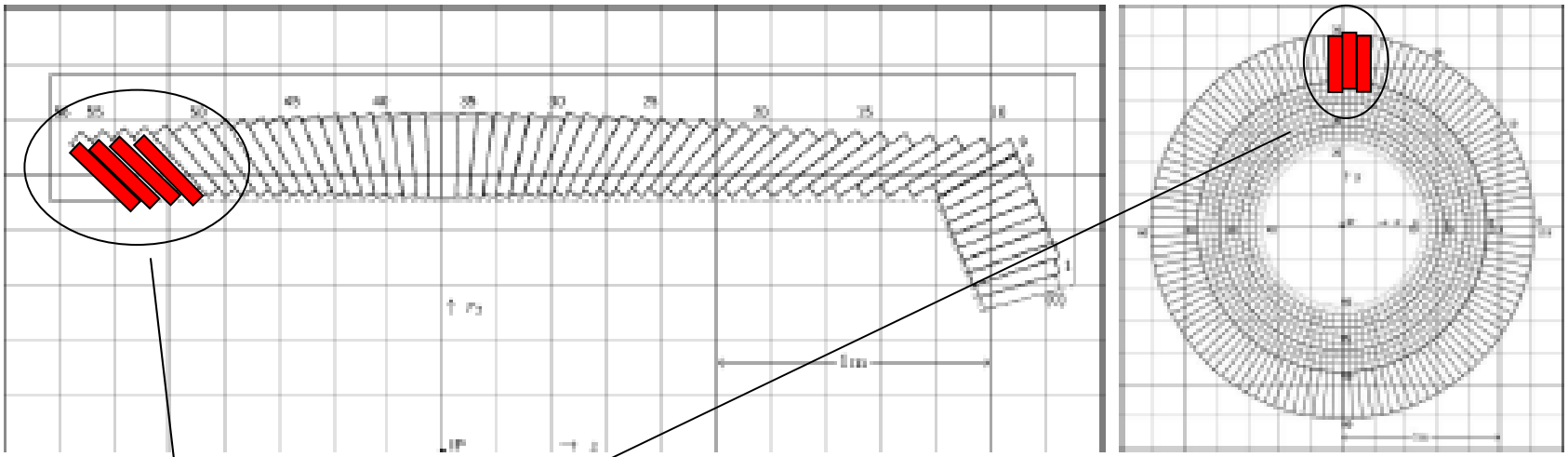


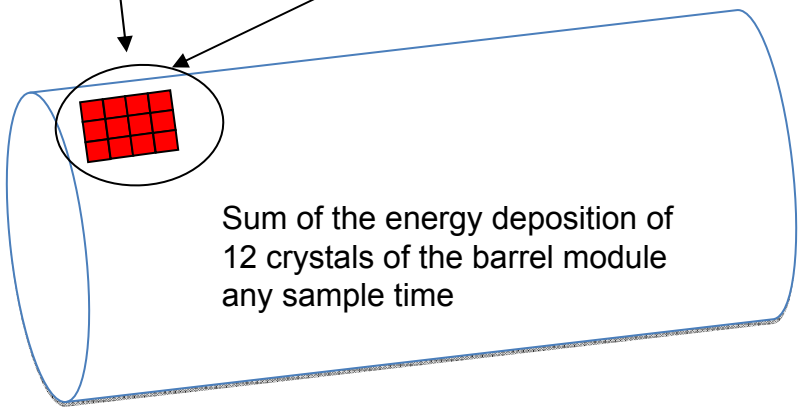


Sum of the energy deposition of the 25 crystals of each Forward module.

- **SuperB EMC Forward = 4400 Lyso Crystals**
- **176 Sums unit**

EMC Barrel Trigger Primitives





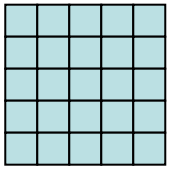
- **EMC Barrel :5760 CsI(Tl) Crystals**
- **480 Sums unit**

EMC Fast Trigger Path and Slow Energy Path

Forward

$N_{cryst} = 25$

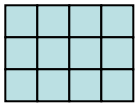
$N_{Towers} = 176$

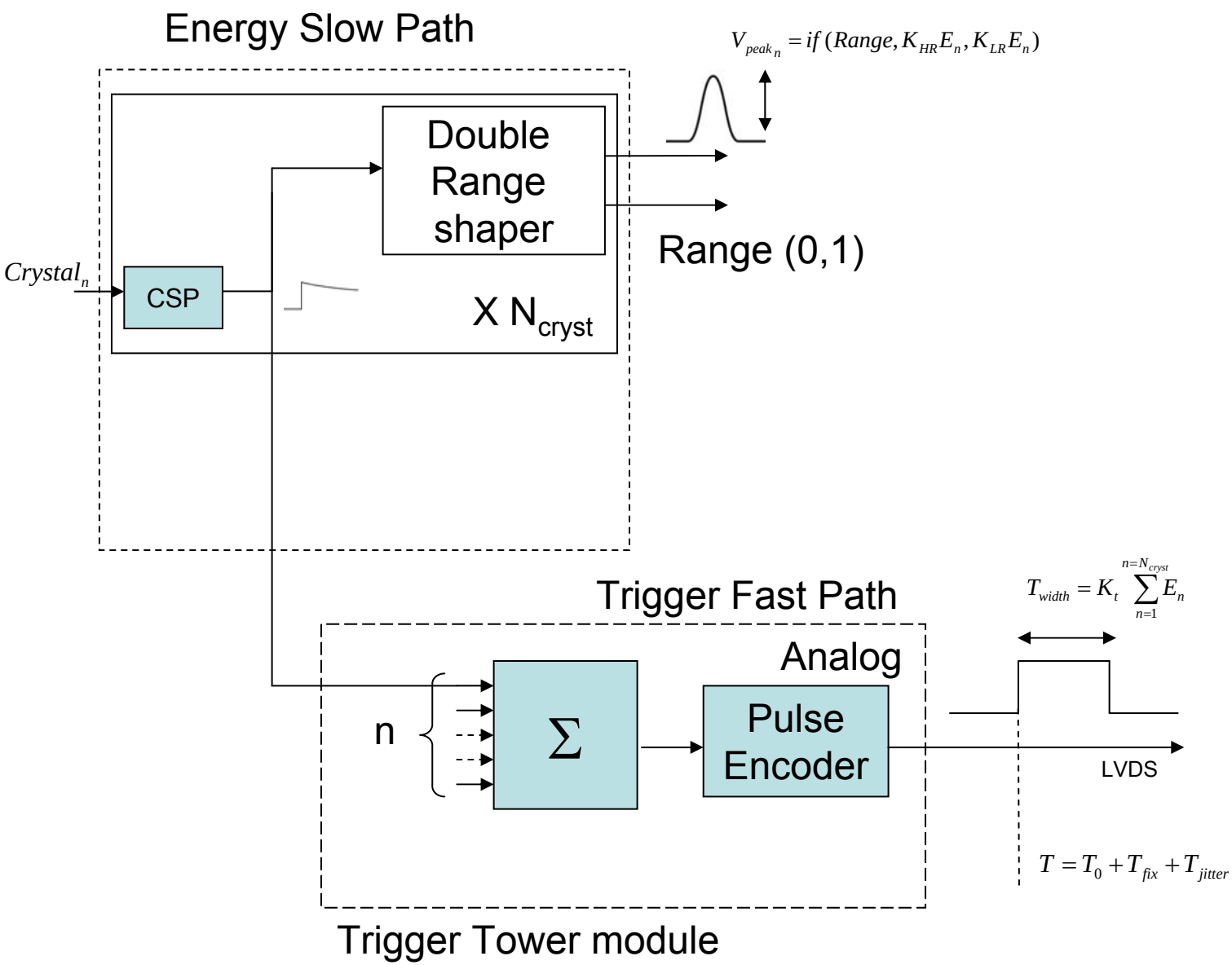


Barrel

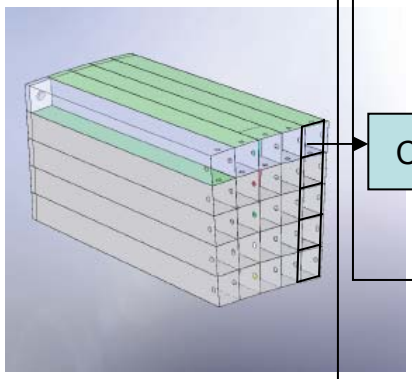
$N_{cryst} = 12$

$N_{Towers} = 480$





EMC Forward tentative of Implementation



5 x 5 =25 crystal tower

CSP

X5

5 input

Σ

VFE

X5

Double Range shaper

X5

Range

VME Range Shaper

New Circuit Analog Sum over 5 input.

5 input

Σ

Analog Pulse Encoder

LVDS

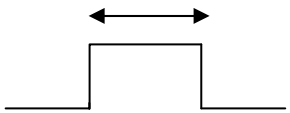
$T = T_0 + T_{fix} + T_{jitter}$

Trigger Tower module

X 176 lvds Links

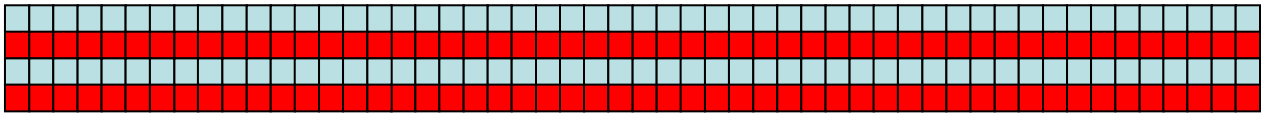
EMC Trigger Processor

$$T_{width} = K_t \sum_{n=1}^{n=N_{cryst}} E_n$$



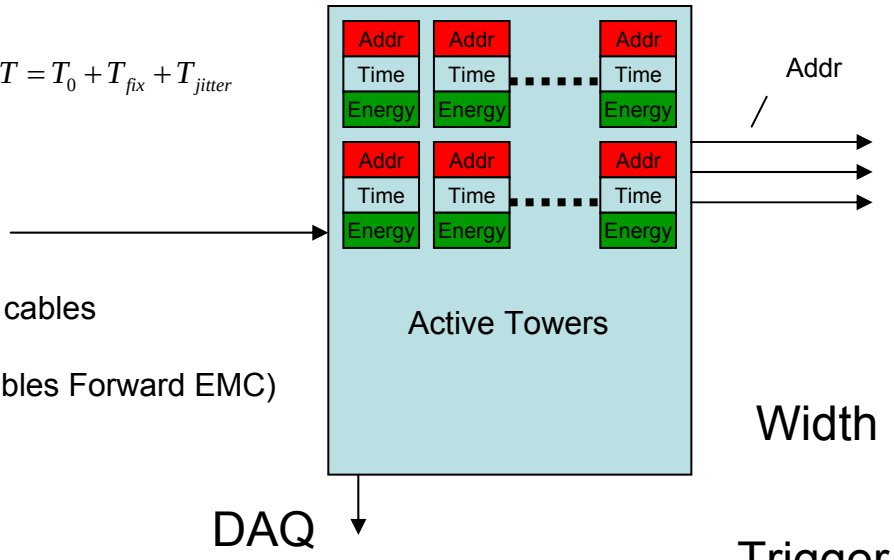
LVDS

$$T = T_0 + T_{fix} + T_{jitter}$$



44x4=176 tower

TP0_EMC



N_{tower} LVDS cables

(176 Lvds cables Forward EMC)

Width

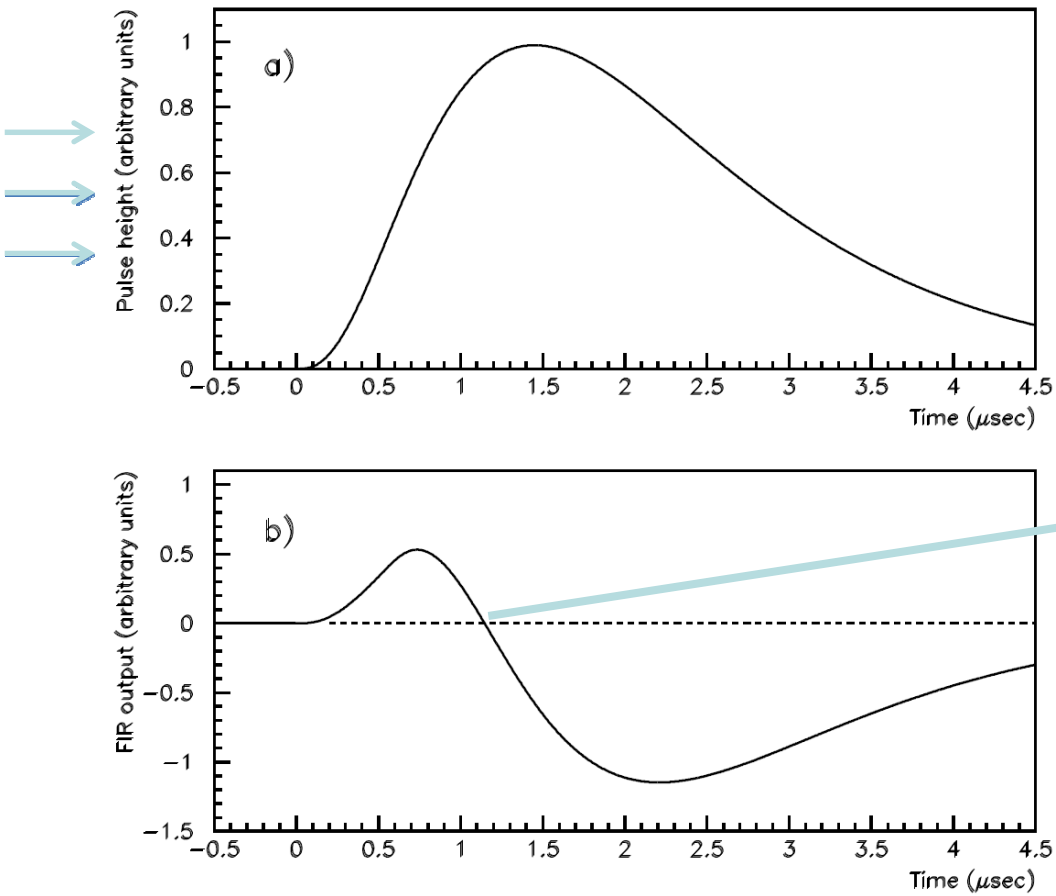
DAQ

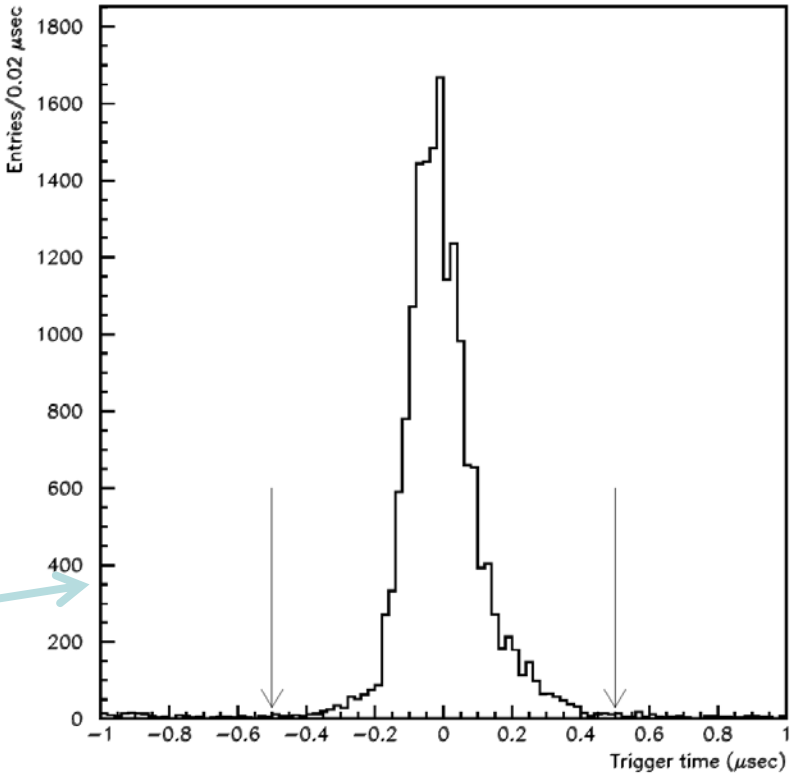
Trigger processor level0
Cluser Information extracted

- Addr of each tower
- Extract Energy for each tower (width measurement)
- Extract T for each Tower

Trigger timing in the BaBarBarrel CsI (Tl doped)

P. D. Dauncey et Al., “Design and performance of the level 1 calorimeter trigger for the BABAR detector” (2001)



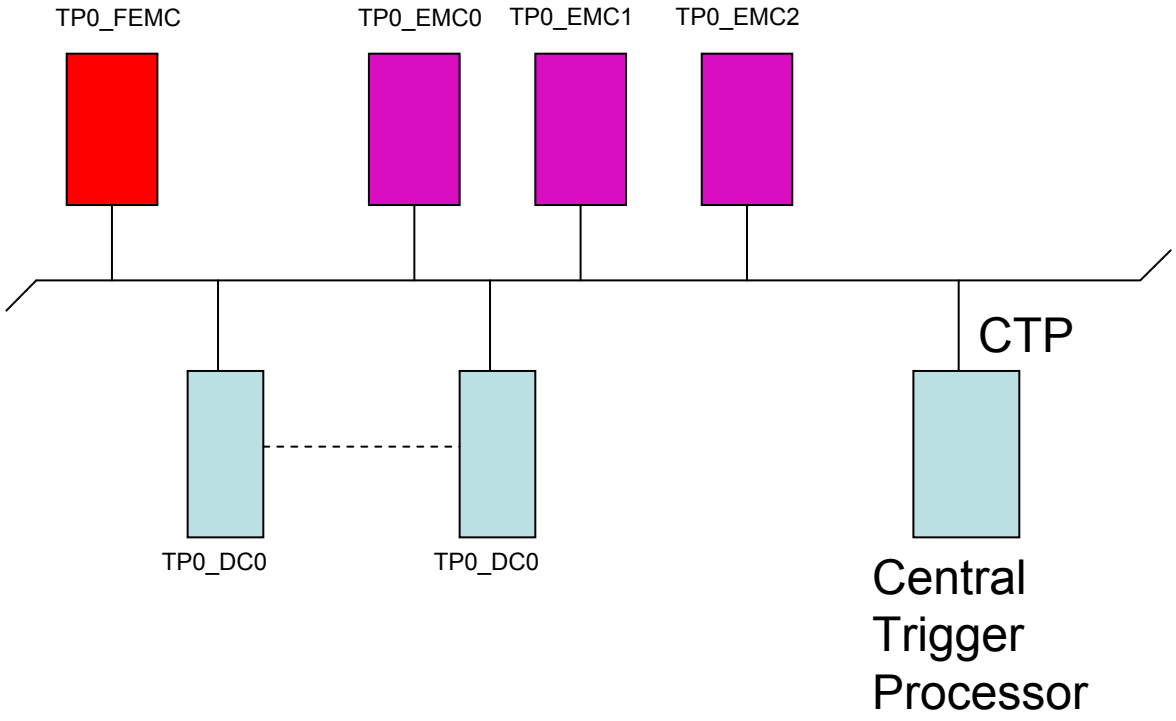


The plot shows the difference between the EMC trigger time and the DC trigger time.

A FIR Filter with 8 parameters was applied to the signal. Its zero crossing occurred at roughly a fixed time distance from the start of the signal, it was used to gate the threshold information. Due to this mechanism the time resolution was about **100 ns**.

Antonio Budano

Trigger Crate



The central trigger processor get the informations from the TP0 units and create the trigger.
The edge of DC chamber has the same addr structure of the EMC.

Electronics Plan

- L'elettronica del calorimetro forward dipende fortemente dal tipo di calorimetro scelto. Tale elettronica supporterà i vari test beam in preparazione.
- Dopo l'approvazione di SuperB l'elettronica del del barrel può iniziare con uno sviluppo serio dato che nel Barrel abbiamo più punti fissi.
- Abbiamo iniziato una collaborazione con le sezioni di Roma3, Napoli, LNF e Perugia, for Central trigger design.

Spare

XV Super*B* General Meeting
Caltech
December 14-17, 2010

Electronics Plan

- The electronics of the Forward follows the discussions of the detector and try to support the test beams. It is not fixed and strongly depends of the detector type.
- After the SuperB approval we have to follow better the electronics of the Barrel where we have more fixed points.
- We startup a collaboration with Roma3,Naples,LNF, Perugia, for Central trigger design.

Reminder of a few system parameters as of today

The maximum trigger rate is 150 kHz, with a latency of 6µs.

Dead-time <1% => minimum trigger spacing < 70 ns.

The estimated event size at the FE is 500 kB.

We set the aggregate input rate for one ROM to 10 Gb/s.

Number of FEE 1.8Gb/s data links : 325

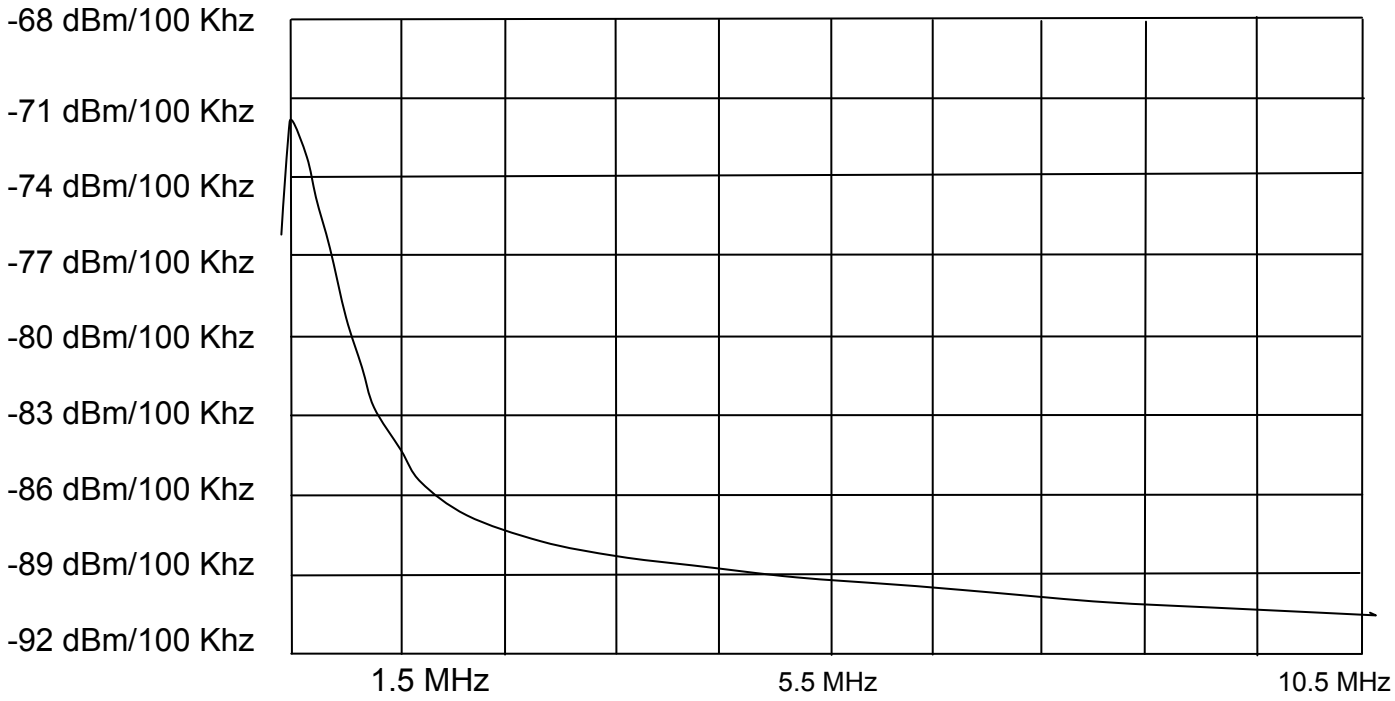
With these assumptions the number of ROMs needed to manage the SuperB data flux can be estimated to be of the order of:

$(8. \times 500. \times 10^3) \times (150. \times 10^3)/(10. \times 10^9) =$

60 boards

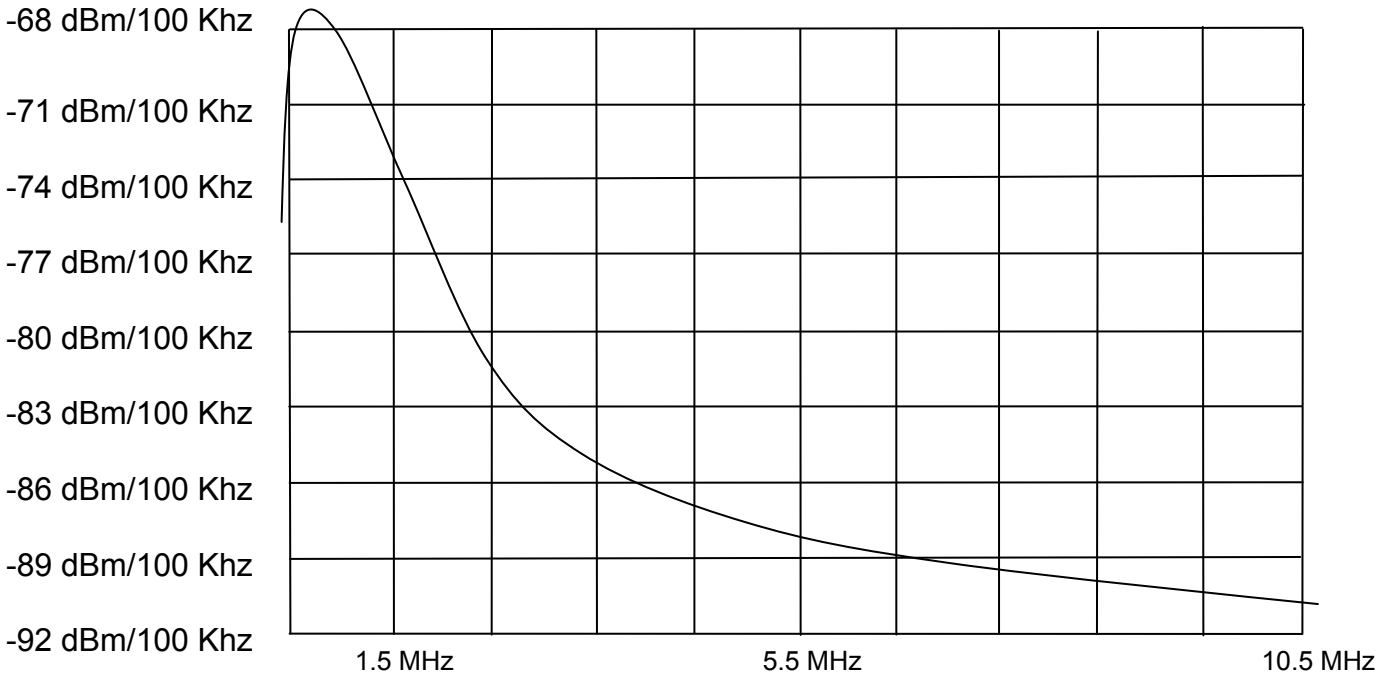
Each ROM will handle 10 kB of fragment size at 150 kHz.

Power Spectrum 500 ns Shaper

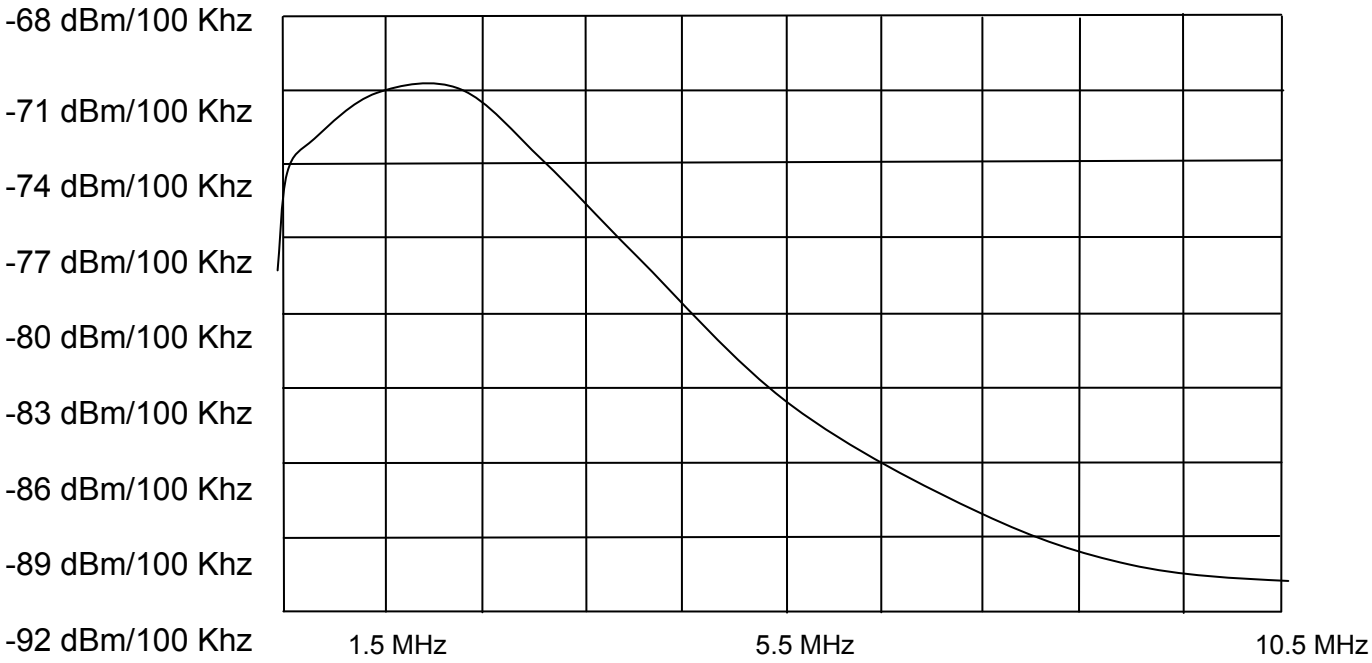


This is the shaping time used in LNF beam test

Power Spectrum 200 ns Shaper



Power Spectrum 100 ns Shaper



This is the shaping time used during the CERN test beam