Advanced sensors and electronics characterisation

Challenges of HEP for tracking and vertexing in extreme conditions of particles rates and radiation

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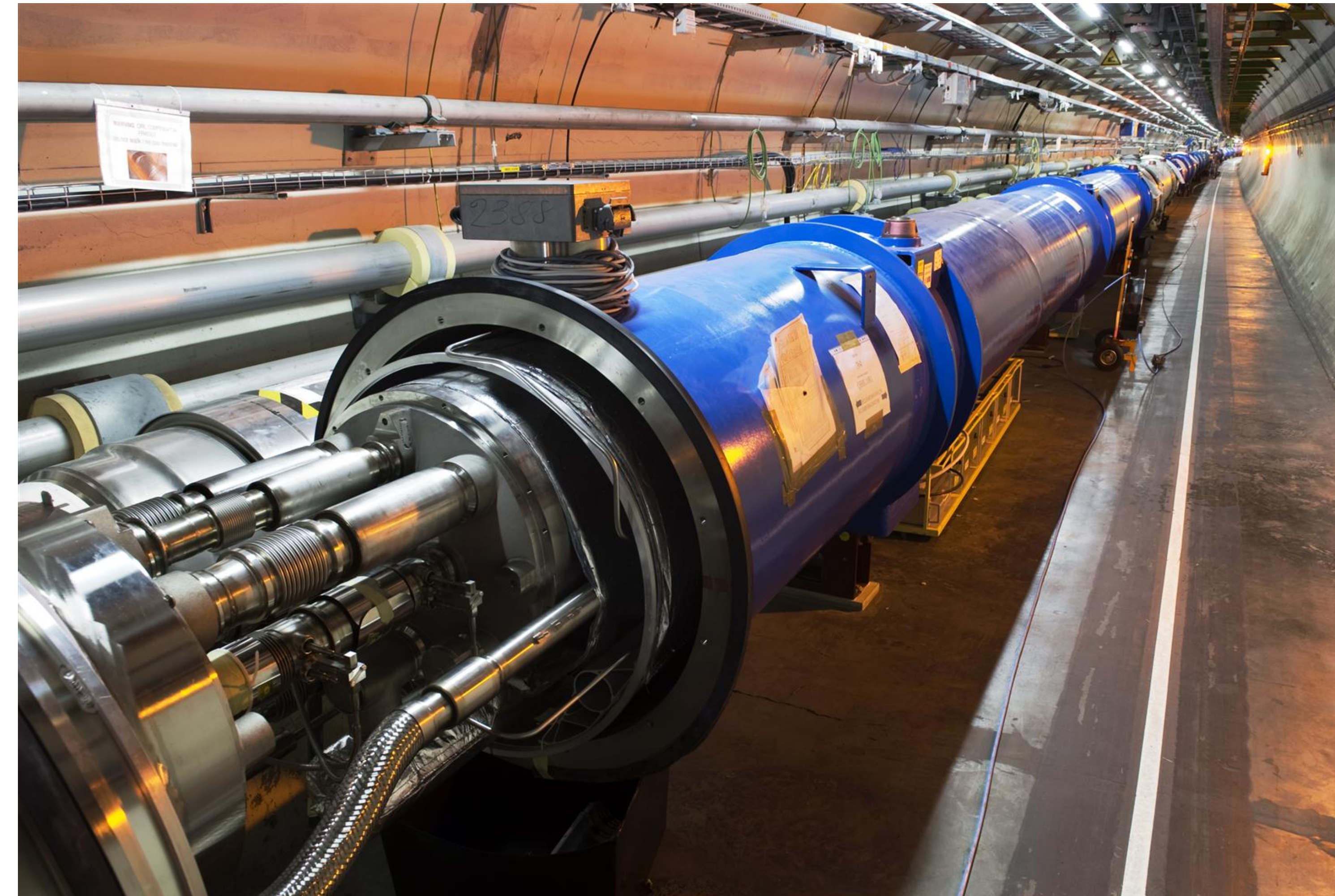
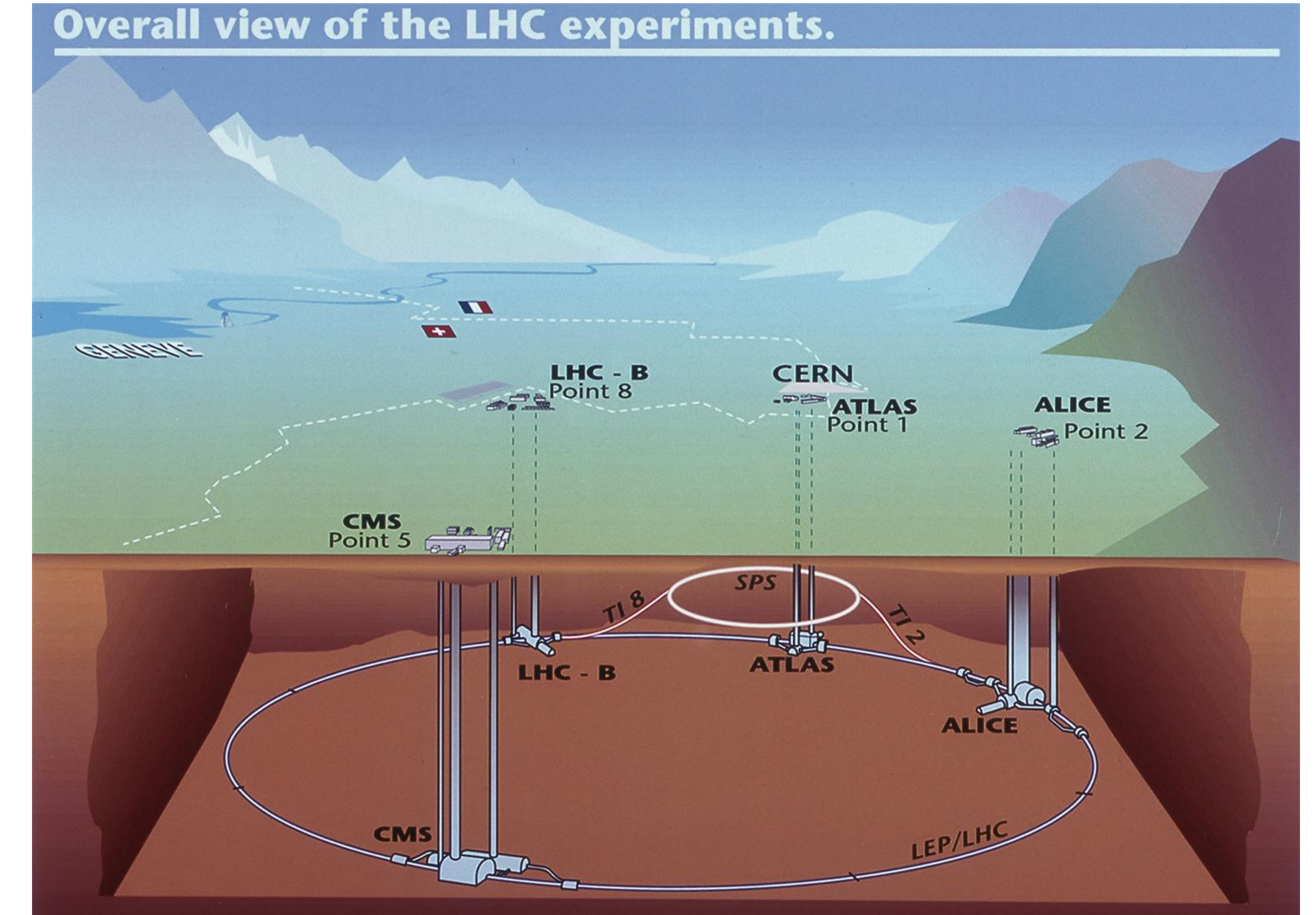
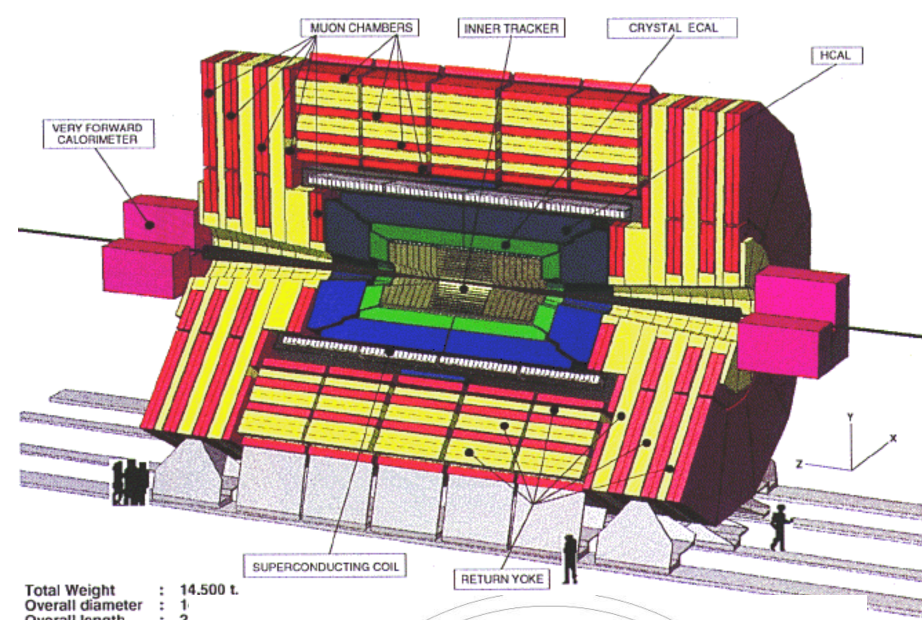
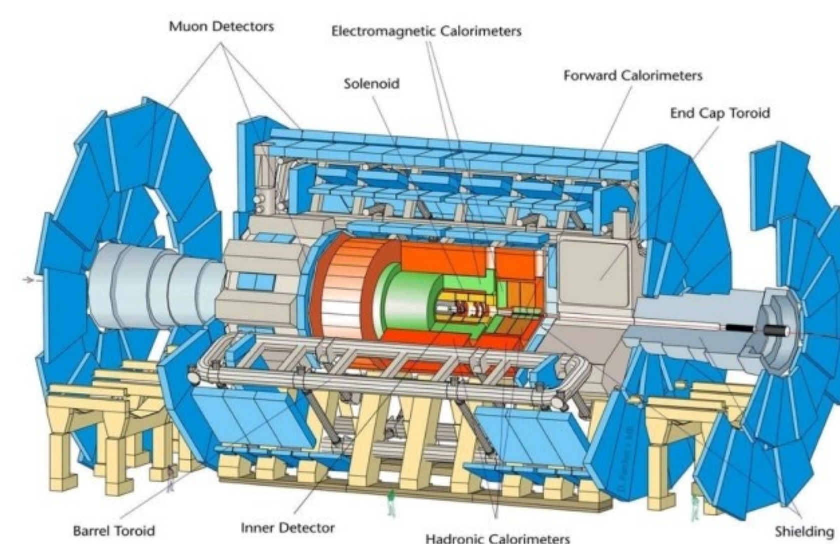
- **Context & Principles :** challenges and goals achieved
- **Lab part-1 :** front-end ectronics testing / characterization with probe-station
- **Lab part-2 :** pixel module verification using an X-ray machine

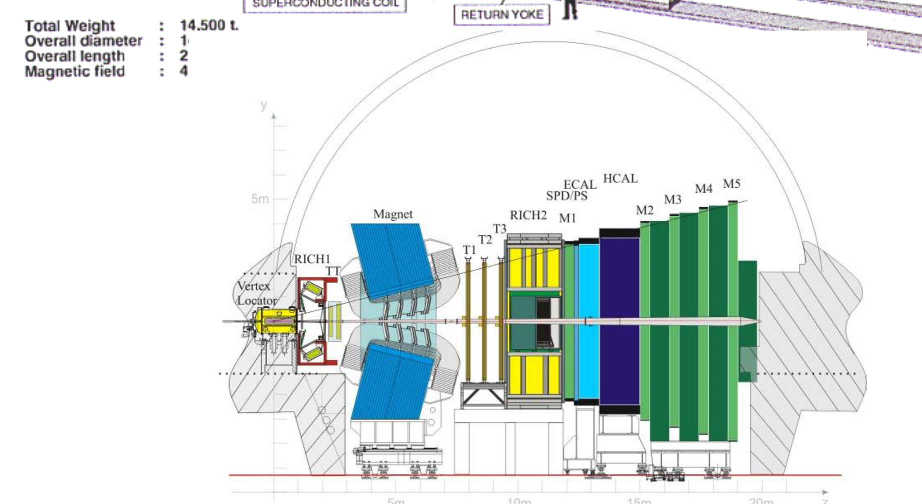
LHC program

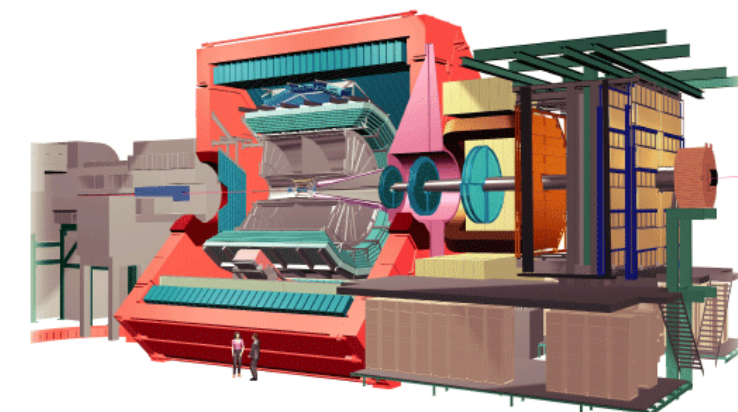












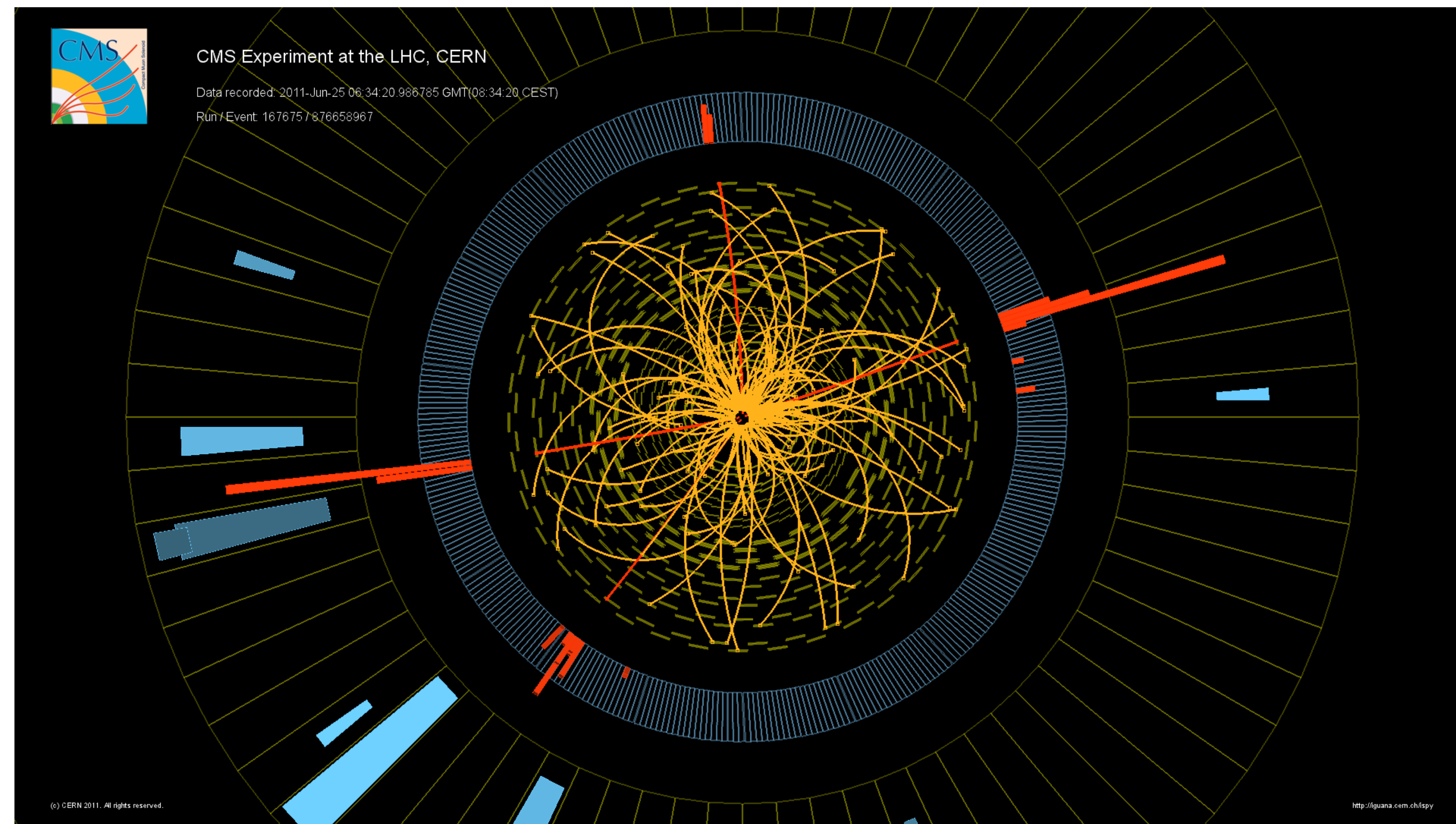
- Biggest and powerful particle accelerator in the world
  - pp collider - 26 Km of length
  - 13 TeV energy

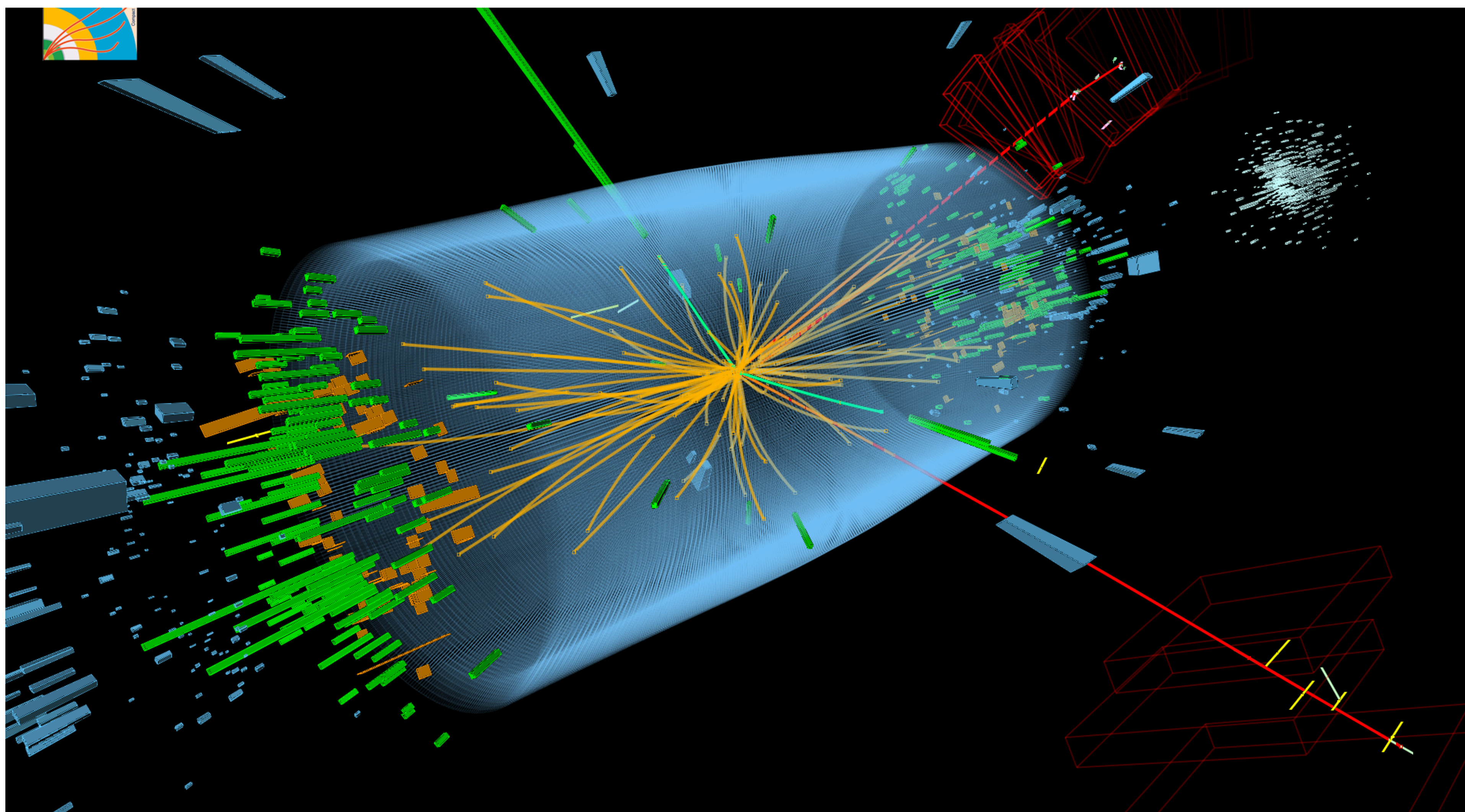
- Large amount of particle collisions
  - 2376 bunches each made of 10^{11} protons at light velocity
  - 25 collisions every 25ns

- Four large experiments to study particle physics,
  - two for new particles, new phenomena
  - one b-particle physics
  - one specialised on ion-ion collisions (qqg plasma)

LHC Upgrade to HL_LHC

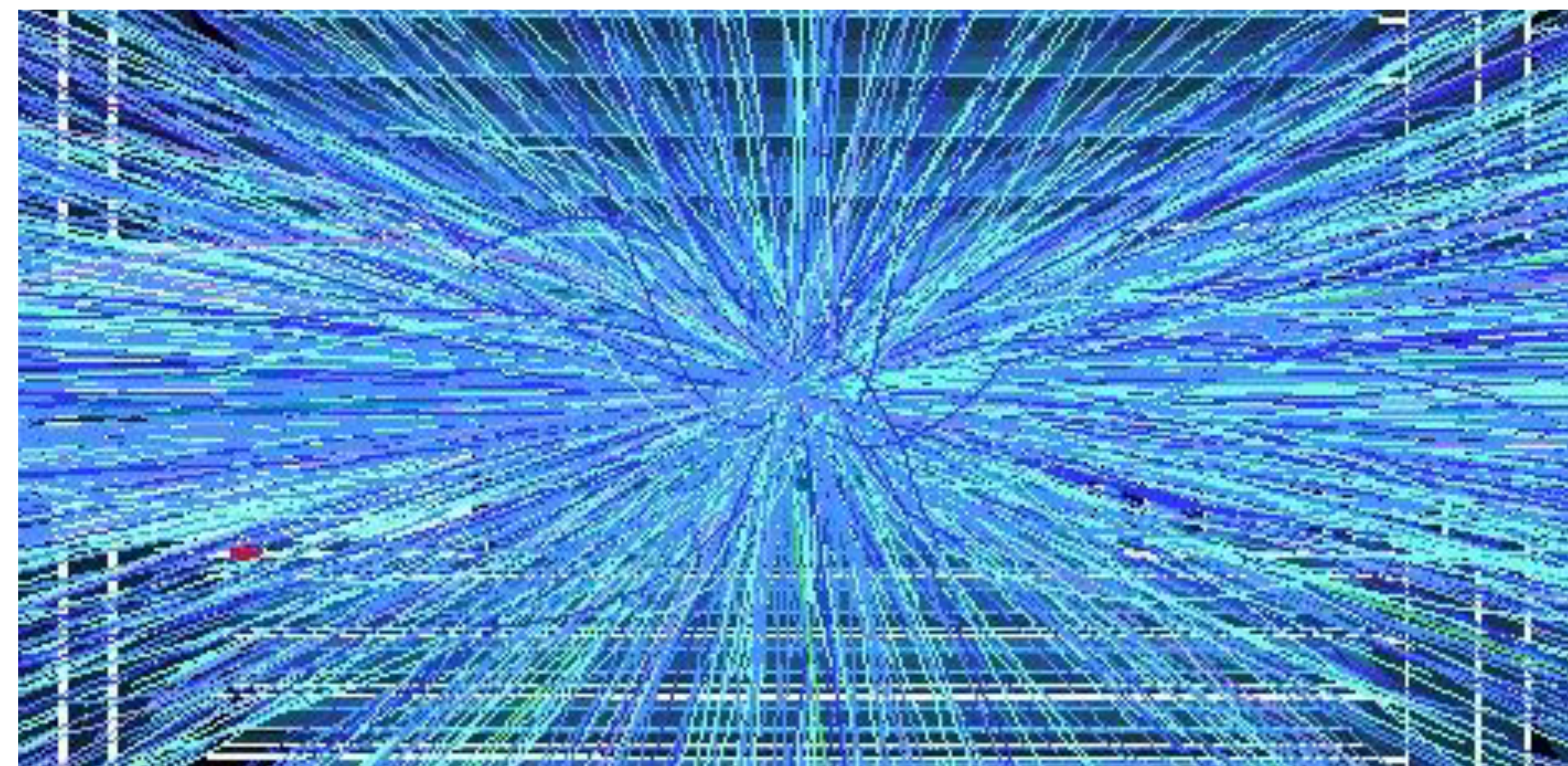
NOW @ LHC





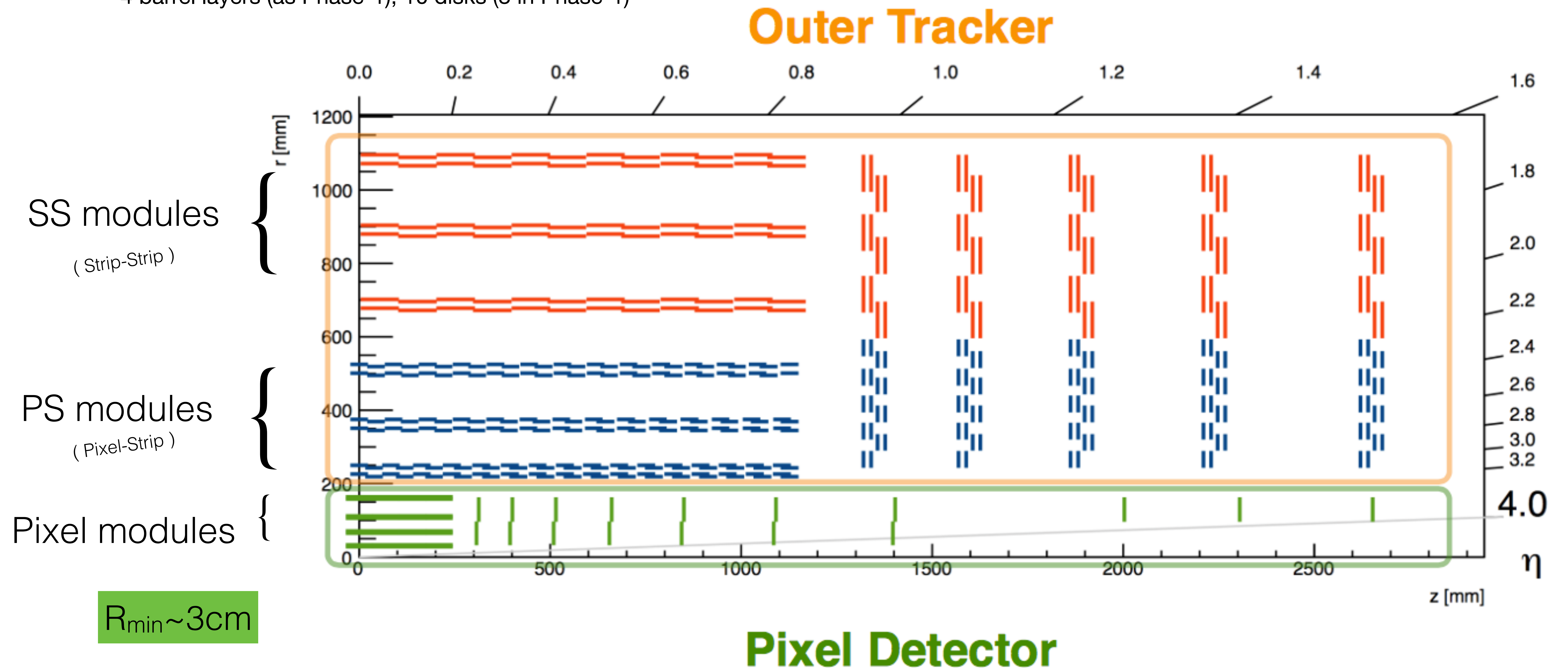
After year 2028

- HL_LHC accelerator: new frontier for particle physics
  - pp-collisions at >3 times LHC; 200 pp collisions at the same time !
  - Experiments: taking data at higher L1-Trigger rate
  - Read-out data increase > **x3** particles, **x7** trigger
  - ALL THIS to make precision study to Higgs sector and search for new phenomena



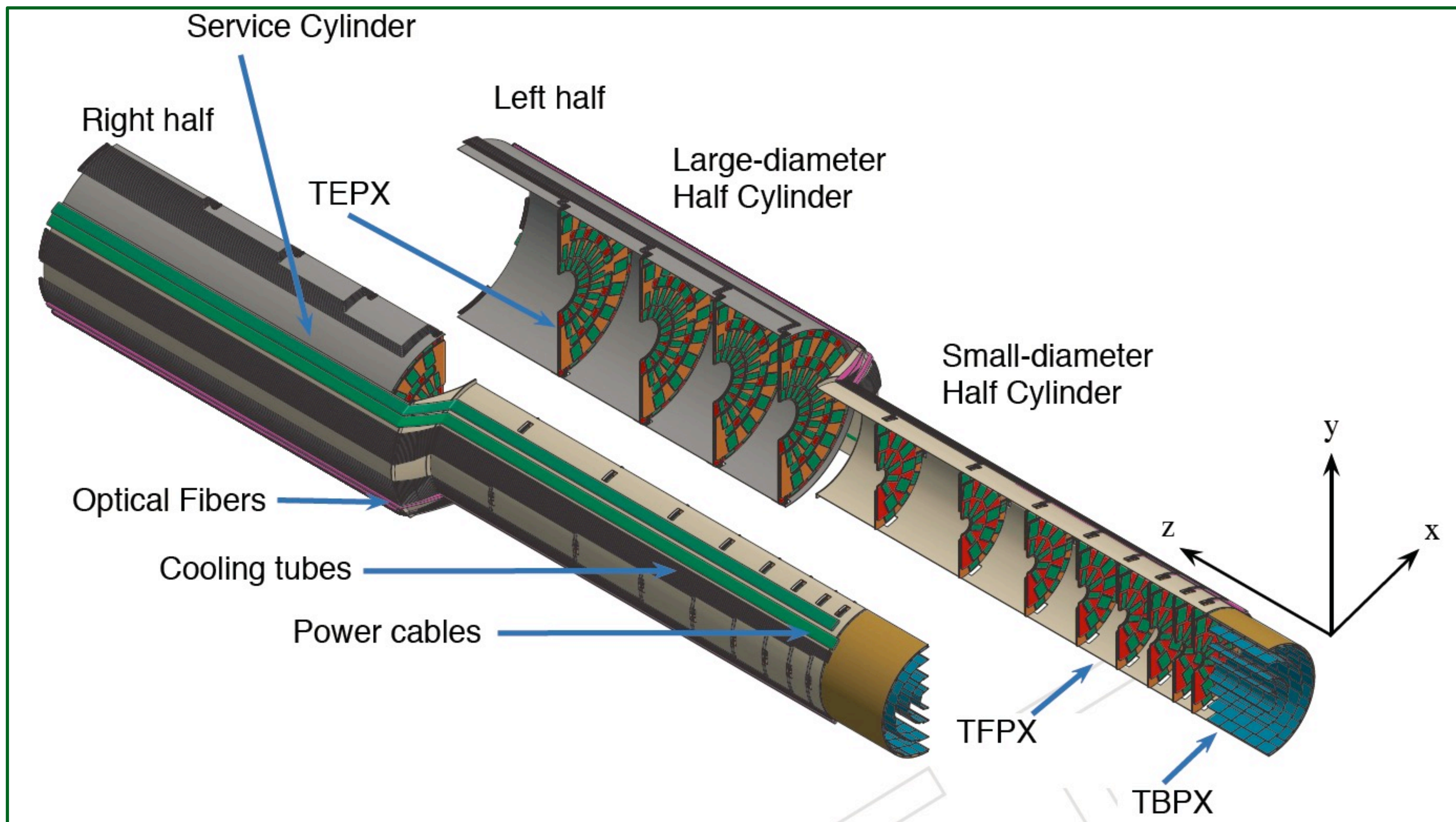
Tracker Detector for HL_LHC

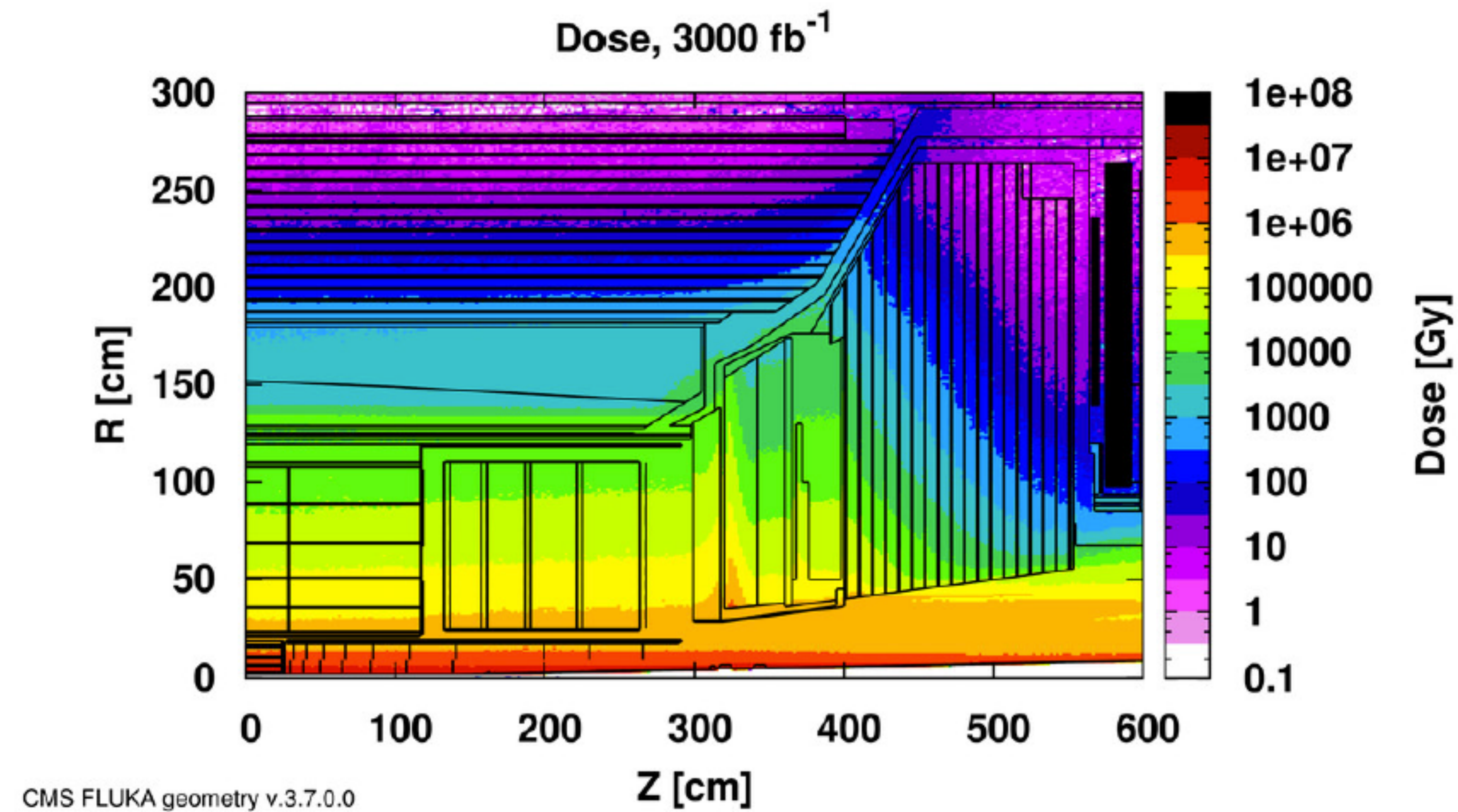
- **OUTER TRACKER** : momentum resolution, tracking trigger (up to $|\eta|$ =2,4)
    - 6 'double-sensor' in barrel (10 single now); 5 double sensors disks (9 now)
- **PIXEL DETECTOR** : tracking seeding, vertex reconstruction, tracking extension
    - 4 barrel layers (as Phase-1); 10 disks (3 in Phase-1)

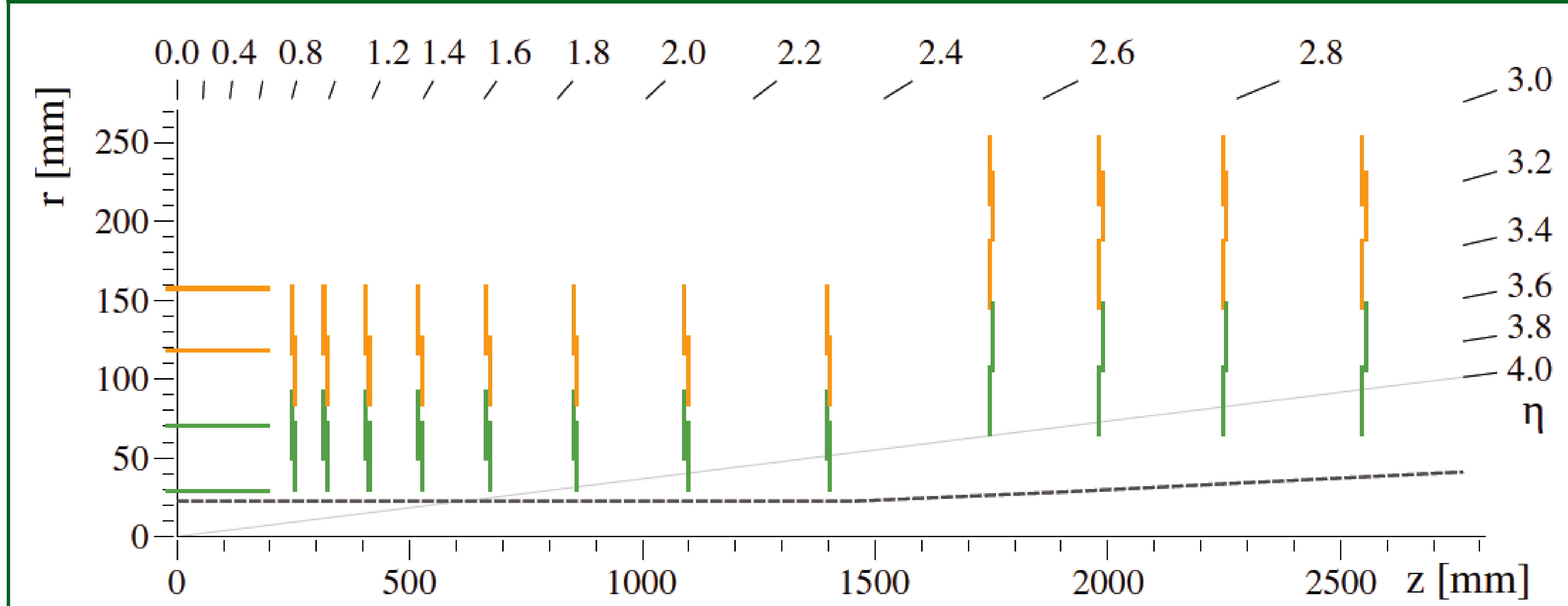


R_{min}~3cm

Pixel Detector







The most demanding layers are the inner ones, at ~3 and 7 cm:

- particle flux
- radiation dose

to mantain same pixel occupation a higher granularity is required (x5). LHC area is ~13000um^2 therefore pixel cell should be reduced at ~2650 um^2

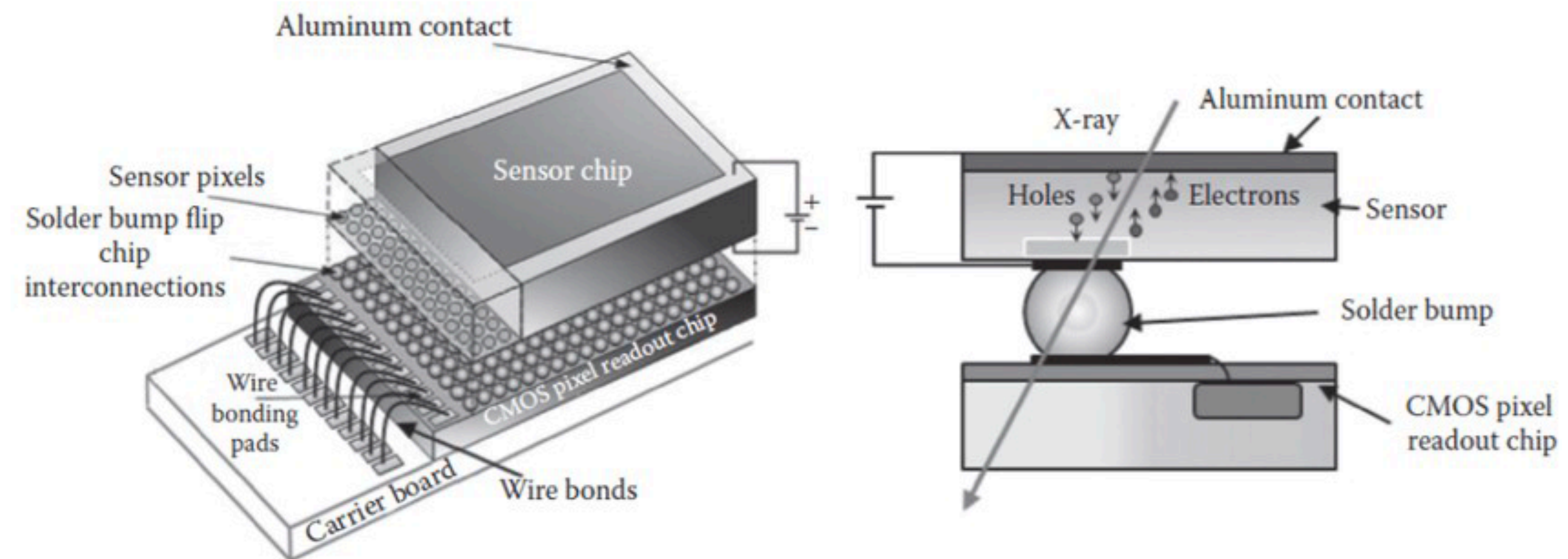
Pixel Detector at HL_LHC : ReadOut Electronics specs

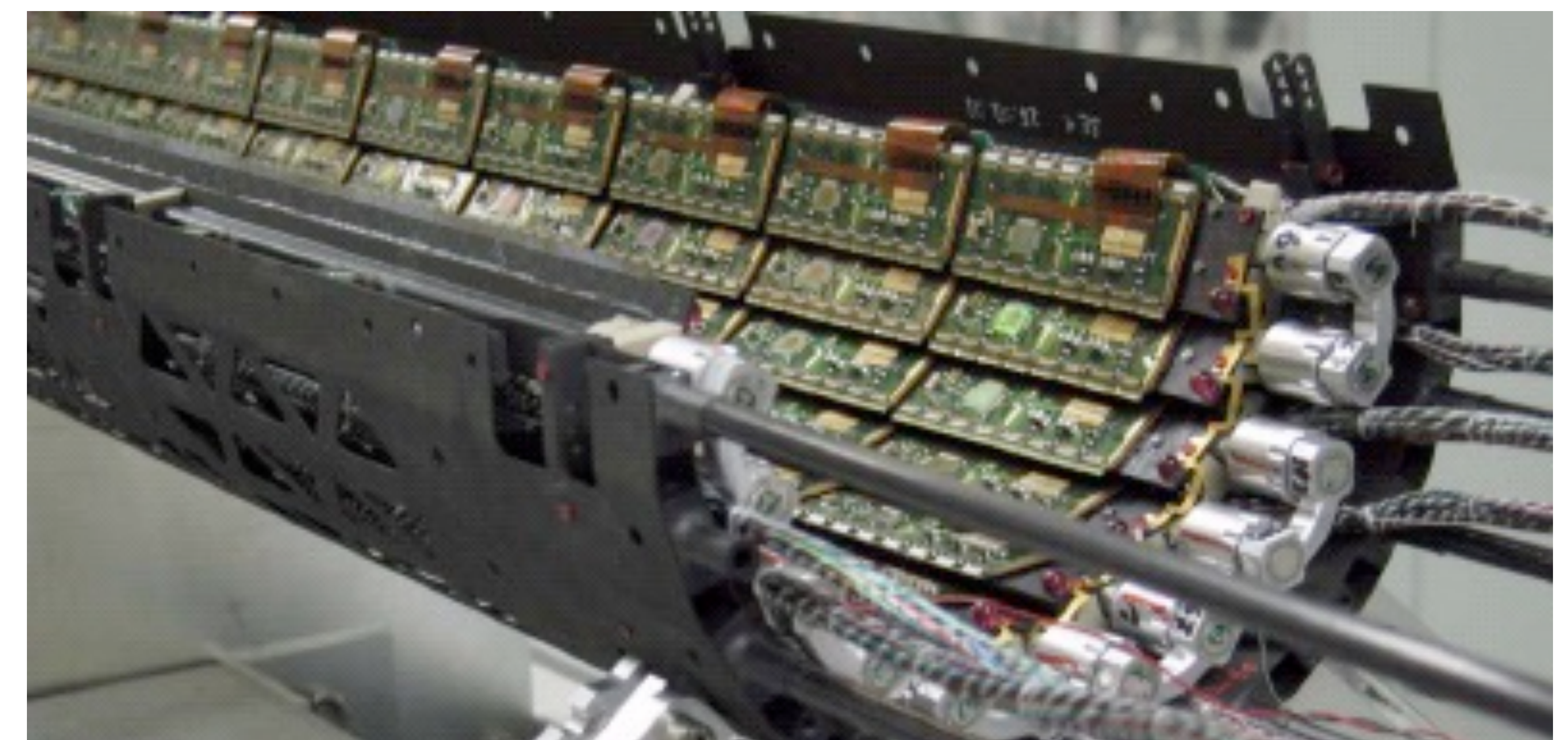
Requirements from HL_LHC experiments

Small pixels: 50x50um^2
Large chips: 2cm x 2cm (~1 billion transistors)
Hit rates: 2 GHz/cm^2
Signal Digitisation : 4-5 bit
Radiation: 1Grad, 10^{16} n/cm^2 (unprecedented)

Trigger: up to 1MHz with 12.5us latency
(~100x buffering and readout)
Low power - Low mass systems

Data readout : up to 4-5 Gbs/s
TRIGGER Latency up to 12.5us (x3) ==> deeper storage buffer





Pixel ReadOut chip: State of the Art

PARAMETER or FEATURE	**1st generation LHC phase 0**	**2nd generation LHC Phase 1**	**3rd generation LHC Phase 2**
CMOS technology	250nm	250nm / 130nm	65nm
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~ 750 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	3 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 μm^2 50x400 μm^2	100x150 μm^2 50x250 μm^2	25x100 μm^2 50x50 μm^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	< 1000 e$^-$
L1 Trigger Latency	2-3 μs	4-6 μs	10-20 μs
L1 Trigger Rates	100 KHz	~100 KHz	200-1000 kHz
ASIC side	~1 cm^2	~4 cm^2	1-4 cm^2
Hit memory per chip	0.1 Mb	1 Mb	>16 Mb
Chip output bandwidth	~40 Mb/s	~320 Mb/s	~3 Gb/s
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.6 W/cm^2

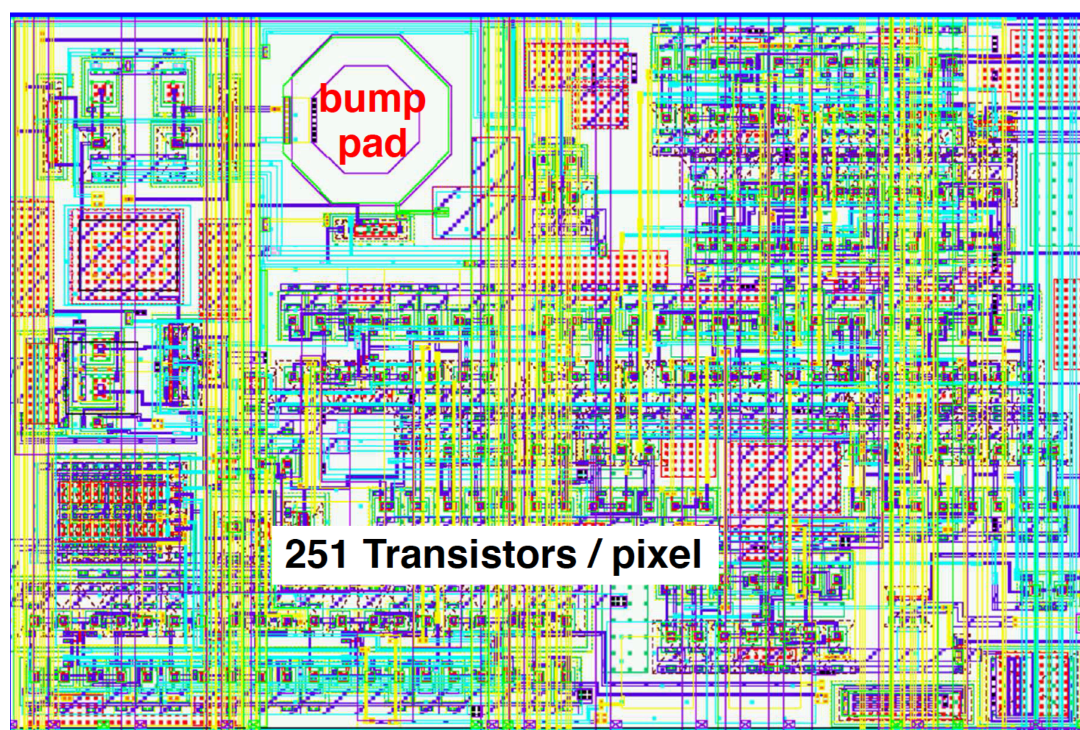
Increasing granularity from Present to HL_LHC

innovation allow to decrease of a factor ~5 the pixel size
either improving performance (threshold, speed, data rates…)

PRESENT DETECTORS for pp@LHC

CMS

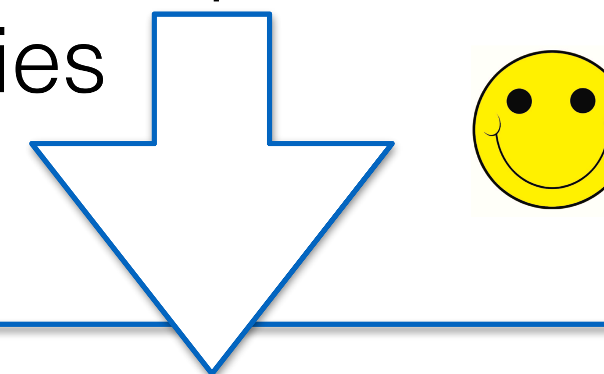
PSI46 (150um x 100um)



- 250nm CMOS tech
- **251** transistors/pix

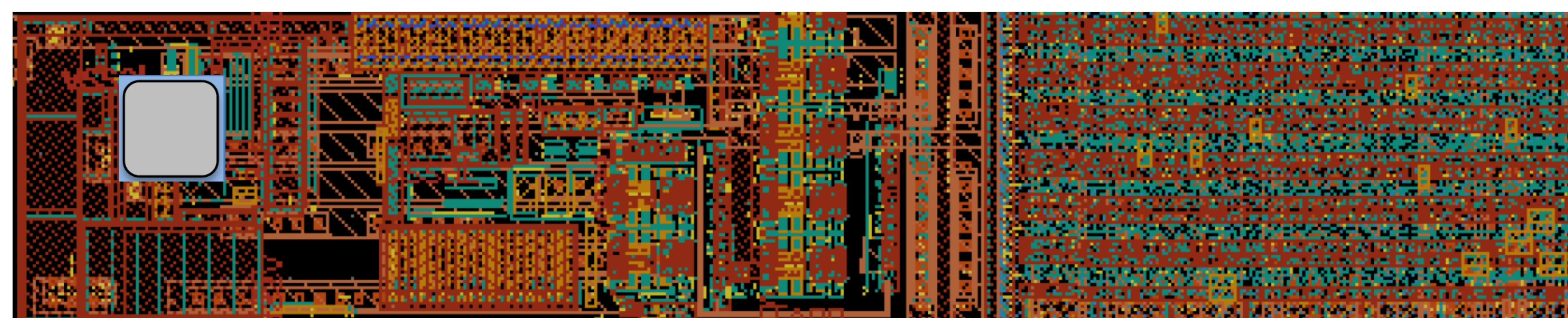
YES !

65nm CMOS technology allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies



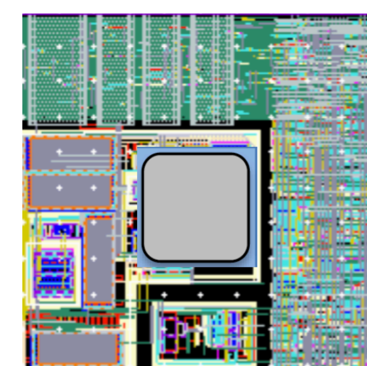
ATLAS

FEI4 (50um x 250um)



- 130nm CMOS techn
- ~**2500** transistors/pix
- ~0,5 trans/um^2

RD53



(50um x 50um)

- 65nm CMOS tech
- ~**2500** transistors/pix
- ~2 trans/um^2

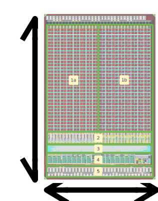
50% of area to digital

for ATLAS & CMS

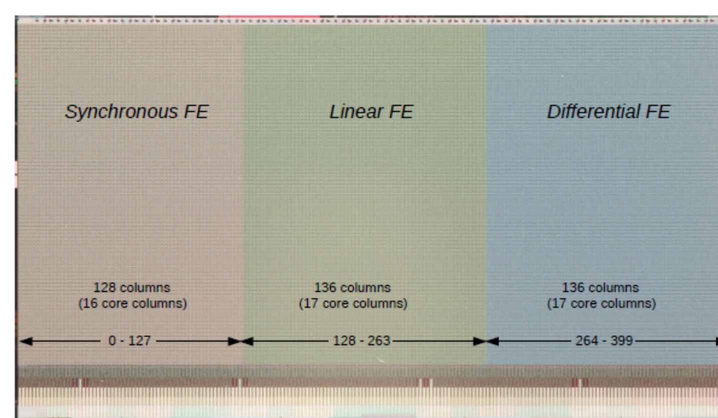
New generation pixel readout chip in 65nm CMOS technology developed by RD53 collaboration

- INFN CHIPIX65 project (dimostratore: 2016) 64x64 pixel matrix
  - RD53 Collaboration: RD53A large size demonstrator: (August-2017) 400x192 pixel matrix
    - RD53 Collaboration: prototype and final version of Atlas and CMS chips ~400x400 pixel matrix

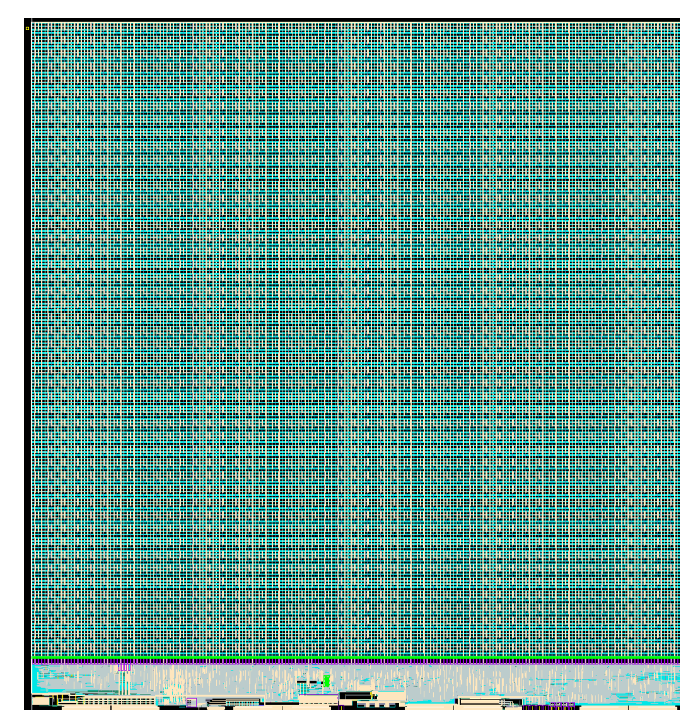
12mm²



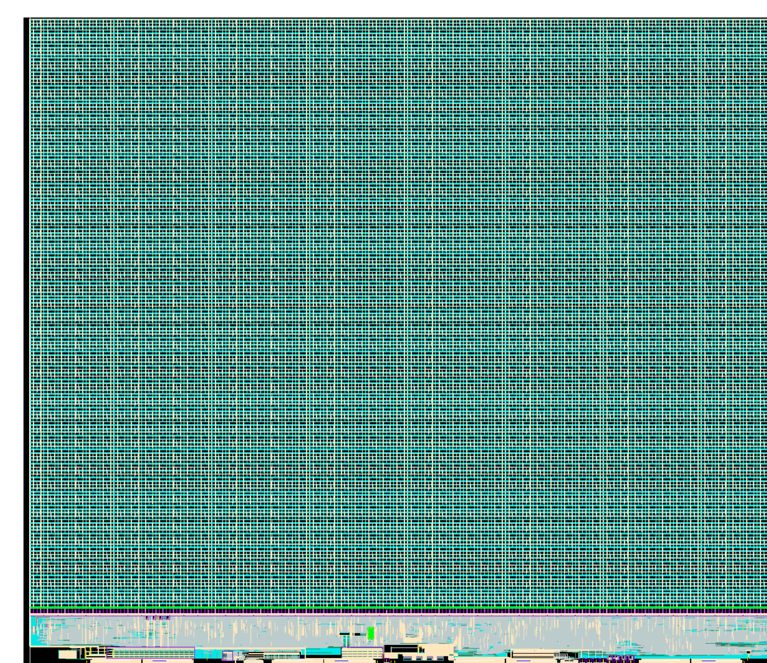
2cm²



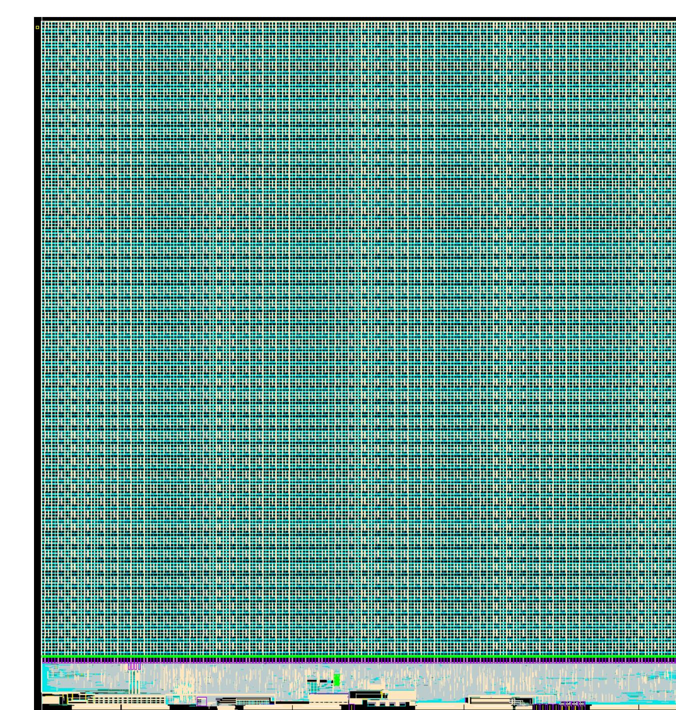
~4cm²



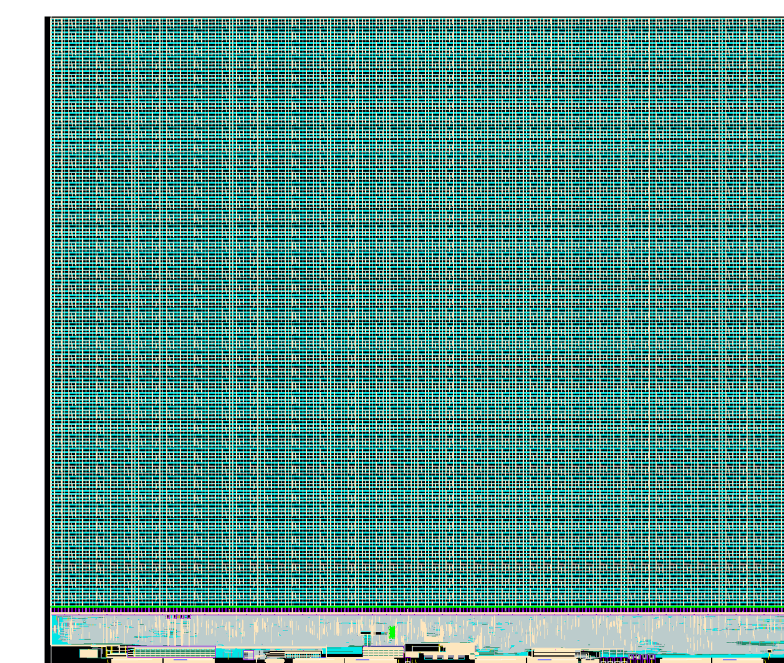
RD53B-ATLAS (ItkPix1)
- March **2020**



RD53B-CMS (CROCv1)
- June **2021**



RD53C-ATLAS (ItkPix2)
- March **2023**



RD53C-CMS (CROCv2)
- fall **2023**

<u>RD53 Collaboration</u> joint effort from ATLAS and CMS Institutes to develop readout chips for the HL-LHC pixel detectors 24 institutes, started in 2013 **- MAJOR contribution from INFN**

Laboratory part one

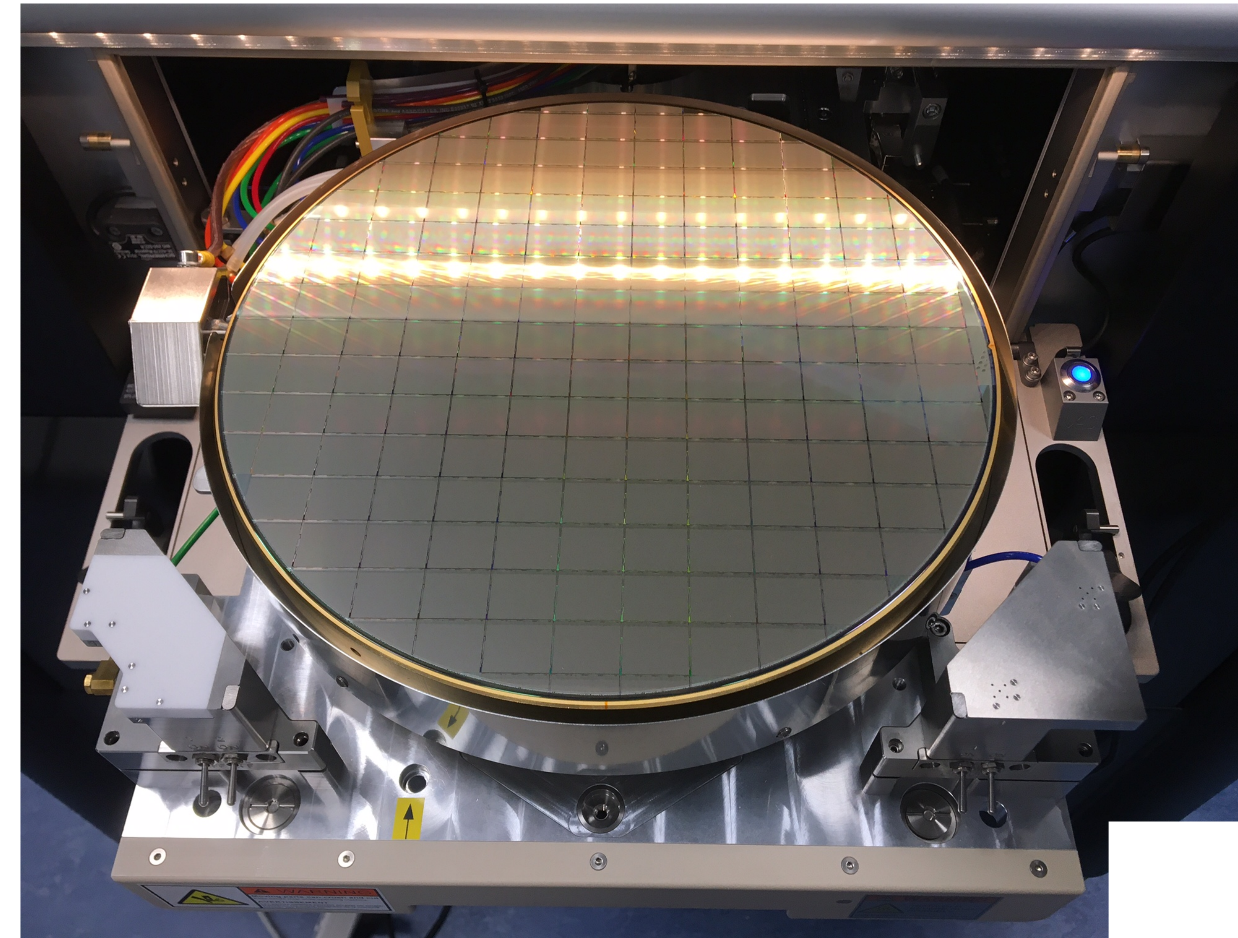
- Fresh from the Fab ! see how ASIC arrives from industry. 12” wafer to be tested and then sent for processing and bump deposition - You will be using a **C-ROC wafer**

- You will enter a clean room: learn how to wear and behave…

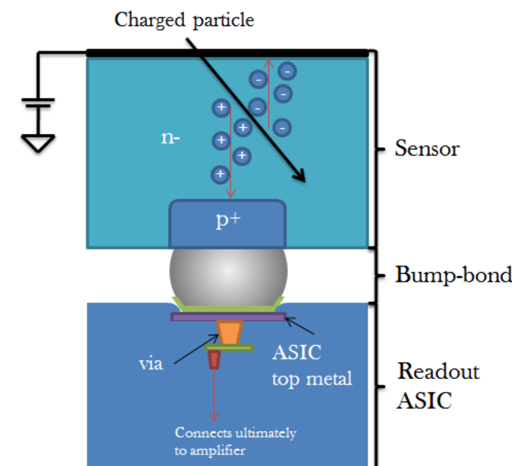
- Look to a Pixel Readout Chip from a Probe-station and navigate precisely on a wafer from chip to chip !

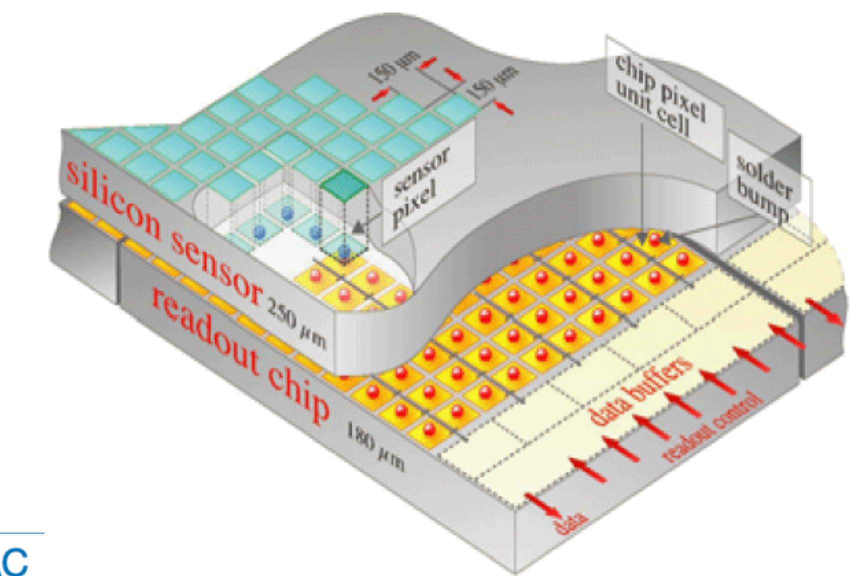
- How to do wafer level testing: you will be testing a real chip

- You will perform the analysis to do Quality assurance and decide if the chip is good or not, looking how you properly calibrated the chip

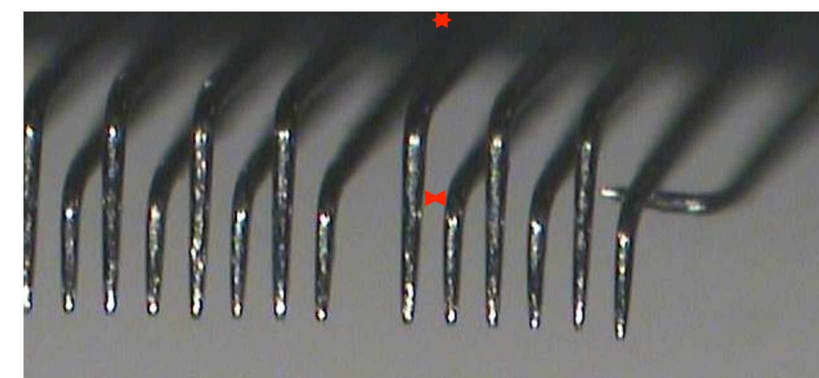


Hybrid technology: chip on wafer has to be processed for UBM and bump deposition

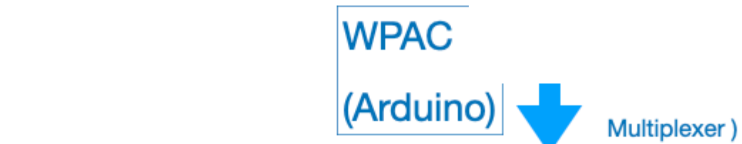




connection to the 184 chip pads via needles: a probe-card allow to power, make I/O, monitor the chip under test (DUT)

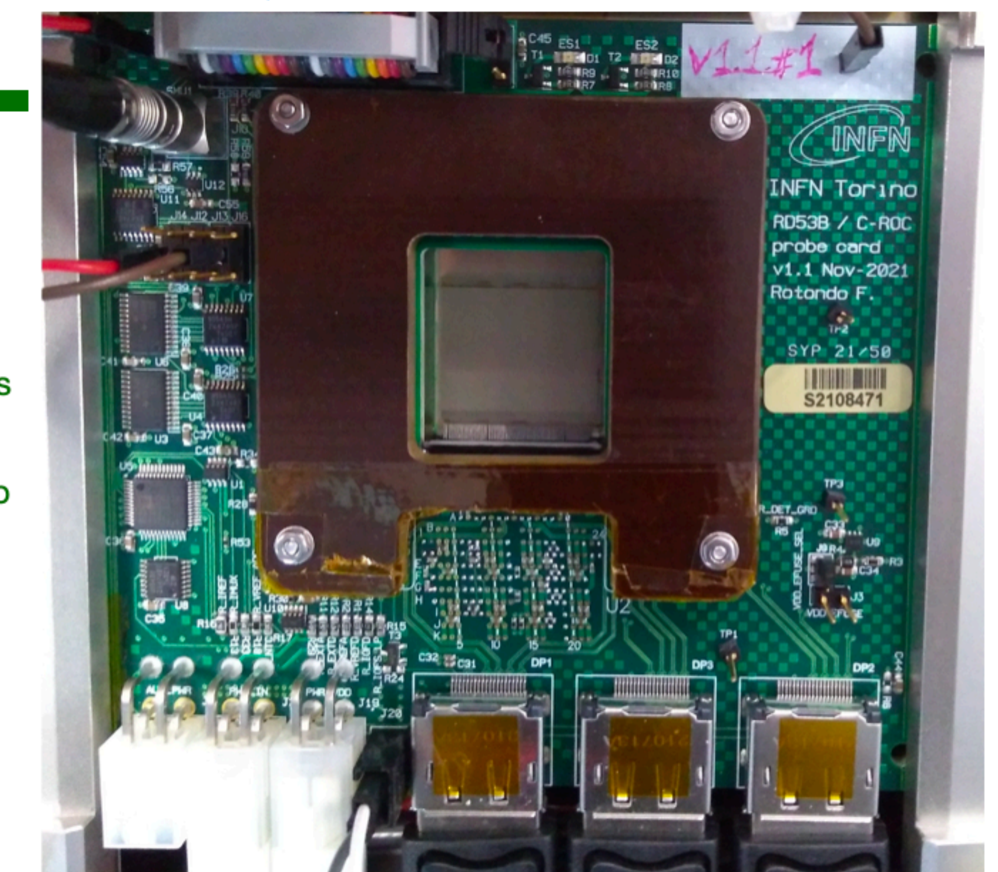


probes: 100um pitch

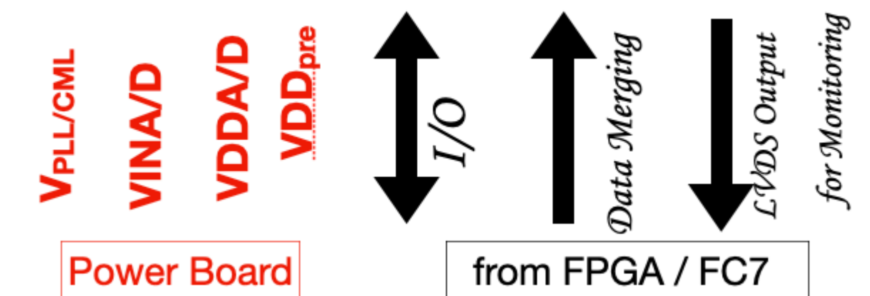


V_{out}

Analog Multiplexer on probe card to allow measurements of many voltages monitored by CROC VMUX and sensing chip additional voltages/GNDs



Probe card



Wafer Probing setup@Torino

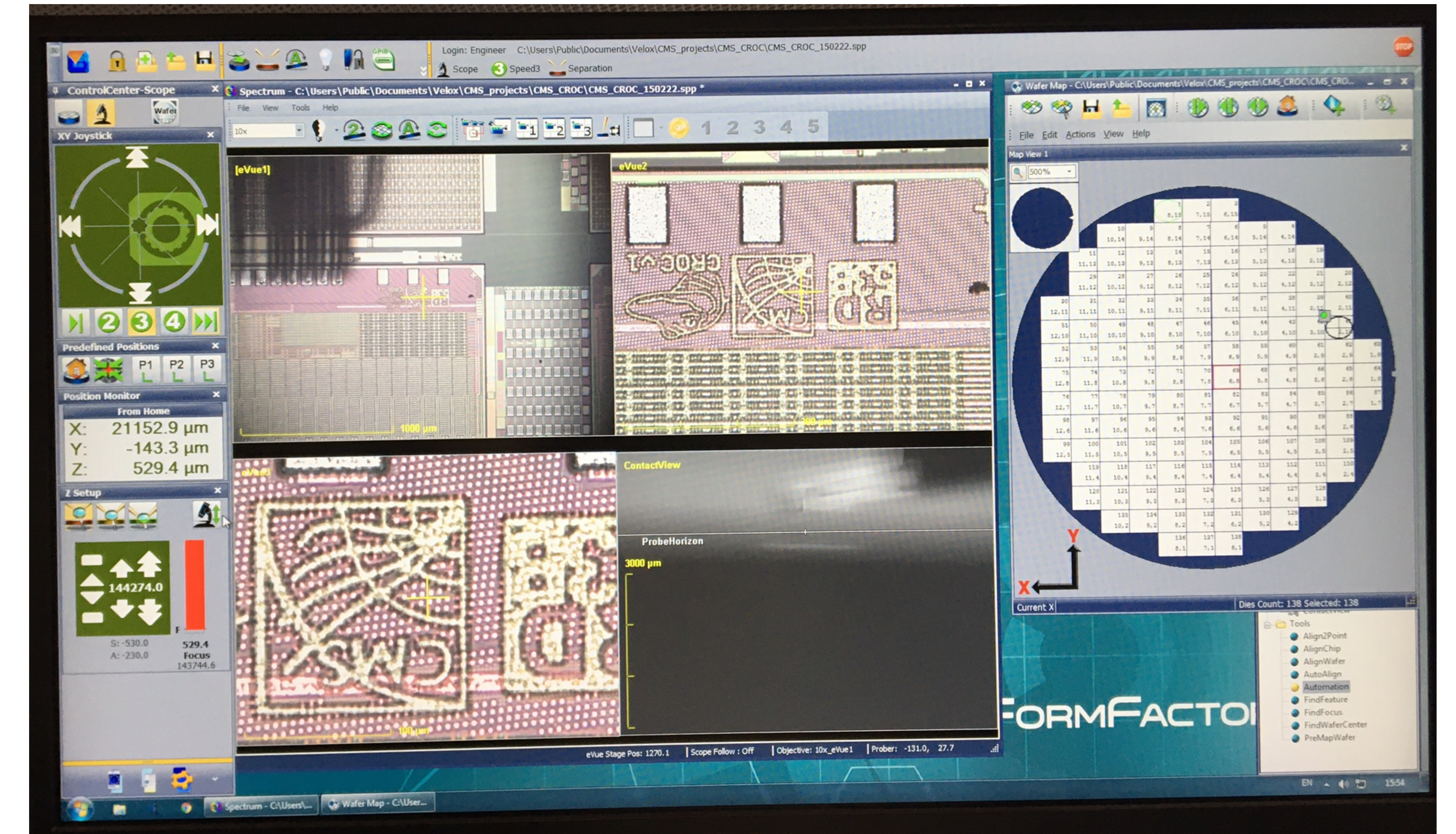
Power supplies

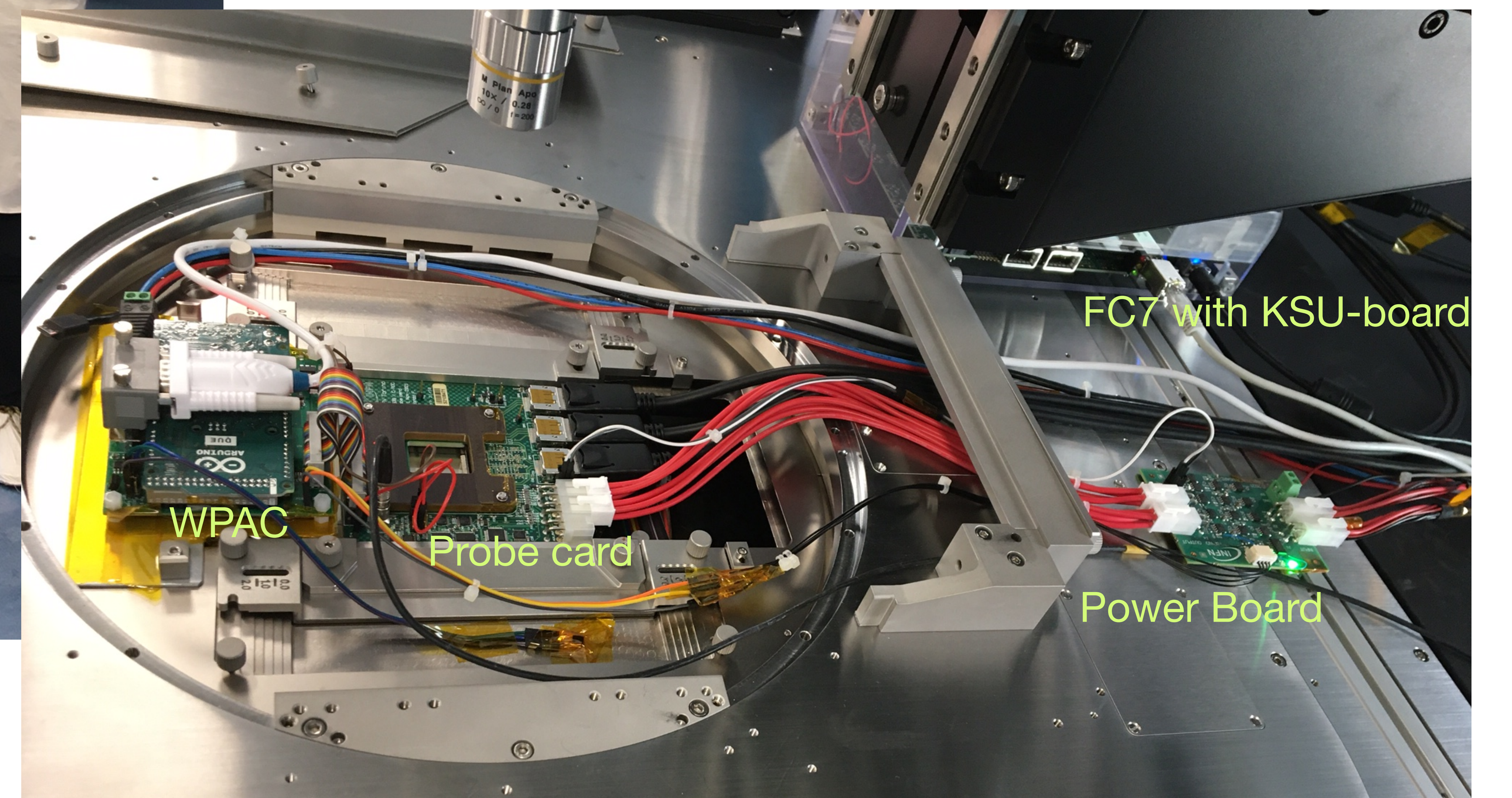
Keithley

FC7

Probe station

Storage





- A probe-station allow to safely travel through all the 138 chips and test them

C-ROC Trimming(s)

Starting from a preregulator and a BandGap, in order to get **calibrated** Voltage and currents distribution a double trimming is needed

1. Trimming of current reference (from ext-pad)
    1. defines chip **wire-bonding** at module construction
2. Trimming of VDDD, VDDA (from configuration registers)

to DAC for Analog Front-End currents distribution

Currents for power distribution and bias to analog

Except the untrimmed current through R_IREF, all other currents scale with IREF_TRIM

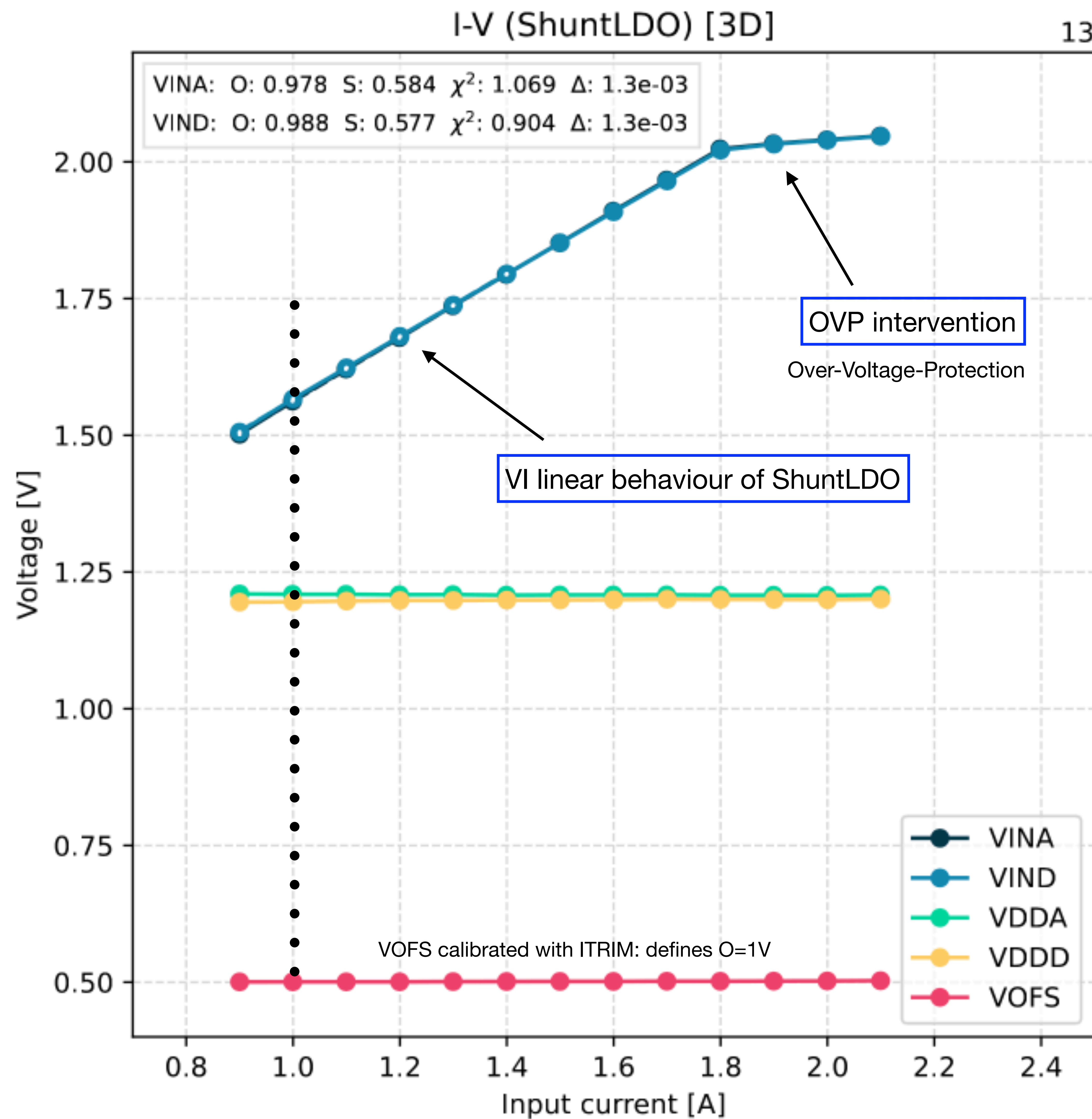
VinA
PreReg
VDD_PRE ~ 1.2V
Core BGR
V_BGR ~ 490 mV
VDD_PRE
4-bit DAC
Trimmed Iref = 4 uA
4uA current mirror
4uA to Bias DACs
VrefA 4-bit DAC
VrefD 4-bit DAC
IMUX
X5
X5
X5
X2.5
53
52
56
54
145
44
4
6
3
20 uA (un-trimmed)
R_IREF
IREF_TRIM pads
GNDA
20 uA
R_OFS
~20 uA
R_VREFA
GNDD
~20 uA
R_VREFD
GNDA
4 uA
R_IMUX
10 uA
R_VREF_ADC
GNDA_REF
GNDD_REF
GNDA_REF

VOFS ShuntLDO

TRIMMING I-REF

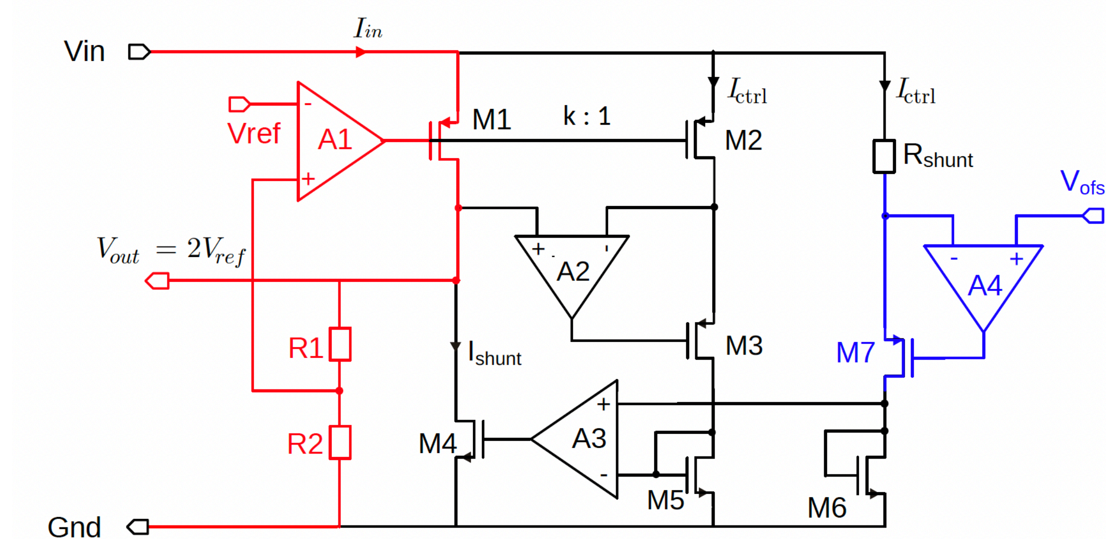
TRIMMING Voltage References for VDDD, VDDA

The power regulator ShuntLDO IV



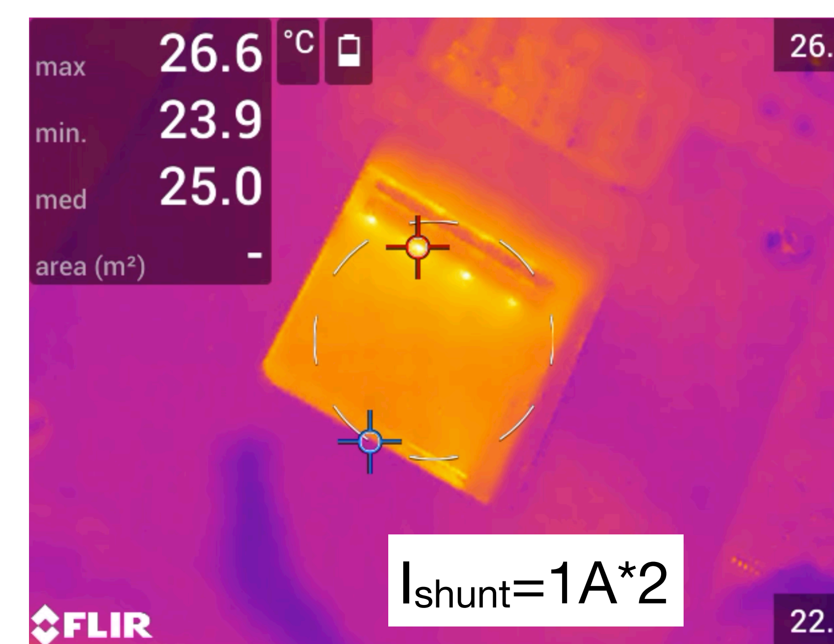
- Fundamental for serial powering of modules: fixed current provide power to CROC, statisfies its consumption request - regardless to current variation - and remaining current goes to a shunt resistor

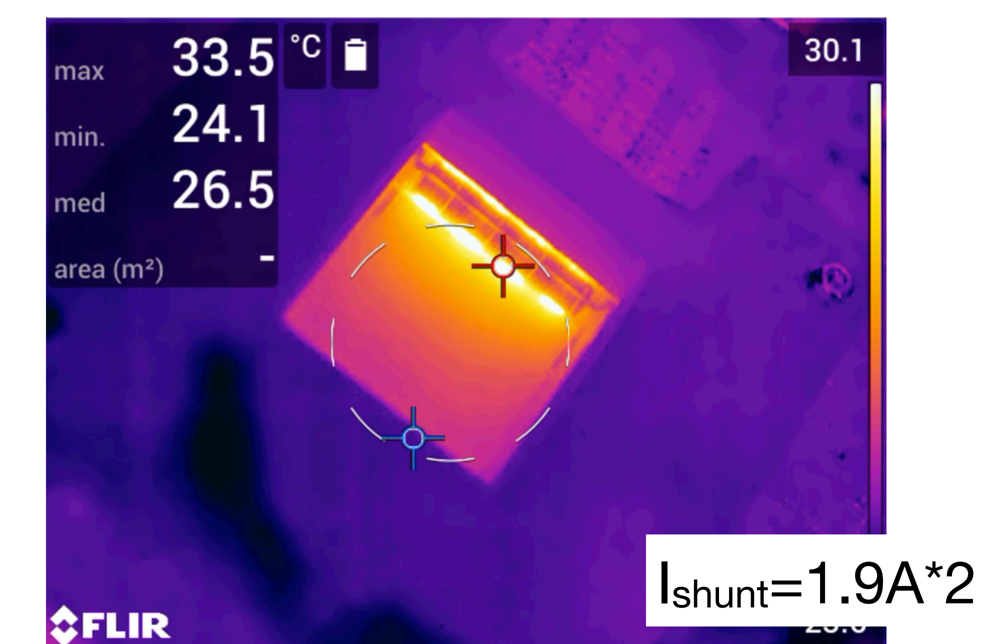
- NB: the current is x-axis is for a single power domain, analog and digital are independent here. This allow to characterise each ShuntLDO



- Chip is configured to operation values, therefore 800mA goes to ACB+Matrix(ana) and 668mA goes to DCB+Matrix(dig)

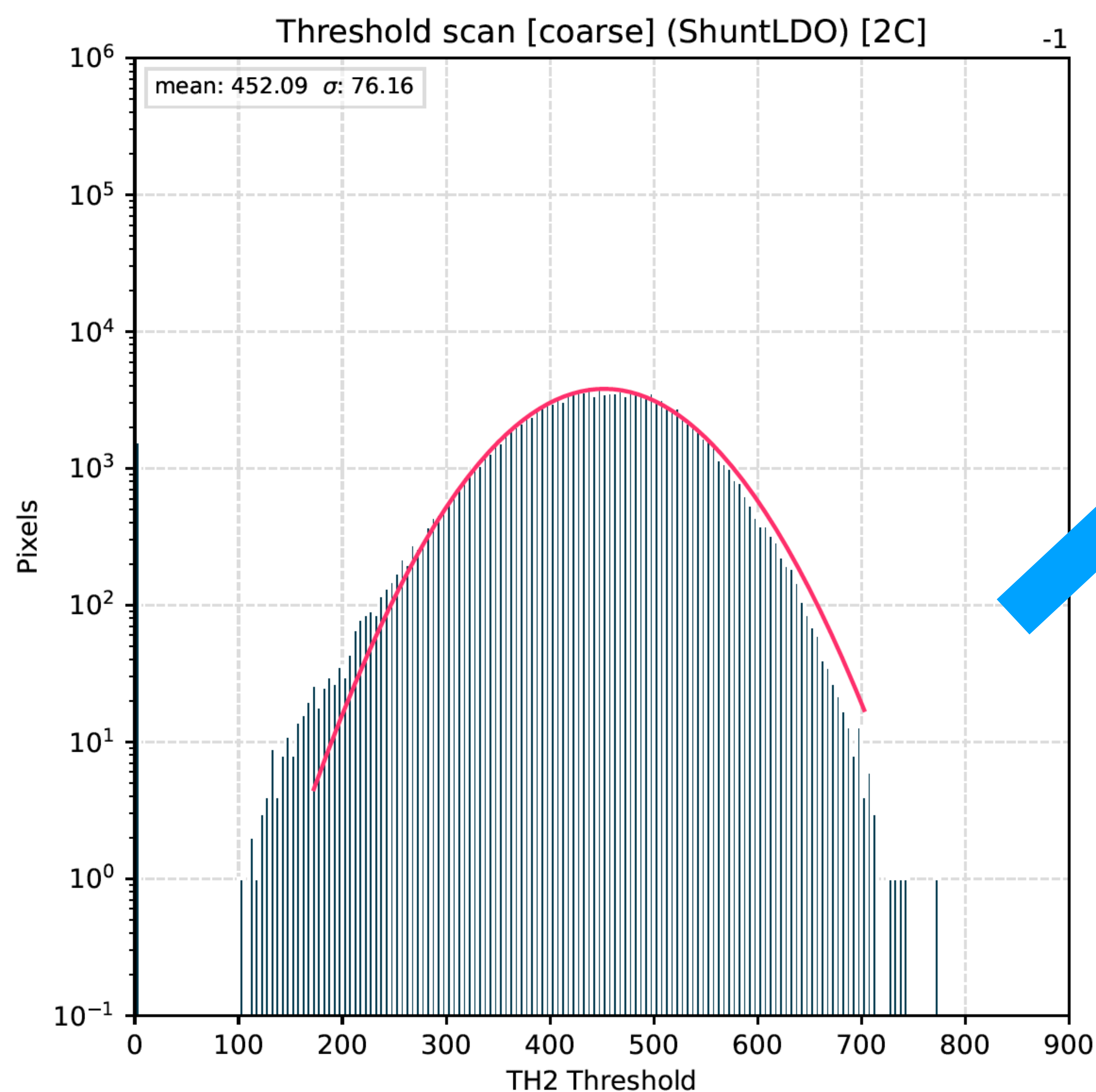
- Over voltage at ~2V is reached at ~1.8A



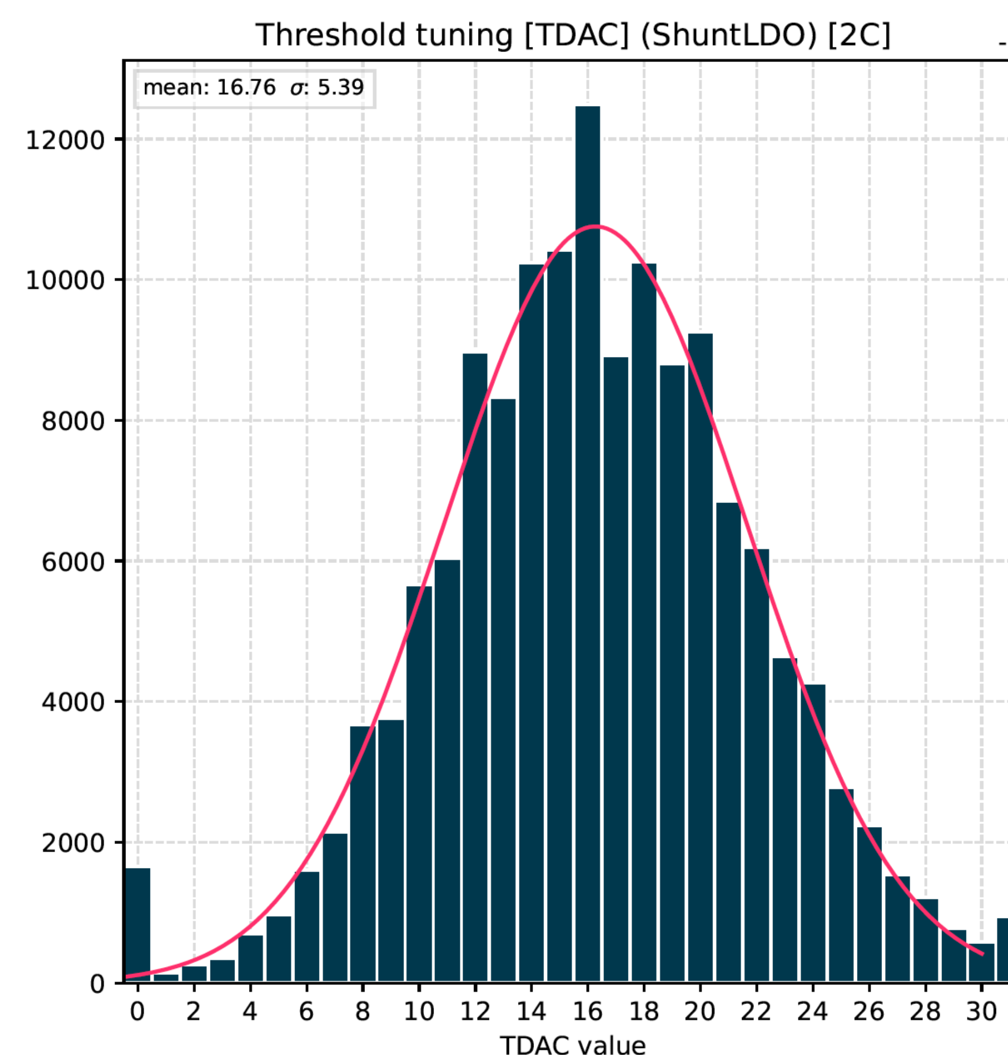


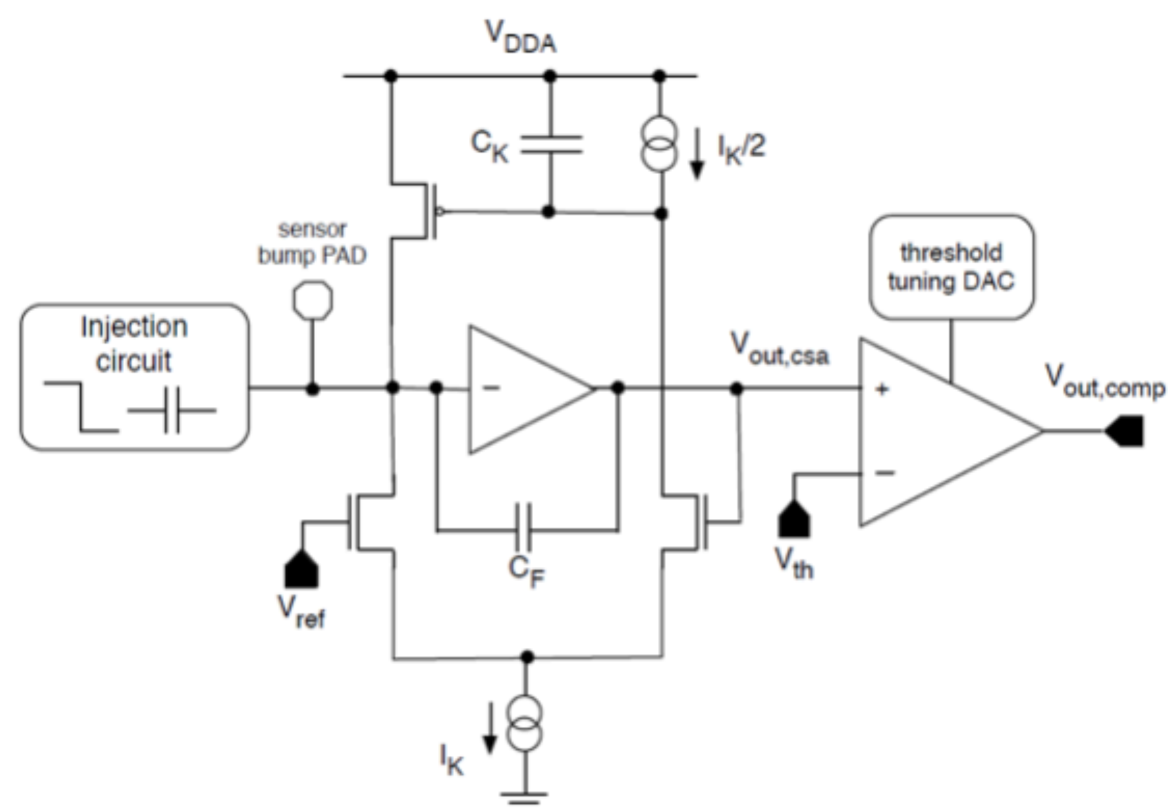
Threshold tuning of analog front-end

From a threshold dispersion between different pixels of 400e- (RMS) ….

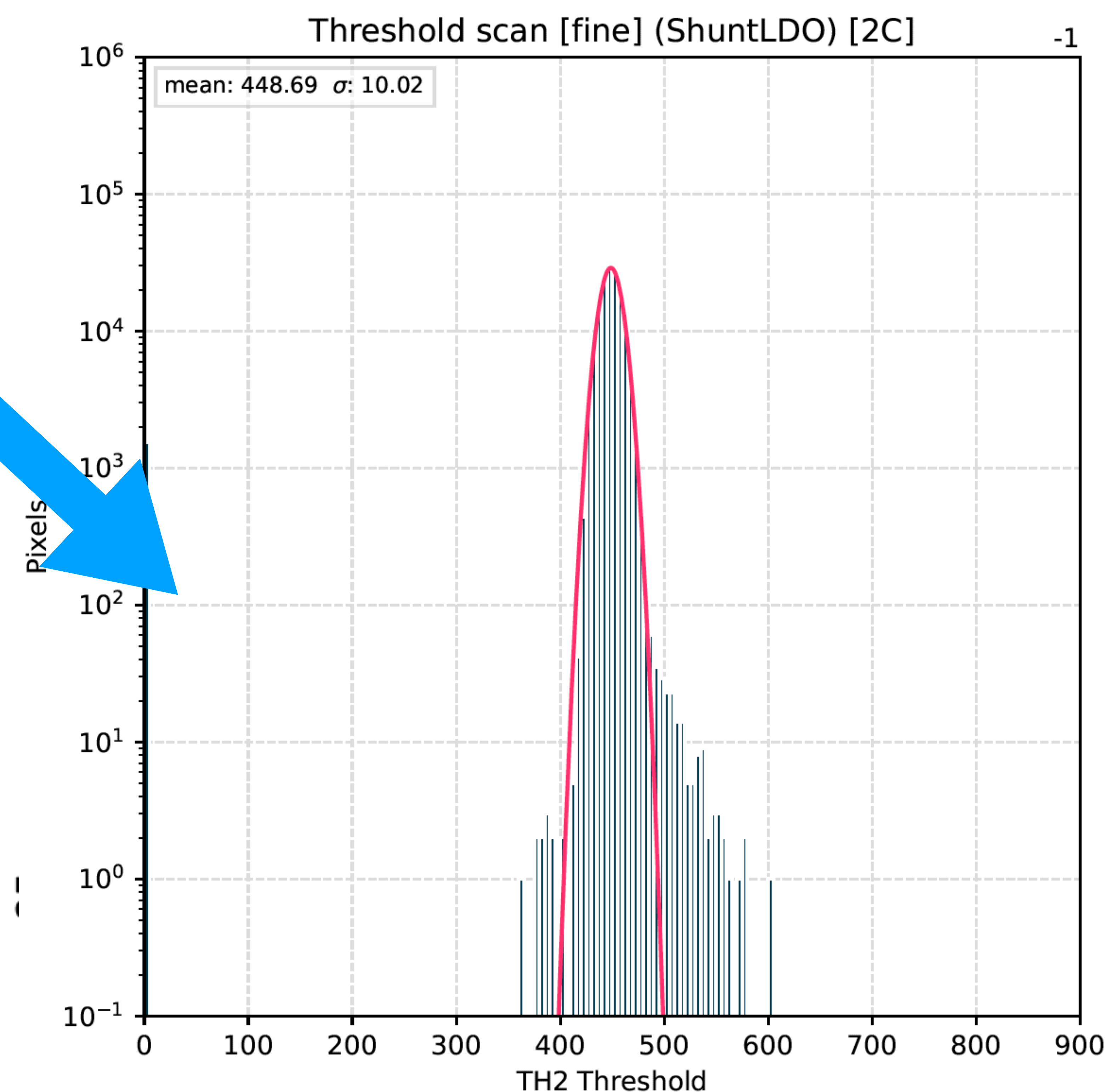


...a per-pixel calibration (5-bits) is made …

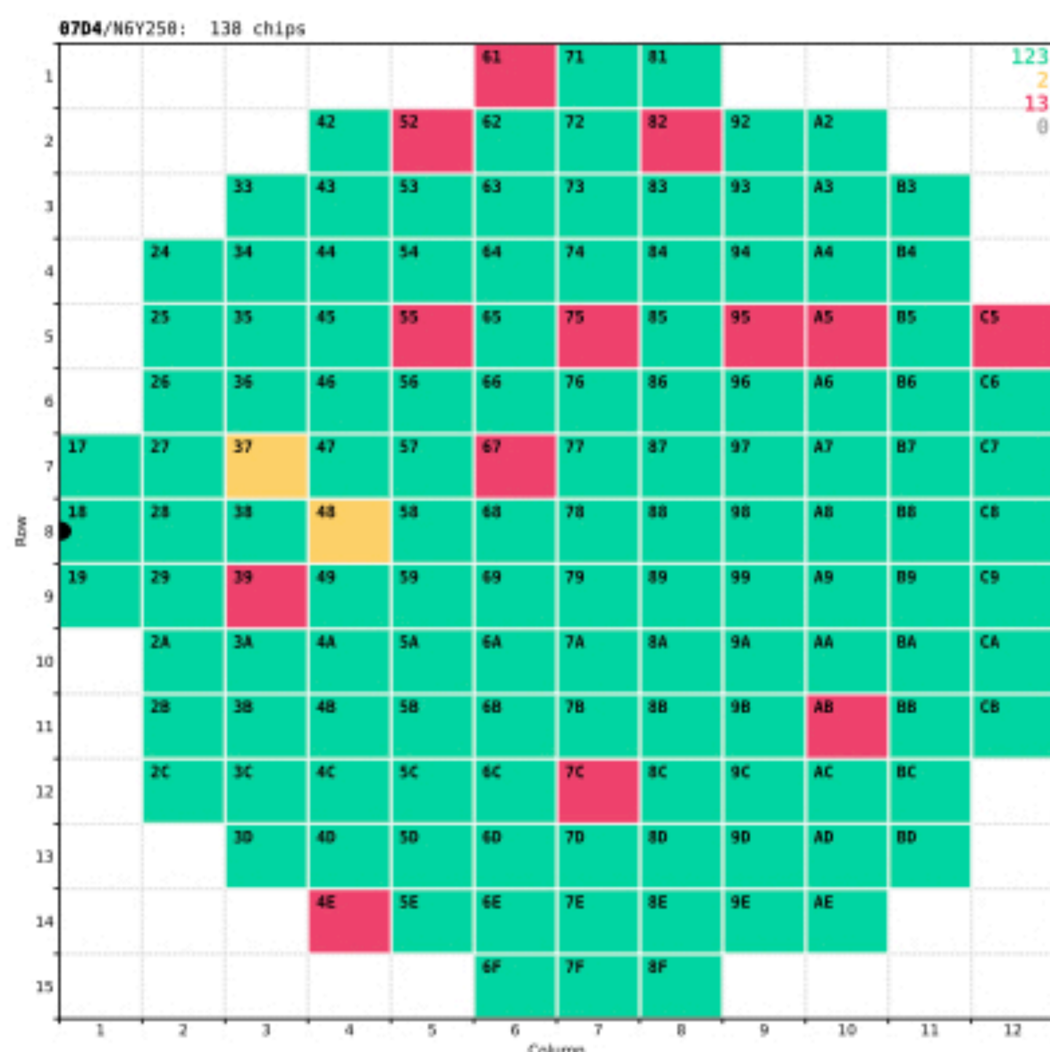


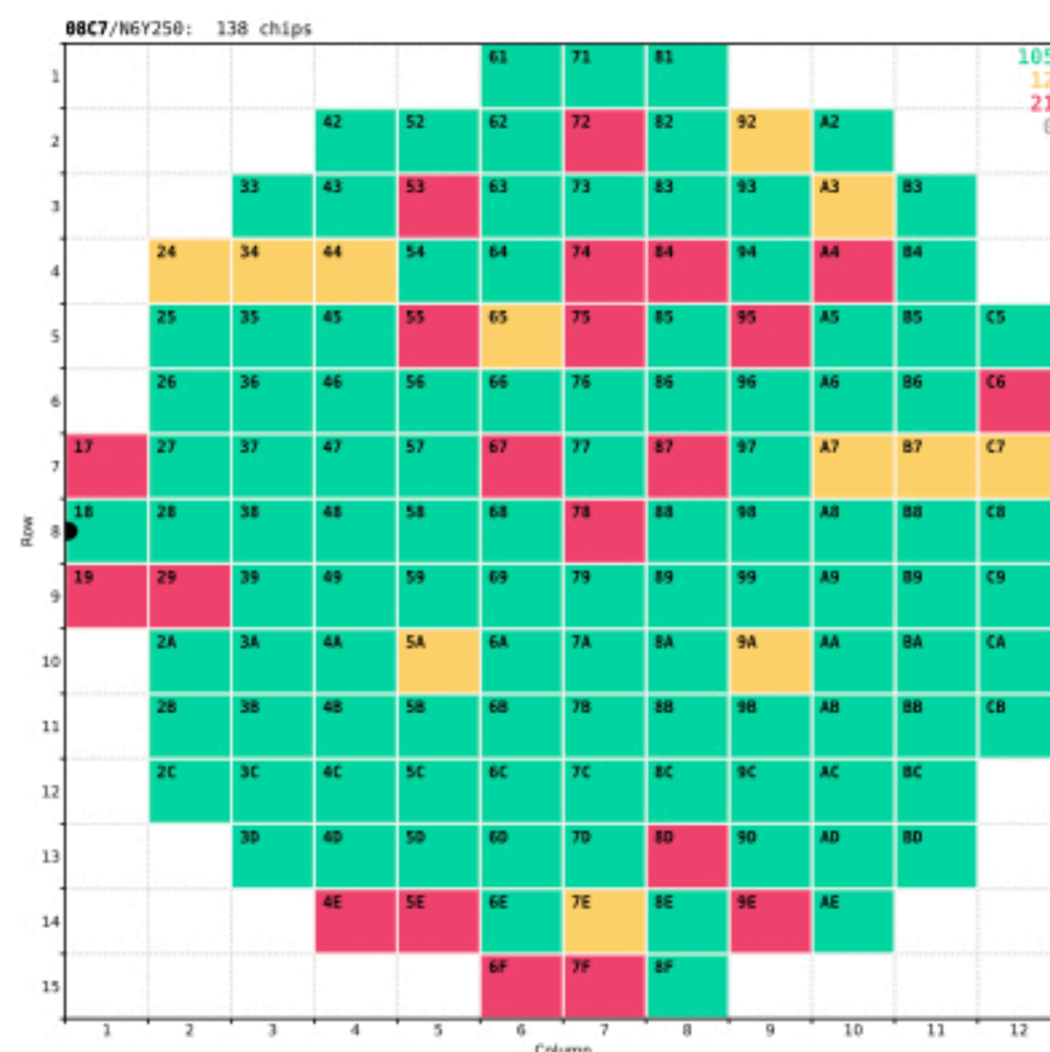


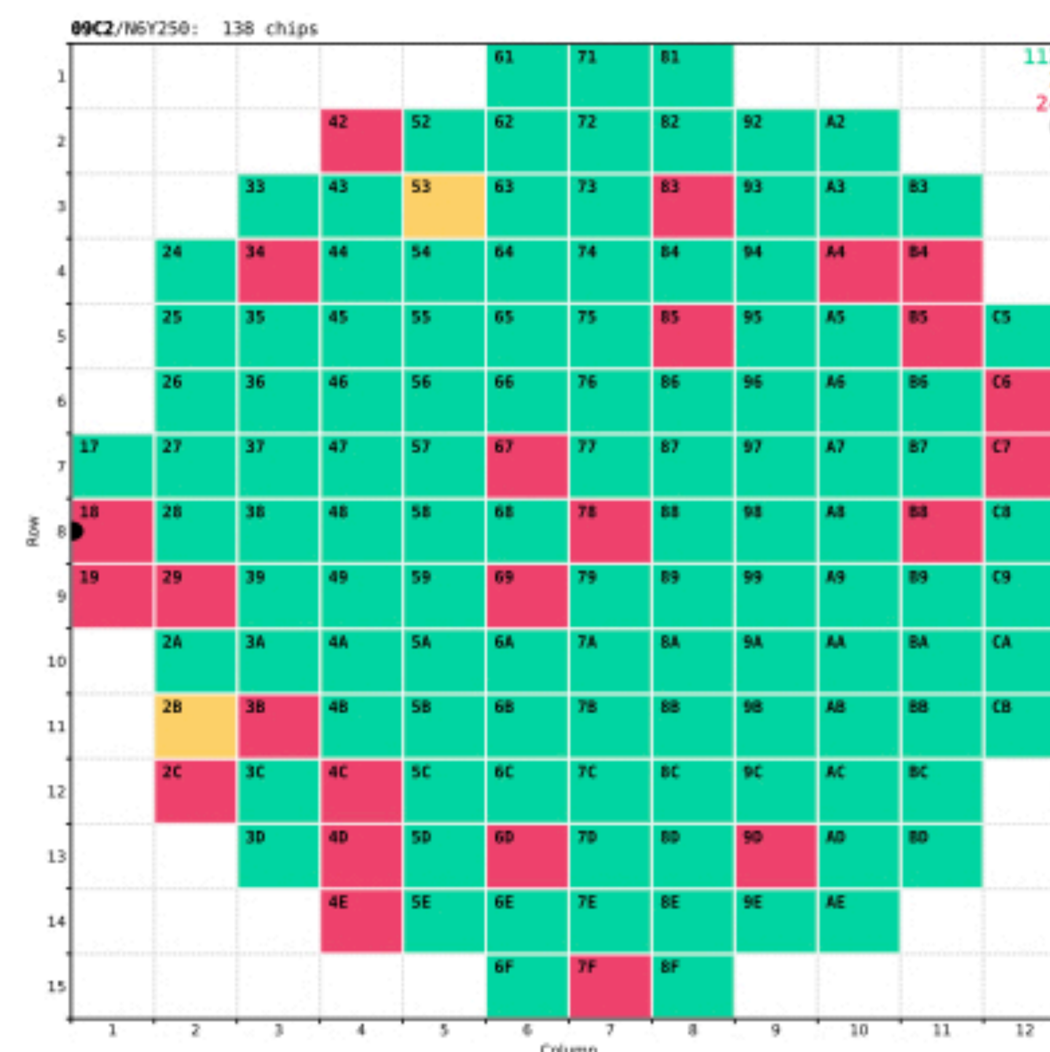
…obtaining the same threshold among 145152 pixels with 50e- RMS !

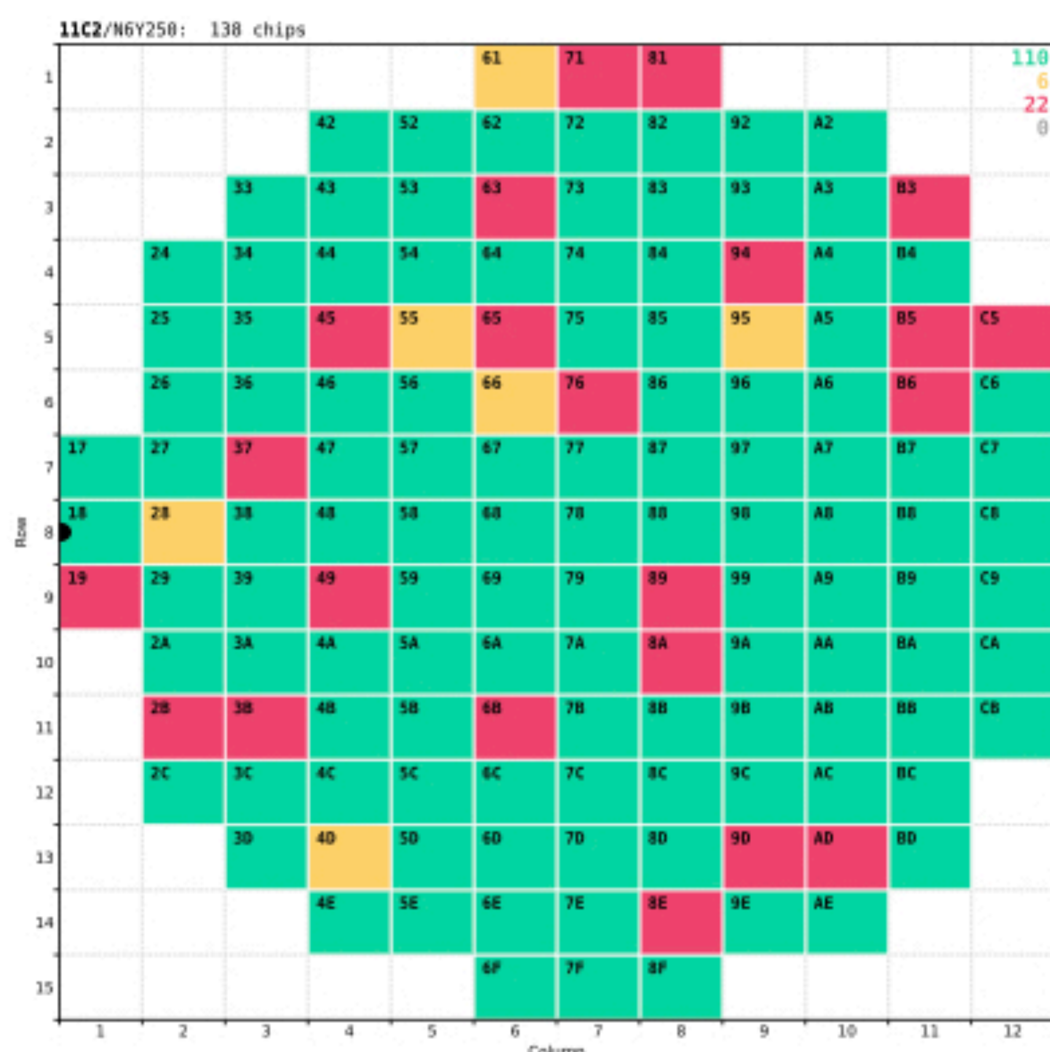


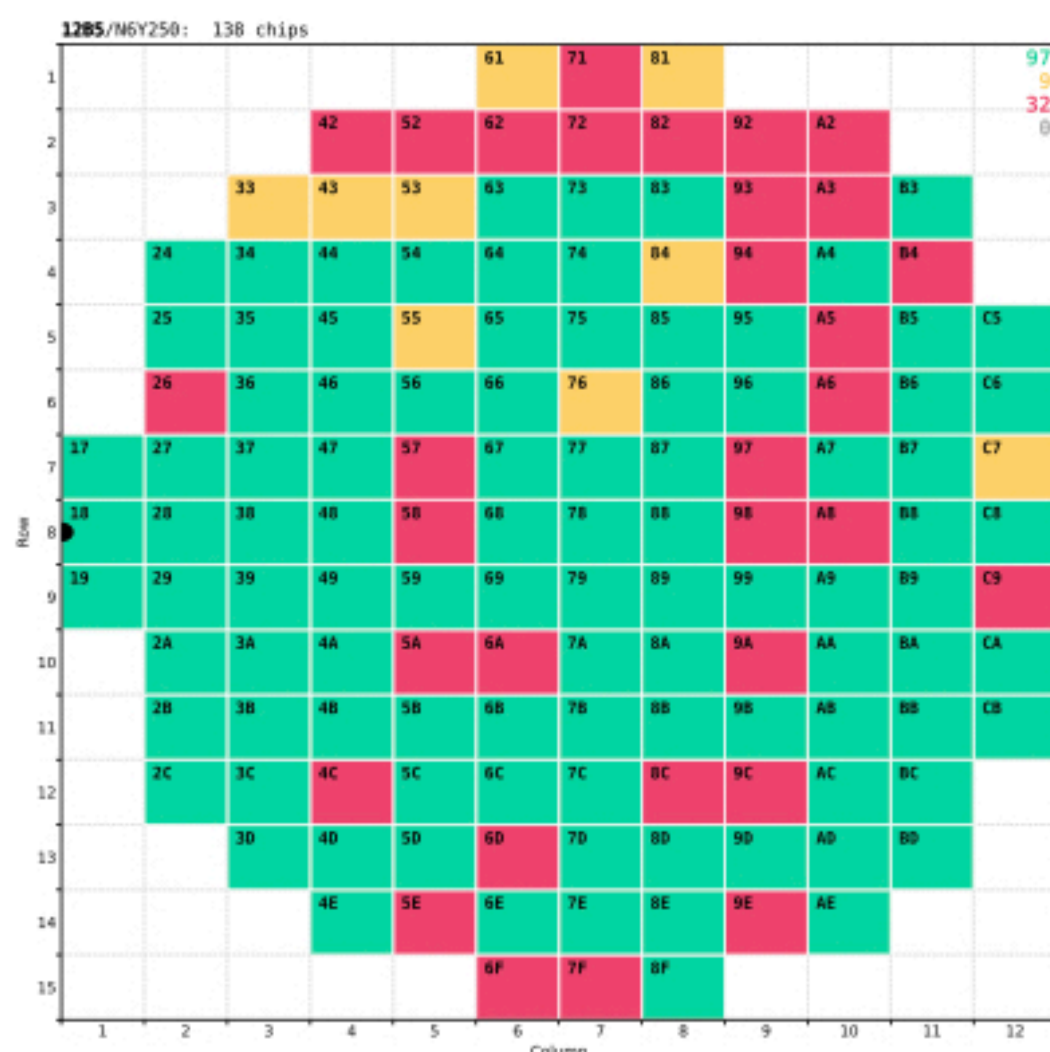
Wafer maps: only good chips are used

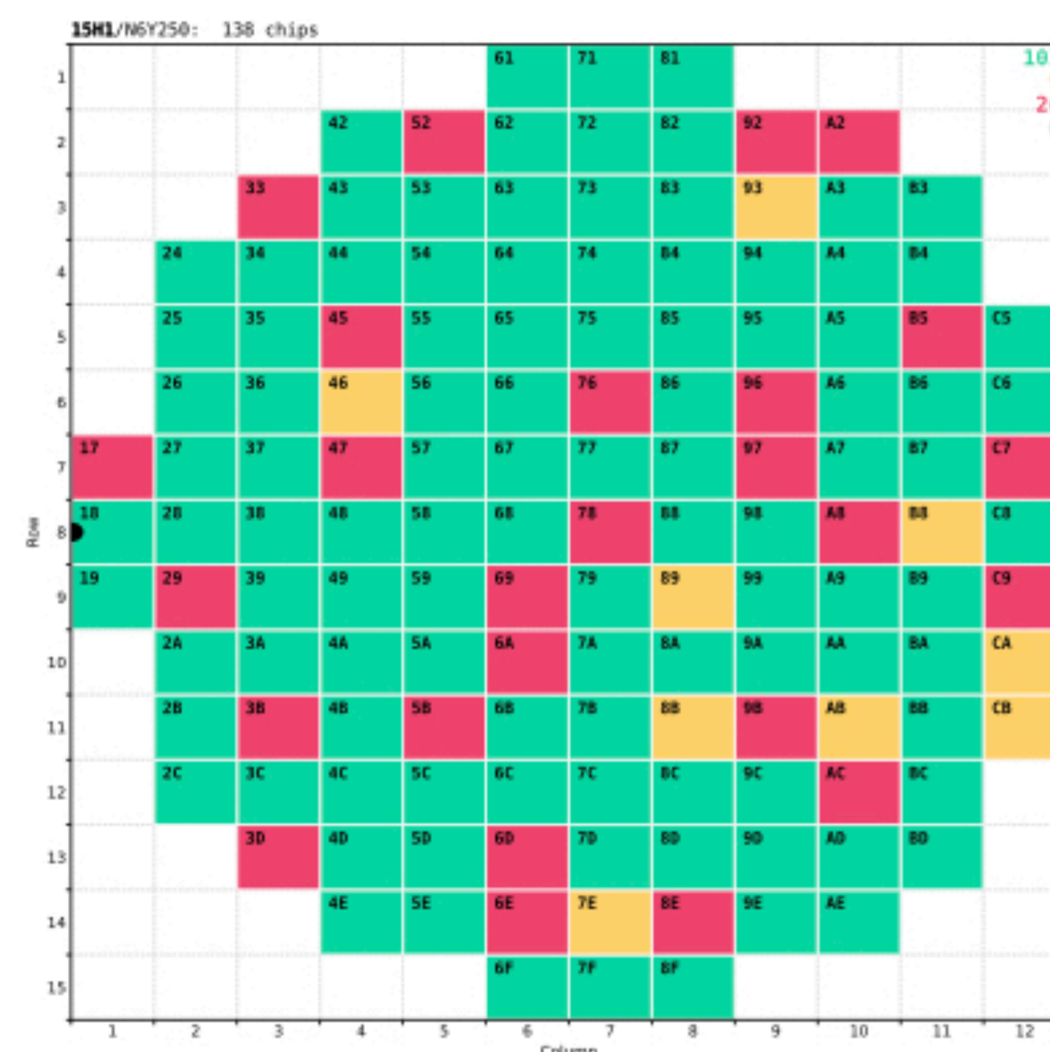












24 different tests are made to select good chips

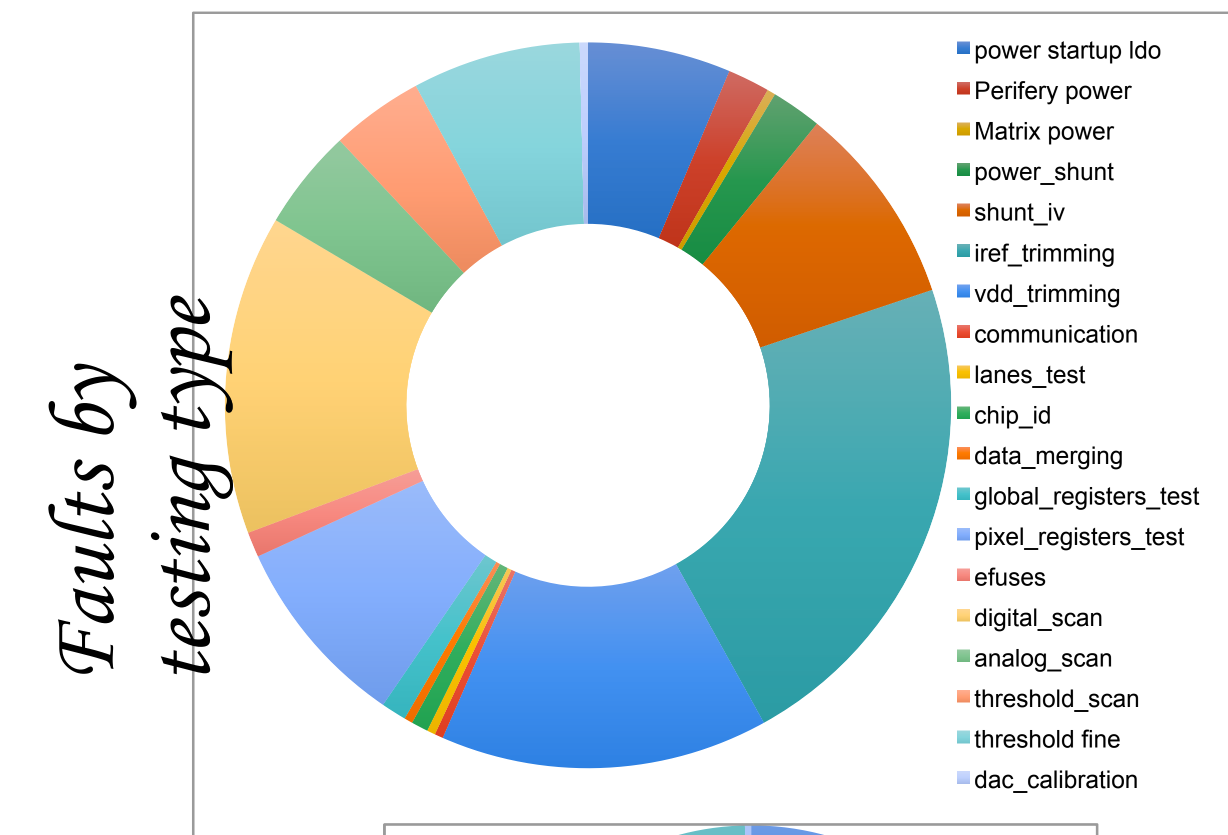
LDO testing

1. Startup in LDO
2. IREF trimming
3. Communication
4. Writing of efuses
5. VDD trimming
6. Global registers ▽
7. Injection capacitance measurement
8. ADC calibration
9. DACs calibration
10. Ring oscillators calibration
11. Temperature sensors calibration
12. Chip bottom and matrix power consumption
13. LDO *IV* curve

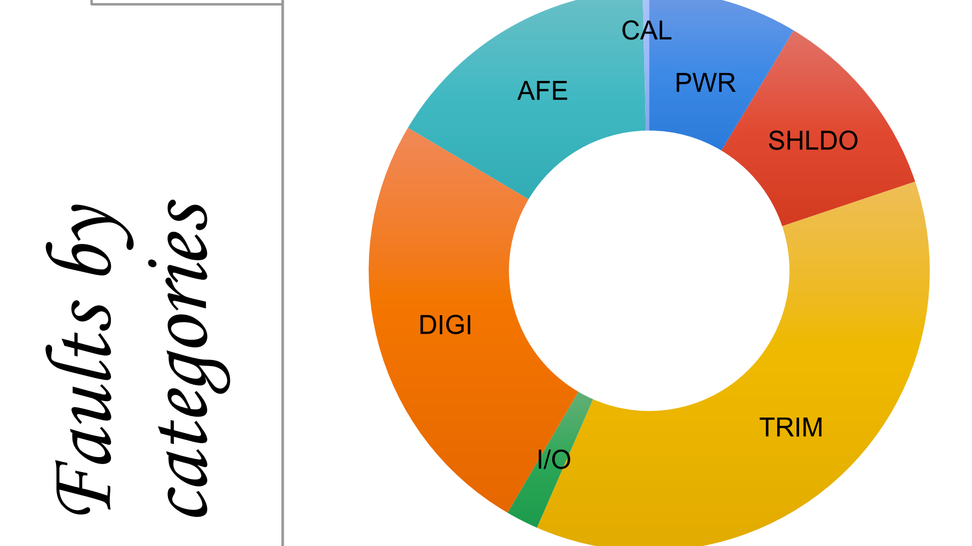
SLDO testing

14. Startup in SLDO
15. SLDO *IV* curve (+ OVP)
16. Aurora lanes ▽
17. Chip ID ▽
18. Pixel registers ▽
19. Data merging ▽
20. Digital scan ▽
21. Analog scan ▽
22. Threshold scan (coarse) ▽
23. Threshold tuning ▽
24. Threshold scan (fine) ▽

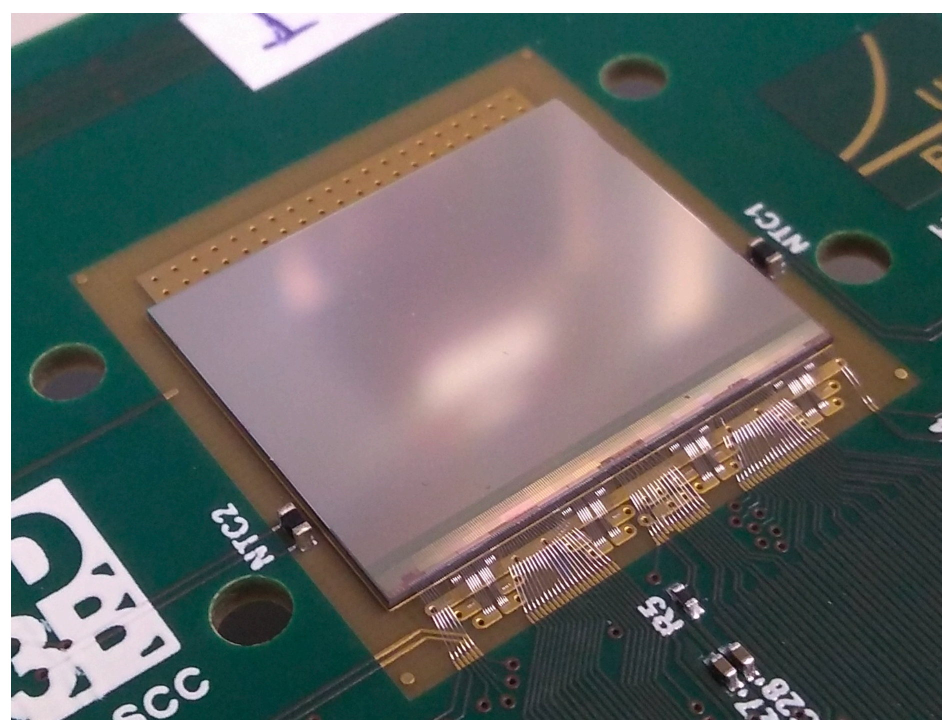
Faults by testing type

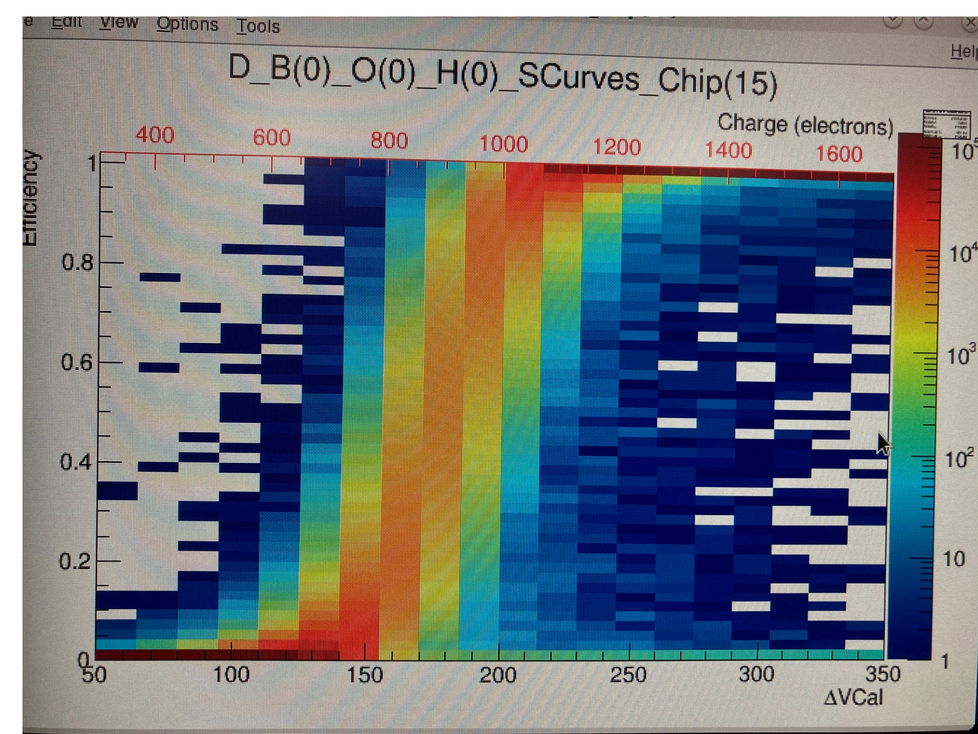


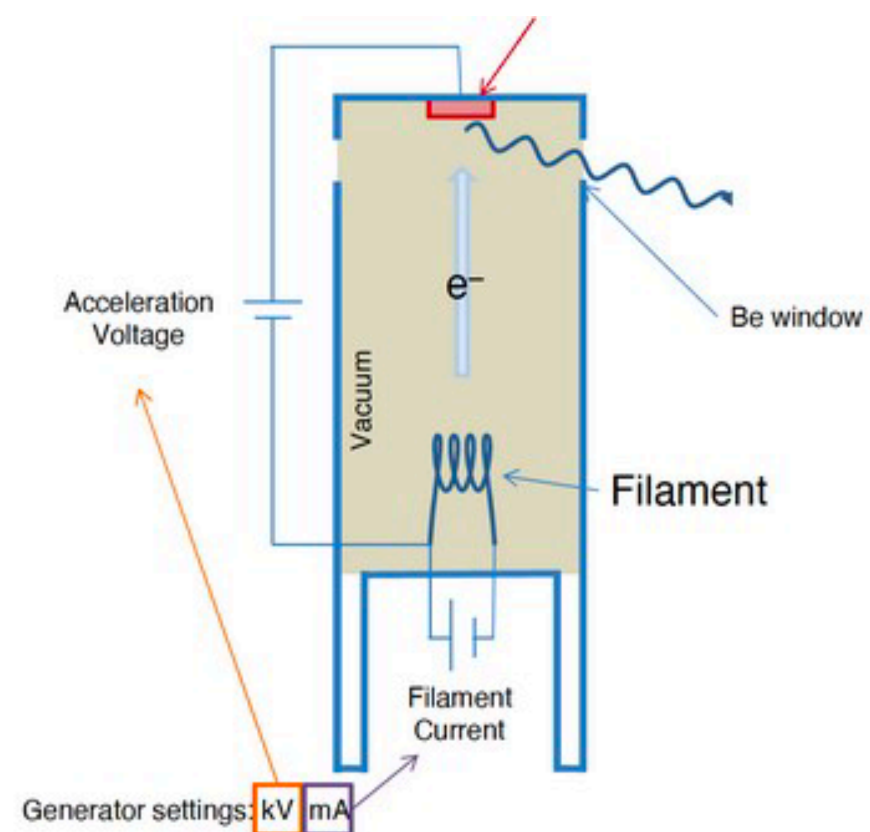
Faults by categories

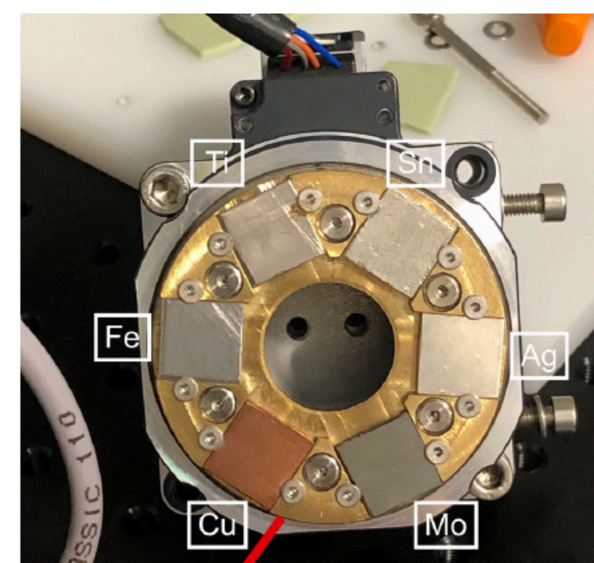


Laboratory part two



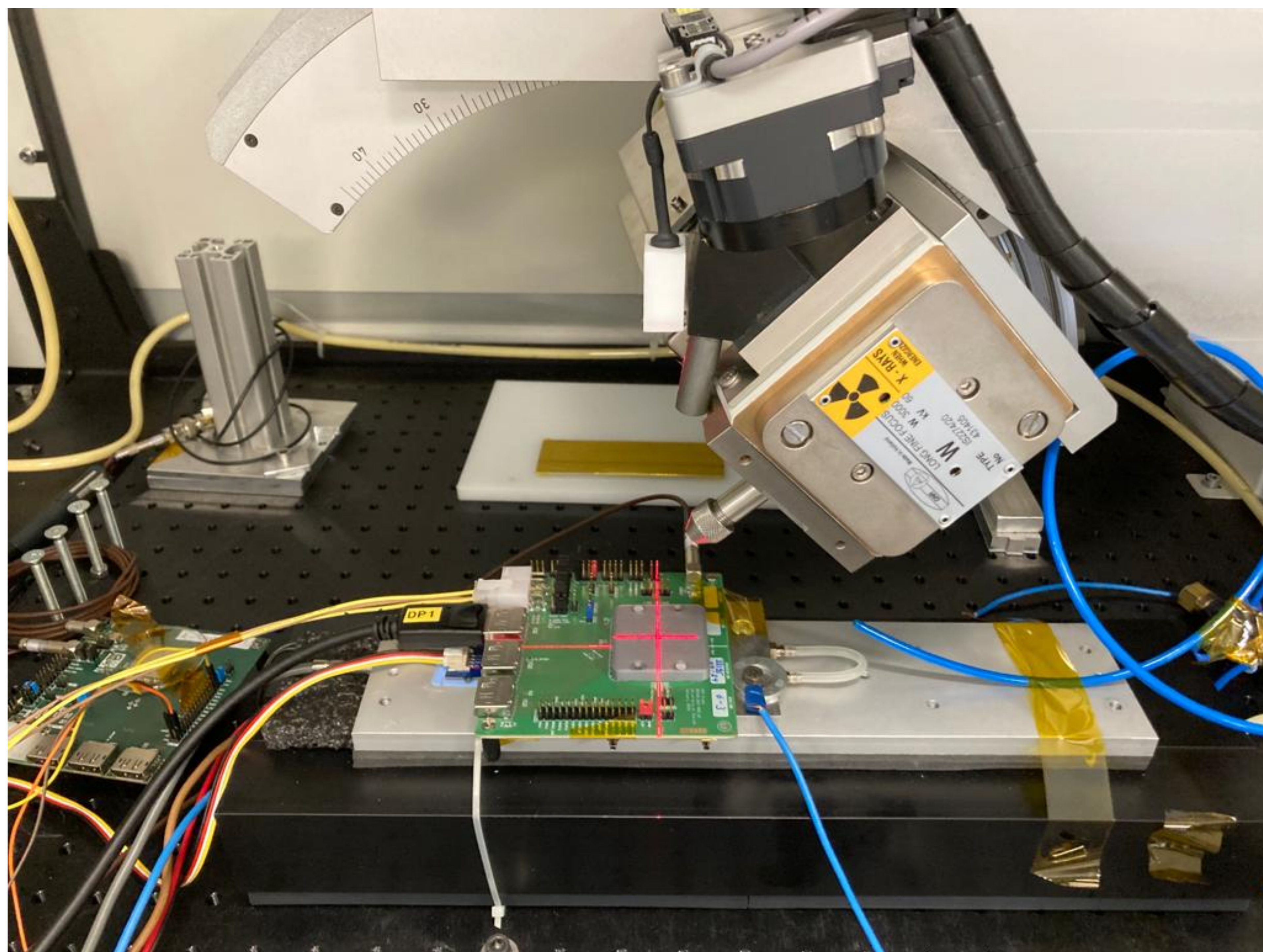


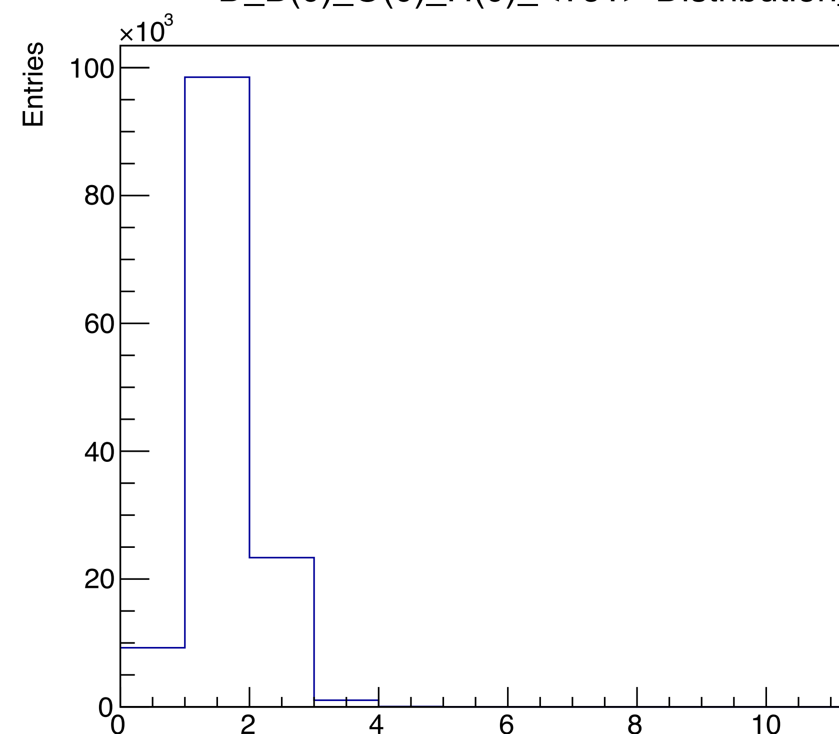


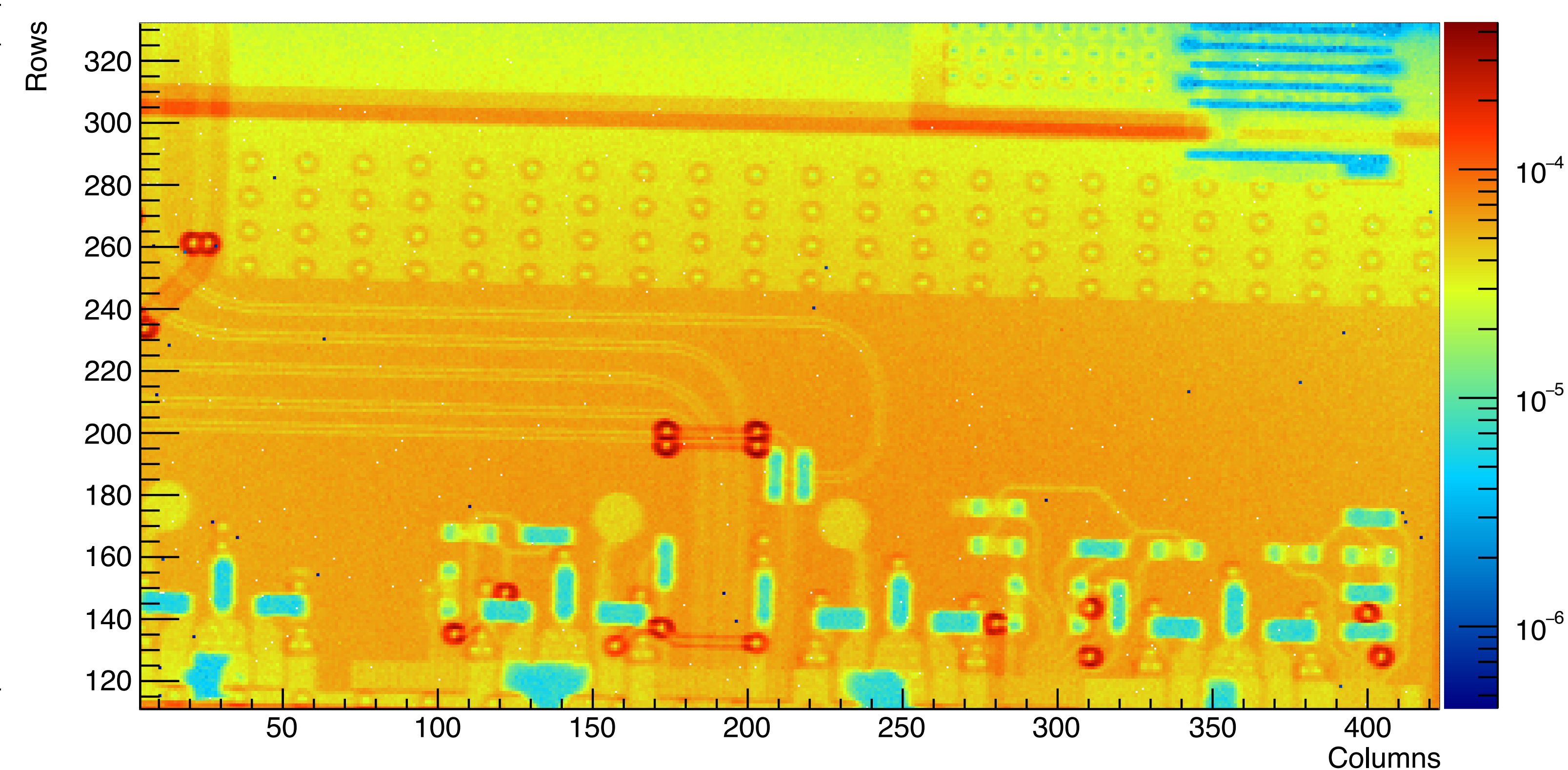


- You will use a Pixel detector with a C-ROC bump-bonded to a planar silicon sensor (cell of 50x50 um2)
- You will cross-check the performance: low silicon current, low threshold, of 1000 electrons; low noise; looking to the S-curve obtained with an calibration injection ==> root files with 1D/2D histograms
- With the help of an expert, you will send real external signal using an x-ray machine (fully screened, validated by radio-protection) :
  - check of good connection / efficiency of CROC + sensor
  - measurement of energy sent by fluorecence light obtained by x-ray to 5 different targets (Ag, Fe, Cu, Mo, Sn)
  - eventually you will be using the detector to make a real x-ray of a part of the CMS Pixel detector (hybrid)

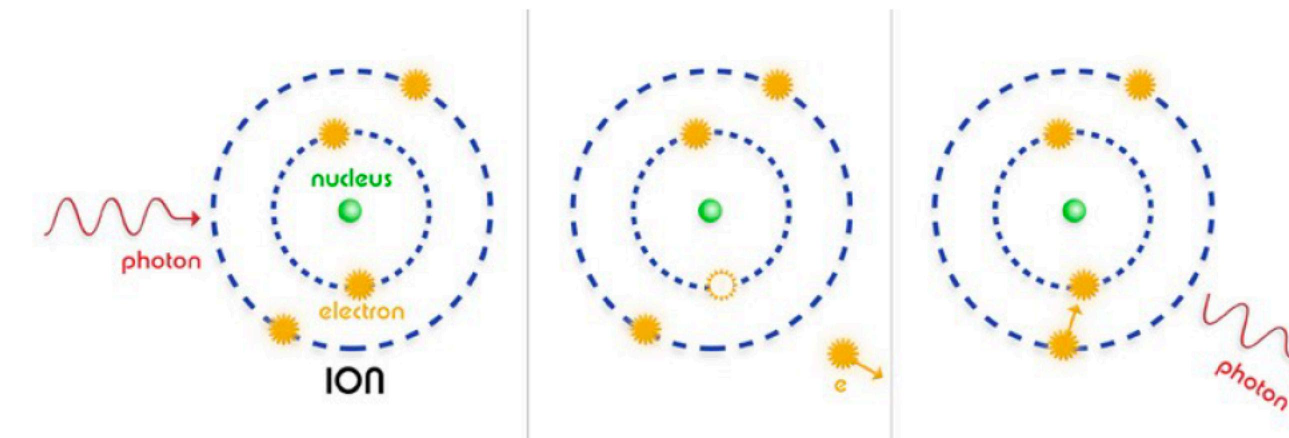
Testing pixel detector with an X-ray machine







Fluorescence emission



	keV			
	kalpha1	kbeta1	La1	Lb1
Cu	8.048	8.905		
Mo	17.479	19.602	2.293	2.395
Ag	22.163	24.942	2.984	3.151
Sn	25.271	28.486	3.443	3.663
Fe	6.403	7.057	0.705	0.718
Ti	4.511	4.932	0.452	0.458
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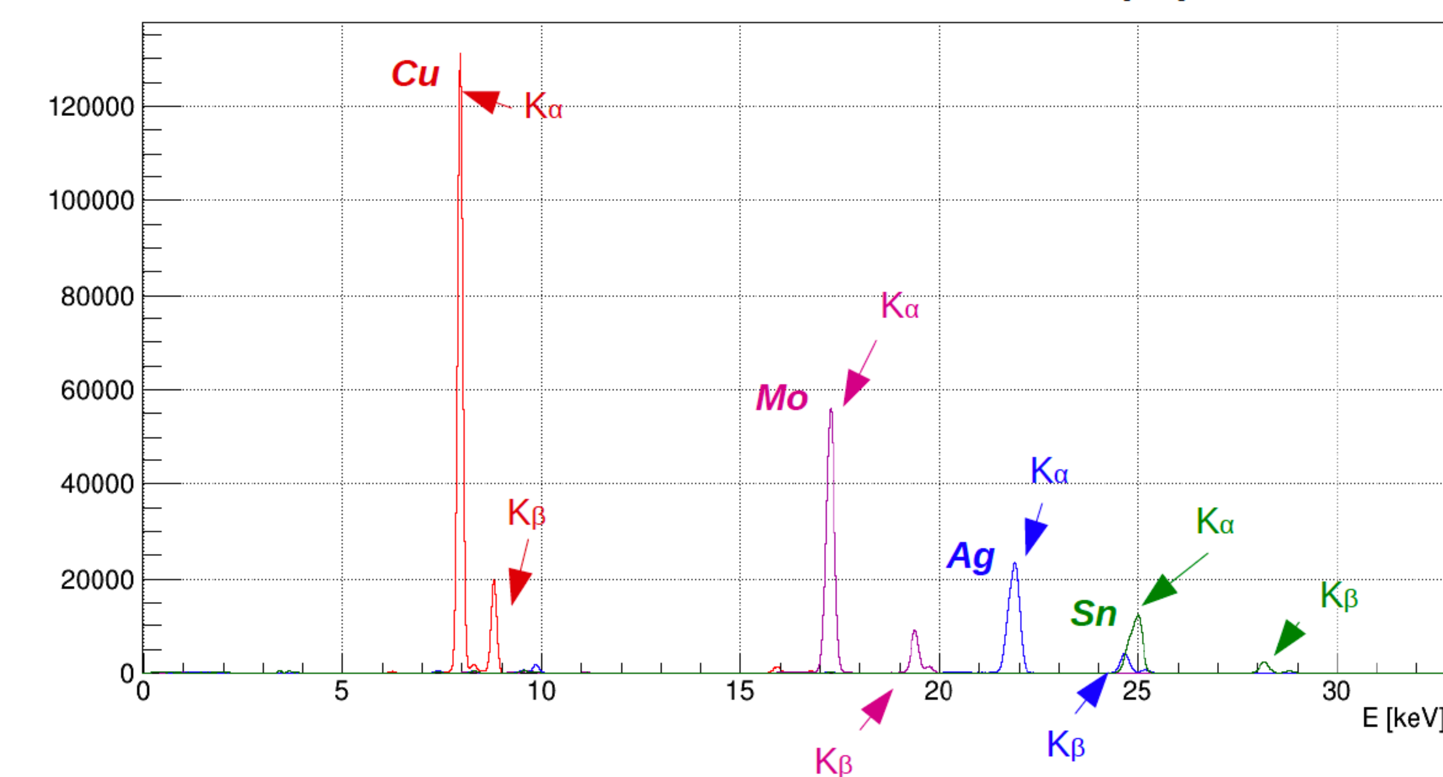
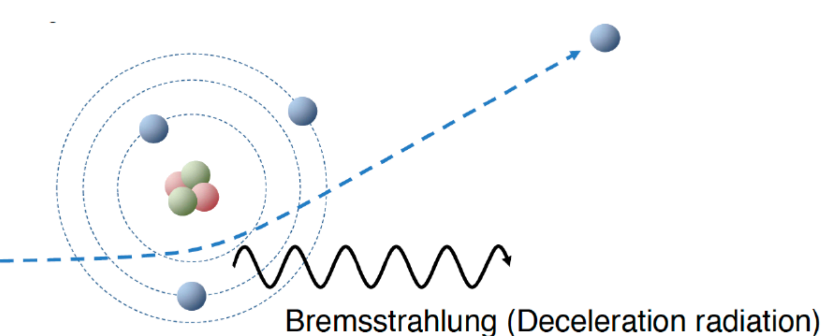


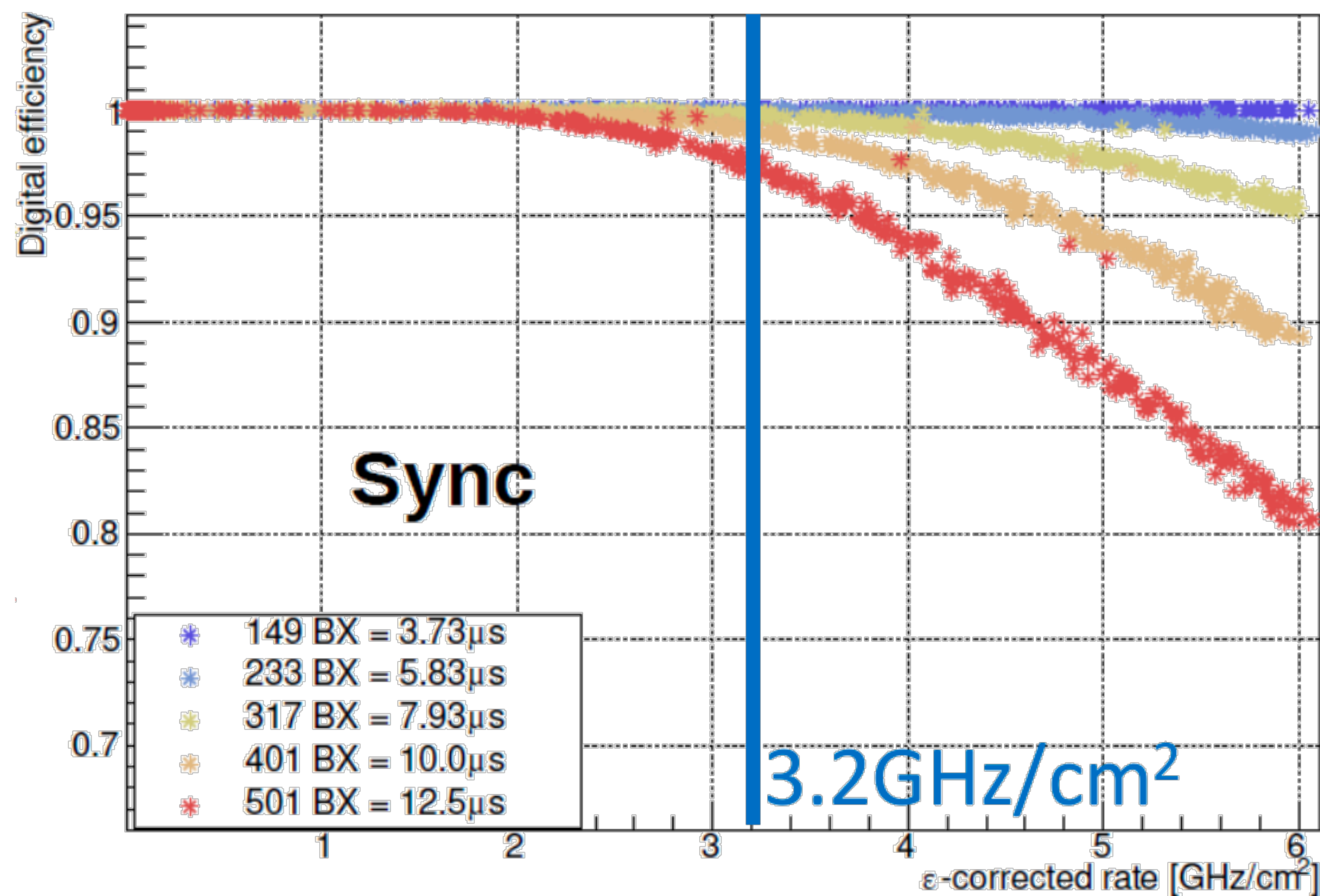
Primary beam

- up to 50kV, 50 mA
- high single pixel rate, to test for HL_LHC fluxes (>3 GHz/cm^2)

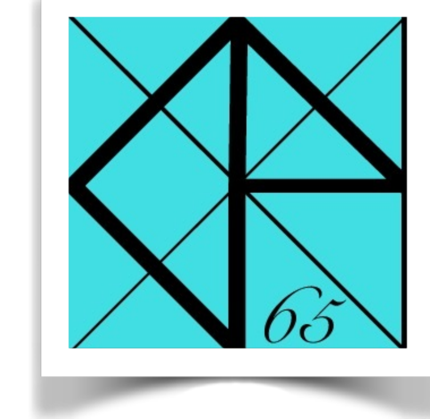


Backup

High rates with X-ray machine



Advantage of technology scaling



Lot of digital logic in the pixel-matrix, organised in pixel regions:
enough space ? Is power going to explode ?

Moving to more scaled technology - from **130nm to 65nm** (relative scaling alpha=2)**,** digital follows:

- **Logic density: x4**
  - both W and L are reduced
- **Power : ~1/2 - 1/4**
  - related to clocked operations, therefore follows

    P = freq C V² (charge/disch. cap)

    where C is the capacitance to be driven, sum of MOS gate capacitance and metal routing.

    C_gate decreases: W,L decrease; Cox increase,
    Metal routing capacitance decreases (width)
- **Speed: ~2**
  - faster electronics, higher frequency reachable