Understanding performance of analog-to-digital converters for radiation detector systems

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Outline

- Basic concepts on data conversion - a reminder
- Main ADC architectures
- Test of high performances ADC
- Case study

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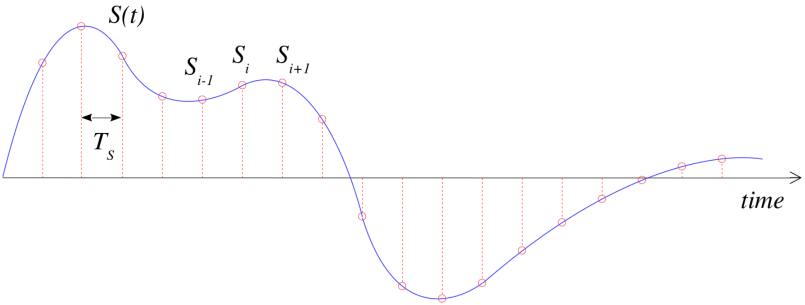
Motivations

- Detector outputs are typically analog signals
  → *however, they are processed digitally*
- A/D conversion is a critical processing step :
  - Several ADC architectures
  - Sampling frequency vs resolution trade-off
  - Converter maximum input frequency
  - Several ADC metrics *(INL, DNL, ENOB, SNR, SFDR, SNDR, ...)*
  - ADC complexity increases exponentially with resolution
- No "one fits all" solution
- Many ADCs concepts apply to TDCs as well

Analog-to-digital conversion

- Analog signals :
  - Infinite number of values in time (in a specific time range)
  - Infinite number of values in amplitude (in a specific amplitude range)
  - "Real life signals"
- Digital signals :
  - Finite number of values in time.
  - Finite number of values in amplitude.
  - Numerical representation of real life signals.
- Converting from analog to digital requires taking a limited number of samples of the signal with a limited amplitude resolution :
  - Time conversion $\rightarrow$ sampling
  - Amplitude conversion $\rightarrow$ quantization

Sampling



$$F_S = \frac{1}{T_S}$$

Sampling theorem

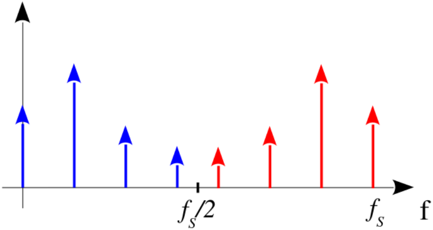
Question : what is the minimum sampling frequency F_S required to correctly represent a given signal ?
Answer *(Sampling theorem)* : for a signal with limited bandwidth B the minimum sampling frequency is given by :

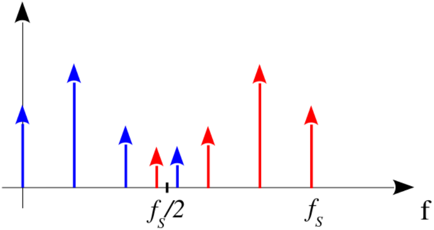
$$F_S = 2 \times B$$

$\frac{F_S}{2}$ is called the Nyqvist frequency of the converter.

Important : the Nyqvist frequency is a theoretical limit !

Aliasing





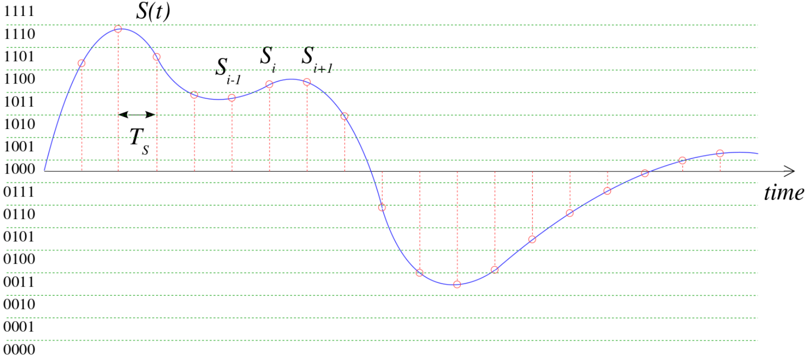
- The signal bandwidth must not exceed the $\frac{F_S}{2}$ limit
- Higher frequencies are mirrored on the baseband at different frequencies

- This is also true for disturbances entering in the ADC at the sampling switch

Quantization

For a converter with N bits and input range FS the quantization error (or quantization noise) is

$$Q_E = FS/2^N \qquad \sigma = FS/(\sqrt{12} \times 2^N)$$

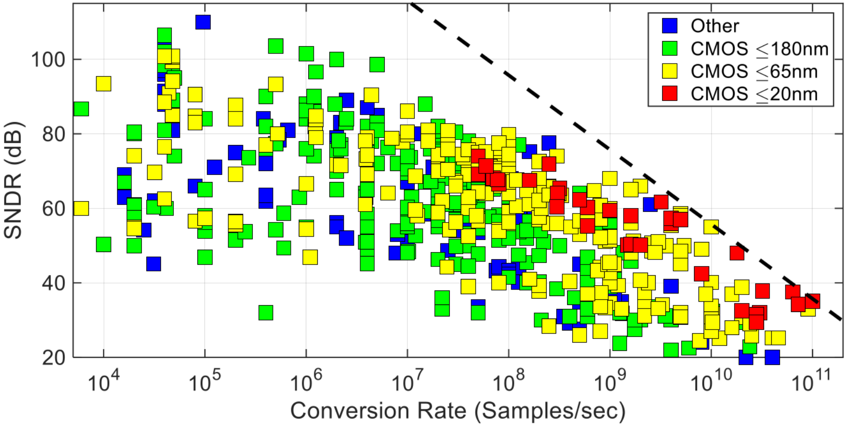


Power supply voltage and LSB

Modern CMOS technologies work with low power supply → ADC maximum full scale is reduced accordingly

Resolution	Voltage levels	LSB (4 V FS)	LSB (1 V FS)
2	4	1 V	250 mV
4	16	250 mV	62.5 mV
8	256	15.6 mV	3.9 mV
10	1024	3.91 mV	976.6 μV
12	4096	976 μV	244.1 μV
16	65536	61.0 μV	15.3 μV
24	16777216	238 nV	59.6 nV

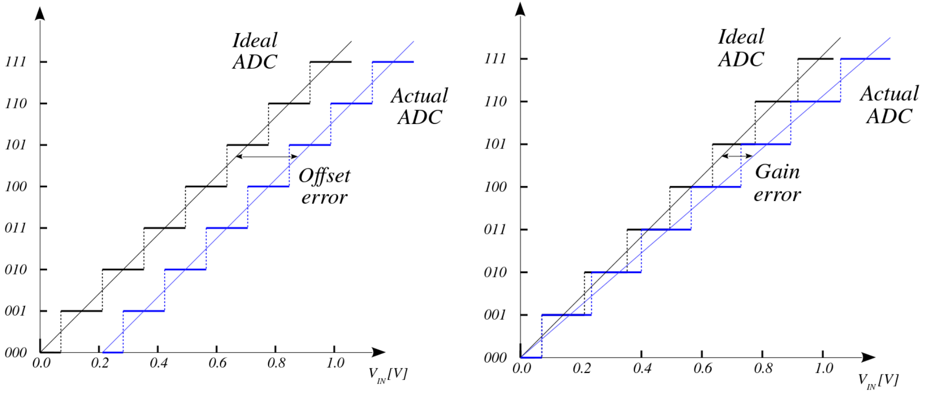
ADC performances vs process node



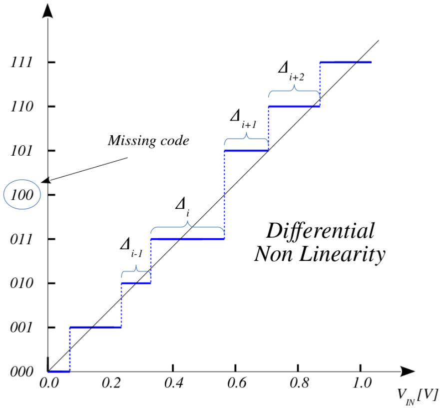
$$SNDR = 6.02 \times N + 1.78$$

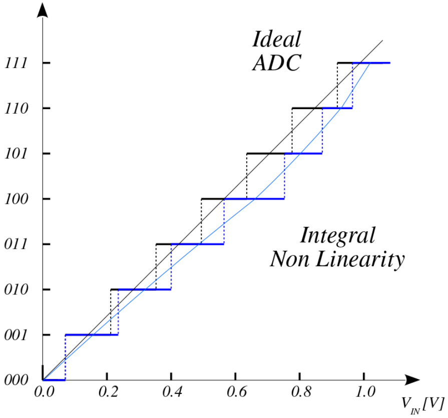
B. Murmann, "ADC Performance Survey 1997-2023," [Available Online]

Errors in data conversion : offset and gain



Errors in data conversion : INL and DNL





$$DNL(i) = \Delta_i - 1\ LSB$$

$$INL(i) = \sum_{j=0}^{i} DNL_j$$

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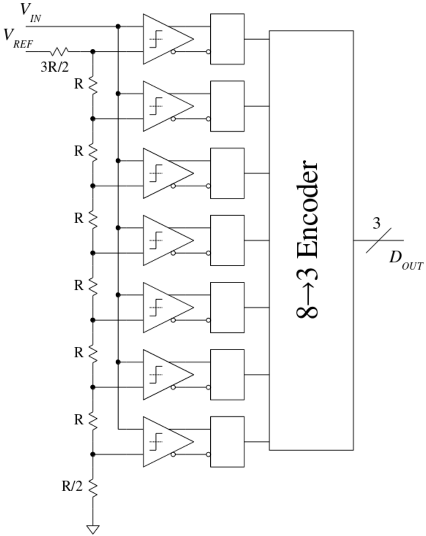
Main ADC architectures

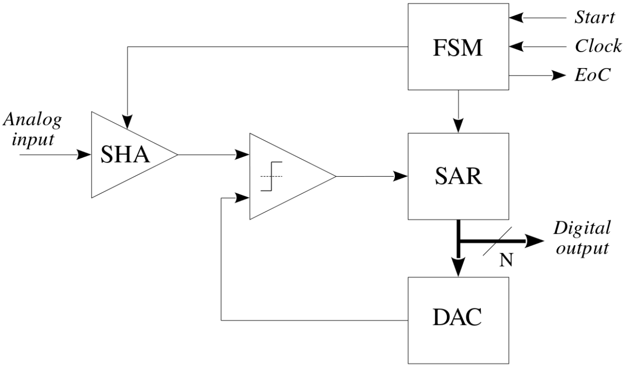
- Parallel converters
- Successive approximation converters
- Single and double ramp converters
- Δ-Σ converters
- Mixed techniques :
  - Dual stage converters
  - Pipelined converters
  - Time interleaved converters

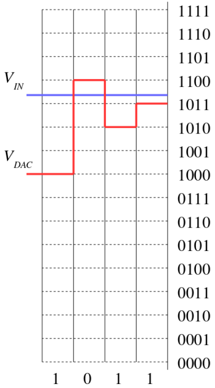
Parallel (flash) converter



- Very fast : single step conversion
- Requires 2^N-1 (or +1) comparators
- Thermometric encoding
- Intrinsecally monotonic ? *Not necessarily*
- S/H non required ? *Only at low signal frequencies*
- Typically limited to $<$ 8 bits

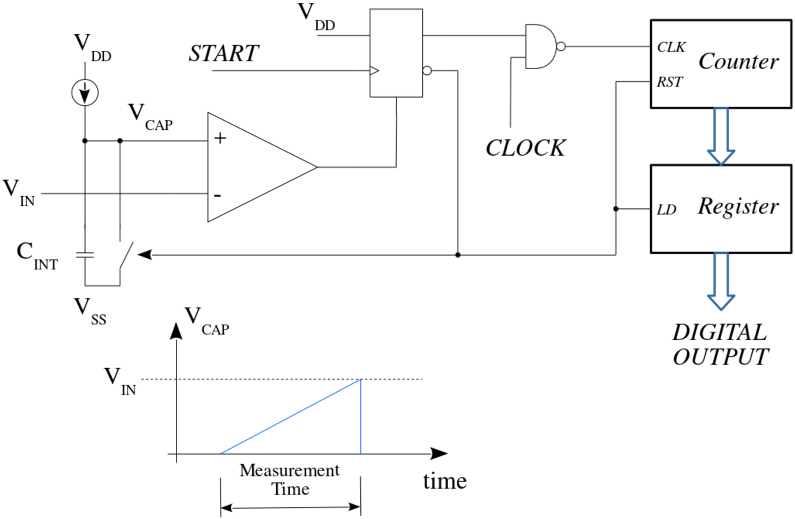
Successive approximation converter





- Conversion time : $T_S + N \times T_{CK}$
- Requires 1 comparator and 1 N-bits DAC
- Binary encoding
- Strong dependence on the DAC quality
- Typical resolution 8-12 bits

Single slope converters



Single slope converter main points

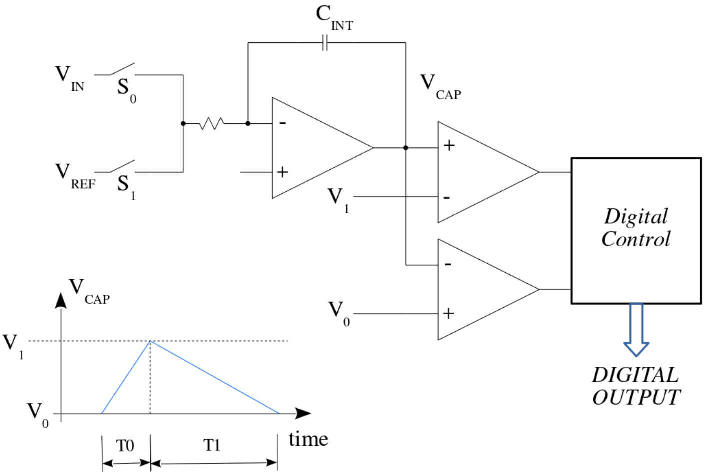
- Signal dependent conversion time :

$$T_C = T_S + \frac{C \ V_{IN}}{I}$$

- Max conversion time : $\mathrm{T_S} + 2^{\mathrm{N}} \times \mathrm{T_{CK}}$
- Very simple : requires 1 comparator and 1 precise integrator
- Binary encoding
- Depends on C and I absolute values
  - Calibration is mandatory in multi-channel systems
- High resolution, low sampling rate

$\rightarrow$ *Can be very interesting in HEP applications where most samples are baseline ones*

Dual slope converters



$$\frac{V_{IN}\ T_0}{RC_{INT}} = \frac{V_{REF}\ T_1}{RC_{INT}}$$

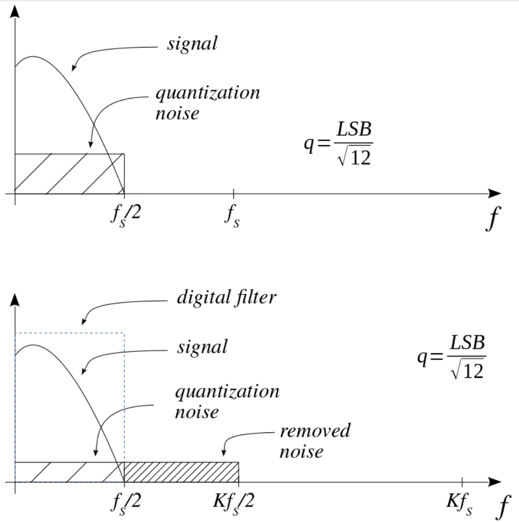
$$V_{IN} = V_{REF}\ \frac{T_1}{T_0}$$

Dual slope converter main points

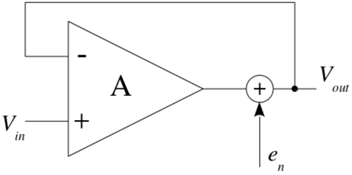
- Signal dependent conversion time
- Max conversion time : $T_S + 2^{N+1} \times T_{CK}$
- Very simple : requires 1 comparator and 1 precise integrator
- Binary encoding
- Independent from C and R absolute values
- High resolution, low sampling rate

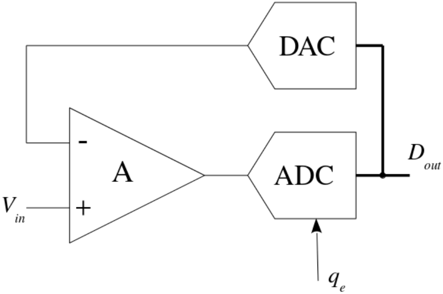
Oversampling

- Noise power is constant and distributed from 0 to $\frac{f_S}{2}$
- By oversampling and digitally filter the output part of the quantization noise can be removed
- The number of samples can be then reduced to f_S (decimation)
- K = 2 → 3 dB gain
- K = 4 → 6 dB gain *(1 bit)*



Noise shaping

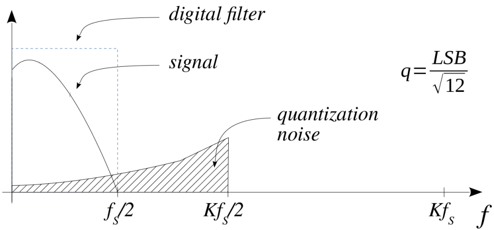


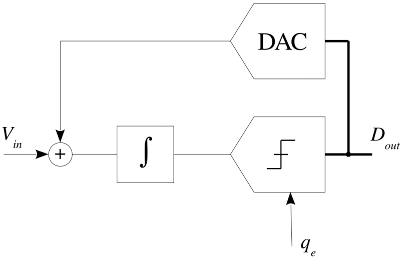


$$V_{out} = \frac{A}{1+A} V_{in} + \frac{1}{1+A} e_n$$

- Continuous system : noise reduced by the open loop gain
- Discrete system : stable loop for A<1 only
- A<1 required for high frequency only $\rightarrow$ an integrator can be added to the loop

$\Delta - \Sigma$ converter

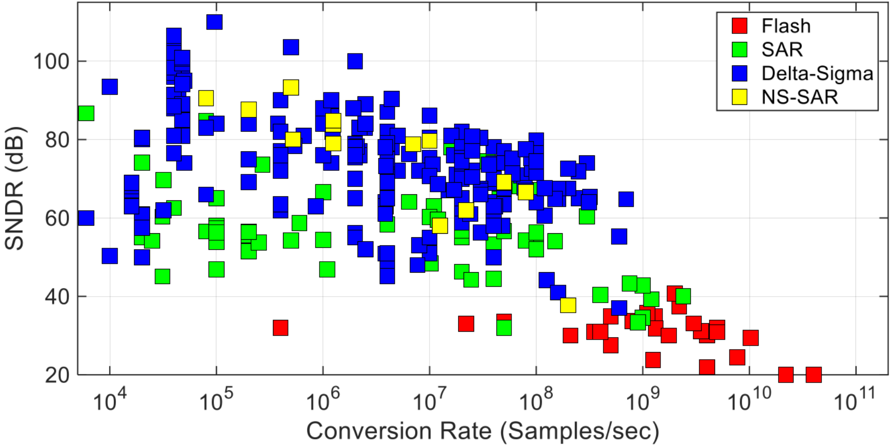




- First-order $\Delta - \Sigma$ converter
- K=2 oversampling ratio $\rightarrow$ 6 dB noise reduction

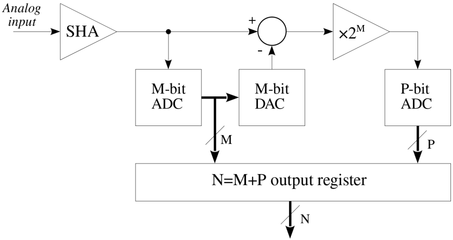
- High order further improves noise shaping
- Typically orders above 2 are difficult to compensate

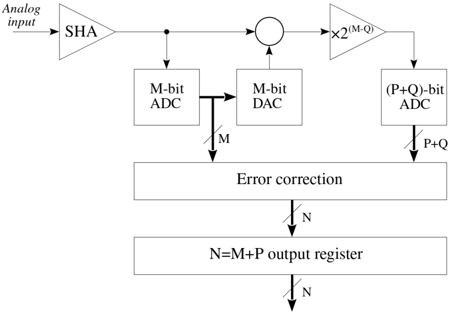
Comparison between architectures - 1



B. Murmann, "ADC Performance Survey 1997-2023," [Available Online]

Two-stages converter

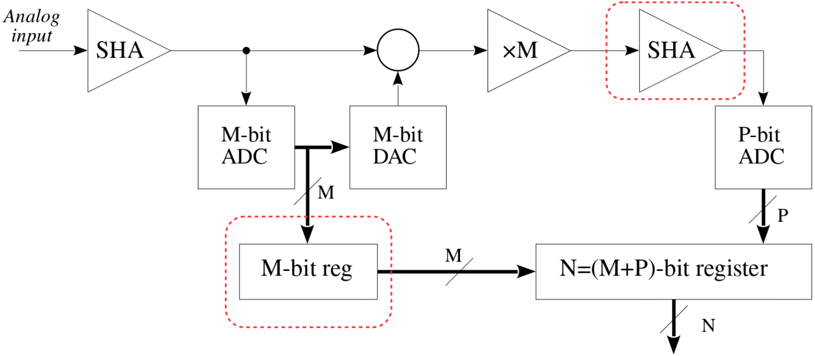




- Conversion performed in two phases
- First ADC INL and DNL must be at N-bit level
- Residue amplifier design critical

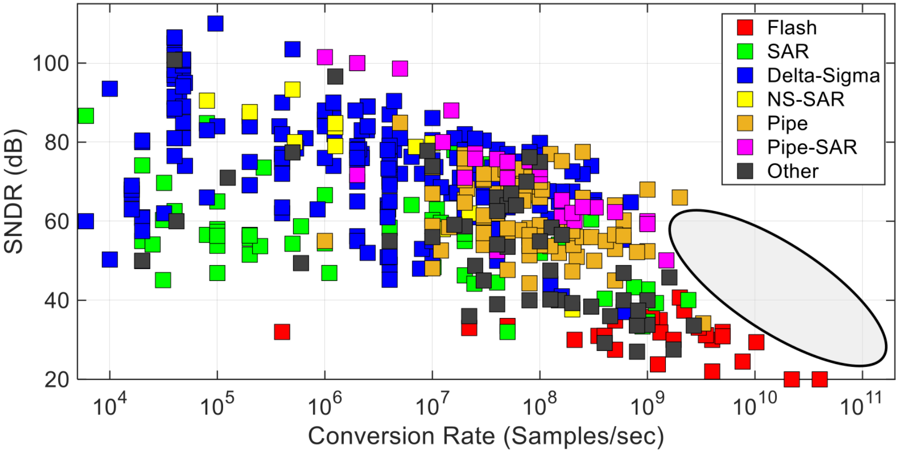
- Q-bit redundancy can be added

Pipeline converter



- With an extra S/H the two phases can be superimposed
- Max sampling rate is equal to the slowest of the two ADCs
- A latency is introduced
- Error correction techniques are usually implemented

Comparison between architectures - 2



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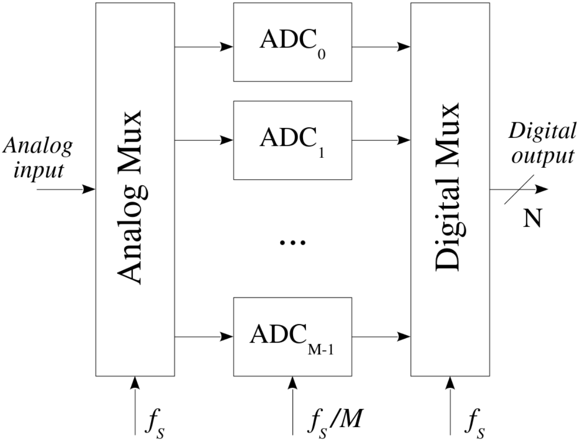
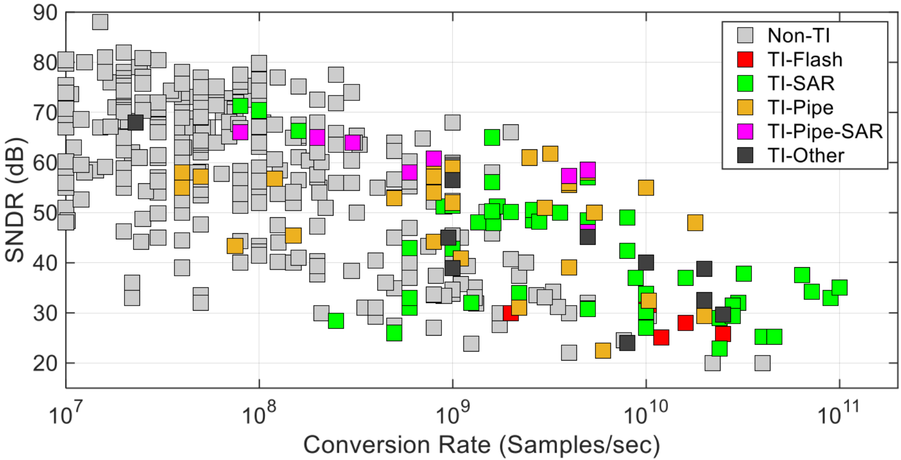
Time interleaved converters



- Widely used in DSO
- Analog mux performances critical
- ADC intercalibration required

Comparison between architectures - 3



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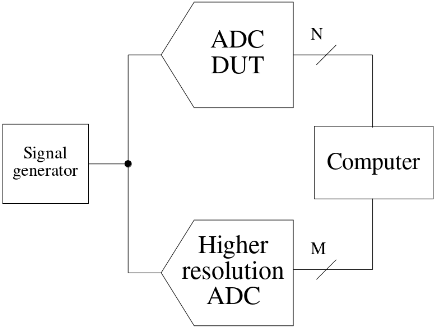
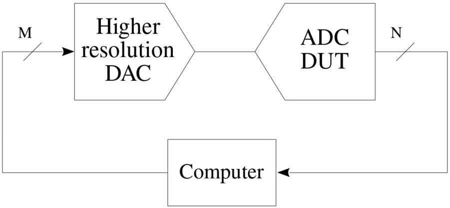
Test with a higher resolution ADC



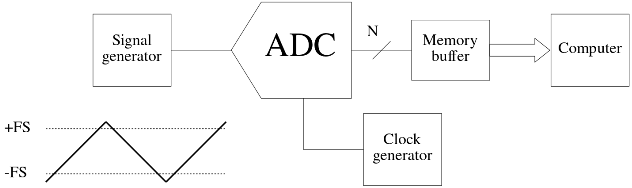
- Input signal split to the DUT and a reference ADC
- Reference ADC resolution : M $\geq N + 2$
- Requires a much better ADC for full speed testing
- Requires a proper input signal: must cover all codes

Test with a higher resolution DAC



- Input signal provided by a reference DAC - no need of a precise signal soruce
- Reference DAC resolution : $\geq N + 2$
- DAC performances are typically better than ADC ones

Histogram (Code Density) Test



- Collect M_T total samples for codes 1 to $2^N - 2$
- Count number of occurrences of each code, $h(n)_{ACTUAL}$
- The theoretical number of occurrences is :

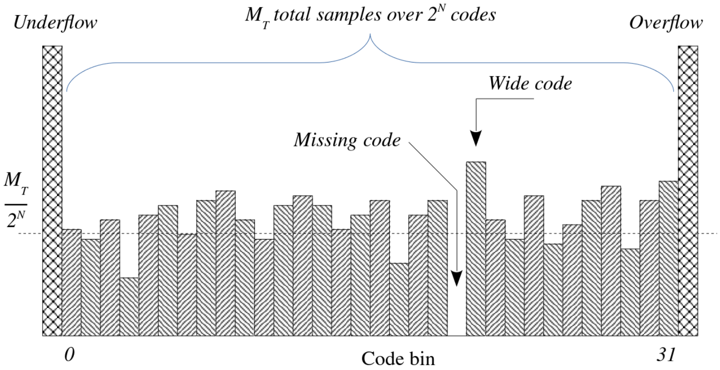
$$h(n)_{THEOR} = \frac{M_T}{2^N - 2}$$

- Calculate DNL of each code as :

$$DNL(n) = \frac{h(n)_{ACTUAL}}{h(n)_{THEOR}} - 1$$

- Integrate DNL to obtain INL

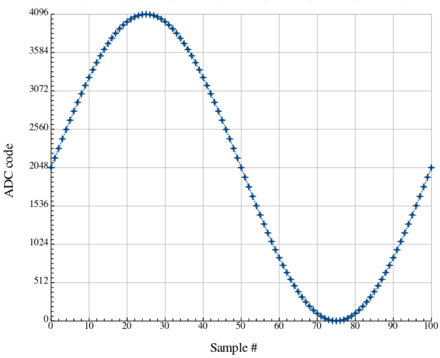
Histogram for Linear Ramp Test

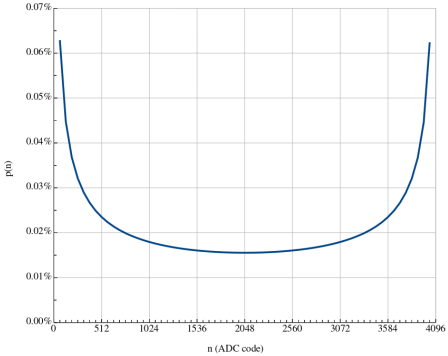


Practical considerations

- Number of samples :
  - With M hits per code bin, DNL resolution is 1/M
  - For a N-bits ADC, $M_T = 2^N \times M$
  - Example : 8 bits, 50 MS/s, M = 20 (5% error on LSB) : M_T=5120, $T_{measure}$=102.4 μs
  - Example : 12 bits, 1 MS/s, M = 20 (5% error on LSB) : M_T=81920, $T_{measure}$=81.92 ms
- For high performances ADCs is very difficult to generate a ramp with the required performances → A sinewave is normally used
  - High quality passive filters to improve the signal
  - Code distribution is not constant anymore
- Important : frequency of the input wave must not be a sub-harmonic of the ADC sampling clock

Histogram for Sinewave Test

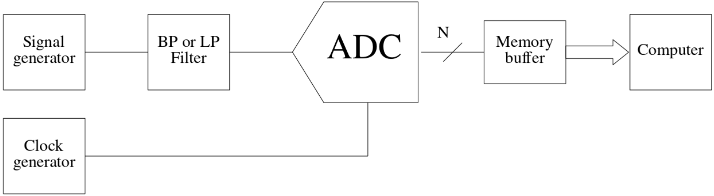




$$V_{IN} = A\ sin(\omega t)$$

$$p(n) = \frac{1}{\pi}\left\{sin^{-1}\left[\frac{V_{FS}(n-2^{N-1})}{A\cdot 2^N}\right] - sin^{-1}\left[\frac{V_{FS}(n-1-2^{N-1})}{A\cdot 2^N}\right]\right\}$$

Sinewave Test setup



- Key points :
  - Input signal specs
  - Clock specs
  - Data transmission

Methodology for ADC characterisation

- Histogram method :
  - The ADC codes distribution is obtained by non-coherently sampling the sinewave input
  - From this distribution, the transition voltages can be derived, and with them the DNL, INL and missing codes
- FFT method :
  - The Fast Fourier Transform of the signal is computed.
  - ENOB, SNDR, SFDR and other noise-related parameters in the frequency domain can be measured
- Fit method :
  - A 4 parameters sinewave fit is applied to the ADC samples
  - The fit-sample residuals distribution is reconstructed and used to calculate the noise-related parameters ENOB and SNDR

Sinewave Test calculations

$$V_O = \frac{\pi}{2} sin \frac{N_P - N_N}{N_T}$$

$$CH(i) = \sum_{j=0}^{i} H(j)$$

$$V(i) = cos\left(\frac{\pi CH(i)}{N_T}\right)$$

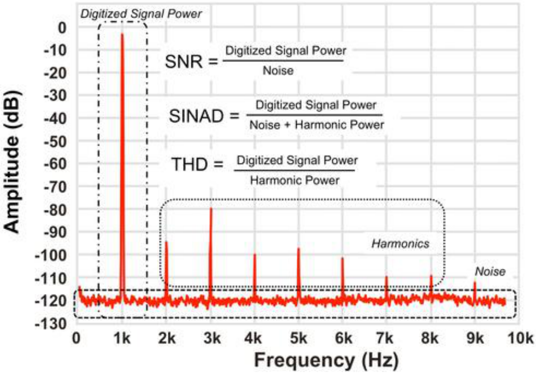
$$INL(i) = \frac{V(i) - V(1)}{1\ LSB} - (i - 1)$$

$$DNL(i) = \frac{V(i+1) - V(i)}{1\ LSB}$$

- N_P, N_N : number of samples above/below midrange
- $N_T = N_P + N_N$
- V_O : offset voltage

Reference : *J. Doenberger et al.*
Full-Speed Testing of A/D Converters
IEEE J. Solid-State Circuits, vol 19, n. 6, Dec 1984

ENOB measurement - from FFT



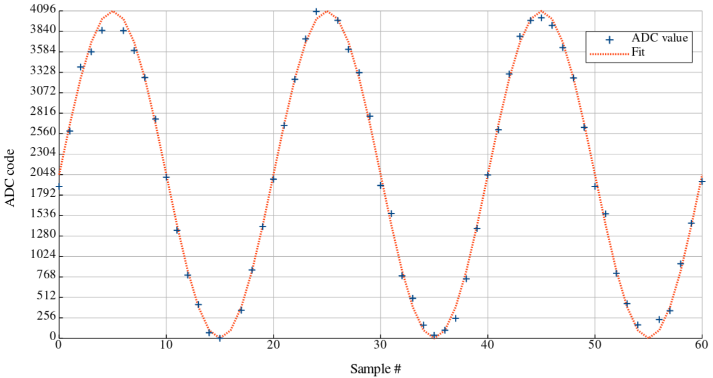
- SNDR or SINAD : Signal to Noise and Distorsion Ratio
- SNR : Signal to Noise Ratio
- ENOB : Effective Number of Bits

$$ENOB = \frac{SNDR - 1.78dB}{6.02}$$

- THD : Total Harmonic Distorsion

ENOB	SNDR	ENOB	SNDR	ENOB	SNDR
4 b	25.86 dB	8 b	49.94 dB	12 b	74.02 dB
6 b	37.90 dB	10 b	61.98 dB	16 b	98.10 dB

ENOB measurement - from fit



$$ND = \sqrt{\frac{1}{M}\sum_{n=1}^{M}(x[n] - x'[n])^2}$$

$$SNDR = \frac{A_{rms}}{ND} = \frac{A_p}{ND\sqrt{2}}$$

$x[n]$: *sample data set*

$x^{'}[n]$: *best fit data set*

M : *number of samples*

Relations between INL, DNL, SFDR and SNR

INL and SFDR

- Type of distortion depend on the INL shape
- Rule of thumb

$$SFDR = 20log\left(\frac{2^N}{INL}\right)$$

DNL and SNR
Assuming:

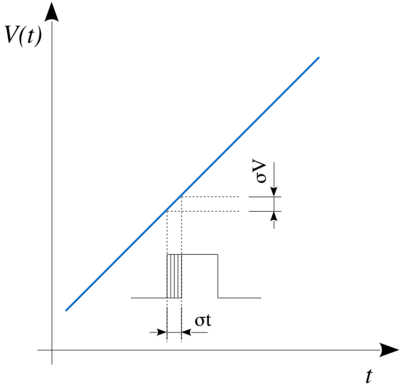
- Uniform DNL distribution
- No missing codes

$$SNR = \frac{\frac{1}{2}\left(\frac{2^N LSB}{2}\right)^2}{\frac{LSB^2}{12} + \frac{DNL^2}{3}}$$

Please do not forget that...

- A converter does not just have one input pin but also :
  - Clock
  - Power supply and ground
  - Reference Voltage
- For good practices on how to avoid issues see e.g.:
  - Analog Devices Application Note 345: *Grounding for Low-and-High-Frequency Circuits*
  - Maxim Application Note 729: *Dynamic Testing of High-Speed ADCs*
- More details in:
  - IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters - *IEEE Std 1241^{TM} - 2010*

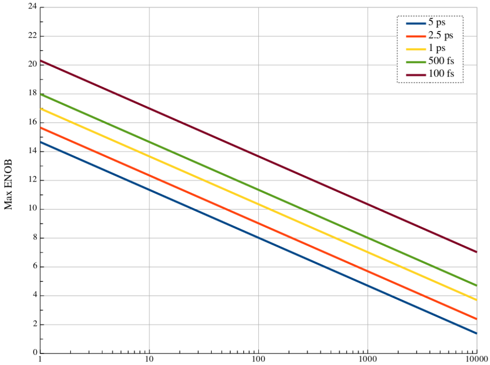
Effects of jitter on the sampling clock



Jitter on the sampling clock adds an error voltage proportional to the product between the time jitter and the input signal slope

$$\sigma_V = \sigma_T \frac{\Delta V}{\Delta t}$$

Maximum SNR *vs* input frequency



$$SNR_{max} = 20 log_{10}\left(\frac{1}{2\pi f_{sig} t_j}\right)$$

$$ENOB_{max} = \frac{SNR_{max} - 1.76}{6.02}$$

f_{sig} : *signal frequency*

t_j : *r.m.s. jitter*

N : *number of bits*

- Note 1 : here we have the **signal** (not the **sampling**) frequency
- Note 2 : this is a worst case. Typical signals have a frequency spectra

How to readout the bits

- Full swing CMOS signaling works well for f_{CLK} <100MHz. For higher frequencies:
  - Uncontrolled characteristic impedance
  - High swing $\rightarrow$ higher level of spurious coupling to other signals
  - High power consumption
- Alternative to CMOS: LVDS (Low Voltage Differential Signaling)
- LVDS *vs* CMOS:
  - Higher speed, more power efficient at high speed
  - Two pins/bit

Typical ADC metrics

1. Gain error : difference between the expected and actual slope of the transfer function
2. Offset error : difference between the expected and actual intercept of the transfer function
3. DNL (Differential Non-Linearity) : difference between an actual step width and the ideal value of 1 LSB.
4. INL (Integral Non-Linearity) : deviation of the values on the actual transfer function from the ideal linear fit.
5. SNDR or SINAD (Signal to Noise and Distorsion Ratio) : ratio of the rms signal amplitude to the mean value of the root sum square of the other spectral components, excluding DC.
6. SNR (Signal to Noise Ratio) : the same as SNDR but without signal harmonics
7. ENOB (Effective Number Of Bits) : equivalent to SNDR.
8. SFDR (Spurious Free Dynamic Range) : ratio between the rms signal amplitude to the rms amplitude of the highest harmonic.
9. THD (Total Harmonic Distorsion) : ratio between the rms value of the signal amplitude to the mean value of the root sum square of its harmonics.

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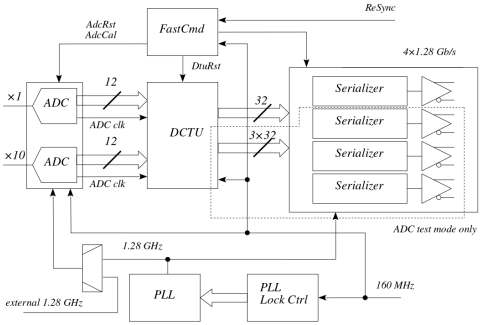
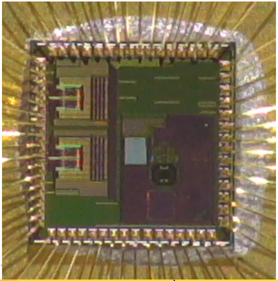
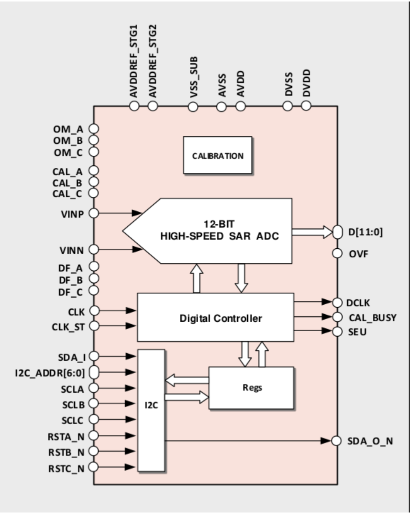
Case study : LiTE-DTU - Data Conversion, Compression and Transmission ASIC for the CMS ECAL



- Data Compression and Transmission Unit
- Fast command and lock control units
- 1.28 Gb/s serializers

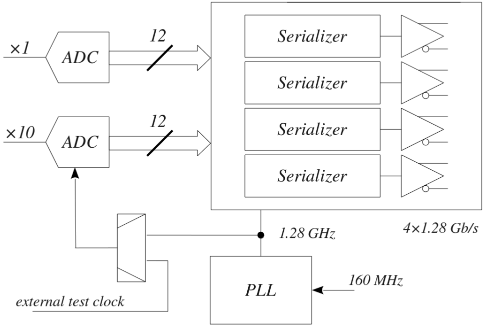
- Two 12 bits, 160 MS/s ADCs
- Clock multiplication PLLs
- I^{2}C interface for slow control (*not shown*)
- Technology : CMOS 65 nm





- Designed by Dialog Semiconductor
- 12 bits, 160 Mb/s
- Two 80 MS/s cores in time interleaving
- Cores based on the successive approximation technique
- Foreground calibration, calibration time 167.3 μs
- Working frequency 1.28 GHz
- Sampling frequency 160 MHz
- Triplicated digital control signals
- SEU-protected I^{2}C interface and registers
- ENOB $\geq$ 10.1
- Power $\leq$ 10.5 mW ($\sim$9 μW in power down mode)

ADC test mode

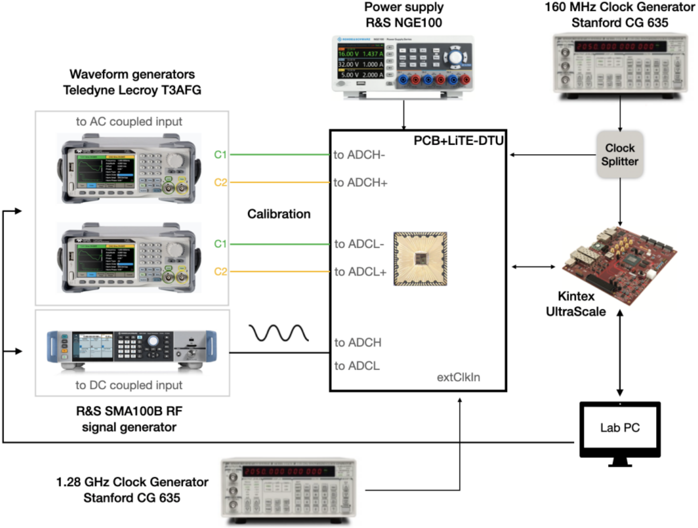


In ADC test mode :

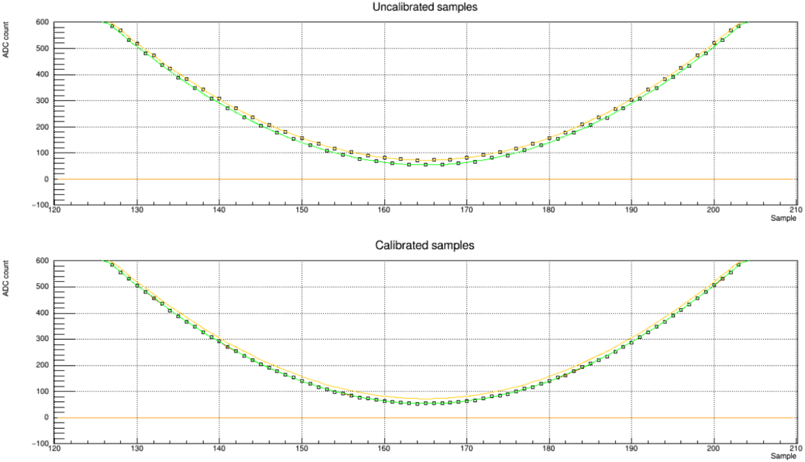
- bypass of the compression logic
- Four 1.28 Gb/s links active
- Samples packed in 32 bit words
- 4 bit patterns in fixed position to simply word alignment
- Allows independent test of ADCs
- Activated by the ATM CMOS input

Bits	31:28	27:16	15:12	11:0
Dout0	0011	ADC H (i+3)	1001	ADC H (i+1)
Dout1	0110	ADC H (i+2)	1100	ADC H (i)
Dout2	1100	ADC L (i+3)	0110	ADC L (i+1)
Dout3	1001	ADC L (i+2)	0011	ADC L (i)

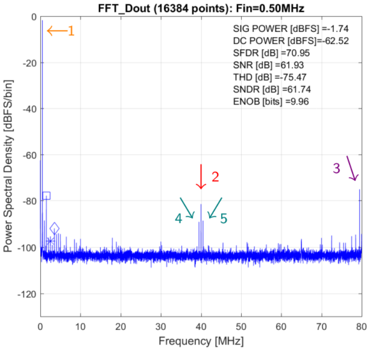
Test Set-up

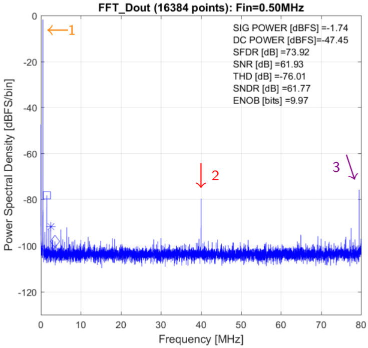

Power supply
R&S NGE100
160 MHz Clock Generator
Stanford CG 635
Waveform generators
Teledyne Lecroy T3AFG
to AC coupled input
C1
C2
C1
C2
PCB+LiTE-DTU
to ADCH-
to ADCH+
Calibration
to ADCL-
to ADCL+
to ADCH
to ADCL
extClkIn
Clock
Splitter
Kintex
UltraScale
to DC coupled input
R&S SMA100B RF
signal generator
Lab PC
1.28 GHz Clock Generator
Stanford CG 635

Interleaving errors



FFT - 500 kHz



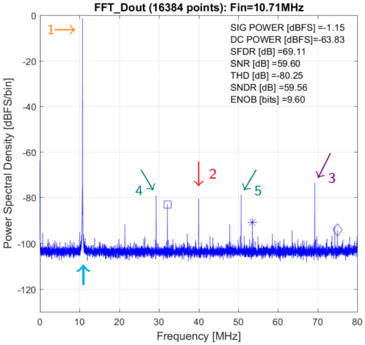


500 kHz FFT with internal clock

- 1: $f_{in} = 500\,\text{kHz}$
- 2: 40 MHz spurs
- 3: $f_S/2 \pm f_{in}$
- 4 and 5: 40 MHz $\pm f_{in}$

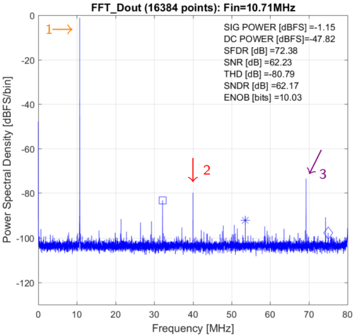
500 kHz FFT with external clock

- 1: $f_{in} = 500\,\text{kHz}$
- 2: 40 MHz spurs
- 3: $f_S/2 \pm f_{in}$



10.7 MHz FFT with internal clock

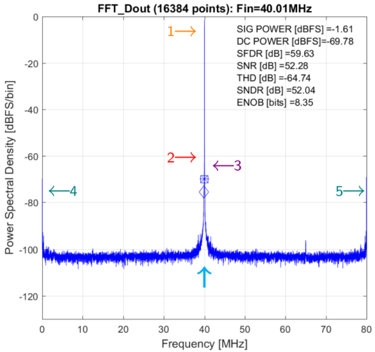
- **1**: f_{in} = 10.7 MHz
- **2**: 40 MHz spurs
- **3**: $f_S/2 \pm f_{in}$
- **4** and **5**: 40 MHz $\pm f_{in}$



10.7 MHz FFT with external clock

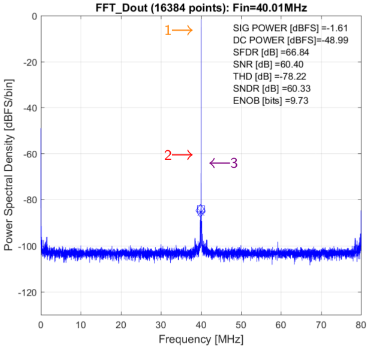
- **1**: f_{in} = 10.7 MHz
- **2**: 40 MHz spurs
- **3**: $f_S/2 \pm f_{in}$

FFT - 40 MHz



40 MHz FFT with internal clock

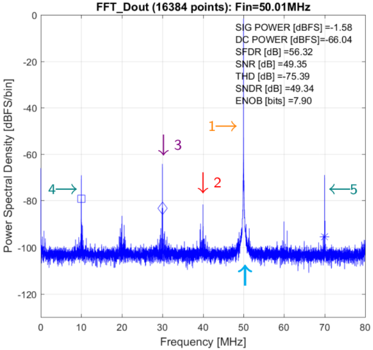
- **1**: $f_{in} = 40$ MHz
- **2**: 40 MHz spurs
- **3**: $f_S/2 \pm f_{in}$
- **4** and **5**: 40 MHz $\pm f_{in}$



40 MHz FFT with external clock

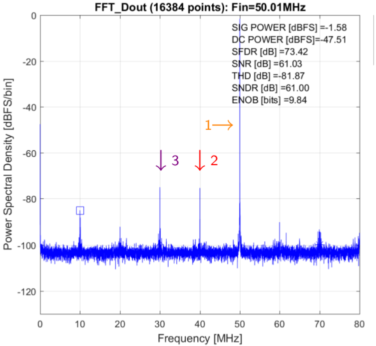
- **1**: $f_{in} = 40$ MHz
- **2**: 40 MHz spurs
- **3**: $f_S/2 \pm f_{in}$

FFT - 50 MHz



50 MHz FFT with internal clock

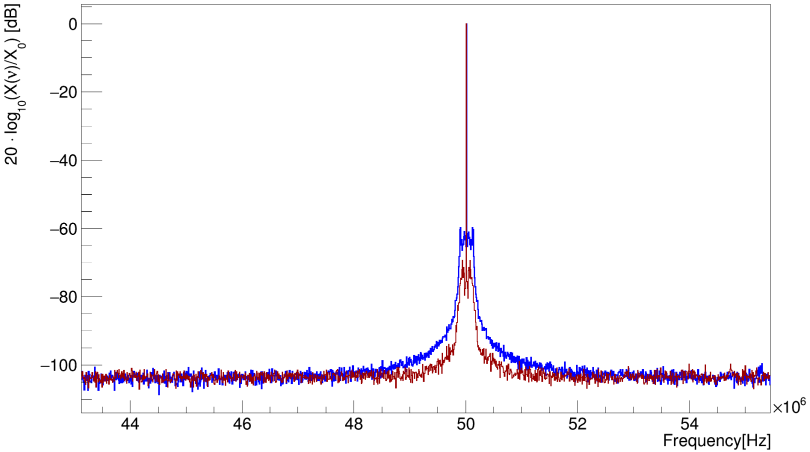
- 1: $f_{in} = 50$ MHz
- 2: 40 MHz spurs
- 3: $f_S/2 \pm f_{in}$
- 4 and 5: 40 MHz $\pm f_{in}$



50 MHz FFT with external clock

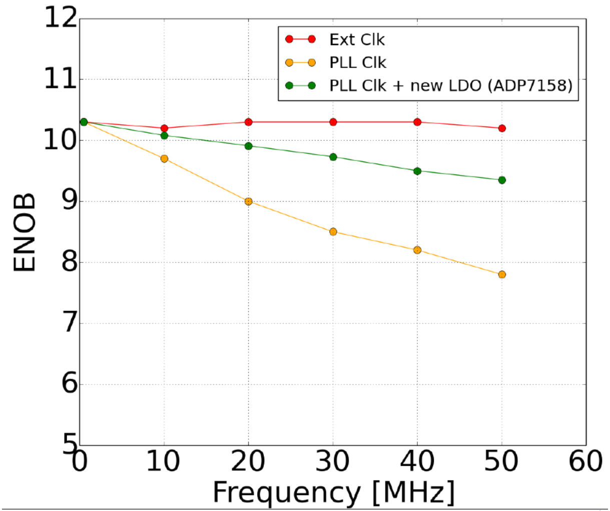
- 1: $f_{in} = 50$ MHz
- 2: 40 MHz spurs
- 3: $f_S/2 \pm f_{in}$

FFT @ 50 MHz : TPS78601 vs ADP7158



TPS78601 → blue curve, ADP715 → red curve

ADC test : ENOB vs F_{IN}



- Strong dependence on voltage regulator on PllVddRF

Conclusions

- High-performances A/D converters are an essential component of an integrated readout electronics
- In HEP experiments, calorimeters are typically the more demanding application for ADCs.
- Modern converters can provide both high resolution and high sampling frequencies
- Modern technologies are powered at $\sim$1 V voltages $\rightarrow$ LSB can in the μV range $\rightarrow$ noise is critical
- Clock jitter requirements can be very challenging to obtain

Bibliography

- *J. Doenberger et al.,* **Full-Speed Testing of A/D Converters**
  IEEE J. Solid-State Circuits, vol 19, n. 6, Dec 1984
- **Defining and Testing Dynamic Parameters in High- Speed ADCs**
  Maxim Tutorial 728
- **Dynamic Testing of High-Speed ADCs**
  Maxim Tutorial 729
- **IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters**
  IEEE Std 1241^{TM} - 2010