

VII Edition
SNRI2023

TORINO,
2023 OCTOBER
9th-13th



*Monolithic C-MOS sensors.
Quality control of light-weight tracking detectors.*



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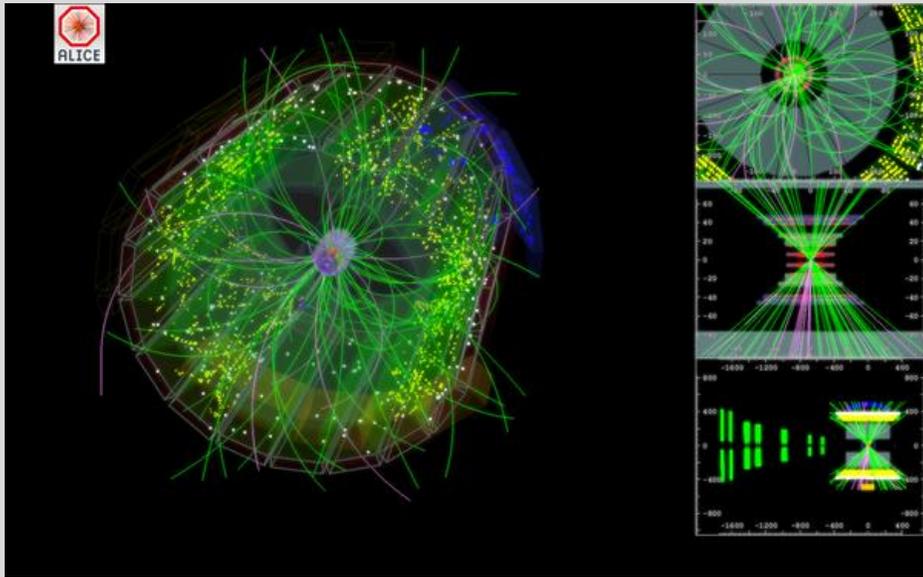
HANDS-ON SESSION



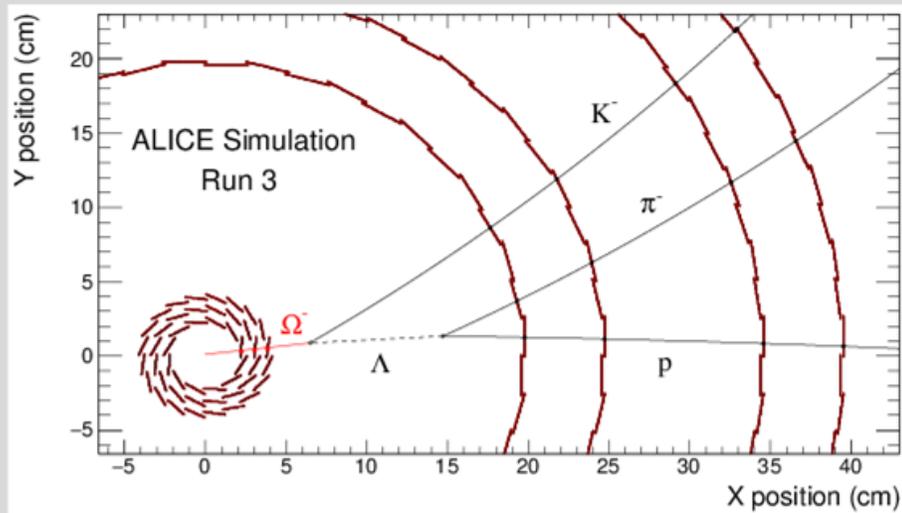
UNIVERSITÀ
DI TORINO



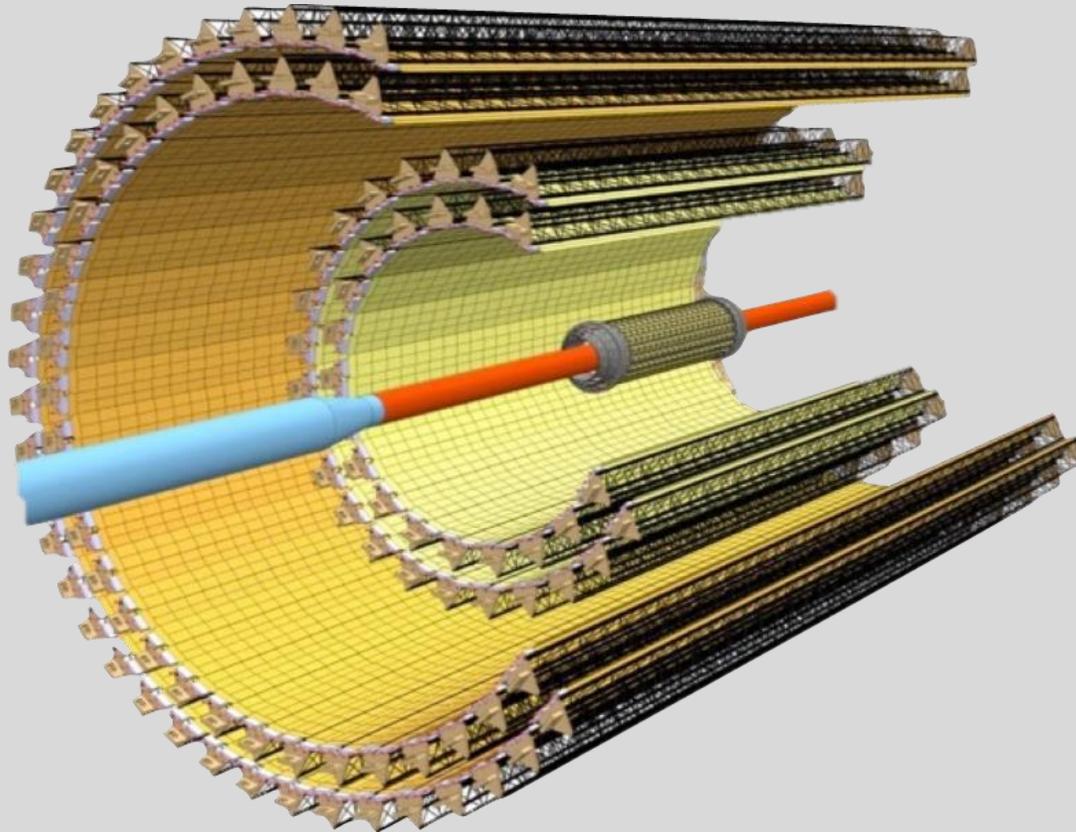
Charged particle trackers: goals



- **Tracking:** Measure trajectory of charged particles
 - Measure several points along the track and fit curves to the points (helix)
- **In collider experiments: extrapolate tracks to the point of origin**
 - Determine positions of primary vertices and identify interesting collision vertex: **VERTEXING**
 - Find secondary: vertices from decay of long-lived particles
- **Use the track curvature to determine the particle momentum: PID**



Charged particle trackers: requirements



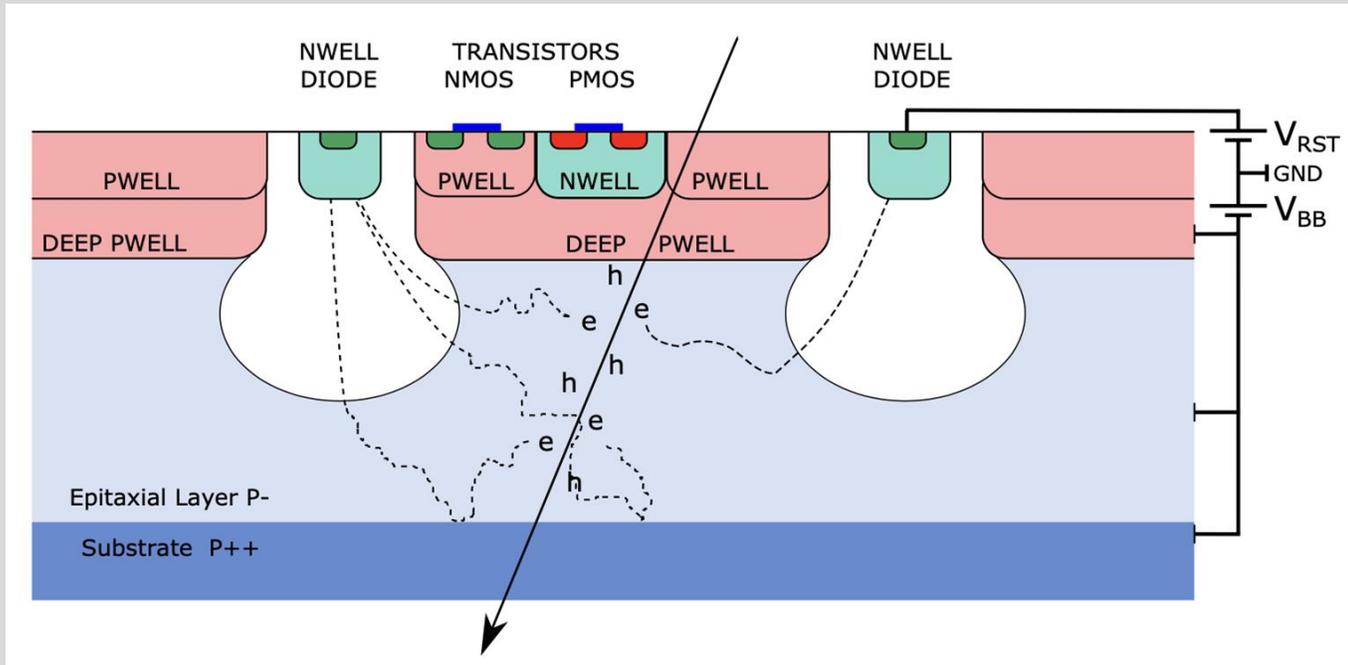
- **SENSOR:**

- Excellent Spatial resolution
- Detection efficiency $\sim 100\%$
- Low fake hit rate
- Time resolution
- Radiation hardness
- Low power

- **TRACKER:**

- First layers close to IP (pointing resolution in collider applications)
- As little material as possible
 - Multiple scattering
 - Photon conversion

Monolithic C-MOS sensors

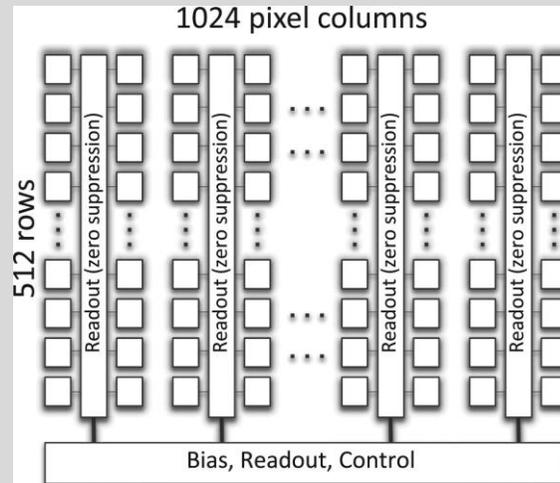
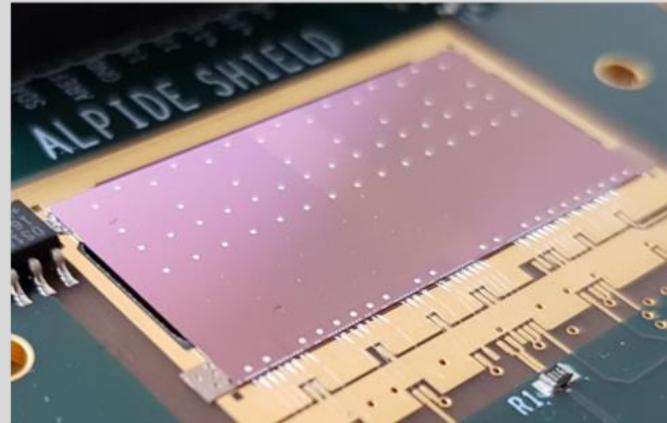


- **Commercial** CMOS technologies, originally developed for imaging sensors: sensor and electronics on the same substrate
- Can be thinned down to 50 μm or less
- Pixel size: 20 x 20 μm^2 or lower
- Charge collection **by diffusion**, more sensitive to bulk damage or **by drift** when reverse bias is applied
- Readout:
 - Analog/Digital
 - Serial readout (rolling shutter), slower
 - Data driven read out, matrix sparsification (priority encoder), faster

ALPIDE/ALTAI chips



Monolithic active pixel sensors developed for the ALICE inner tracker (ALPIDE) and optimised for space (ALTAI) in the Tower Semiconductor **180nm CMOS Imaging Sensor (CIS) Process**



ALPIDE Key Features

Digital output

In-pixel: Amplification, Discrimination, multi event buffer

In-matrix zero suppression: priority encoding

Ultra-low power $< 40\text{mW}/\text{cm}^2$ ($< 140\text{mW}$ full chip)

Detection efficiency $> 99\%$

Spatial resolution $\sim 5\mu\text{m}$

Low fake-hit rate: $\ll 10^{-6}/\text{pixel}/\text{event}$

($10^{-8}/\text{pixel}/\text{event}$ measured in data taking @ ALICE)

Radiation tolerance: $> 270\text{krad}$ (TID), $> 1.7 \cdot 10^{13}$ $1\text{MeV}/n_{\text{eq}}$ (NIEL)

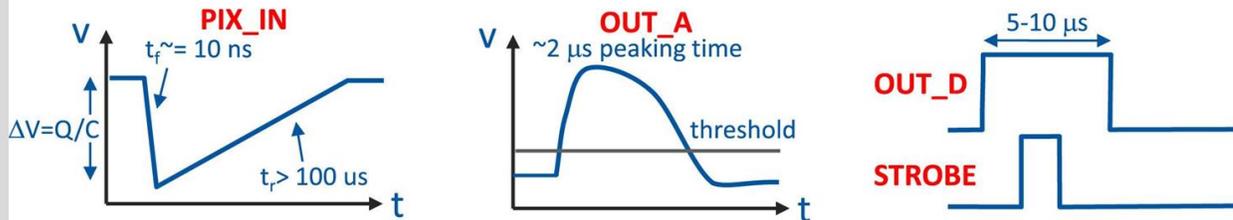
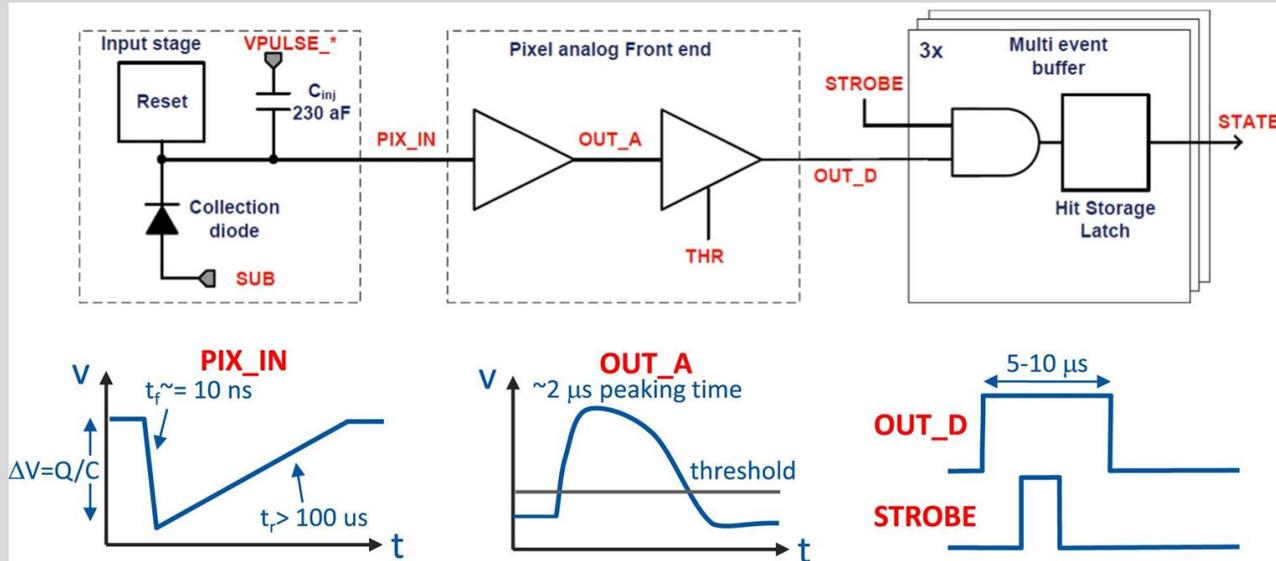
Detector size: $15 \times 30\text{mm}^2$

Pixel pitch: $26.88 \times 29.24\mu\text{m}^2$

Columns x rows: 1024×512

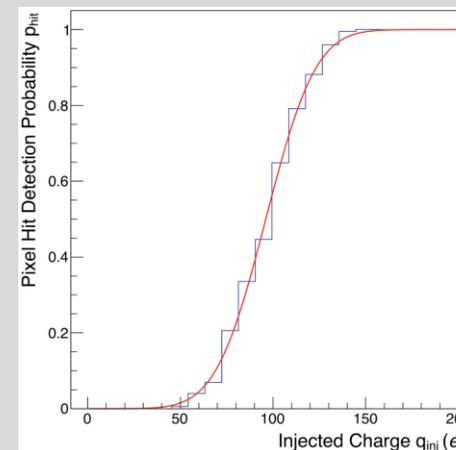
Thickness: $50\text{-}100\mu\text{m}$

ALPIDE/ALTAI chips front-end scheme



- It is possible to pulse a charge on the amplifier to study the pixel response (Threshold scan)
- It is also possible to set the pixel outcome to true for tests (Digital scan)
- Each pixel can be masked and ignored during readout

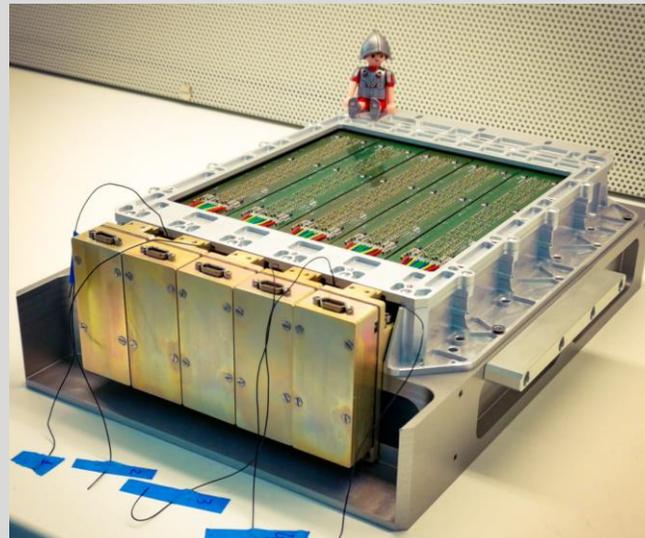
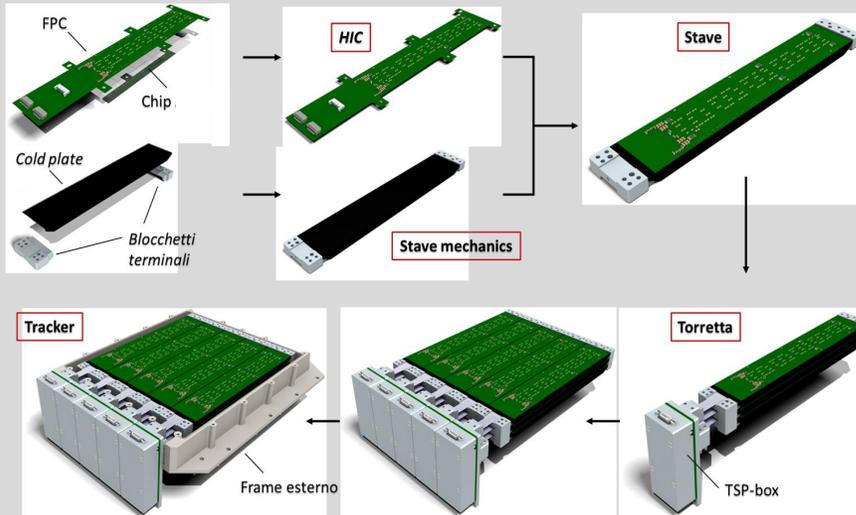
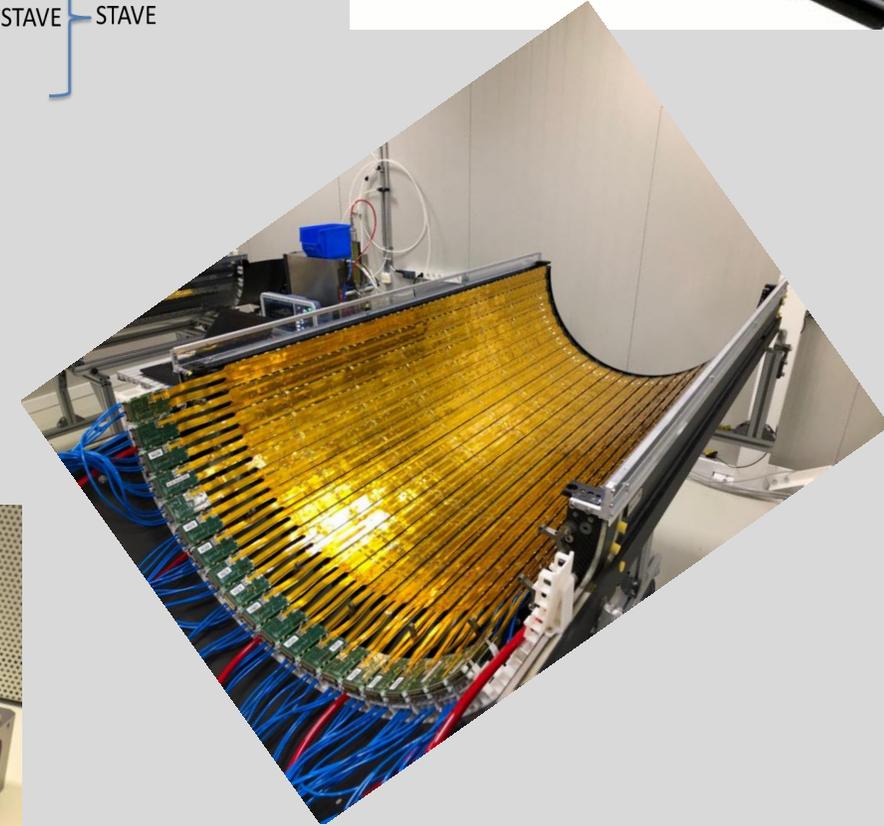
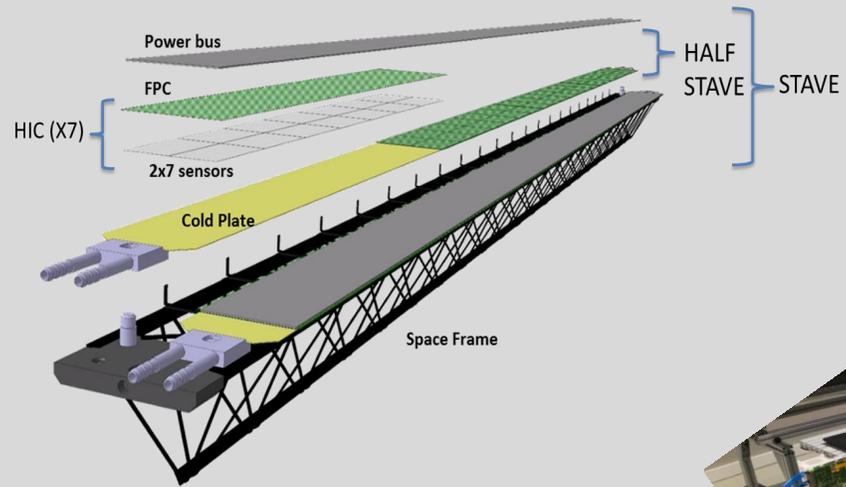
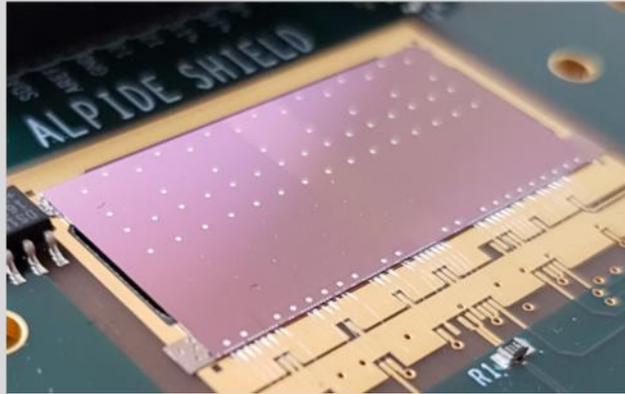
- Each ALPIDE pixel has an independent readout
- Signal is shaped with an amplifier
- Signal from the amplifier is compared with a threshold voltage common to all pixels
- If the signal is higher than the threshold, it is fed to a logic AND.
- The other input of the logic AND is the trigger signal (strobe)
- If both the signals are true, the pixel is registered as “fired” in either of the three hit storage registers (multi event buffer)



Example for one pixel
S-curve \square **erf() fit**

Pixel Threshold = Mean value of erf for each pixel
Noise = sigma

From sensor to tracking system



Collider application: ALICE ITS2 @LHC

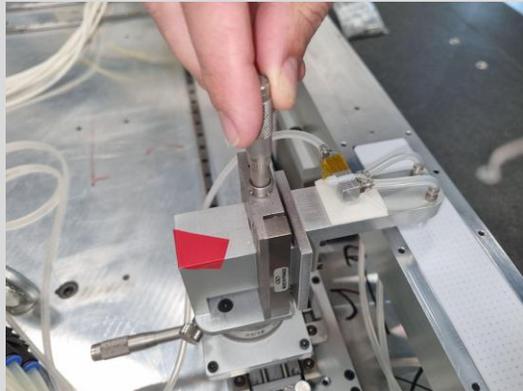
Space application: HEPD-02 on CSES2 satellite

Monolithic C-MOS sensors. Quality control of light-weight tracking detectors.

LAB ACTIVITY



HIC Assembly



SHOW:
Tracker Mechanical supports

Tracker element assembly/
handling tools

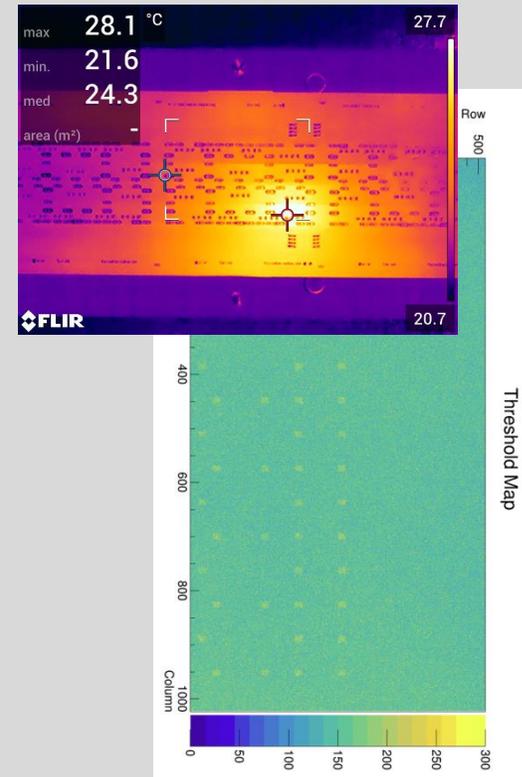
HANDS-ON:
Chip positioning guided by
CMM

Chip position survey

HIC assembly with FPC



HIC Characterization



SHOW:
Tracker HICs and STAVES

Test system and typical
outputs

HANDS-ON:
HIC power on with check on
power consumption and
hotspot (with thermocam)

Readout test on every chip

Threshold scan

LAB Equipment

CMM machine

Glue dispenser

Cutter plotter (for the masks)

Air system in pressure

- for the CMM machine
- for the glue dispenser

Vacuum air system

- for the HIC alignment tools
- or the HIC handling
- for the glue dispenser



LAB ORGANIZATION

Shared spaces for tools

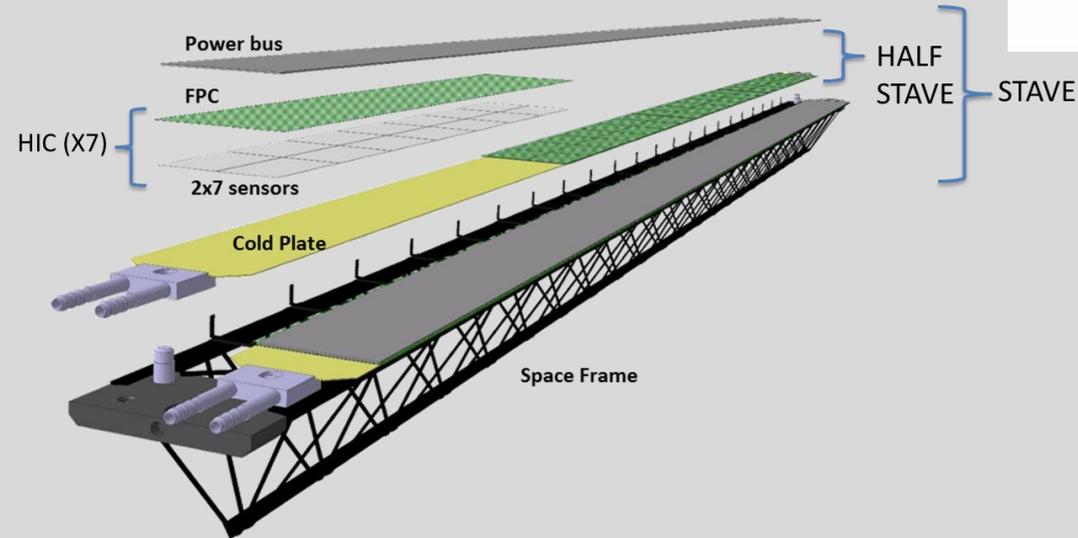
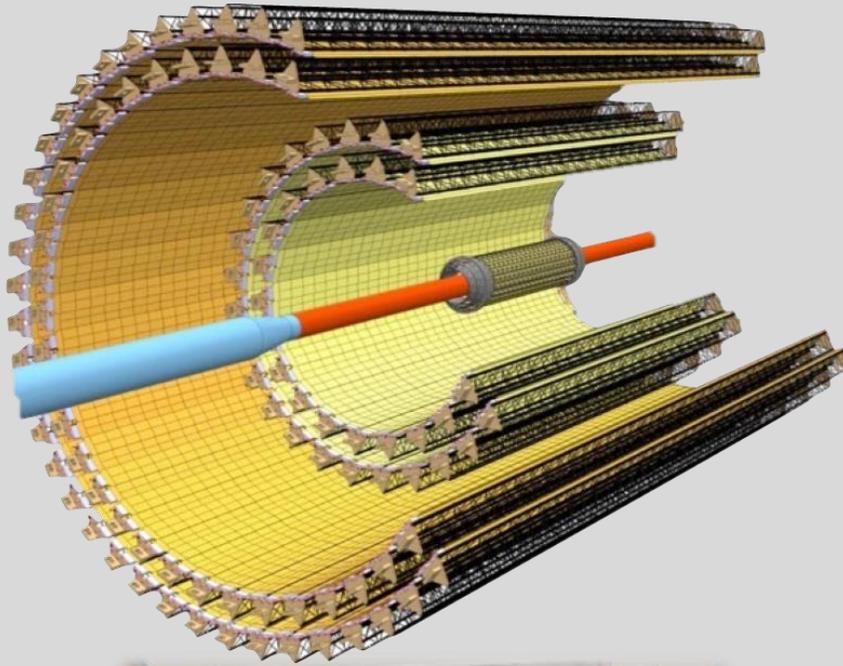
Shared Air pressure/
vacuum systems for
manipulation

Shared space for
maneuvering and
material stockage

GOWN and OVERSHOES are MANDATORY

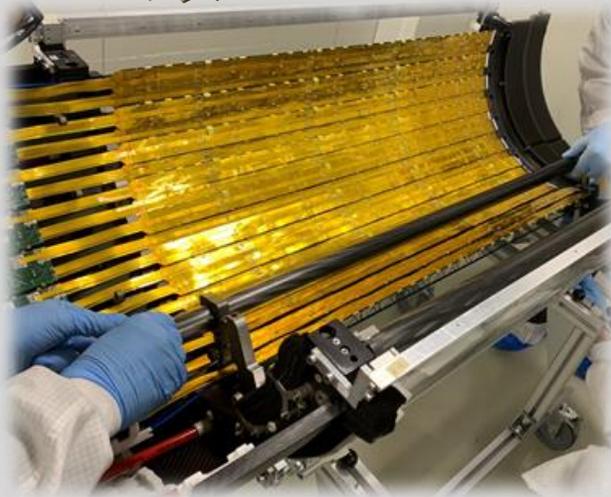


Tracker Particle Detector (LHC): Components



Tracker: 7 layers of staves (inner Barrel + outer Barrel)

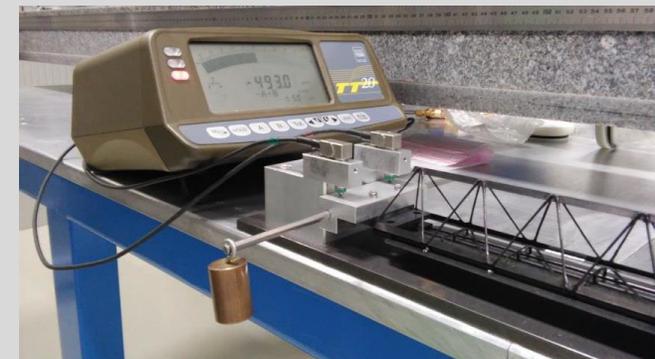
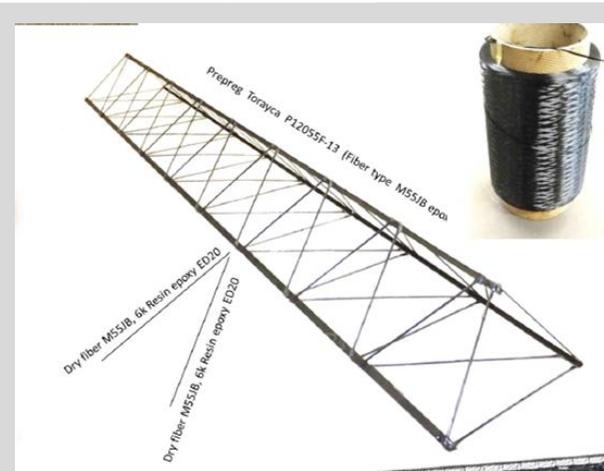
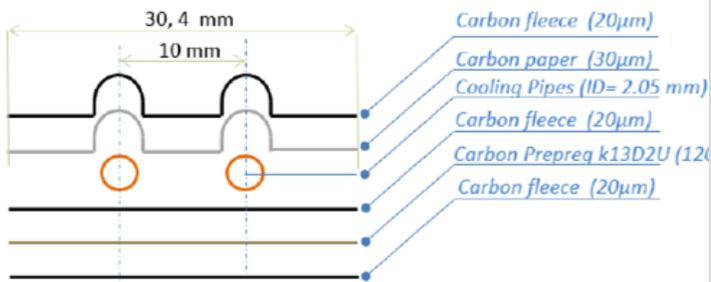
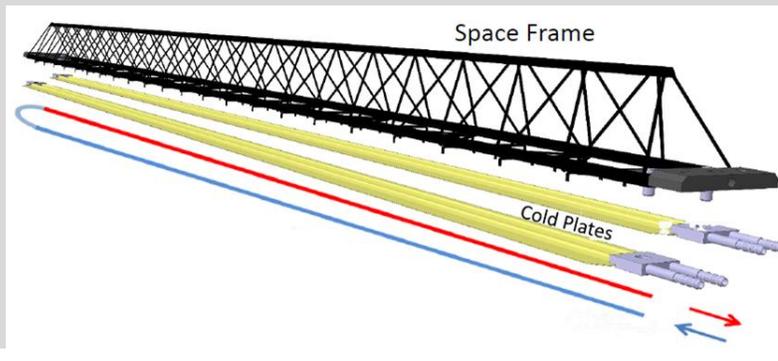
- **OB Stave:**
 - **HIC (Hybrid Integrated Circuit):**
 - 2x7 Chip (MAPS Detector)
 - **FPC (Flexible Printed Circuit)**
 - **Mechanical structure:**
 - *CF cold plate /integrated cooling*
 - *CF space frame*
 - **Power bus**



Tracker Mechanical Supports

CF Cold plates and Space frame Design Layout:

CF plates with integrated water cooling aims at power dissipation and at minimizing temperature gradients



Qualification Test:

Structural and vibrational test needed for the qualification of the mechanics



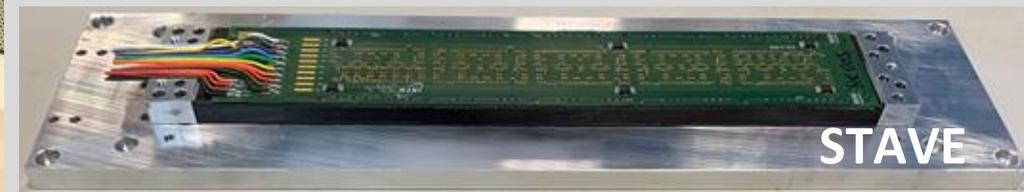
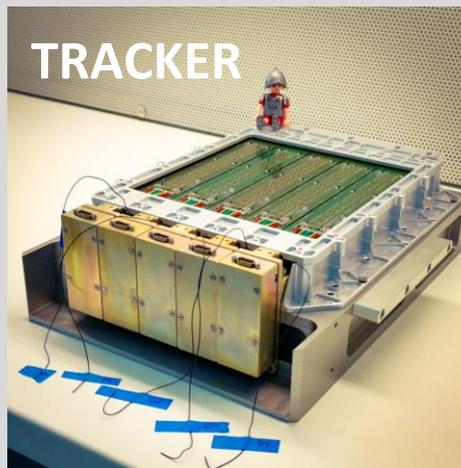
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Tracker Particle Detector (Space): Components



Tracker: 5 Turrets + external frame

- **Turret:** 3x Staves + TSP-box
- **Stave:** HIC + mechanic stave
 - **HIC (Hybrid Integrated Circuit):**
 - 2x5 Chip (MAPS Detector)
 - **FPC (Flexible Printed Circuit)**
 - **Mechanic Stave:**
 - *CF Cold Plate*
 - Aluminum End blocks
- **TSP-box (electrical interface):**
 - PCB-TSP (*Printed Circuit Board*)
 - Aluminum box

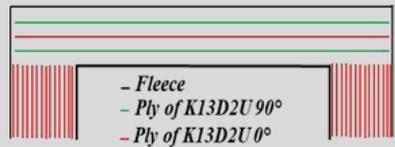
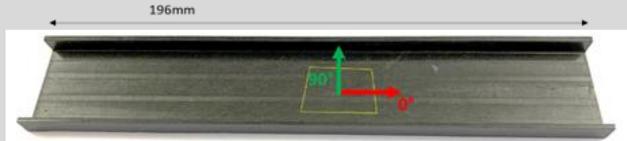


Tracker Mechanical Supports

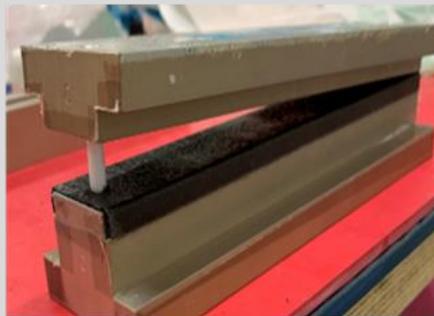


CFRP Cold Plate (CP) Design Layout and manufacturing process

A lightweight structure (K13D2U + EX1515) with plies properly oriented aims at minimizing the temperature gradients and the material budget.



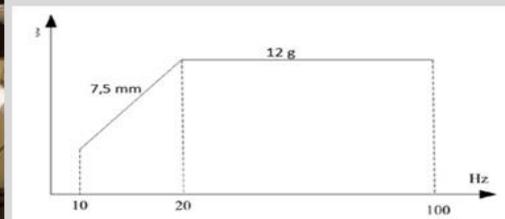
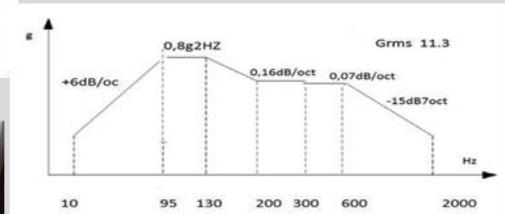
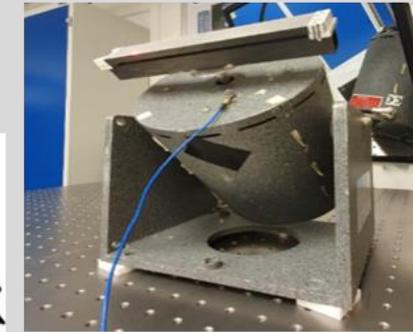
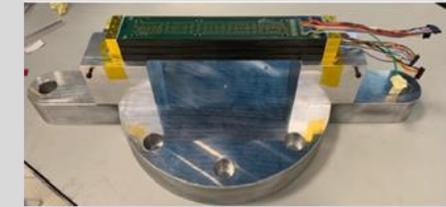
0.4mm: material thickness in sensitive area



Mold for CP production.

Qualification TEST:

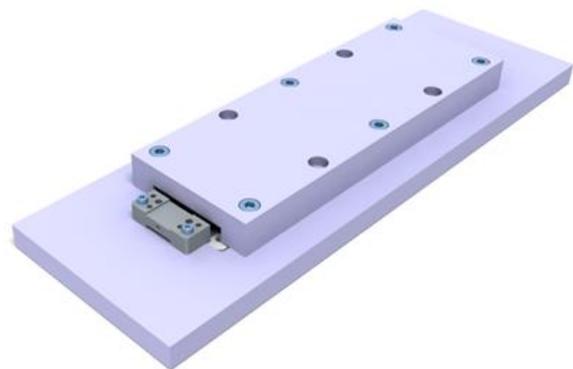
An intense campaign of thermo-mechanical and vibrational qualification test was required by the space register. Lightness and stiffness, premises for the supports in a tracker system, need to balance with the submitted elevate structural and vibrational stress in the extended range of temperature occurring during the launch phase.



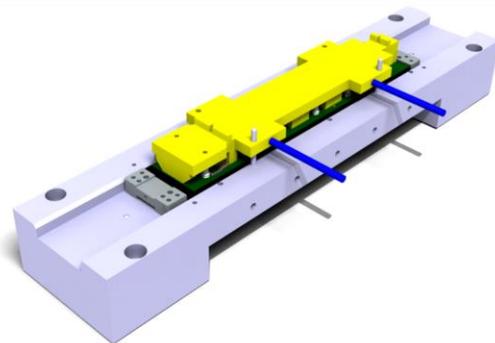
Tracker elements assembly/ handling tools



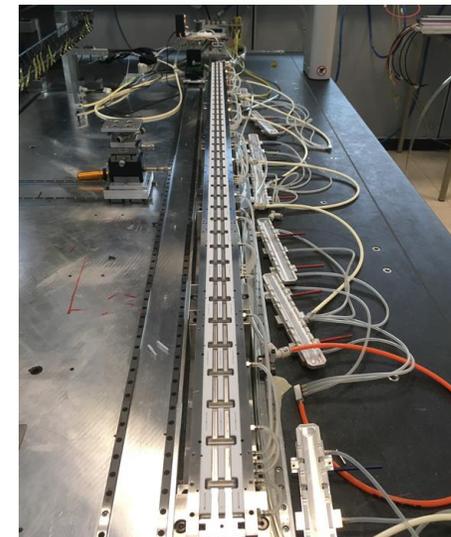
Mechanic stave assembly tool



HIC holder

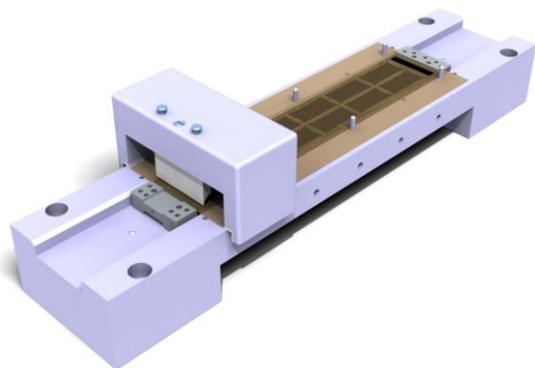


PB assembly tool

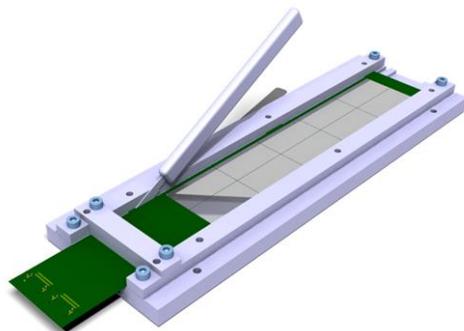


Half Stave assembly tool

Stave alignment station



Tab/Wings cutting tool



Stave handling tool



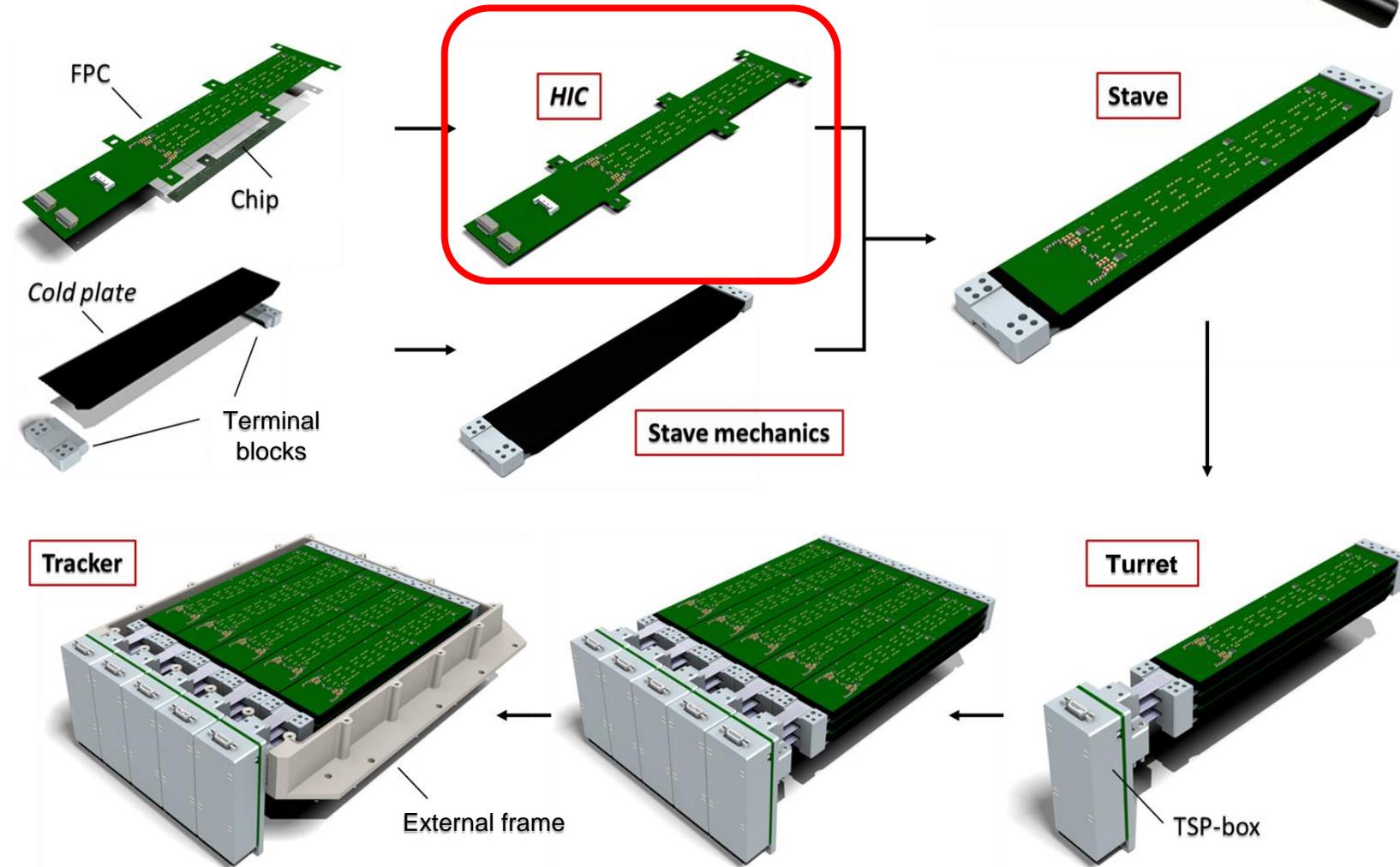
Survey tool



LAB activity: HIC ASSEMBLY



1. Reference system definition
2. 10x chips positioning
3. Chip position survey
4. Glue deposition on FPC
5. FPC positioning \Rightarrow HIC Assembly
6. HIC survey
7. Wire bonding step
8. Electrical test
9. HIC Tab/wings cut
10. Electrical test/ HIC characterization
11. Stave mechanics Assembly
12. Survey
13. Stave Assembly
14. Survey
15. Electrical test/ Stave characterization
16. TSP box Assembly
17. Turret Assembly
18. Electrical test/ Turret characterization
19. Tracker Assembly
20. Validation /qualification test



CMM (Coordinate Measuring Machine)



CMM: MITUTOYO Crysta Apex S-9206

Measuring range:

X-axis 900 mm

Y-axis 2000 mm

Z-axis 600mm

Resolution: 0.0001 mm (0.1 μm)

Guide method: Air bearings on each axis

Max. measuring speed: 8 mm/s

Workpiece:

- Maximum height: 800 mm

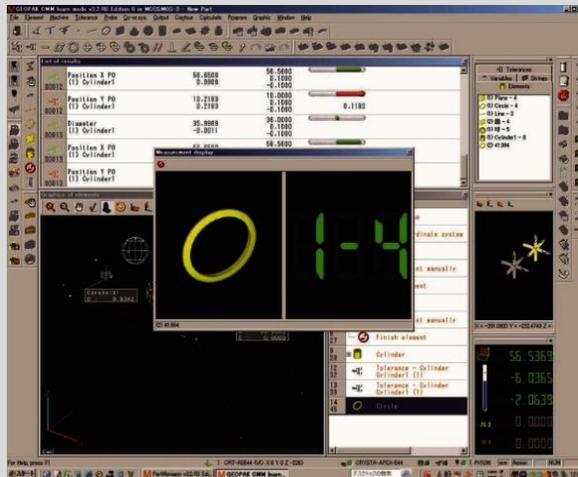
- Maximum mass: 1800 kg

Mass (including the control device and installation platform): 3912 kg

Air supply

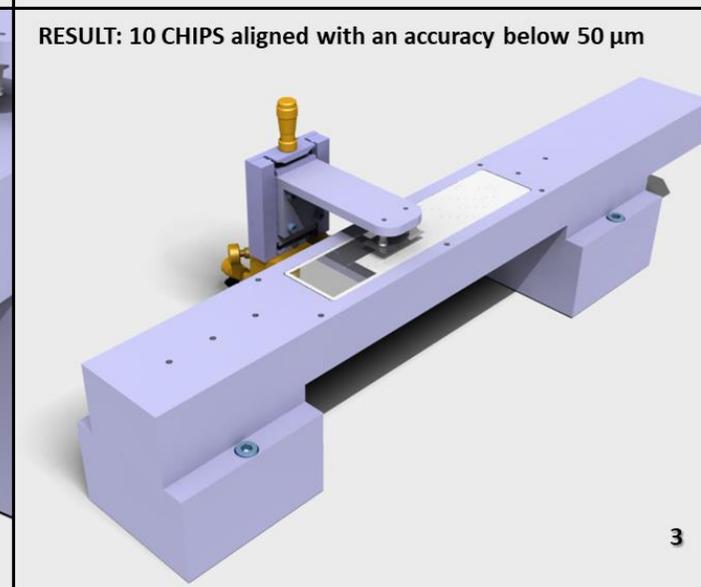
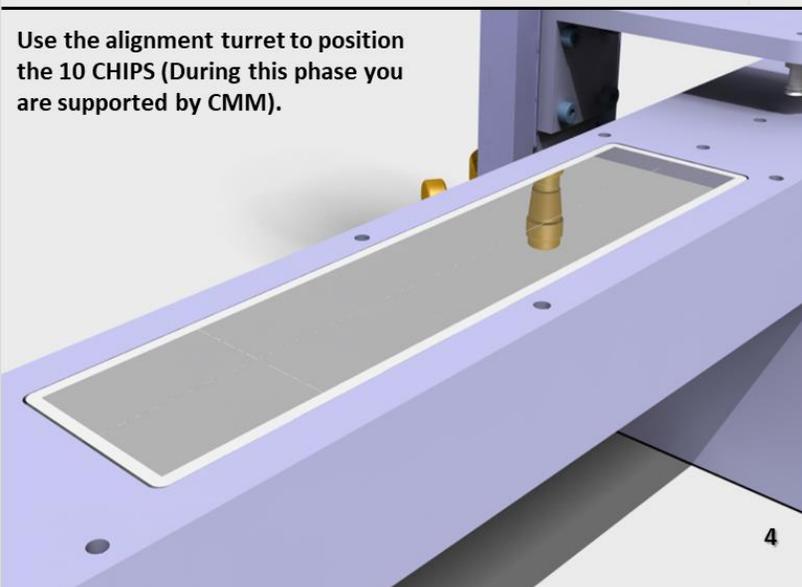
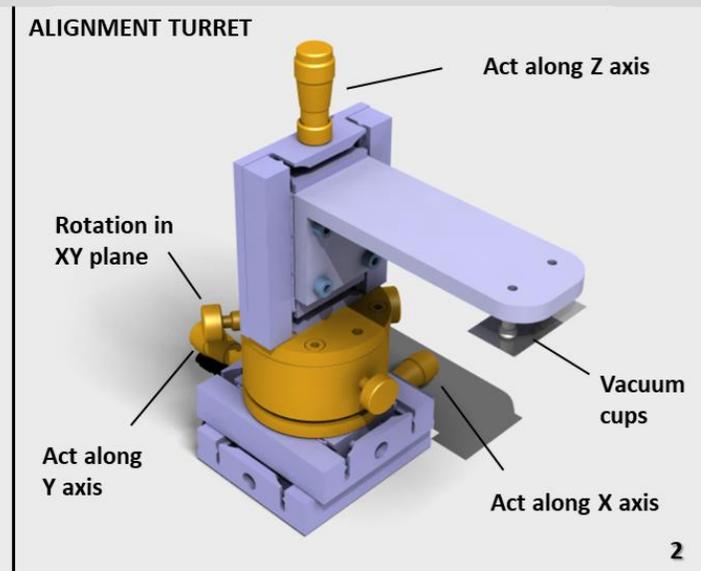
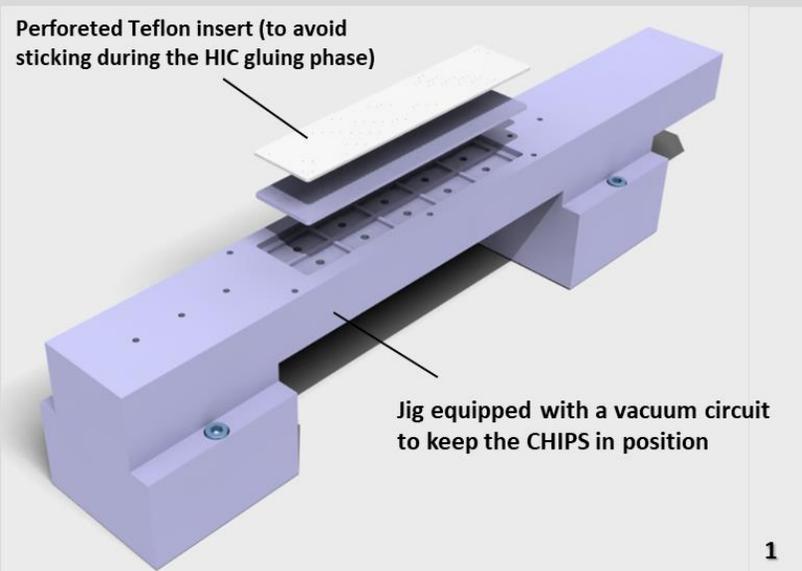
- Pressure: 0.4 MPa

- Consumption: 60 L/min under normal conditions (air source: 120 L/min)



- ❖ Equipped with **touch probe**, **video probe** and **Joystick**, for the manual guide.
- ❖ **MCOSMOS** is the software for dedicated programs which guide the operator during all the steps for the chip positioning and the metrological survey for the quality check and data analyses.

Chip Alignment tool



Base for the chip alignment, equipped with vacuum and alignment station for the chip positioning.

Teflon layer for the gluing step.

Compatible with handling tools and with FPC holders.

Video probe stays at 44mm from the focus: dedicated programs foresee movements to avoid collision with structure.

Database/logbook



Chip database

	1	2	3	4	5	6	7	8
A	NK	NK	NK	NK	NK			NK
B	NK	NK			NK			
C				NK			NK	

4th layer

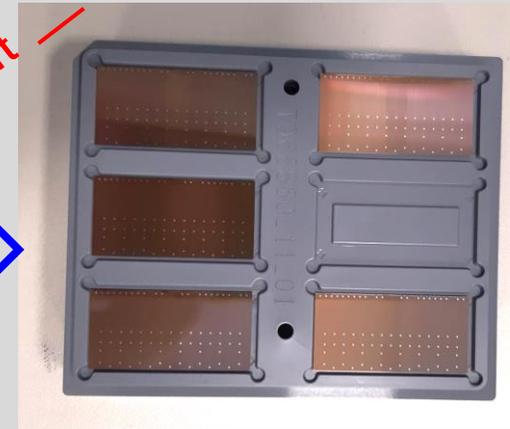
3rd layer

2nd layer

1st layer of the chip box



top-left corner



Chip database report tables of the chip organization in the storage boxes.

It is divided by chip-quality:

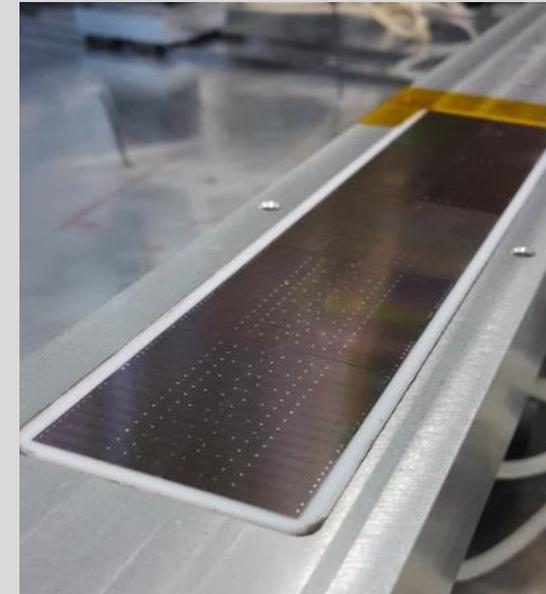
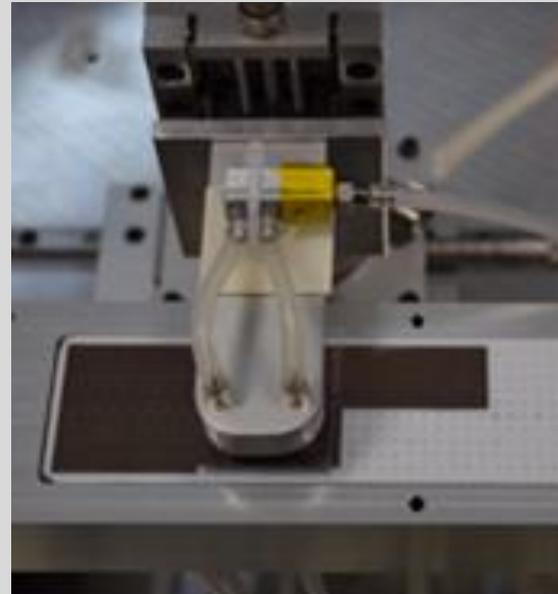
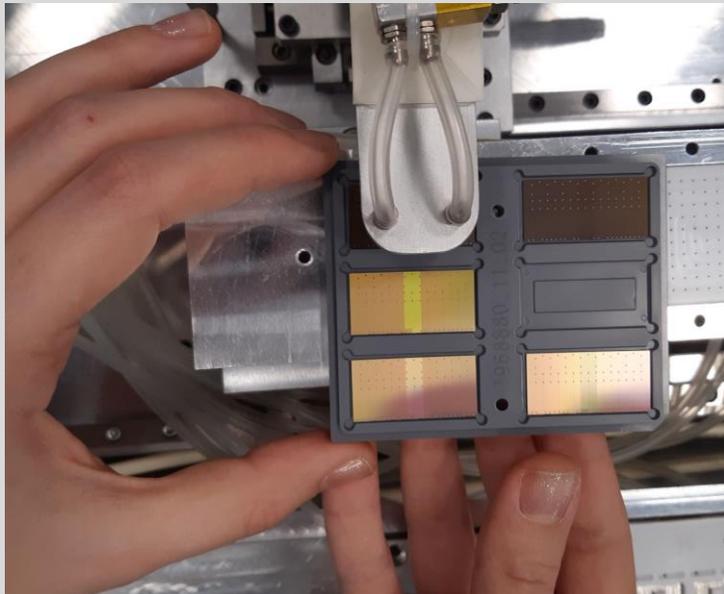
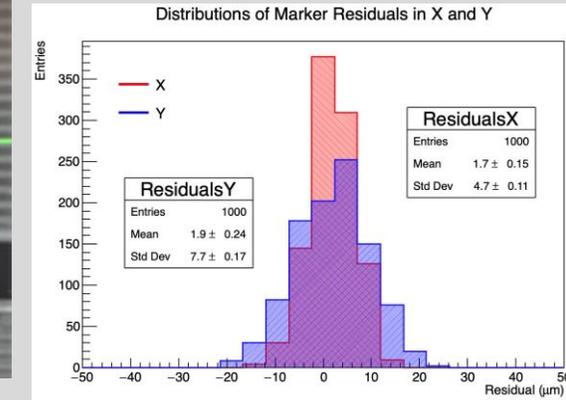
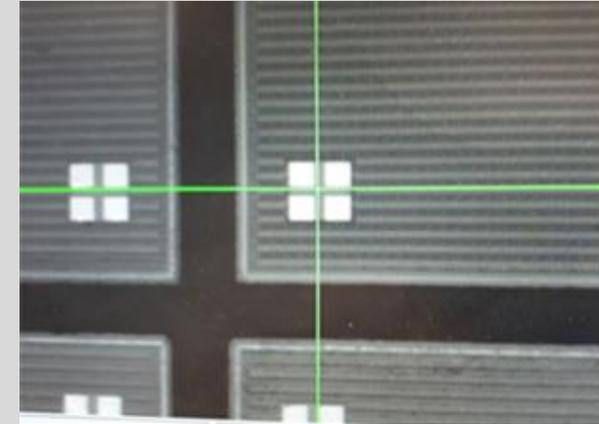
- OBG (GOLD)
- OBS (SILVER)
- OBB (BRONZE)
- OBZ (NK)

	10	9	8	7	6
TAB					0x70
	0x78				
	1	2	3	4	5

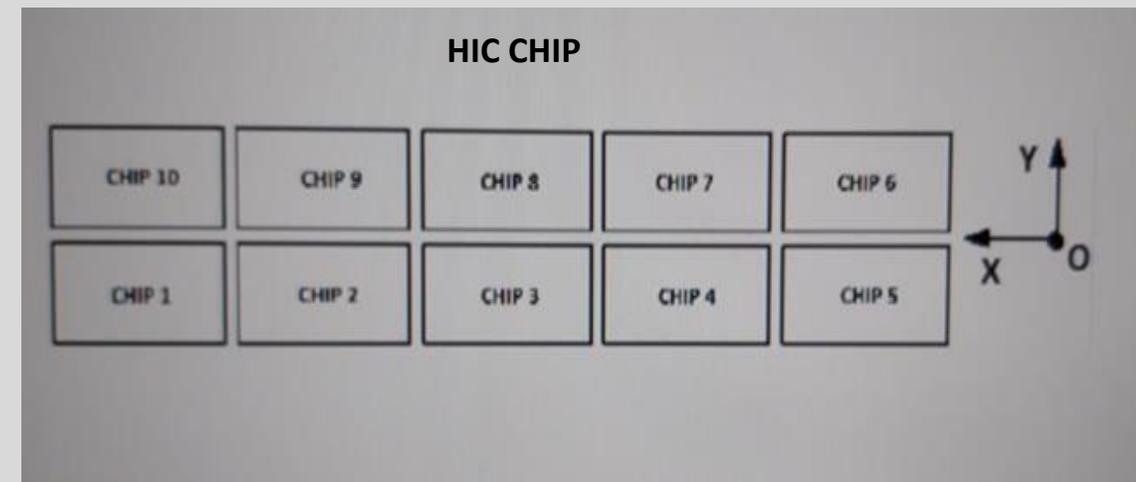
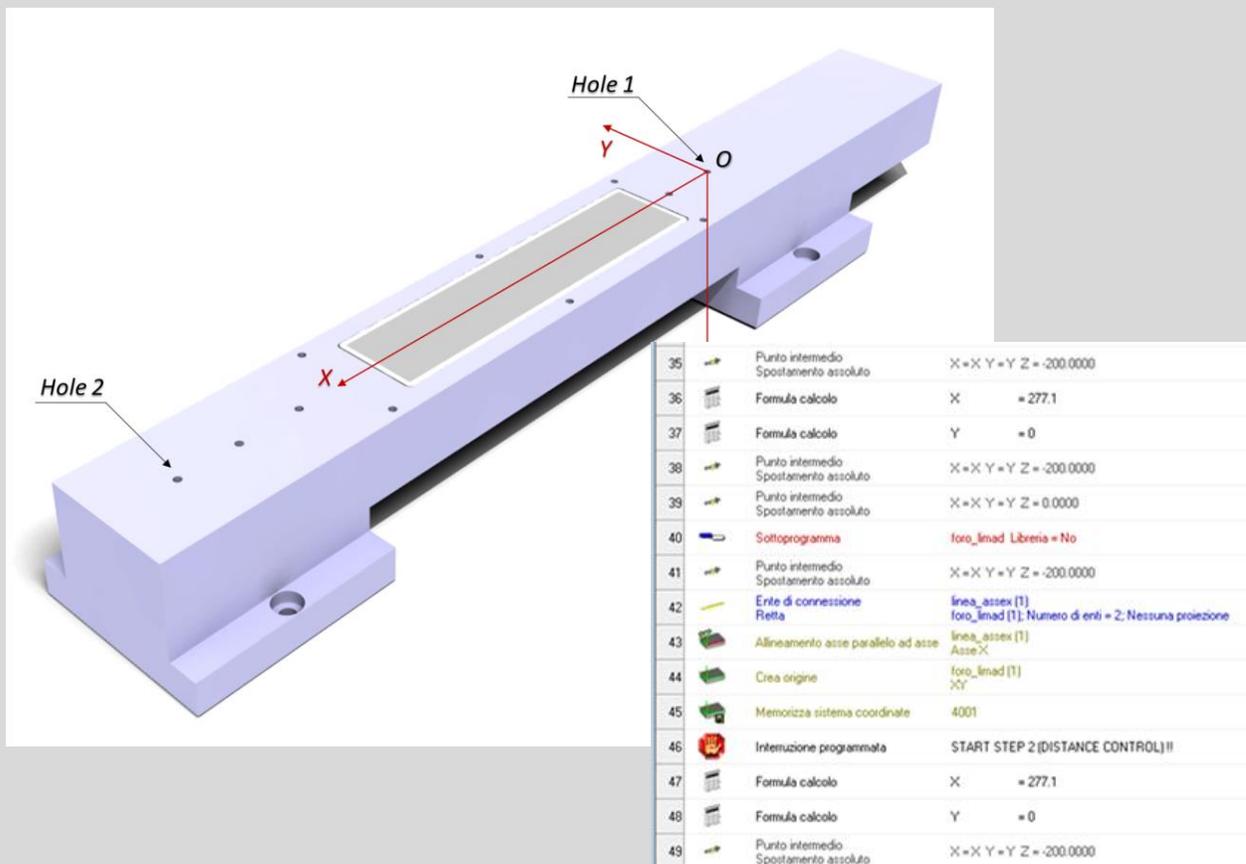


HIC ASSEMBLY/ Chip positioning

1. Reference system definition on chip alignment tool
2. 10x chips positioning
3. Chip position survey
4. Glue deposition on FPC
5. FPC positioning HIC Assembly
6. HIC survey



Reference system



NOMINAL CHIP MARKER POSITION (X,Y)

	CHIP 10		CHIP 9		CHIP 8		CHIP 7		CHIP 6	
D	188.725	-14.995	158.575	-14.995	128.425	-14.995	98.275	-14.995	68.125	-14.995
C	159.076	-14.995	128.926	-14.995	98.776	-14.995	68.626	-14.995	38.476	-14.995
B	159.076	-0.219	128.926	-0.219	98.776	-0.219	68.626	-0.219	38.476	-0.219
A	188.725	-0.219	158.575	-0.219	128.425	-0.219	98.275	-0.219	68.125	-0.219

	CHIP 1		CHIP 2		CHIP 3		CHIP 4		CHIP 5	
D	188.725	0.219	158.575	0.219	128.425	0.219	98.275	0.219	68.125	0.219
C	159.076	0.219	128.926	0.219	98.776	0.219	68.626	0.219	38.476	0.219
B	159.076	14.995	128.926	14.995	98.776	14.995	68.626	14.995	38.476	14.995
A	188.725	14.995	158.575	14.995	128.425	14.995	98.275	14.995	68.125	14.995

Reference system program updates the reference system every day.

Reference system always visible during assembly.

Chips positioned in the nominal marker position wrt the reference system.

Chip positioning/ survey programs



Interactive Chip alignment program

NAME OF EXCEL FILE

Insert HIC serial number: LIMADOU_HIC_001
Ex : HIC-001

HIC ID for database

CHOOSE THE CHIP AND THE MARKER

chip: 1

starting marker: D

continue alignment
exit alignment

Chip alignment position

CHOOSE ALIGNMENT OPERATION :

- 1 - Rotation in XY plane
- 2 - Shift to nominal XY
- 3 - Check adjacent CHIP
- 4 - The CHIP is aligned. Continue

Chip alignment steps

- rotation (1)
- shift (2)
- chip deposition (4)

Confirma Annulla

Chip Survey program

CHOOSE THE CHIP

chip: all chip

continue planarity measurement
exit planarity measurement

CHIP 10 CHIP 9 CHIP 8 CHIP 7 CHIP 6
CHIP 1 CHIP 2 CHIP 3 CHIP 4 CHIP 5

Y
X

Confirma Annulla

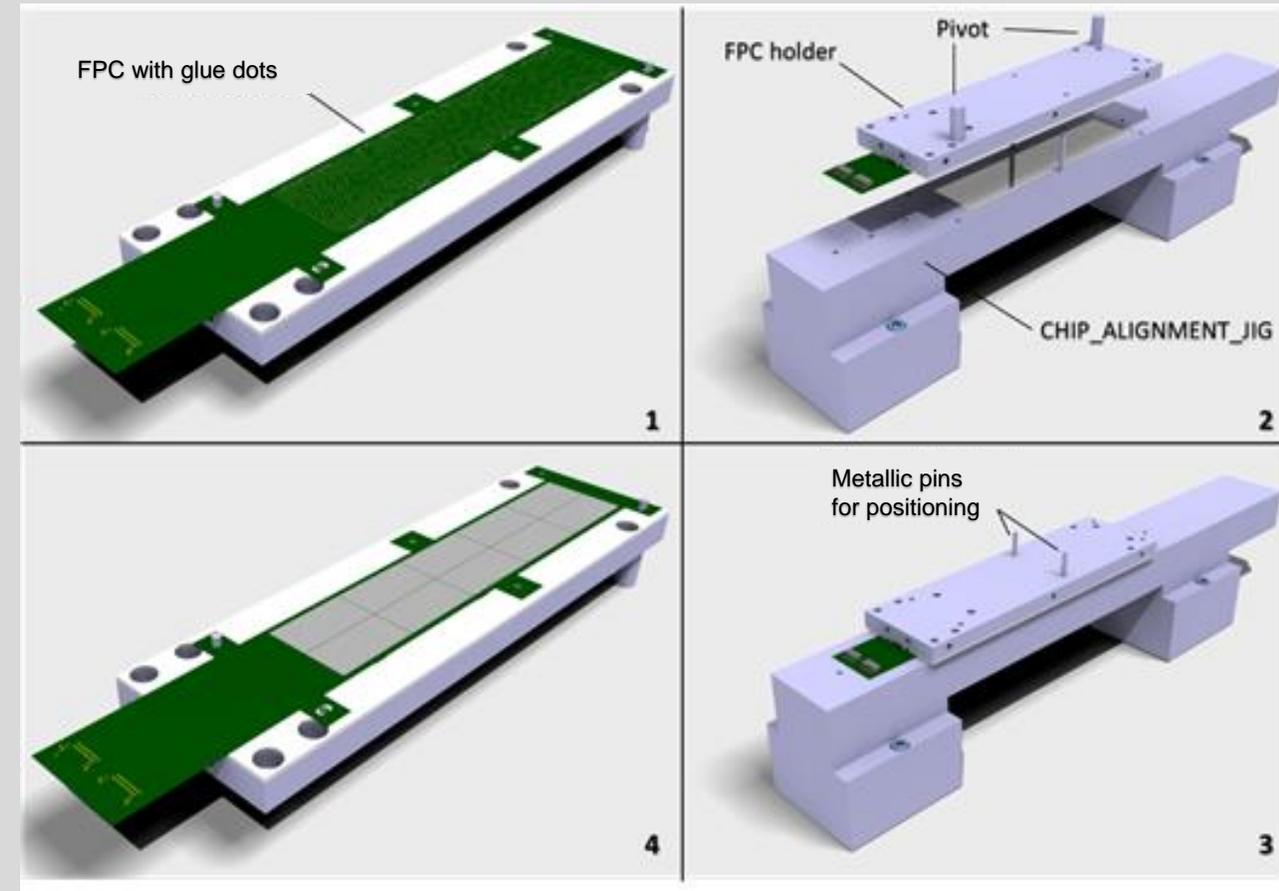
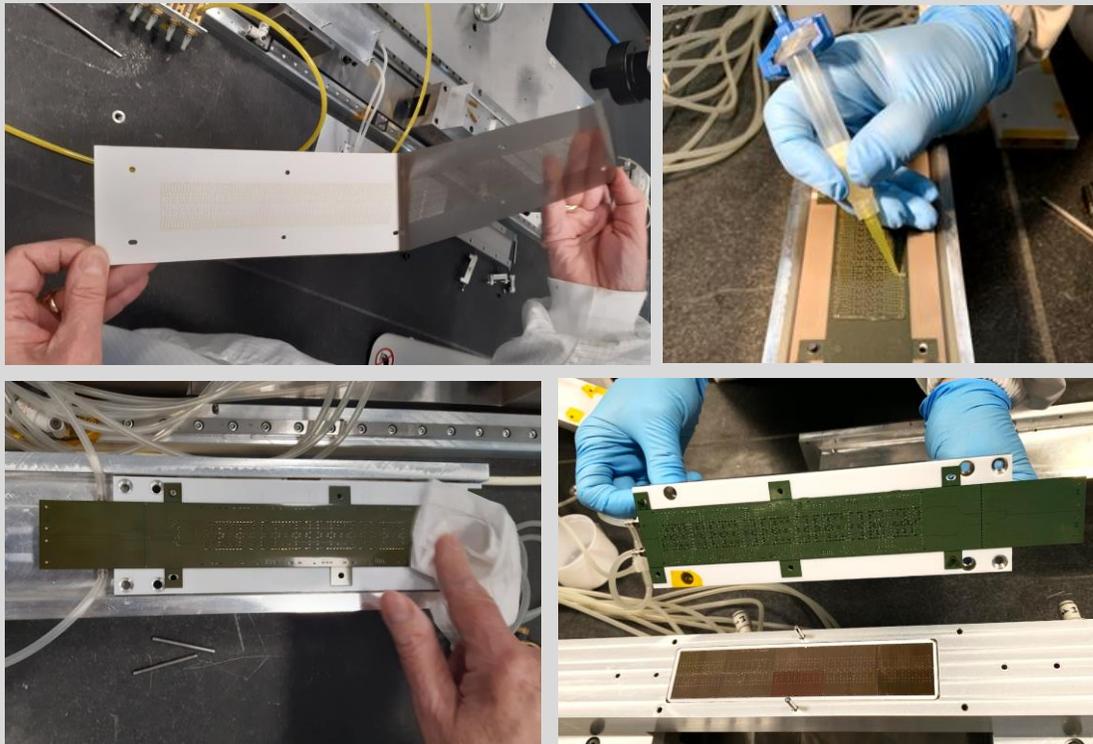
survey output

			X	Y	Z
1,00	4,00point	1,00	188,722	-15,003	-0,017
2,00	4,00point	1,00	159,074	-14,993	-0,023
3,00	4,00point	1,00	159,079	-0,217	-0,011
4,00	4,00point	1,00	188,727	-0,228	-0,017
5,00	4,00point	1,00	158,577	-14,993	-0,043
6,00	4,00point	1,00	128,928	-14,993	-0,026
7,00	4,00point	1,00	128,929	-0,218	-0,028
8,00	4,00point	1,00	158,577	-0,218	-0,009
9,00	4,00point	1,00	128,428	-14,995	-0,031
10,00	4,00point	1,00	98,779	-14,992	-0,049
11,00	4,00point	1,00	98,781	-0,216	-0,026
12,00	4,00point	1,00	128,430	-0,220	-0,027
13,00	4,00point	1,00	98,276	-14,997	-0,019
14,00	4,00point	1,00	68,627	-14,992	-0,012
15,00	4,00point	1,00	68,628	-0,217	-0,006
16,00	4,00point	1,00	98,278	-0,221	-0,020
17,00	4,00point	1,00	68,126	-15,000	-0,010
18,00	4,00point	1,00	38,477	-14,984	-0,050
19,00	4,00point	1,00	38,485	-0,208	-0,035
20,00	4,00point	1,00	68,133	-0,224	-0,016
21,00	4,00point	1,00	68,123	0,223	-0,013
22,00	4,00point	1,00	38,476	0,229	-0,026
23,00	4,00point	1,00	38,478	15,006	-0,020
24,00	4,00point	1,00	68,127	15,000	-0,019
25,00	4,00point	1,00	98,282	0,220	-0,014
26,00	4,00point	1,00	68,633	0,229	-0,008
27,00	4,00point	1,00	68,637	15,005	-0,038
28,00	4,00point	1,00	98,287	14,995	-0,039
29,00	4,00point	1,00	128,426	0,228	-0,029
30,00	4,00point	1,00	98,777	0,226	-0,012
31,00	4,00point	1,00	98,776	15,002	-0,048
32,00	4,00point	1,00	128,423	15,006	-0,035
33,00	4,00point	1,00	158,579	0,223	-0,010
34,00	4,00point	1,00	128,930	0,224	-0,009
35,00	4,00point	1,00	128,930	15,000	-0,048
36,00	4,00point	1,00	158,579	14,999	-0,018
37,00	4,00point	1,00	188,724	0,225	-0,019
38,00	4,00point	1,00	159,075	0,226	-0,012
39,00	4,00point	1,00	159,076	15,001	-0,016
40,00	4,00point	1,00	188,724	15,000	-0,036
	Plane_Chip				
100,00	58,00Gauss	40,00	113,603	0,003	-0,024
			0,000	0,000	-1,000
100,00	59,00Plane_Chip			210,100	0,045
	Planarità				0,045

HIC ASSEMBLY/ FPC glueing



1. Reference system definition
2. 10x chips positioning
3. Chip position survey
4. **Glue deposition on FPC**
5. **FPC positioning** ? HIC Assembly
6. HIC survey

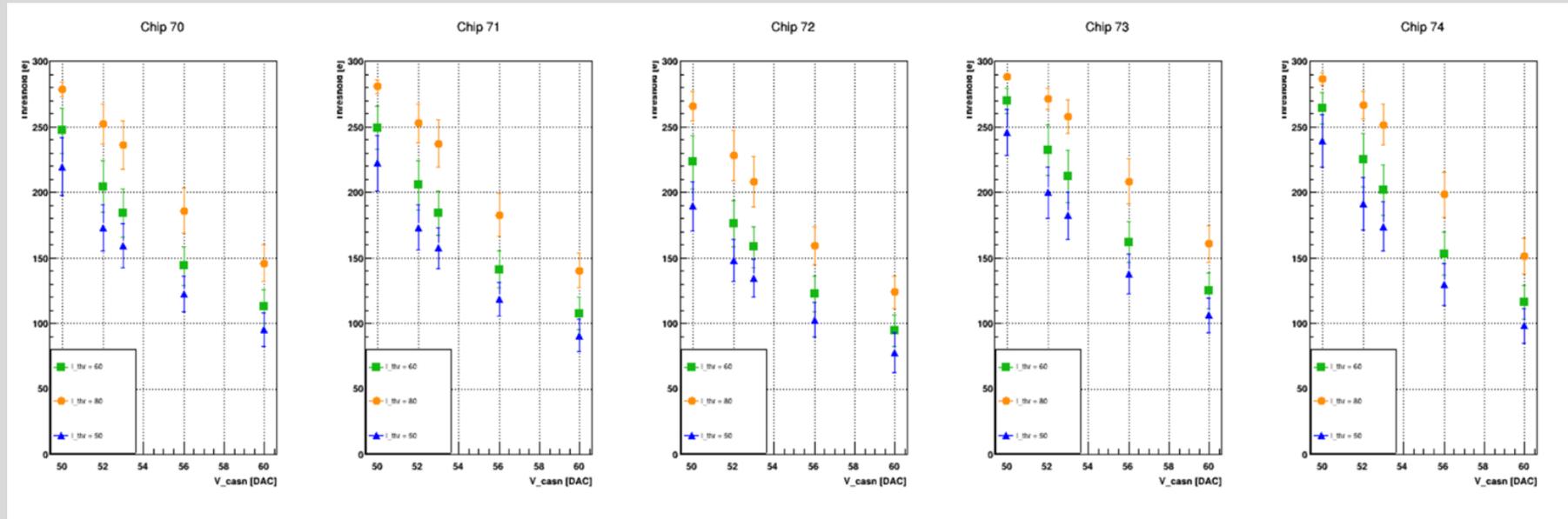


Dedicated final survey program for database

Qualification tests

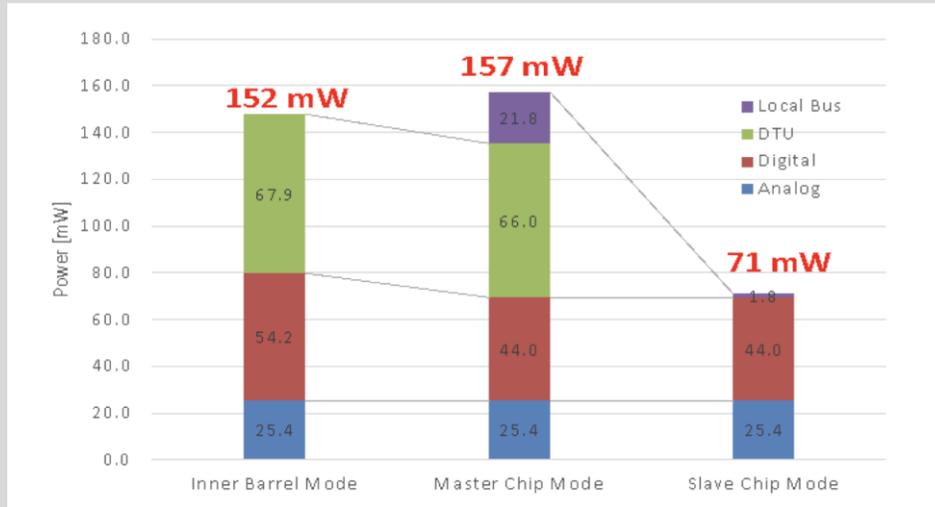


- **Limited power budget** in space applications
- Identification of **damages** that can induce current leakage
- Read/write check to **assess the quality** of the tracker modules
- **Threshold scan** to check the the every chip response



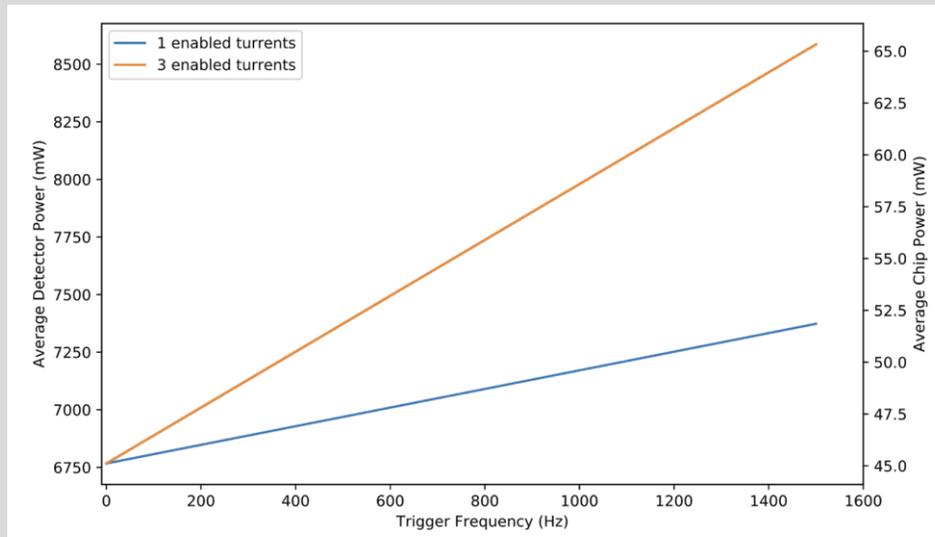
Threshold is tuned a priory, based on scientific requirements, by tuning voltage settings.

Power consumption mitigation



ALICE ITS OB **Master-slave architecture** (1 master out of 5 chips) with sequential slave read-out through master.

Permanent **switch-off of fast data transmission unit** (DTU) and read-out through serial slow-control line. Acceptable increase of dead time, given the relatively low trigger rate sustainable by the HEPD-02 system (up to few kHz).



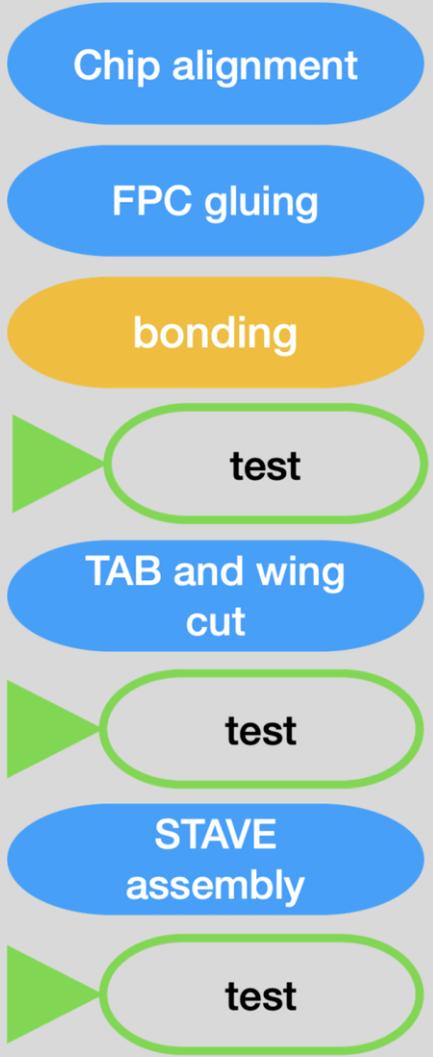
Clock gating: ALTAI clock normally off, set on with trigger:

- trigger: clock on (17 mW/cm²);
- wait for signal digitization;
- transmit data to control/read-out electronics;
- clock off (7 mW/cm²): wait for new trigger.

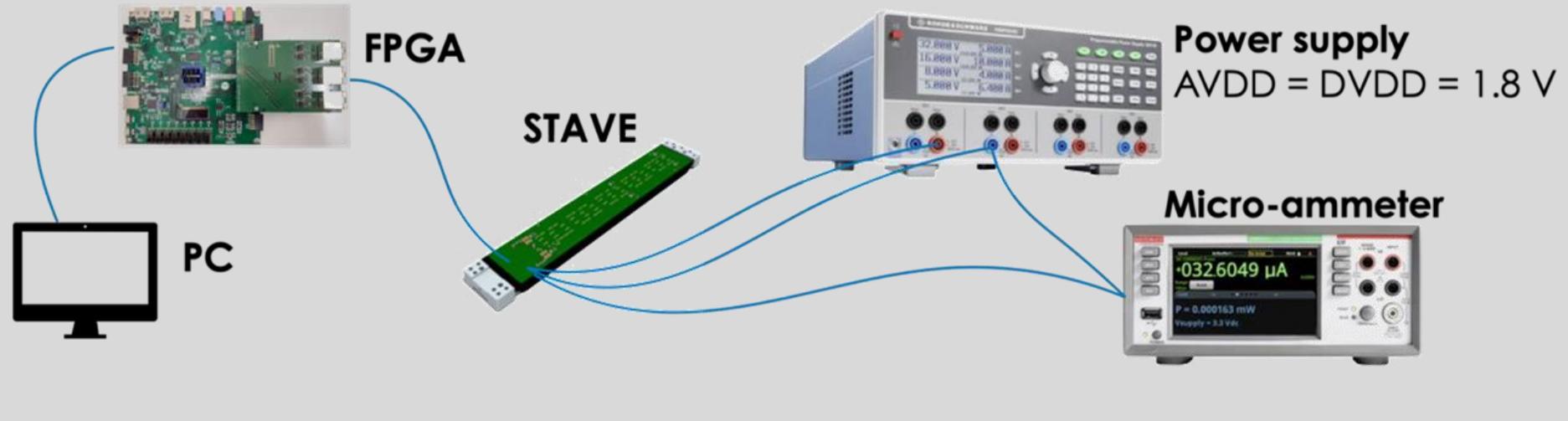
Qualification tests setup



--- HIC assembly ---



- **Power supply**: AVDD and DVDD power on
- **Micro-ammeter**: check reverse bias currents
- **FPGA**: interface with PC
- **Thermo cam**



Power test



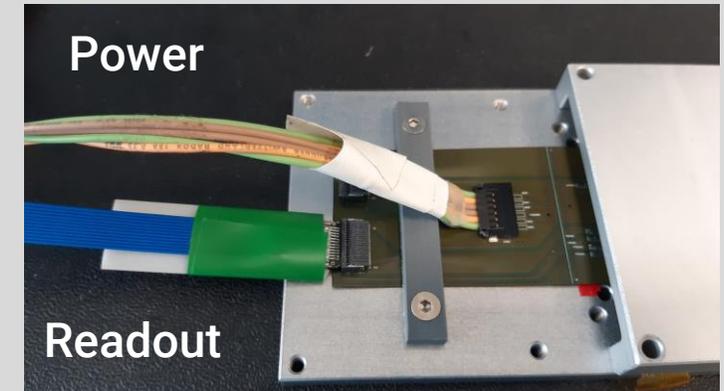
HIC/STAVE power on:

- 0 V [50 mA c.l.] on reverse bias
- 1.8 V [1 A c.l.] for analog and digital channels

Check of the power consumption at clock off and on:

```
bash clock_toggle.sh on
```

```
bash clock_toggle.sh off
```



Staves power consumption (clk on)

	BRONZE	SILVER	GOLD	GOLD spare
AVDD [mA]	124 ± 1	124 ± 2	125 ± 5	112 ± 2
DVDD [mA]	466 ± 6	460 ± 21	451 ± 11	421 ± 10

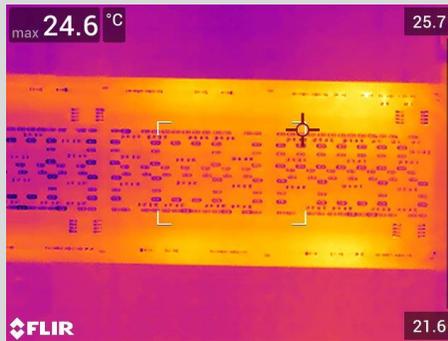
* the software is located in the folder: `~/LIMADOU/hepd-tracker-daq_master-20220610_1814/software_test`

Chip write/read response



Testing procedure to assess HIC/STAVE quality:

- check for **hotspot with thermocam** while turning the clock on



- **chip scan** → read/write procedure returning chip ID

```
bash chip_scan.sh
```

```
>> 0x070 0x071 0x072 0x073 0x074 0x078 0x079 0x07a 0x07b 0x07c
```

- **digital scan** → inject charge and check the digital readout

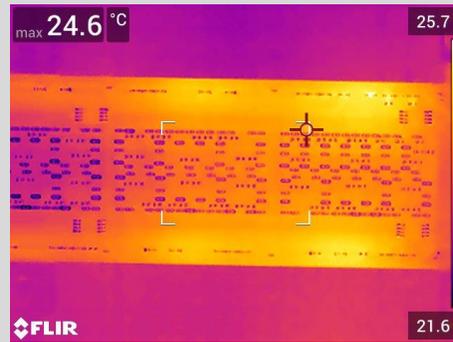
```
bash run_digitalscan.sh
```

>> produces an output into /output/ folder with hitmaps

Identification of damages

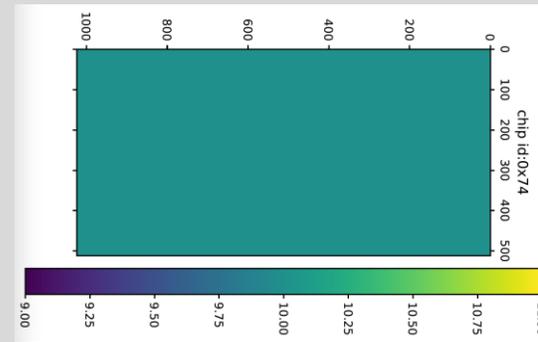


Thermocam

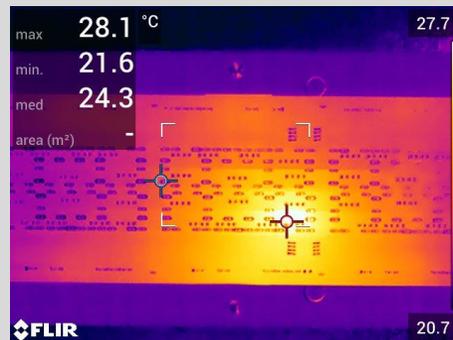
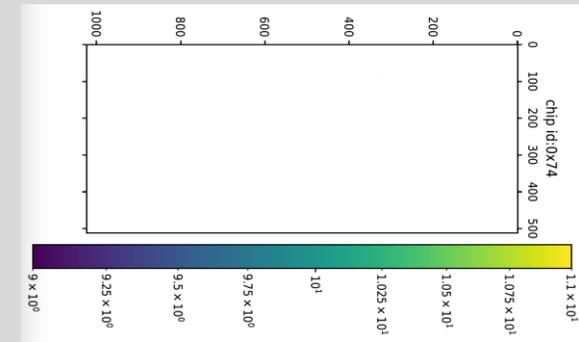


HIC-080
DVDD 433.8 mA

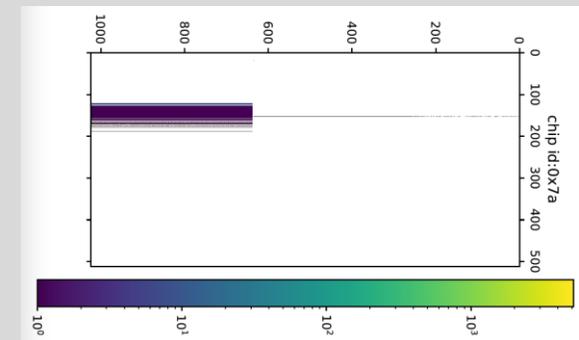
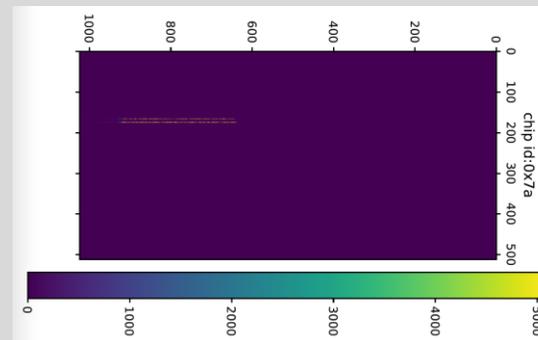
Hitmap



Unmasked pixels



HIC-074
DVDD 618.5 mA



Threshold scans

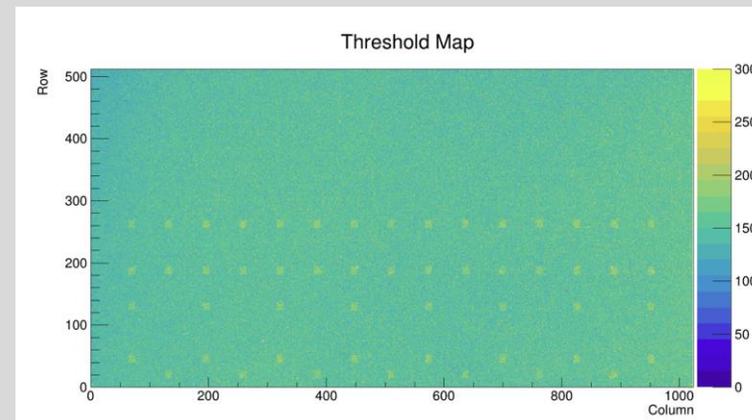
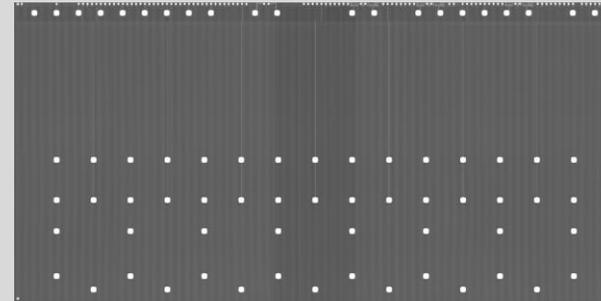
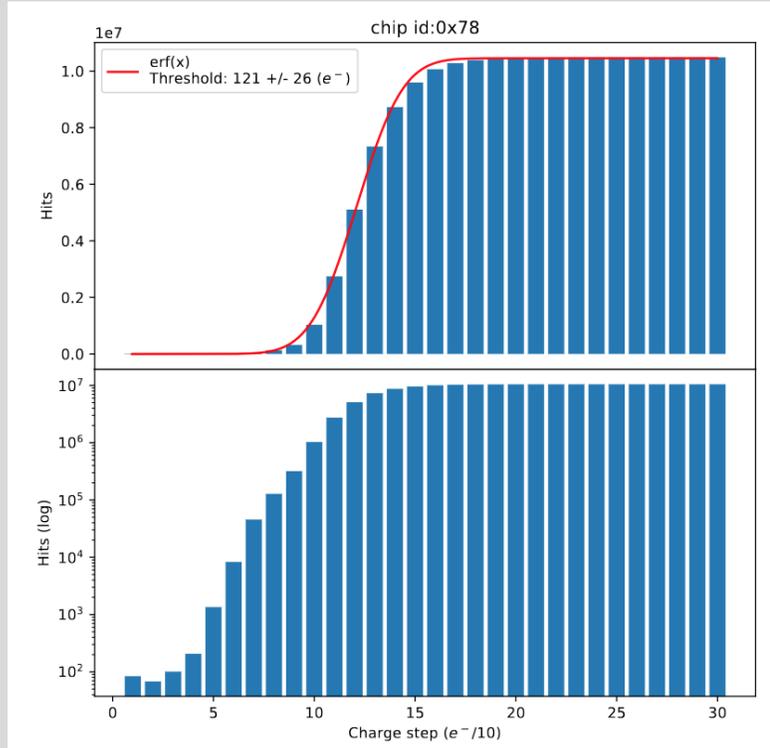


Testing procedure to assess HIC/STAVE quality:

- **threshold scan** → charge injection ramp to check the threshold

```
bash run_thresholdscan.sh
```

>> produces an output into /output/ folder with hitmaps and charge collection distributions





Thank you for your attention



We are waiting for you in the lab!
Hands on...

TORINO, 2023 OCTOBER 9th-13th